PALCE16V8

# Flash-Erasable Reprogrammable CMOS PAL® Device

Features

- **Active pull-up on data input pins**
- **Low power version (16V8L)**
  - **— 55 mA max. commercial (10, 15, 25 ns)**
  - **— 65 mA max. industrial (10, 15, 25 ns)**
  - **— 65 mA military (15 and 25 ns)**
- **Standard version has low power**
  - **— 90 mA max. commercial (10, 15, 25 ns)**
  - **— 115 mA max. commercial (7 ns)**
  - **— 130 mA max. military/industrial (10, 15, 25 ns)**
- **CMOS Flash technology for electrical erasability and reprogrammability**
- **PCI-compliant**
- **User-programmable macrocell**
  - **— Output polarity control**
  - **— Individually selectable for registered or combinatorial operation**

- **Up to 16 input terms and eight outputs**
- **7.5 ns com'l version**
  - **5 ns t_{CO}**
  - **5 ns t_S**
  - **7.5 ns t_{PD}**
  - **125-MHz state machine**
- **10 ns military/industrial versions**
  - **7 ns t_{CO}**
  - **10 ns t_S**
  - **10 ns t_{PD}**
  - **62-MHz state machine**
- **High reliability**
  - **— Proven Flash technology**
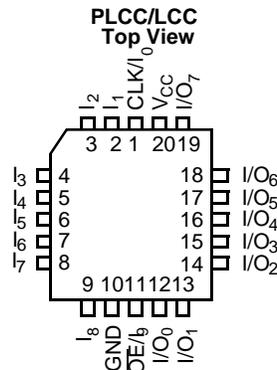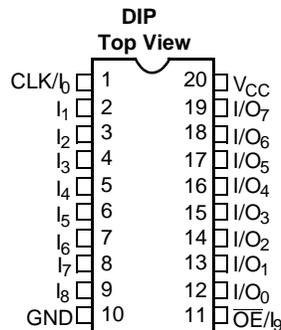 - **— 100% programming and functional testing**

Functional Description

The Cypress PALCE16V8 is a CMOS Flash Electrical Erasable second-generation programmable array logic device. It is implemented with the familiar sum-of-product (AND-OR) logic structure and the programmable macrocell.

Logic Block Diagram (PDIP/CDIP)
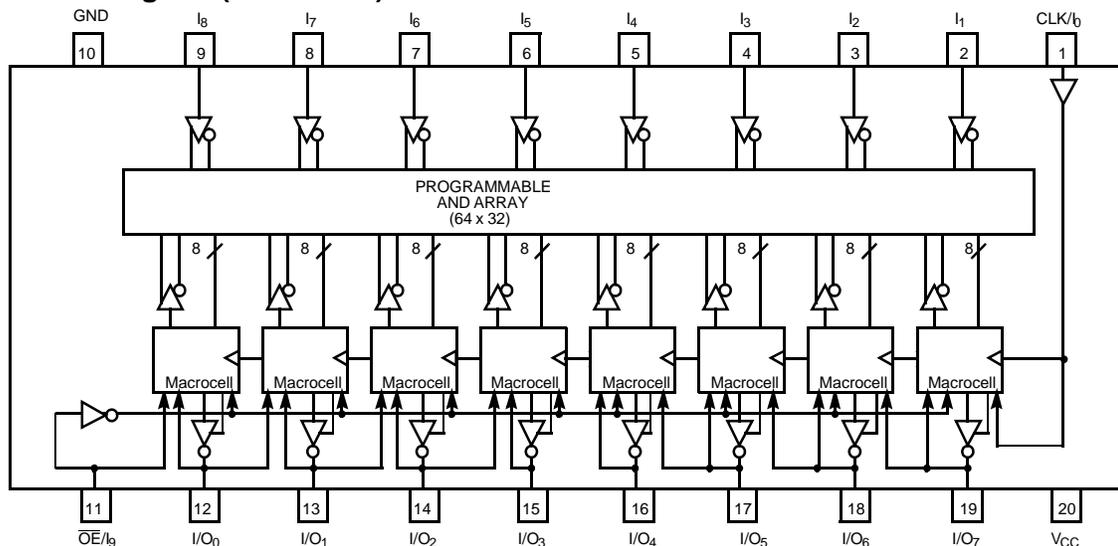
Pin Configurations

Selection Guide

Generic Part Number	t_{PD} ns		t_S ns		t_{CO} ns		I_{CC} mA	
	Com'l/Ind	Mil	Com'l/Ind	Mil	Com'l/Ind	Mil	Com'l	Mil/Ind
PALCE16V8-5	5		3		4		115	
PALCE16V8-7	7.5		7		5		115	
PALCE16V8-10	10	10	10	10	7	10	90	130
PALCE16V8-15	15	15	12	12	10	10	90	130
PALCE16V8-25	25	25	15	20	12	12	90	130
PALCE16V8L-15	15	15	12	12	10	12	55	65
PALCE16V8L-25	25	25	15	20	12	20	55	65

Shaded areas contain preliminary information.

Functional Description

The PALCE16V8 is executed in a 20-pin 300-mil molded DIP, a 300-mil cerdip, a 20-lead square ceramic leadless chip carrier, and a 20-lead square plastic leaded chip carrier.

The device provides up to 16 inputs and 8 outputs. The PALCE16V8 can be electrically erased and reprogrammed. The programmable macrocell enables the device to function as a superset to the familiar 20-pin PLDs such as 16L8, 16R8, 16R6, and 16R4.

The PALCE16V8 features 8 product terms per output and 32 input terms into the AND array. The first product term in a macrocell can be used either as an internal output enable control or as a data product term.

There are a total of 18 architecture bits in the PALCE16V8 macrocell; two are global bits that apply to all macrocells and 16 that apply locally, two bits per macrocell. The architecture bits determine whether the macrocell functions as a register or combinatorial with inverting or noninverting output. The output enable control can come from an external pin or internally from a product term. The output can also be permanently enabled, functioning as a dedicated output or permanently disabled, functioning as a dedicated input. Feedback paths are selectable from either the input/output pin associated with the macrocell, the input/output pin associated with an adjacent pin, or from the macrocell register itself.

Power-Up Reset

All registers in the PALCE16V8 power-up to a logic LOW for predictable system initialization. For each register, the associated output pin will be HIGH due to active-LOW outputs.

Electronic Signature

An electronic signature word is provided in the PALCE16V8 that consists of 64 bits of programmable memory that can contain user-defined data.

Security Bit

A security bit is provided that defeats the readback of the internal programmed pattern when the bit is programmed.

Low Power

The Cypress PALCE16V8 provides low-power operation through the use of CMOS technology, and increased testability with Flash reprogrammability.

Product Term Disable

Product Term Disable (PTD) fuses are included for each product term. The PTD fuses allow each product term to be individually disabled.

Configuration Table

CG_0	CG_1	$CL0_x$	Cell Configuration	Devices Emulated
0	1	0	Registered Output	Registered Med PALs
0	1	1	Combinatorial I/O	Registered Med PALs
1	0	0	Combinatorial Output	Small PALs
1	0	1	Input	Small PALs
1	1	1	Combinatorial I/O	16L8 only

Macrocell
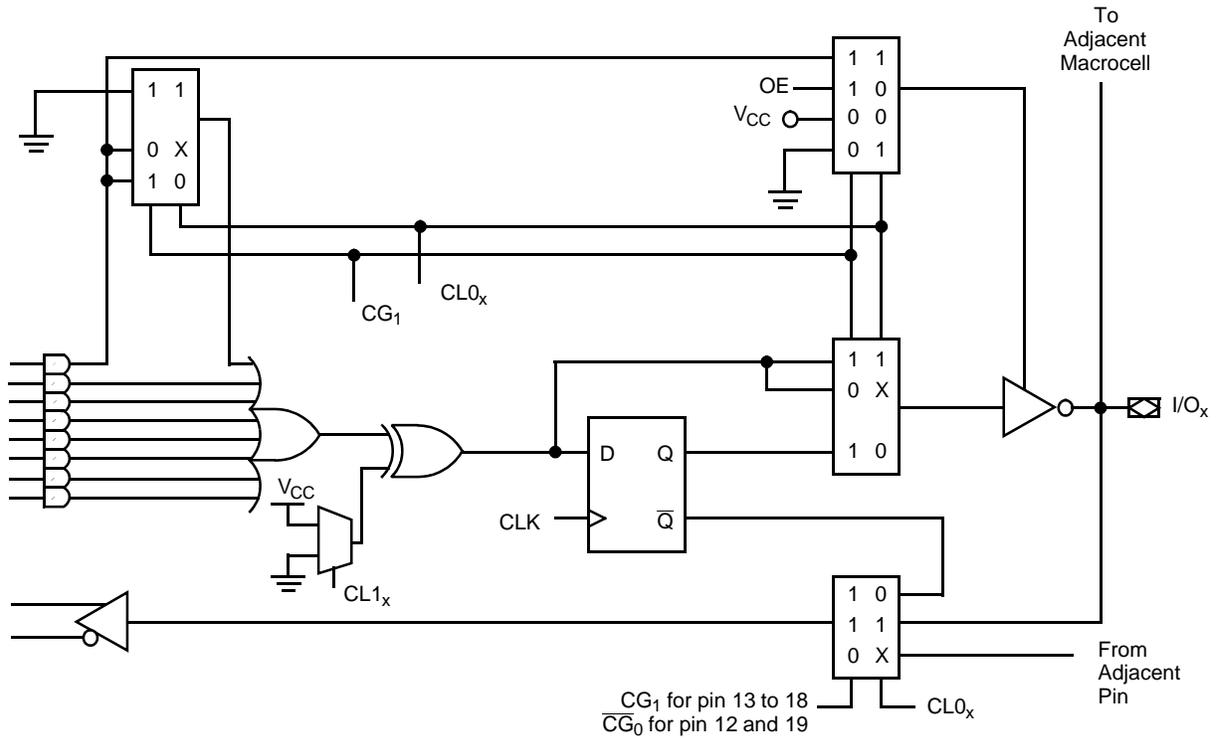
Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with
Power Applied...–55°C to +125°C

Supply Voltage to Ground Potential
(Pin 24 to Pin 12) .... –0.5V to +7.0V

DC Voltage Applied to Outputs
in High-Z State .... –0.5V to +7.0V

DC Input Voltage ....–0.5V to +7.0V

Output Current into Outputs (LOW)............................. 24 mA

DC Programming Voltage.. 12.5V

Latch-Up Current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±5%
Military[1]	–55°C to +125°C	5V ±10%
Industrial	–40°C to +85°C	5V ±10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = –3.2 mA	Com'l	2.4		V
			I_{OH} = –2 mA	Mil/Ind			
V_{OL}	Output LOW Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 24 mA	Com'l		0.5	V
			I_{OL} = 12 mA	Mil/Ind			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[3]			2.0		V
V_{IL} [4]	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[3]			–0.5	0.8	V
I_{IH}	Input or I/O HIGH Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$				10	µA
I_{IL} [5]	Input or I/O LOW Leakage Current	$0V \leq V_{IN} \leq V_{IN}$ (Max.)				–100	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., $V_{OUT} = 0.5V$[6, 7]			–30	–150	mA
I_{CC}	Operating Power Supply Current	V_{CC} = Max., $V_{IL} = 0V$, $V_{IH} = 3V$, Output Open, f = 15 MHz (counter)	5, 7 ns	Com'l		115	mA
			10, 15, 25 ns			90	mA
			15L, 25L ns			55	mA
			10, 15, 25 ns	Mil/Ind		130	mA
			15L, 25L ns	Mil.		65	mA
			15L, 25L ns	Ind.		65	mA

Capacitance[7]

| Parameter	Description	Test Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz	5	pF

Endurance Characteristics[7]

Parameter	Description	Test Conditions	Min.	Max.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions	100		Cycles

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. V_{IL} (Min.) is equal to –3.0V for pulse durations less than 20 ns.
5. The leakage current is due to the internal pull-up resistor on all pins.
6. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
7. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms
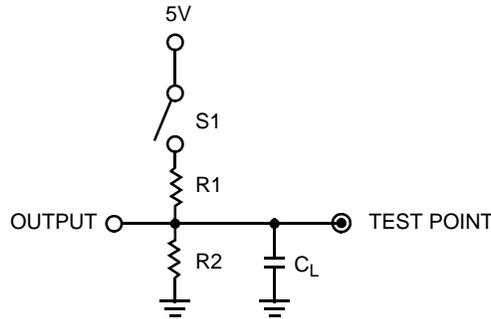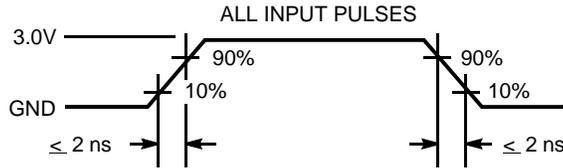
Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	200Ω	390Ω	390Ω	750Ω	1.5V
t_{PZX}, t_{EA}	Z · H: Open Z · L: Closed						1.5V
t_{PXZ}, t_{ER}	H · Z: Open L · Z: Closed	5 pF					H · Z: $V_{OH} - 0.5V$ L · Z: $V_{OL} + 0.5V$

Commercial and Industrial Switching Characteristics [2]

Parameter	Description	16V8-5		16V8-7		16V8-10		16V8-15		16V8-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[8, 9]	1	5	3	7.5	3	10	3	15	3	25	ns
t_{PZX}	OE to Output Enable	1	6		6		10		15		20	ns
t_{PXZ}	OE to Output Disable	1	5		6		10		15		20	ns
t_{EA}	Input to Output Enable Delay[7]	1	6		9		10		15		25	ns
t_{ER}	Input to Output Disable Delay[7, 10]	1	5		9		10		15		25	ns
t_{CO}	Clock to Output Delay[8, 9]	1	4	2	5	2	7	2	10	2	12	ns
t_S	Input or Feedback Set-up Time	3		5		7.5		12		15		ns
t_H	Input Hold Time	0		0		0		0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	7		10		14.5		22		27		ns

Shaded areas contain preliminary information.

Notes:
8. Min. times are tested initially and after any design or process changes that may affect these parameters.
9. This specification is guaranteed for all device outputs changing state in a given access cycle.
10. This parameter is measured as the time after OE pin or internal disable input disables or enables the output pin. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max.
11. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
12. This specification indicates the guaranteed maximum frequency at which the device can operate in data path mode.
13. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate.
14. This parameter is calculated from the clock period at f_{MAX} internal ($1/f_{MAX3}$) as measured (see Note 7 above) minus t_S.

Commercial and Industrial Switching Characteristics (continued)[2]

| Parameter	Description	16V8-5 Min.	16V8-5 Max.	16V8-7 Min.	16V8-7 Max.	16V8-10 Min.	16V8-10 Max.	16V8-15 Min.	16V8-15 Max.	16V8-25 Min.	16V8-25 Max.	Unit
t_{WH}	Clock Width HIGH[7]	3		4		6		8		12		ns
t_{WL}	Clock Width LOW[7]	3		4		6		8		12		ns
f_{MAX1}	External Maximum Frequency $(1/(t_{CO} + t_S))$[7, 11]	143		100		69		45.5		37		MHz
f_{MAX2}	Data Path Maximum Frequency $(1/(t_{WH} + t_{WL}))$[7, 12]	166		125		83		62.5		41.6		MHz
f_{MAX3}	Internal Feedback Maximum Frequency $(1/(t_{CF} + t_S))$[7, 13]	166		125		74		50		40		MHz
t_{CF}	Register Clock to Feedback Input[7, 14]		3		3		6		8		10	ns
t_{PR}	Power-Up Reset Time[7]	1		1		1		1		1		µs

Military Switching Characteristics[7]

Parameter	Description	16V8-10 Min.	16V8-10 Max.	16V8-15 Min.	16V8-15 Max.	16V8-25 Min.	16V8-25 Max.	Unit
t_{PD}	Input to Output Propagation Delay[8, 9]	3	10	3	15	3	25	ns
t_{PZX}	$\overline{OE}$ to Output Enable		10		15		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable		10		15		20	ns
t_{EA}	Input to Output Enable Delay[7]		10		15		25	ns
t_{ER}	Input to Output Disable Delay[7, 10]		10		15		25	ns
t_{CO}	Clock to Output Delay[8, 9]	2	7	2	10	2	12	ns
t_S	Input or Feedback Set-up Time	10		12		15		ns
t_H	Input Hold Time	.5		.5		.5		ns
t_P	External Clock Period $(t_{CO} + t_S)$	17		22		27		ns
t_{WH}	Clock Width HIGH[7]	6		8		12		ns
t_{WL}	Clock Width LOW[7]	6		8		12		ns
f_{MAX1}	External Maximum Frequency $(1/(t_{CO} + t_S))$[7, 11]	58		45.5		37		MHz
f_{MAX2}	Data Path Maximum Frequency $(1/(t_{WH} + t_{WL}))$[7, 12]	83		62.5		41.6		MHz
f_{MAX3}	Internal Feedback Maximum Frequency $(1/(t_{CF} + t_S))$[7, 13]	62.5		50		40		MHz
t_{CF}	Register Clock to Feedback Input[7, 14]		6		8		10	ns
t_{PR}	Power-Up Reset Time[7]	1		1		1		µs

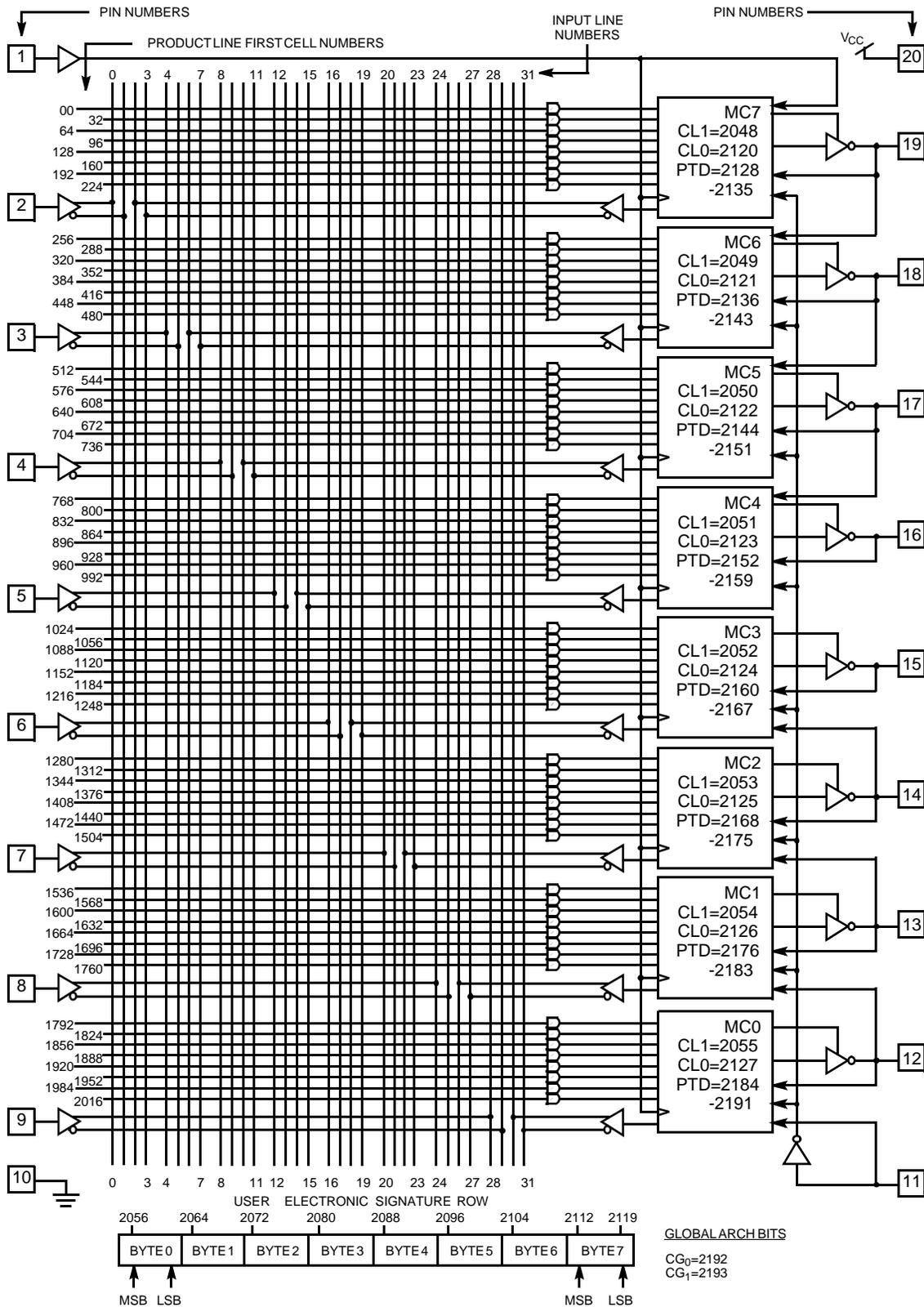## Switching Waveform
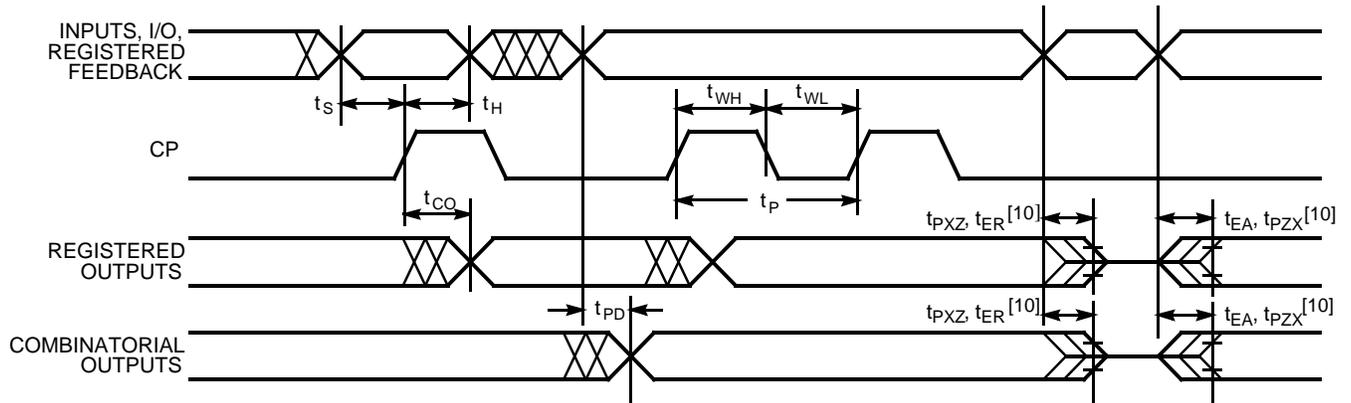
Power-Up Reset Waveform
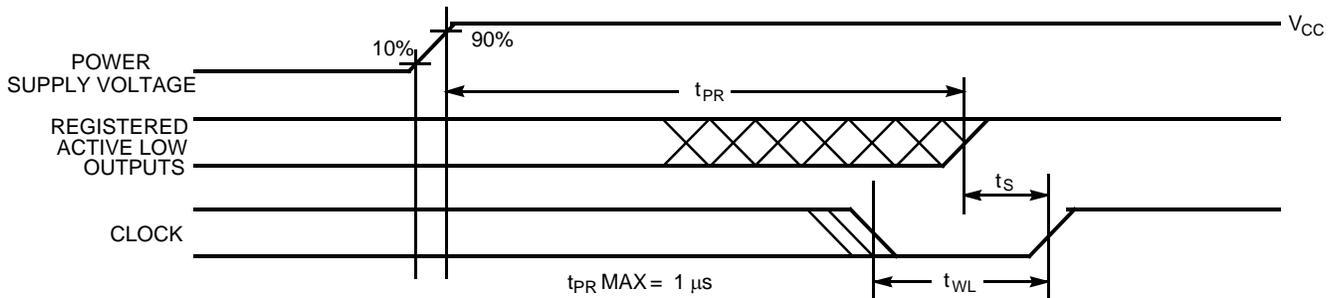
Functional Logic Diagram for PALCE16V8

Ordering Information

I_{CC} (mA)	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package Name	Package Type	Operating Range
115	5	3	4	PALCE16V8-5JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
115	7.5	5	5	PALCE16V8-7JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE16V8-7PC	P5	20-Lead (300-Mil) Molded DIP	
90	10	7.5	7	PALCE16V8-10JC	J61	20-Lead Plastic Leaded Chip Carrier	
				PALCE16V8-10PC	P5	20-Lead (300-Mil) Molded DIP	
130	10	7.5	7	PALCE16V8-10JI	J61	20-Lead Plastic Leaded Chip Carrier	Industrial
				PALCE16V8-10PI	P5	20-Lead (300-Mil) Molded DIP	
130	10	10	7	PALCE16V8-10DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALCE16V8-10LMB	L61	20-Pin Square Leadless Chip Carrier	
90	15	12	10	PALCE16V8-15JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE16V8-15PC	P5	20-Lead (300-Mil) Molded DIP	
130	15	12	10	PALCE16V8-15PI	P5	20-Lead(300Mil) Molded DIP	Industrial
				PALCE16V8-15DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALCE16V8-15LMB	L61	20-Pin Square Leadless Chip Carrier	
90	25	15	12	PALCE16V8-25JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE16V8-25PC	P5	20-Lead (300-Mil) Molded DIP	
130	25	15	12	PALCE16V8-25JI	J61	20-Lead Plastic Leaded Chip Carrier	Industrial
				PALCE16V8-25DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALCE16V8-25LMB	L61	20-Pin Square Leadless Chip Carrier	
55	10	7.5	7	PALCE16V8L-10JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE16V8L-10PC	P5	20-Lead (300-Mil) Molded DIP	
65	10	10	7	PALCE16V8L-10JI	J61	20-Lead Plastic Leaded Chip Carrier	Industrial
				PALCE16V8L-10PI	P5	20-Lead (300-Mil) Molded DIP	
55	15	12	10	PALCE16V8L-15JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE16V8L-15PC	P5	20-Lead (300-Mil) Molded DIP	
65	15	12	10	PALCE16V8L-15DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALCE16V8L-15LMB	L61	20-Pin Square Leadless Chip Carrier	
55	25	15	12	PALCE16V8L-25JC	J61	20-Lead Plastic Leaded Chip Carrier	Commercial
				PALCE16V8L-25PC	P5	20-Lead (300-Mil) Molded DIP	
65	25	15	12	PALCE16V8L-25DMB	D6	20-Lead (300-Mil) CerDIP	Military
				PALCE16V8L-25LMB	L61	20-Pin Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

MILITARY SPECIFICATIONS
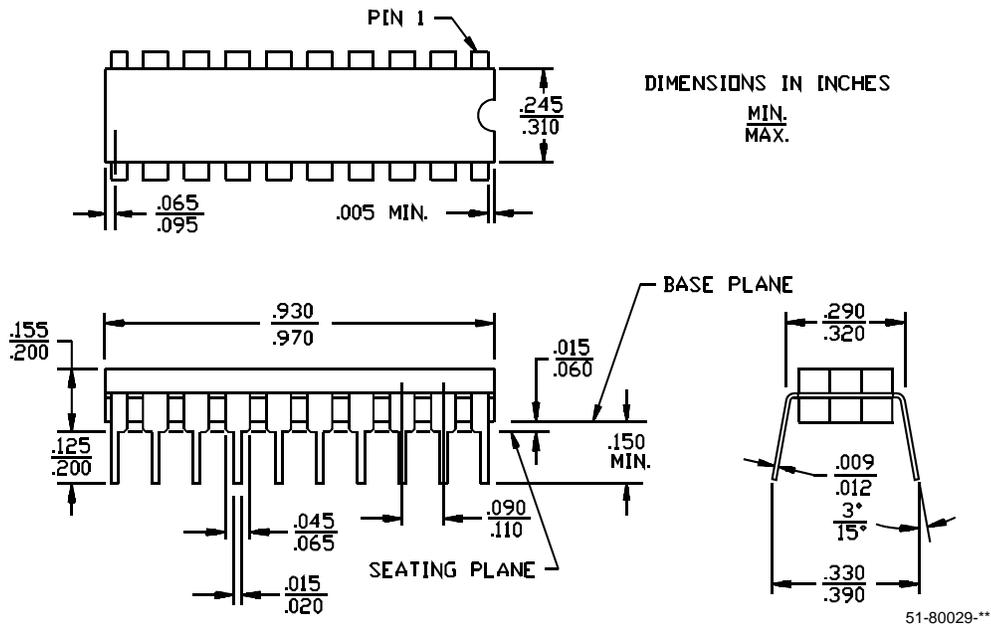## Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

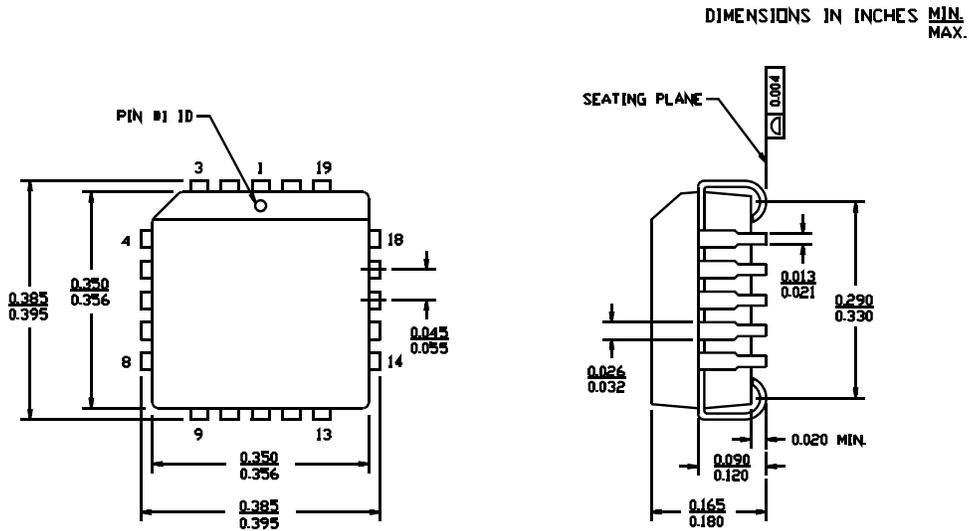| Parameter	Subgroups
t_{PD}	9, 10, 11
t_{CO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11

Package Diagrams

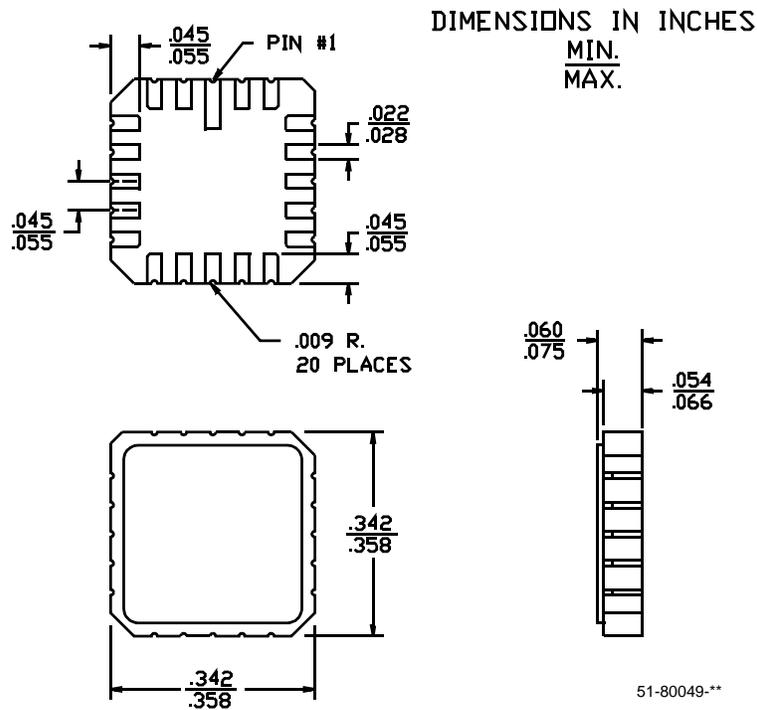### 20-Lead (300-Mil) CerDIP D6
MIL-STD-1835 D-8 Config. A

51-80029-**

Package Diagrams (continued)
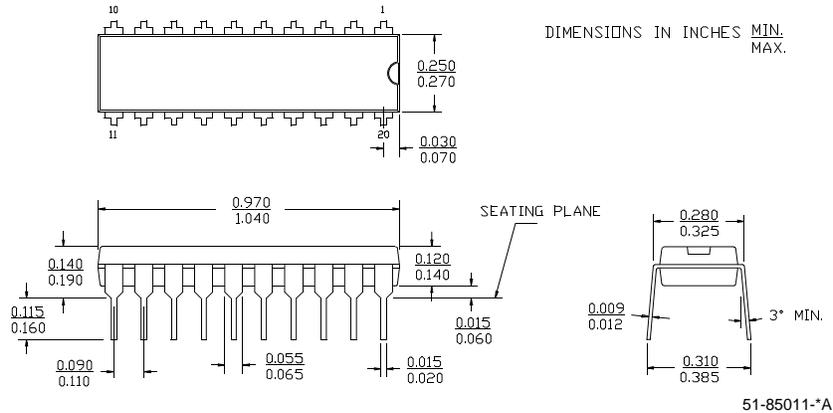
20-Lead Plastic Leaded Chip Carrier J61

DIMENSIONS IN INCHES $\frac{MIN.}{MAX.}$

51-85000-*A

20-Square Leadless Chip Carrier L61

DIMENSIONS IN INCHES
$\frac{MIN.}{MAX.}$

51-80049-**

Package Diagrams (continued)

20-Lead (300-Mil) Molded DIP P5

DIMENSIONS IN INCHES $\frac{MIN.}{MAX.}$

51-85011-*A

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Document History Page

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REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106370	07/11/01	SZV	Change from Spec Number: 38-00364 to 38-03025
*A	213375	See ECN	FSG	Added note to title page: "Use Ultra37000 For All New Designs"