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Take Note!

Before using this information and the product it supports, be sure to read the general information under "Special Notices" on page xv.

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This edition applies to the various PS/2 and PS/ValuePoint models as of December, 1992.

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Abstract

This document describes various hardware subsystems of the IBM PS/2 and PS/ValuePoint product range.

It explains the SCSI (Small Computer Systems Interface) standard and the implementation of SCSI in PS/2 computers as well as the IDE (Integrated Drive Electronics) standard and the IDE implementation in PS/ValuePoint computers. The video subsystems XGA (Extended Graphics Adapter) and XGA-2 as found in PS/2s and the SVGA implementations of the PS/ValuePoint systems are described. In addition, this document gives an overview on security standards and security features as implemented in some PS/2 models.

This document is intended for IBM customers and systems engineers who need an understanding of the various hardware subsystems found in PS/2 and PS/ValuePoint systems.

PS (147 pages)

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Special Notices

This publication is intended for IBM customers and IBM systems engineers to provide an introduction to the various PS/2 Subsystems. The information in this publication is not intended as the specification of any programming interfaces that are provided by the PS/2 subsystems. See the PUBLICATIONS section of the IBM programming announcement for the PS/2 products for more information about what publications are considered to be product documentation.

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Preface

This document is intended to provide an overview of the various subsystems that make up the IBM PS/2 and IBM PS/ValuePoint systems. It contains information on SCSI, IDE, XGA-2, SVGA, C2 Security and the various standards that govern them.

This document is intended for persons requiring an overview and a quick reference for the various subsystems.

How This Document is Organized

The document is organized as follows:

- Chapter 1, "What is SCSI"

  This chapter describes the various functions and features that SCSI provides and how they all work together.

- Chapter 2, "IBM Implementation of SCSI"

  This chapter describes the IBM implementation of SCSI.

- Chapter 3, "Integrated Drive Electronics (IDE)"

  This chapter discusses the IDE (Integrated Drive Electronics) standard, also known as the AT Attachment (ATA) interface.

- Chapter 4, "XGA-2 Video Subsystem"

  This chapter describes the XGA video subsystem, and how IBM has implemented it.

- Chapter 5, "Programming the XGA"

  This section discusses some programming aspects of XGA.

- Chapter 6, "SVGA Video Subsystems"

  This chapter discusses the SVGA subsystems that are implemented on the IBM PS/ValuePoint range.

- Chapter 7, "Processor Complexes"

  This chapter describes the processor upgrade options available for the PS/2 and PS/ValuePoint range.

- Chapter 8, "C2 Security"

  This chapter discusses the C2 Security guidelines, and how IBM has implemented some of these guidelines in the PS/2 range.

- Chapter 9, "Standards"

  This chapter is an overview of the ISO 9241 standard, as well as the VESA standards.

- Appendix A, "Video Comparison"

  This appendix compares the PS/2 XGA-2 video interface to the PS/ValuePoint SVGA interface.

- Appendix B, "Feature Comparisons"

  This appendix compares the various features as found in some PS/2 and PS/ValuePoint computers.

- Appendix C, "POST Error Codes"

  This appendix contains a listing of POST (power-on self test) error codes.

- Appendix D, "IBM SCSI POST Error Codes"

  This appendix lists all IBM SCSI error codes that may be shown during power-on self test (POST) of a PS/2.

Related Publications

The following publications are considered particularly suitable for a more detailed discussion of the topics covered in this document.

- *ET4000 Graphics Controller, High Performance Video Technology*, Including Revision G, dated 1992, published by Tseng Labs, Inc., Newton, PA 18940
- *TrueColor VGA Family - CLGD5422, Technical Reference Manual*, dated June 1992 and published by Cirrus Logic, Inc., Fremont, CA 94538
- *IBM PS/VP 386 SVGA Drivers/Utilities User's Guide*, IBM Part Number 53G0178
- *IBM PS/VP 486 SVGA Drivers/Utilities User's Guide*, IBM Part Number 53G0165
- *ATA/IDE Fixed Disk Drives Technical Reference*, dated 1992 American National Standard for Information Systems,
- *ATA (AT Attachment)*, dated November 1992, Irvine, CA 92714

The *Technical Reference Library* is intended to be used by individuals who develop hardware and software products for PS/2 systems. These individuals should understand computer architecture and programming concepts. The current IBM Personal System/2 Technical Reference library contains the following manuals (followed by a list of updates):

1. *IBM Personal System/2 Hardware Interface Technical Reference - Architectures*

   This manual describes IBM architectures used by Personal System/2 products.

   - Form Number S84F-9808-00, Part Number 84F9808
   - *9/92 Update*

     Form Number S10G-6466-00, Part Number 10G6466
   - *Supplement (Subsystem Control Block Architecture)*

     Form Number S85F-1678-00, Part Number 85F1678

2. *IBM Personal System/2 Hardware Interface Technical Reference - Common Interfaces*

   This manual describes devices and interfaces that are common to Personal System/2 Micro Channel systems.

   - Form Number S84F-9809-00, Part Number 84F9809
   - *9/91 Update*

Form Number S04G-3281-00, Part Number 04G3281

- *6/92 Update (DMA)*

  Form Number S10G-6464-00, Part Number 10G6464

3. *IBM Personal System/2 Hardware Interface Technical Reference - System-Specific Information*

   This manual describes specific models of Personal System/2 Micro Channel systems.

   - Form Number S84F-9807-00, Part Number 84F9807
   - *6/92 Update (90/95)*

     Form Number S41G-3108-00, Part Number 41G3108
   - *6/92 Update (76/77)*

     Form Number S41G-3108-00, Part Number 41G3108
   - 10/92 Update (56/57)

     Form Number S42G-0558-00, Part Number 42G0558

4. *IBM Personal System/2 Hardware Interface Technical Reference - Non-Micro Channel Computers*

   This manual describes the common interfaces and system-specific information for the Personal System/2 AT-Bus systems.

   - Form Number S85F-1646-00, Part Number 85F1646
   - *3/92 Update (35/40)*

     Form Number S41G-2950-00, Part Number 41G2950
   - *3/92 Update*

     Form Number S41G-5096-00, Part Number 41G5096

5. *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference*

   This manual describes Personal Computer and Personal System/2 BIOS and Advanced BIOS.

   - Form Number S04G-3283-00, Part Number 04G3283
   - *9/92 Update*

     Form Number S10G-6467-00, Part Number 10G6467

6. *IBM Personal System/2 Hardware Interface Technical Reference - Video Subsystems.*

   This manual describes the common interfaces and video-specific information for the XGA Video subsystems.

   - Form Number S42G-2193-00

International Technical Support Center Publications

A complete list of International Technical Support Center publications, with a brief description of each, may be found in:

- *Bibliography of International Technical Support Centers Technical Bulletins,* GG24-3070.

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Chapter 1. What is SCSI

This chapter explains the Small Computer System Interface (SCSI).

1.1 SCSI - A Brief Overview

SCSI (usually pronounced "scuzzy") stands for Small Computer System Interface. It is fully documented in ANSI standard X3.131-1986.

SCSI is a standard interface bus through which computers may communicate with attached intelligent peripheral devices such as fixed disks, CD-ROMs, printers, plotters, scanners, etc.

With SCSI, a large number of devices of different types can be connected to the system unit via a single SCSI bus cable and a SCSI attachment feature. This SCSI attachment feature may be in the form of an adapter or an integrated unit on the planar board. The SCSI interface is also device independent, allowing the user to attach intelligent devices of any form that adhere to the SCSI standard. Overall, SCSI means less cabling and saves valuable attachment space in the personal computer by having one SCSI attachment feature to support multiple devices.

Up to a maximum of seven devices can be directly attached to the SCSI bus cable and each of these devices can support up to eight more. This means that it is possible for one SCSI attachment feature to support up to 56 devices. This gives the user the benefit of an extremely flexible method of attaching peripheral devices to his system unit.

Other features of SCSI, such as arbitration and disconnect/reconnect, allow several devices to be operating concurrently and to efficiently share the SCSI bus. This is an obvious benefit in a multitasking environment.

With the SCSI interface, high data transfer rates allow enhanced performance over other, non-SCSI systems.

1.2 SCSI Standards

The American National Standards Institute (ANSI) has a subcommittee responsible for developing the SCSI standard. There are three SCSI standards defined, SCSI I, SCSI II, and SCSI III. Each new standard is required to be compatible with the previous standard. Only SCSI is a formal standard, while SCSI II and SCSI III are draft proposals.

The IBM* implementation of SCSI follows the standard of SCSI I and IBM will only provide formal support for devices that comply with the SCSI I standard. However, it will allow certain devices of the SCSI II standard to attach, due to the fact that some of the features of SCSI II are included in the IBM implementation. This is not supported, however. The following table outlines briefly some of the key differences between the SCSI I standard and the draft proposals SCSI II and III.

Table 1. Comparison between SCSI I, II and III

Attribute	SCSI I X3.131-1986	SCSI II X3.131-199X	SCSI III
SCSI Bus Width	8 bit	8,16,32 bit	8,16,32 bit Parallel (Serial Optional)
Cabling	50 Pin "A" Cable	50 Pin "A" Cable, 68 Pin "B" Cable	50 Pin "A" Cable, 68 Pin "B" Cable, 68 Pin "P" Cable (16 Bits Data), 68 Pin "Q" Cable (Extra 16 Bits Data)
Data Rate			
8 bit	5 MBps	5 MBps (10-FAST[2])	
16 Bit	N/A	10 MBps (20-FAST[2])	10 MBps (20-FAST[2])
32 Bit	N/A	20 MBps (40-FAST[2])	20 MBps (40-FAST[2])
Parity	Optional	Mandatory	Mandatory
Tagged Command Queueing (TCQ)	N/A	Optional	Optional
Command Sets, MSG Sets	CCS[1] for DASD Addendum 4.B	CCS[1] as Part of Standard, also for non-DASD	

Note:

[1] CCS is the SCSI Common Command Set

[2] FAST is a data transfer method as defined in SCSI II

N/A = not available

1.3 The SCSI Interface

A normal personal computer setup for SCSI consists of a SCSI attachment feature and one cable connecting it to multiple intelligent devices. Both the SCSI attachment feature and the attached devices must conform to the SCSI ANSI standard X3.131-1986. The SCSI interface is the "means of communication" between the SCSI attachment feature and the attached intelligent devices.

There are two main types of interfaces for attaching devices. These are device level interfaces and bus level interfaces.

1.3.1 Device Level Interface

With a device level interface such as ESDI or ST-506 for fixed disks, the controlling circuitry is held on a separate adapter away from the physical drive. This means that the formatting, head select, error detection etc. is done on the adapter and *not* on the device itself, in this case a fixed disk. All the device does is the actual mechanical operation of reading and writing the data. Figure 1 on page 3 shows a device level interface. This is also referred to as a "dumb device".

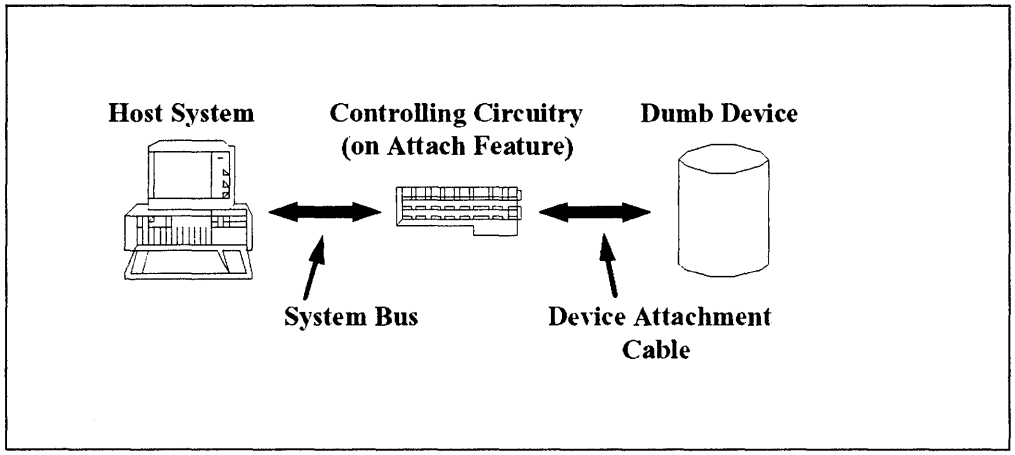

Figure 1. Device Level Interface

This makes it very hard to create new devices, as what the device can do is determined by what the controller will allow it to do. Plus, the type of device that can be attached to one controller is limited. This is because it would be impossible for one controller to hold all of the circuitry to control CD-ROMs, fixed disks etc. This means that in order to attach multiple devices multiple adapters would be needed, which is both expensive and takes up valuable attachment space on a personal computer.

1.3.2 Bus Level Interface

With a bus level interface, the controlling circuitry is built into the device's own electronics. This means that the drive itself has most of the intelligence for formatting, error detection etc.

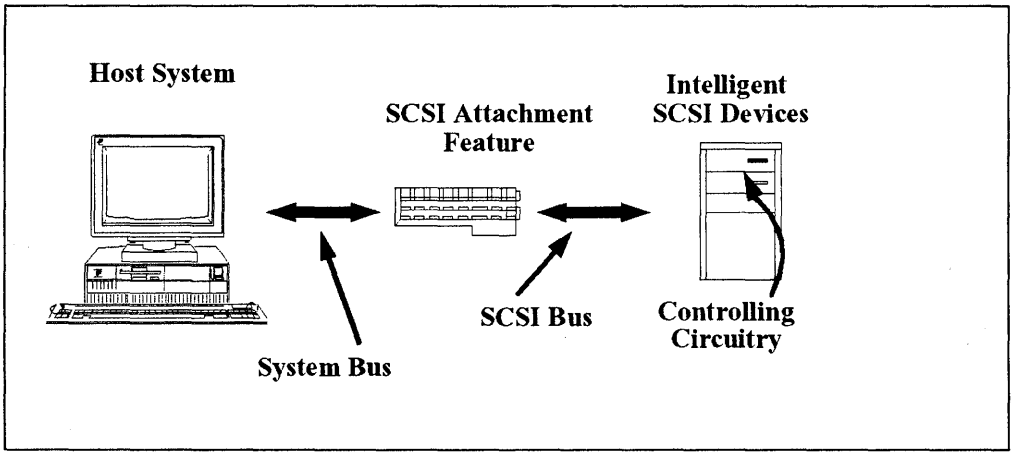

Figure 2. Bus Level Interface

SCSI is a bus level interface. It describes the interface between a SCSI attachment feature and an attached intelligent device. This gives device independence and allows devices of any nature to be attached to one attachment feature. As SCSI is also a defined ANSI standard, it minimizes the integration problems often found on today's non-SCSI systems.

1.4 SCSI "Overall" Configuration

The basic SCSI configuration is as follows.

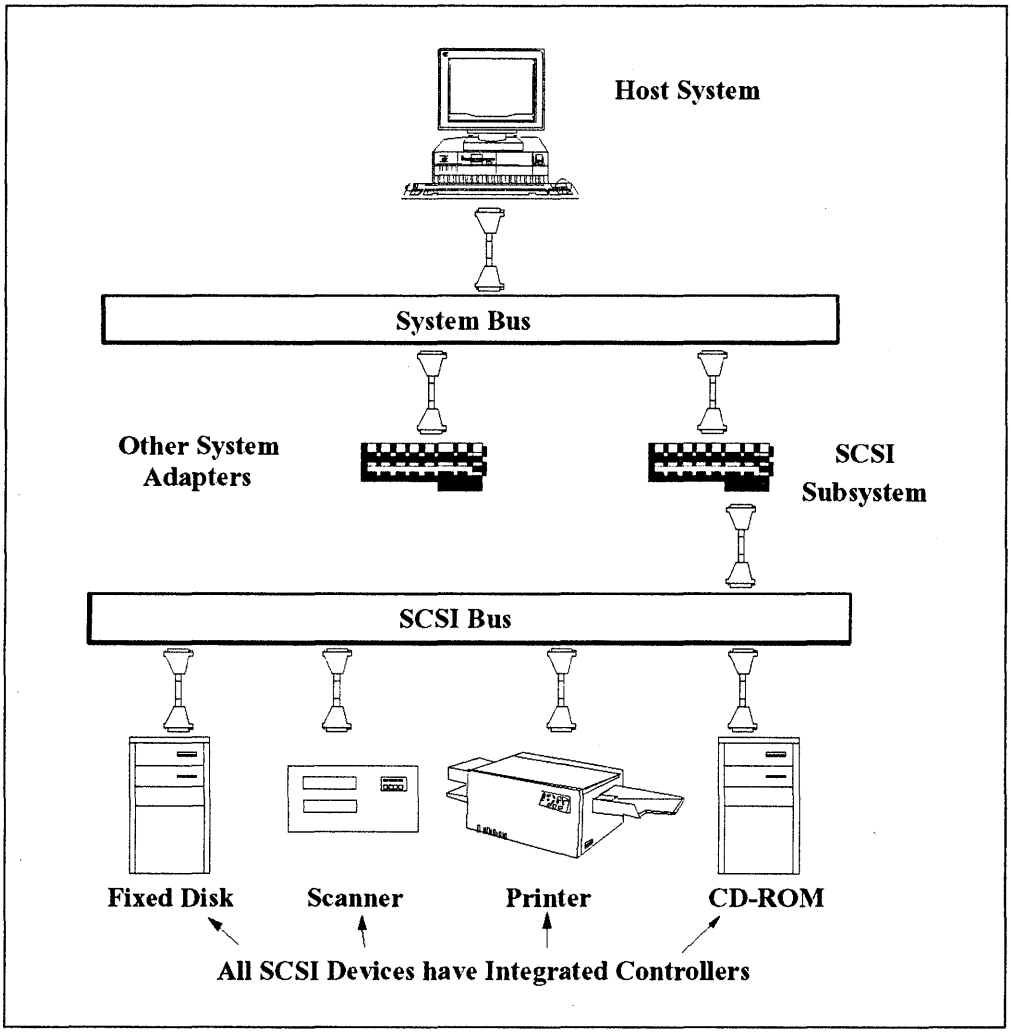

Figure 3. SCSI Overall Configuration

A SCSI attachment feature is connected to the system bus.

Attached to the SCSI attachment feature are multiple intelligent peripheral devices such as fixed disks, CD-ROMs, printers etc. They are connected via a single 50-conductor cable commonly known as the "SCSI bus". This SCSI bus is an 8-bit parallel bus monitored by logic on the SCSI attachment feature.

Each of the devices attached to the SCSI bus and the SCSI attachment feature itself conform to the ANSI standard X3.131-1986. This ANSI standard specifies the mechanical, electrical and functional requirements and the command sets used by devices in the SCSI setup.

1.5 SCSI Physical Configuration

The physical configuration of SCSI includes at least one SCSI attachment feature, a 50-conductor connecting cable (the "SCSI bus") and one or more SCSI devices up to the maximum defined by the standard.

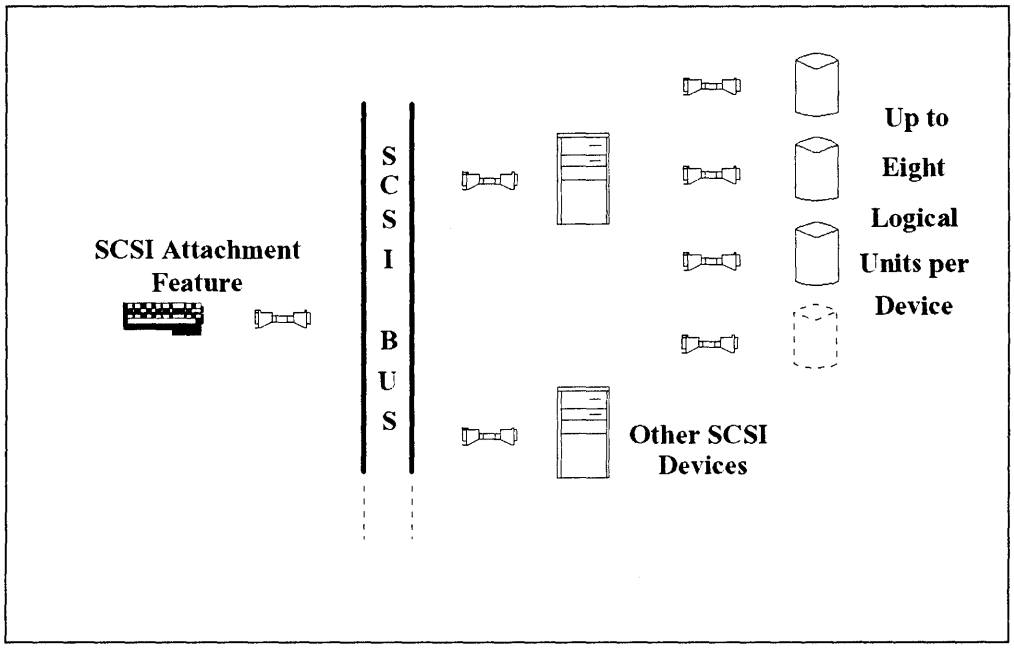

Figure 4. SCSI Physical Configuration

1.5.1 The 50-conductor Cable or "SCSI Bus"

In Figure 4, the SCSI bus is the 50-conductor cable. This cable consists of a set of eight data lines, a data parity line and various control lines. All of the signals carried on this cable are defined in the SCSI ANSI specifications. In all SCSI configurations this bus must be terminated at both ends. In the case where there is an internal and an external bus, logically it is all seen as one long bus and so termination points will only be at the end of the internal bus and the end of the external bus.

The 50-conductor cable itself daisy-chains the various devices. This means that each device has a cable going into and coming out of it (plus a power cable), apart from the last device in the chain which has the incoming cable plus a terminator at the outgoing connector.

The maximum length supported for the SCSI bus is six meters. This means that the distance between the SCSI attachment feature and the last SCSI device on the SCSI bus can be no longer than six meters. This is because most SCSI attachment features on personal computers support a "single-ended" bus, which uses a voltage line that changes between 0-5 volts. With such a small range of change, six meters is the longest distance before the bus may be affected by noise.

There is a set of SCSI attachment features that support a "differential" bus. These can have much longer buses (up to 25 meters) because they use a much wider voltage change range (above or below 0 volts). They are, however, much more expensive and not common in the personal computer arena.

1.5.2 SCSI Devices - Configuration

Each of the devices directly attached to the SCSI bus is known as a SCSI device. Each one has an ID number which is unique on its bus and is called the SCSI ID. This is set via hardware switches or jumpers located on the SCSI device. The SCSI attachment feature itself also has a SCSI ID number (1.6.1, "SCSI Device Addressing" describes the function of these ID numbers).

Each SCSI attachment feature supports up to seven SCSI devices. In addition, each SCSI device can support up to eight logical units. This means that each SCSI attachment feature can support up to 56 devices (see 1.6.2, "Logical Units (LUs)" on page 7).

1.6 SCSI Logical Configuration

The following sections describe the internal workings of SCSI, including how it addresses the various SCSI devices, command signals and other features of the interface.

1.6.1 SCSI Device Addressing

Each device attached directly to the SCSI bus is known as a SCSI device. It is assigned a SCSI ID number from 0 to 7. This ID has two main uses:

1. Allows devices to be selected.

   With each SCSI device and the SCSI attachment feature being assigned a unique ID, it is impossible for a device to receive commands that are really meant for another device. It enables, for example, the SCSI attachment feature to talk easily to any SCSI device attached to the SCSI bus.

2. Sets the priority of the device during arbitration.

   As there are many devices wishing to use the SCSI bus, a scheme has to be used to work out who can use the bus at any one time. This is called arbitration and will be covered in 1.6.5, "SCSI Bus Arbitration" on page 9. The SCSI ID determines the priority of the device during arbitration.

Note: The SCSI attachment feature is usually assigned a SCSI ID of 7. This ID has the highest priority.

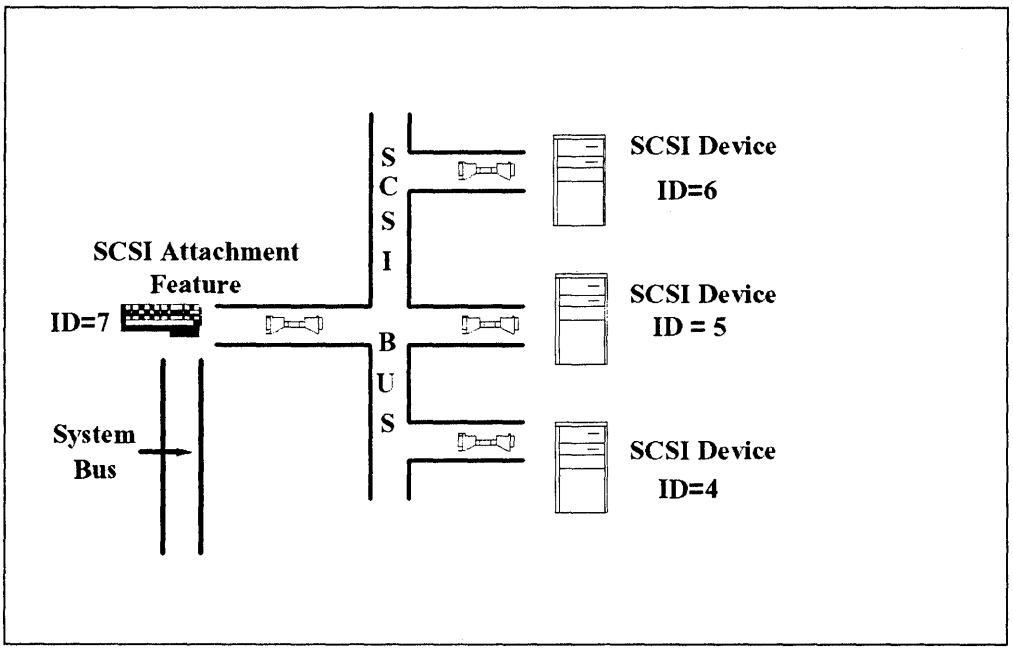

Figure 5. SCSI Device Addressing

The ID number of a particular SCSI device is set during configuration of the particular device. As was seen in 1.5.2, "SCSI Devices - Configuration" on page 6, this is set by hardware switches on the device.

1.6.2 Logical Units (LUs)

The SCSI attachment feature may allow each SCSI device to have attached up to eight logical units (LUs). These logical units are controlled by a SCSI device. The logical units are *not* attached directly to the SCSI bus. Instead they are attached to a SCSI device.

Figure 6 serves as an example.

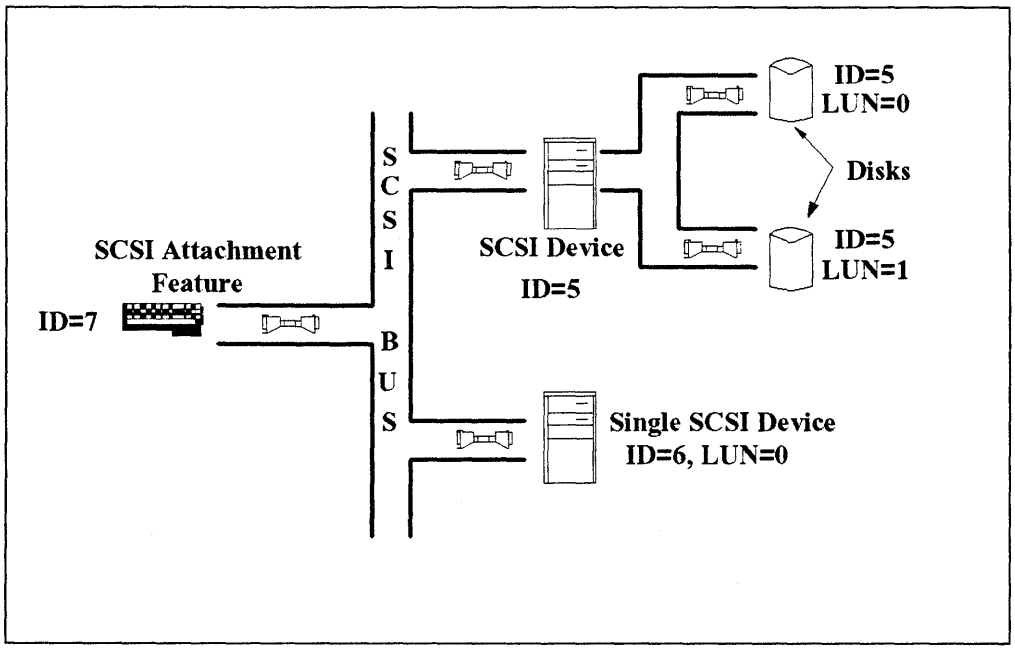

Figure 6. SCSI Logical Units

SCSI device 5 in Figure 6 on page 7 is a SCSI to ESDI controller. This means that the controller would be attached to the SCSI bus as a SCSI device and then the ESDI part of the controller would attach to up to eight ESDI drives. None of these ESDI drives would be attached directly to the SCSI bus. They would be attached to the SCSI device. Therefore, they would *not* be SCSI devices; they would be LUs.

It is easiest to think of the controllers as the SCSI device (or the controlling circuitry as the SCSI device) and the device itself (that is, a disk actuator) as the logical unit. In order for any device to be accessed, a pair of addresses will be needed: a SCSI device number and a logical unit number.

As an example, here is how a SCSI attachment feature would send a command across the SCSI bus to the second ESDI drive.

1. The SCSI attachment feature selects a SCSI device. In this example it selects SCSI device 5.
2. The SCSI attachment feature then sends a command to SCSI devices.
3. The command contains a 3-bit field, which indicates a logical unit number. In this case the 3-bit field would contain the number 1.
4. When SCSI device 5 receives the command, it reads the 3-bit field and passes on the command instructions to the logical unit number specified. In this example, it would be logical unit number 1.

In the case of a single integrated unit where it is impossible to distinguish between controller circuitry and device circuitry, this form of addressing still applies. It is the same even though it does not support any extra LUs. For example, a write command for SCSI device 6 in Figure 6 on page 7 would be sent to SCSI device 6, LUN 0.

Note: The LUs defined here bear no relationship to LUs referred to in a Systems Network Architecture (SNA) communications environment.

1.6.3 Initiators and Targets

When two SCSI devices talk to each other on the SCSI bus, one sends out a command and one acts upon it. The SCSI device that sends out the commands is called an *initiator*. The SCSI device that processes the command is called the *target*.

1.6.4 Device-Level Copying

With SCSI, it is possible to have more than one initiator attached to the SCSI bus. This means that two devices can talk to each other on the SCSI bus without the SCSI attachment feature doing the data transfer.

For example, assume there is a SCSI device such as a tape drive, that is capable of being an initiator and a target. The SCSI attachment feature could send the tape drive a command to copy information from the tape to a fixed disk also attached to the SCSI bus (at this point the tape drive will be a target). Once it has read the data from the tape, it than can become an initiator and send a write command to the fixed disk in order to write the tape data to the fixed disk. This is all done *without* further involvement of the SCSI attachment feature.

1.6.5 SCSI Bus Arbitration

SCSI, because of the nature of its design, specifies a scheme for bus arbitration. Bus arbitration is required where multiple devices attached to a bus (in this case the SCSI bus) can bid to gain control of the bus and perform their data transfer.

On the SCSI bus, arbitration is controlled by logic on the SCSI attachment feature. Arbitration on the SCSI bus can be initiated by any SCSI device on the bus provided that it has this capability built in.

Arbitration works as follows: The SCSI device that wants to use the SCSI bus puts its SCSI ID number onto the bus. It checks to see if there is a device with a higher SCSI ID bidding for the bus. If there is no SCSI ID higher, the SCSI device gains control of the bus. If a higher SCSI ID is on the SCSI bus, then the other SCSI device would gain control of the SCSI bus.

More information on arbitration can be found in Figure 9 on page 12.

1.6.6 Disconnect/Reconnect and Overlapped Command Processing

As soon as a target has received a command, it can disconnect from the bus. This means that an initiator is free to send commands to another target while the previous target is still processing the commands it received before.

Figure 7 below shows the various stages in a common disconnect and reconnect cycle.

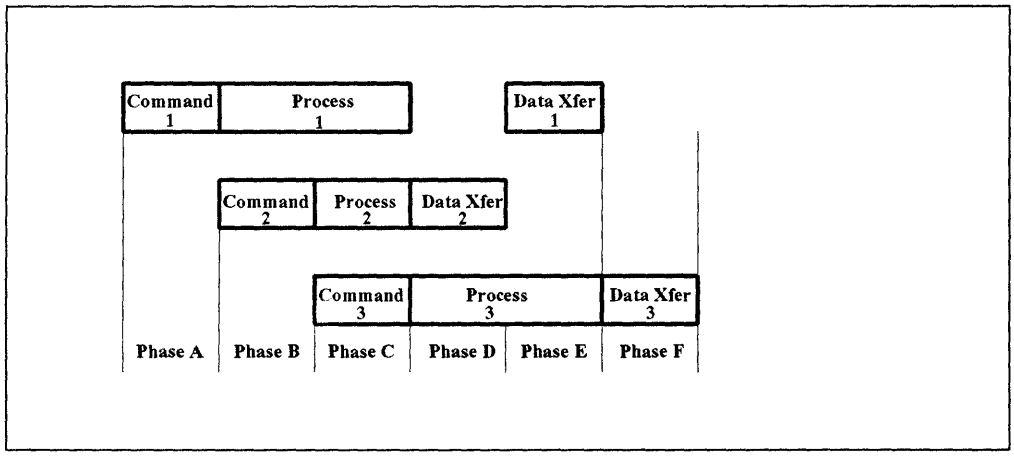

Figure 7. Overlapped Command Processing on the SCSI Bus

PHASE A The SCSI attachment feature sends a command to SCSI device 1. After device 1 has received the command, device 1 disconnects from the SCSI bus.

PHASE B The SCSI attachment feature now sends a command to SCSI device 2. After device 2 has received the command, device 2 disconnects from the SCSI bus. At the same time SCSI device 1 is still processing its command.

PHASE C The SCSI attachment feature now sends a command to SCSI device 3. After device 3 has received the command, device 3 disconnects from the SCSI bus. At the same time SCSI devices 1 and 2 are still processing their commands.

PHASE D SCSI devices 1 and 2 both finish their processing and arbitrate for the SCSI bus, in order to reconnect to it and perform a data transfer. SCSI device 2 wins as it has the higher ID number and device 2 performs its data transfer. SCSI device 3 is still processing its command.

PHASE E SCSI device 1 now arbitrates for the bus and takes control in order to do its data transfer. SCSI device 3 is still processing its command.

PHASE F SCSI device 3 now arbitrates for the bus, wins and performs its data transfer.

This processing of multiple commands at a time is known as overlapped command processing. Many SCSI attachment features only support overlapped command processing of a certain number of commands. For example, the IBM SCSI attachment feature supports overlapped command processing for up to 15 logical units. This means that the maximum number of devices that can be processing commands at any one time is 15.

1.6.7 Synchronous and Asynchronous Data Transfer

There are two modes of data transfer supported across the SCSI interface. These are asynchronous and synchronous modes of data transfer.

- Asynchronous mode

  In this mode each byte of data sent between the initiator and the target must be requested and acknowledged. For example, an initiator cannot send another byte of data until the target acknowledges that it has received the previous one. This series of "handshakes" makes this the slower of the two modes with maximum transfer rates across the SCSI bus of around 3 MBps.

- Synchronous mode

  In this mode multiple bytes of data can be transferred before acknowledgments are received. For example, 512 bytes of data can be transferred and during these transfers acknowledgements are being received, but not at a regular interval, as with the asynchronous mode. At the end of the transfer, the number of acknowledgments received is counted and provided there are 512 of them the transfer is regarded as being successful. This mode is much faster and allows for data transfer speeds across the SCSI bus of up to 5 MBps.

  It is up to the initiator to check to see if the target is capable of doing synchronous transfers. Most of the SCSI attachment features do support synchronous transfers, but some SCSI devices only support the asynchronous mode of data transfer.

1.7 Commands Sent Across the SCSI Bus

For a target to perform an operation, an initiator must successfully arbitrate for use of the bus, select the appropriate SCSI device and transfer the command to be executed. The command transferred across the SCSI bus is known as a SCSI command. The format that it takes is that of a Command Descriptor Block. The diagram below shows a typical block layout.

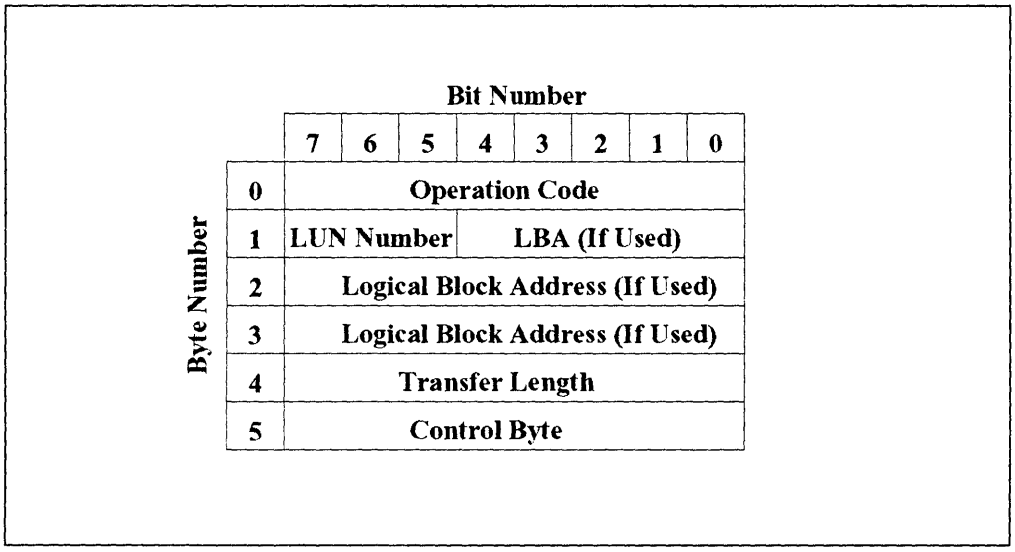

Figure 8. SCSI 6-Byte Command

Figure 8 shows the layout for a 6-byte SCSI command. The layout is also similar for 10-byte SCSI commands.

The 10-byte SCSI commands are known as extended commands. They are used when information being passed to the target will not fit in the normal 6-byte command block.

SCSI commands are precisely defined instructions in the SCSI ANSI standard. When SCSI was first defined, a large number of SCSI commands were defined. The number was considered too large for a common standard to be set so a subset of them was used as a standard for direct access storage devices (DASD). This suite of commands is known as the SCSI Common Command Set or CCS.

With the SCSI commands, the user does not have to know how each of the different SCSI devices function internally. Knowledge of which SCSI commands the device understands is enough to be able to use the device at SCSI device level.

Many devices will support commands not included in the CCS and it is up to the individual to check that both the SCSI attachment feature and the target device support these extra commands.

1.8 How Does the SCSI Bus Work

The SCSI bus is, similar to a personal computer bus, capable of many different states. These states are known as phases and the SCSI bus is architected to include seven distinct phases. The SCSI bus can never be in more than one phase at any given time.

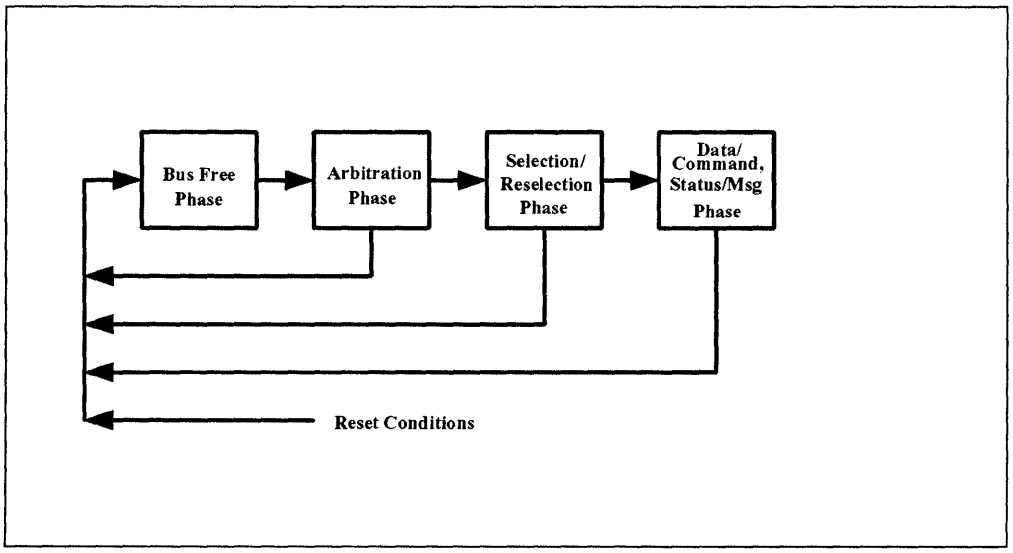

Figure 9. SCSI Bus Phases

During each of the phases shown in Figure 9, the devices attached to the SCSI bus are able to perform certain tasks. These phases are described below in detail.

Bus-free phase: When the SCSI bus is in this phase, it indicates that no SCSI device (initiator or target) is using the SCSI bus and that it is available for any user. Any interaction that is to take place on the bus between SCSI devices can begin only when the SCSI bus is in the bus-free phase.

Arbitration phase: This phase allows one SCSI device to gain control of the SCSI bus so that it can assume the role of an initiator. How it gains control of the bus is as follows:

1. The device waits for the bus free phase to occur.
2. The device now arbitrates for the SCSI bus by doing two things. It changes the status of the busy line on the SCSI bus to busy. At the same time it activates one of the lines of the data bus on the SCSI bus. Because the SCSI bus can carry eight bits of data at a time, there are eight data lines. This means that each SCSI device can use one of these lines during arbitration. For example, if the SCSI device with an ID of 6 was arbitrating for the SCSI bus, the sixth data line would be activated.
3. The device then waits for a period (an arbitration delay), during which it examines the SCSI data bus. If a higher priority SCSI ID is on the bus (where 7 is the highest), the device has lost the arbitration and must start again at point 1. If no higher priority SCSI device ID was found on the data bus, the SCSI device has won arbitration, gained control of the SCSI bus and proceeds to the selection or reselection phase.

Selection/Reselection Phase: The device that has control of the SCSI bus will place its own ID and that of the target SCSI device on the bus. The target device will automatically recognize that it has been selected when it detects a certain bus condition and that its own SCSI ID is represented on the data bus. It then confirms to the initiator that it has been successfully selected and allows the initiator to enter the message or command phase.

Command Phase: This is the phase during which there is a transfer of information from the initiator to the target. It is *always* from the initiator to the target. The target requests information and the initiator puts the necessary values onto the SCSI data bus. The target then reads the data off the data bus.

The target continues to request more data in this way until it has read the specified number of bytes of information. This number is always the first part of the command descriptor block (see Figure 8 on page 11).

Data In/Out Phase: This is when the *data* transfer takes place. Data is sent either from the initiator to the target or from the target to the initiator.

Status Phase: In this phase the target sends a status byte to the initiator. This byte indicates the completion of the command.

Message Phase: In this phase the target and initiator *may* pass messages to each other. These messages convey information about the SCSI bus and how the devices will be talking to each other. Examples would be:

- A message may be sent from the initiator to the target advising it to abort the current command.
- Messages may be sent between the initiator and the target to establish the speed at which the data transfer is to take place.
- An identifier message is normally sent to the target after selection, prior to sending of the command to specify which LUN is being selected.

1.9 SCSI - Performance

There are many different figures given in a SCSI environment relating to the speed of data transfer.

SCSI Interface Data Transfer Rate: This figure indicates how quickly data can be transferred between the SCSI attachment feature and the devices that are attached to it. The maximum supported by the SCSI interface is 5 MBps.

Note: The SCSI device itself can determine this rate. This may not always be the SCSI bus maximum of 5 MBps. This means that data is transferred from the buffer on different SCSI devices across the SCSI bus to the SCSI attachment feature at different speeds.

SCSI Device Data Transfer Rate: The SCSI device transfers its data into its own buffer before transferring it across the SCSI bus.

It is very important to understand that the figures quoted are all at various stages of one request for information. Be careful when looking at benchmarks for SCSI versus ESDI. It is important that benchmarks are done to pick up the advantages of a SCSI environment such as multiple devices all working at the same time. 2.7.1, "Benchmarks" on page 27 discusses the benchmark environment.

1.10 SCSI versus ESDI

This section explains the differences between a common current device interface, Enhanced Small Device Interface (ESDI), and the Small Computer System Interface (SCSI). It explains how ESDI works and compares this to how SCSI works. Advantages and disadvantages of both are given.

1.10.1 Position of Controlling Circuitry

1. ESDI (Enhanced Small Device Interface)

   ESDI is a device-level interface. This means that it specifies the interface between the controlling circuitry for the device and the device itself. Consequently, error detection, formatting, etc. are all performed by the controller and *not* by the device.

   So with ESDI, the controlling circuitry is on an attachment feature, which is usually separate from the device itself. This means that any device attached to the controller can do only what the controller will allow it to do.

   ESDI is really designed only to support fixed disks. This is because it would be expensive, if not impossible, to put all of the circuitry needed to support CD-ROM drives, fixed disks, printers, etc. onto one attachment feature.

   Another disadvantage is that the drives are often manufactured completely separately from the controller manufacturer. This means that not all ESDI drives are certain to work with the controller that has been installed in the PS/2*.

   ESDI also never became a true standard. Although used widely across the personal computer arena, it was never a defined ANSI standard.

2. SCSI (Small Computer System Interface)

   SCSI is a bus-level interface. This means that it defines an interface between a SCSI attachment feature and intelligent devices.

   This provides for many advantages.

   - With the intelligence for functions such as error detection, formatting etc. being placed with the device itself, there is a significant drop in the restrictions imposed by the attachment feature. This means that manufacturers can develop SCSI devices to perform any function without relying on the attachment feature for all of the support.

     This is made easier under SCSI with the SCSI Common Command Set (see Figure 8 on page 11). The CCS means that manufacturers of SCSI devices can make their SCSI device be or do anything, provided that they understand this basic set of commands.

   - For the user this means that any SCSI device that conforms to the SCSI ANSI standard will work with their SCSI attachment feature.

   - As SCSI is such a high-level interface, the devices attached to the SCSI attachment feature can be any peripheral device type. For example CD-ROM drives, scanners and printers can all be attached to the same SCSI attachment feature at the same time.

1.10.2 Physical Configuration

1. ESDI (Enhanced Small Device Interface)

   In an ESDI environment, each drive is attached to the attachment feature by three cables. These are a data cable, a control cable and a power cable. With this number of cables the ESDI environment can lead to a congested personal computer with too much cabling.

   The maximum distance between the ESDI controller and an ESDI device is three meters (10 feet). The maximum number of devices supported by an ESDI controller is 7.

2. SCSI (Small Computer System Interface)

   In a SCSI environment each SCSI device is attached to the SCSI attachment feature with one daisy-chained cable. This means that the personal computer has only one long cable and a daisy-chained power cable which removes congestion from the system.

   The maximum distance supported under SCSI is six meters. This means that the total length of the SCSI bus can be six meters.

   The maximum number of devices that one SCSI attachment feature will support is 56. This not only saves the cost of multiple attachment features, but also valuable attachment space in the personal computer.

1.10.3 Performance

1. ESDI (Enhanced Small Device Interface)

   The rate at which data can be transferred across the IBM ESDI interface is 10 MBps. This maximum can been increased but this is not usual for the ESDI interface.

   The device, as we have discussed, is reliant on the ESDI controller. The actual data transfer rate of the device *must* be equal to that of the controller. So if there is a controller that transfers data at 10 MBps, the drive must send or receive data at 10 MBps. There are DASD devices available now that can transfer data at up to 24 MBps.

   Because the device is reliant on the ESDI controller, when the ESDI controller is transferring data to or from the device, it has to wait until that device has finished processing that command before it can talk to another device. Only commands such as *seeks* which do not transfer data can be overlapped.

   The ESDI interface is also being outgrown by the speeds of the new systems. It is only designed for use in personal computers with a clock speed up to 25 MHz.

2. SCSI (Small Computer System Interface)

   The maximum data transfer rate across the SCSI Interface is 40 MBps. This is five times faster than ESDI.

   However, because the SCSI devices are all independent of the SCSI attachment feature, they do not have to transfer data at the same rate. The disconnect/reconnect feature of SCSI means that devices can receive a command and process it in its own time. So, for example, if the printer can only receive data at 100 kbps, it would disconnect from the SCSI bus and perform its task leaving the SCSI attachment feature and SCSI bus free for other devices to use.

The disconnect/reconnect also enables multiple SCSI devices to be working concurrently. This is a major advantage in a multitasking environment.

The SCSI interface is also designed to work in personal computers with clock speeds well in excess of 25 MHz.

1.10.4 Other Advantages of SCSI

1. Since SCSI is a defined ANSI standard, it is much easier to build up a versatile peripheral subsystem without having integration problems.
2. With such intelligent devices it is possible for devices in the subsystem to do things independently of the main SCSI attachment feature. For example a fixed disk can dump requested data directly to a tape drive.

1.11 Summary

SCSI stands for Small Computer System Interface. It is a fully documented ANSI standard number X3.131-1986.

SCSI is a standard interface bus through which computers may communicate with attached intelligent devices such as fixed disks, CD-ROMs, etc.

With SCSI, a large number of devices of different types can be connected to the system unit via a single SCSI bus cable and a SCSI attachment feature. This SCSI attachment feature may be in the form of an adapter or integrated on the planar board. The SCSI interface is also device independent, allowing the user to attach intelligent devices of any form that adhere to the SCSI standard. Overall SCSI means less cabling and saves valuable attachment space in the personal computer by having one SCSI attachment feature to support multiple devices.

Up to a maximum of seven devices can be directly attached to the SCSI bus cable and each of these devices can support up to eight more. This means that it is possible for one SCSI attachment feature to support up to 56 devices.

All of the SCSI devices attached to the SCSI bus compete to share the bus. This is known as arbitration. If a SCSI device wins control of the bus and is an initiator, it can send commands to another device known as a target. When a target has received a command it can disconnect from the bus. This means the initiator can then send a command to another target. When the target has finished its task it reconnects to the bus. This enables multiple devices to be working concurrently on the SCSI bus enabling the initiator (normally the SCSI attachment feature) to perform other tasks.

With the SCSI interface, high data transfer rates allow enhanced performance over other, non-SCSI systems. A maximum data transfer speed of 5 MBps is supported across the SCSI bus. The maximum distance for device positioning devices away from the SCSI attachment feature is six meters.

Chapter 2. IBM Implementation of SCSI

This chapter describes how IBM has implemented SCSI in its Personal System/2* systems.

2.1 IBM SCSI Subsystem

This section briefly describes the IBM SCSI subsystem and its specifications.

2.1.1 Brief Descriptive Overview

The IBM SCSI subsystem is available as an option for any of the current PS/2 Micro Channel* systems, either as an adapter, or preinstalled in various models. The IBM SCSI subsystem provides an intelligent SCSI device interface capable of transferring data rapidly to a number of devices such as fixed disks, CD-ROMs, printers etc.

The are four SCSI subsystems available from IBM:

- 16-bit SCSI adapter
- 32-bit SCSI adapter with cache
- 16-bit SCSI subsystem integrated on planar
- 32-bit SCSI subsystem integrated on planar

The IBM SCSI subsystem has an internal SCSI bus connector. This enables the attachment of internal SCSI devices with an appropriate cable. It also has an external SCSI bus connector to which a special option cable can be attached to allow for external SCSI device support.

The highlights of the IBM SCSI subsystem are:

- Bus Master subsystem
- Conforms to SCSI ANSI standard X3.131-1986 for attached devices
- Asynchronous and synchronous device support
- Supports attachment of up to seven SCSI devices
- Each SCSI device can support eight logical units
- Overlapped command processing for up to 15 devices
- Disconnect and reconnect features
- SCSI bus arbitration
- 16-bit data bus (Micro Channel bus)
- A 24- or 32-bit address bus (automatically configurable)

2.2 IBM SCSI Subsystem Physical Configuration

This section describes the physical aspects of the IBM SCSI subsystem and how the IBM SCSI Adapter should be installed.

2.2.1 Subsystem Physical Design

The IBM SCSI subsystem is a 16-bit Micro Channel subsystem. Looking at the IBM SCSI subsystem one will note that it has a 32-bit Micro Channel extension. This extension enables the Subsystem to have 32-bit addressing capabilities when installed in a 32-bit slot. The data signal pins for 32-bit data transfers are not implemented.

2.2.2 Adapter Installation

The adapter is installed just like any other PS/2 Micro Channel adapter. There are no switch settings or jumpers to set. It can fit in any 16 or 32-bit slot on the planar board.

There is no option diskette for the IBM SCSI subsystem. The user should ensure that the latest reference diskette for the relevant model of PS/2 is available before attempting to install the adapter. IBM dealerships have access to the latest reference diskettes. The reference diskettes contain the necessary files to support the IBM SCSI subsystem. These include diagnostic files and the adapter description file (ADF) for the IBM SCSI adapter. The ADF for the 16-bit SCSI adapter is @8EFE.ADF, the ADF for the 32-bit SCSI adapter with cache is @8EFF.ADF.

From the Set Configuration menu of the reference diskette the following options can be set:

1. IBM SCSI subsystem I/O addresses. There are eight different I/O address sets to choose from for the IBM SCSI subsystem. These range from (3540H to 3547H) to (3578H to 357FH).
2. The DMA Arbitration level. This sets the arbitration level for the IBM SCSI subsystem DMA bus master features. This will determine the priority of the IBM SCSI Subsystem during an arbitration cycle on the Micro Channel bus. Levels 1 through E can be chosen excluding levels 2 and 4. The normal level should be C.
3. Fairness ON or OFF. This should always be set to ON. This controls whether or not IBM SCSI subsystem will release control of the Micro Channel bus when it has been using it exclusively.
4. ROM Wait State Disable. This determines whether a wait state is added to accesses of the ROM on the IBM SCSI subsystem. Performance of the IBM SCSI subsystem could be degraded if this is set to the "NO wait state".
5. IBM SCSI subsystem SCSI ID number. This should normally be set to 7. This makes the IBM SCSI subsystem the highest priority device on the SCSI bus. The ID can be anywhere in the range 0 to 7.

2.3 Attachment of SCSI Devices

SCSI devices can be attached to the IBM SCSI subsystem both internally and externally.

The IBM SCSI Subsystem is designed with two SCSI interface connectors. One is a pin edge connector mounted on the top edge of the card, or on the planar of the PS/2. This connector allows the attachment of SCSI devices mounted internally in the system unit via a flat ribbon cable. For attaching external SCSI devices a shielded female 60 pin connector is mounted on the end of the card, or

on the planar at the back of the PS/2, for a cable to extend from the rear of the system unit.

The diagram below shows the SCSI device attachment configuration.

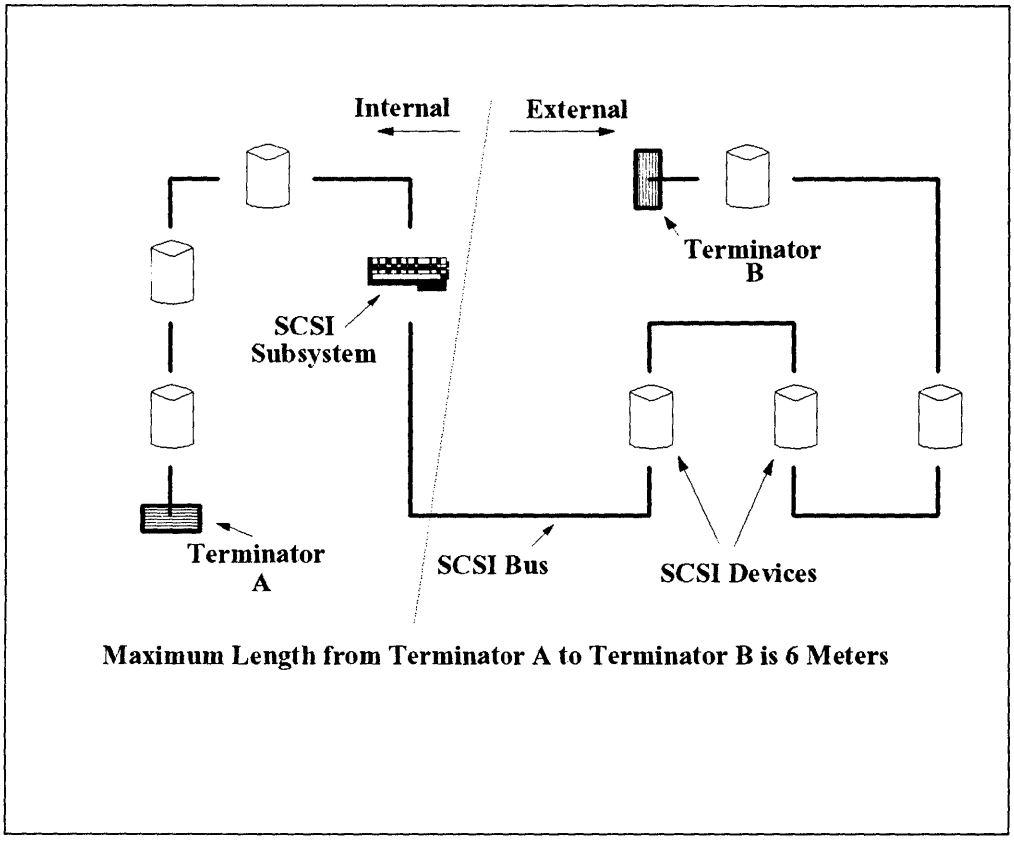

Figure 10. SCSI Device Attachments

2.3.1 Internal Connections

To fit SCSI devices internally into a PS/2 two things in addition to the IBM SCSI subsystem are needed: an internal cable option to attach the device to the IBM SCSI subsystem and a special mounting bracket. Please note that the maximum number of devices supported internally will vary from machine type to machine type, due to space constraints.

There are two installation kits available that contain parts for installing extra internal SCSI devices.

1. Fixed disk installation kit A consists of:
   - Power cable with two connectors
   - SCSI cable with two connectors
   - SCSI cable with four connectors
   - One mounting bracket with screws.

2. CD-ROM drive installation kit A consists of:
    - Power cable with one connector.
    - SCSI cable with one connector.
    - Front plate.

Cables: The internal cables contain a connector to attach to the IBM SCSI subsystem's internal connector and a number of connectors for attaching SCSI devices.

Installing an internal CD-ROM drive in any of the floor-standing PS/2 systems will require the CD-ROM installation kit.

Mounting Brackets: Internally on certain PS/2 models, there are 5.25-inch peripheral bays. As the IBM SCSI fixed disk drives are all 3.5-inch in size, a mounting bracket is needed to support them in these 5.25-inch bays. One mounting bracket supports two IBM SCSI fixed disks.

Certain older PS/2 models already have one bracket with one SCSI fixed disk installed. An additional fixed disk can be installed by attaching it to this bracket. If a third or a fourth fixed disk has to be installed in one of these systems, fixed disk installation kit A will be needed.

The internal CD-ROM drive takes up the whole front bay of any PS/2 floor-standing systems, and requires the CD-ROM installation kit A to install it.

The SCSI devices can attach to the SCSI cable in any order provided that one of the SCSI devices is attached to the last connector on the internal SCSI cable. This SCSI device must have a terminator installed (see 2.3.3, "Terminator Positioning").

2.3.2 External Connections

A 60-pin to 50-pin cable connects the external connector on the Subsystem to the first external option. The next SCSI device is connected via a 50-pin to 50-pin cable which comes out of the first option and into the second. The last option attached must have a terminator attached to it.

A maximum of seven SCSI devices can be attached up to the IBM SCSI subsystem. This includes both internal and external devices. So if there was only one internal device attached then up to six devices could be attached externally and so on.

Both the internal and external cables will often be referred to as the "SCSI bus". The total length of the SCSI bus must not exceed 6 meters.

2.3.3 Terminator Positioning

In order for the SCSI bus to function correctly a terminator is required at each end of the SCSI bus. There are three main types of terminator:

Internal Terminators: These come with each device and differ in the way that they are implemented. Do not mix the terminators.

SCSI Subsystem Terminator: Certain IBM SCSI subsystems come with a terminator installed. This is usually in the form of a small orange rectangle plugged into the SCSI subsystem. If it needs to be removed do so carefully with a chip puller or similar tool.

External Terminator: This terminator is usually the same for all external SCSI devices. It attaches to the back of the last SCSI device attached externally.

The following three diagrams show the terminator and device positions that must be adhered to where attaching SCSI devices the IBM SCSI subsystem.

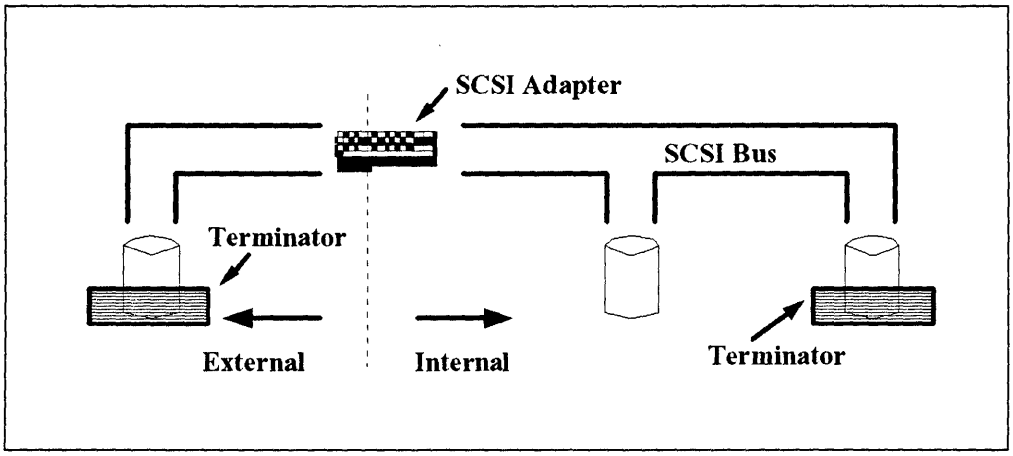

Figure 11. SCSI Terminator Positions: Internal and External Devices

In the following diagram, the terminator illustrated can be one of two kinds. In older model SCSI subsystems, it is an external device that must be attached to the SCSI adapter. In newer model SCSI subsystems this terminator has been included in the subsystem itself and therefore does not need an external terminator to be attached. Users should check with their IBM dealer which adapter they have installed in their systems.

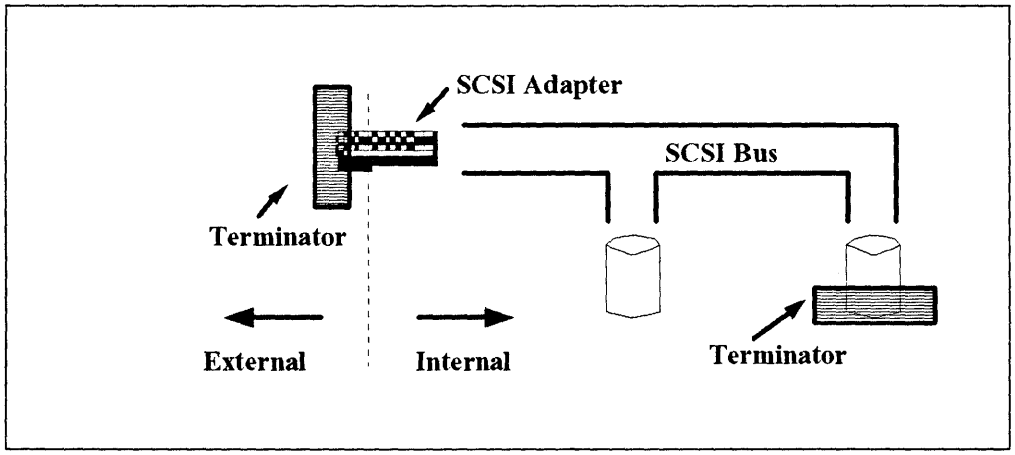

Figure 12. SCSI Terminator Positions: Internal Devices Only

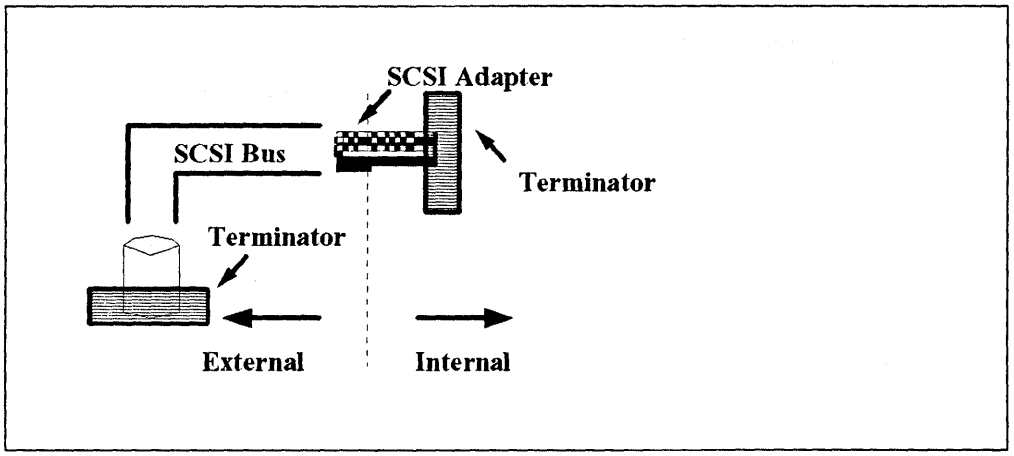

Figure 13. SCSI Terminator Positions: External Device Only

2.3.4 What SCSI Devices can be Attached

The connectors on the internal SCSI bus and the external SCSI bus cables will enable any SCSI device that conforms to the ANSI standard X3.131-1986 to attach. They must also support the mandatory commands and messages specified in Addendum 4.B to the ANSI specification, known as the SCSI Common Command Set (CCS).

The maximum number of SCSI devices that can be attached to the IBM SCSI Subsystem is seven.

2.4 Configuration of the SCSI Devices

This section explains how SCSI devices are configured so that they can be accessed by the IBM SCSI Subsystem.

2.4.1 Physical Configuration

Each SCSI device attached to the SCSI bus must be assigned a unique SCSI ID number. This number is in the range 0 to 7 and allows each SCSI device to be addressed.

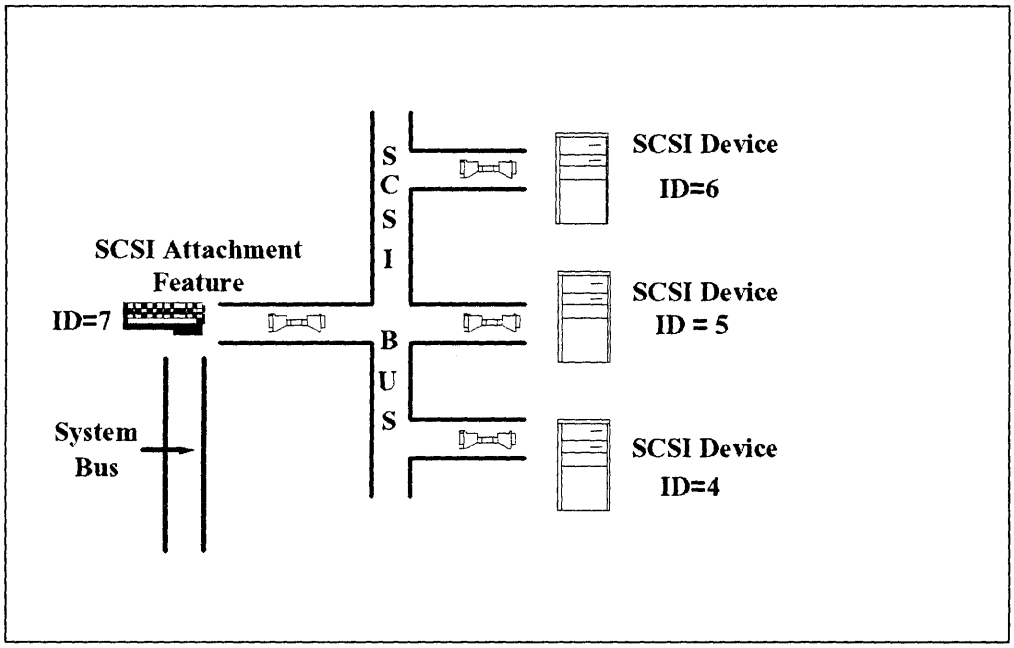

Figure 14. SCSI Physical Configuration

The SCSI ID number of a particular SCSI device is set during configuration of the particular device. For example, on the IBM 320 MB SCSI fixed disk a series of jumpers determines the ID number of the drive, but this varies from manufacturer to manufacturer.

The SCSI ID number not only acts as a number by which the device can be recognized. It also determines the priority of the device on the SCSI bus during arbitration (see 1.6.5, "SCSI Bus Arbitration" on page 9).

2.4.2 Reference Diskette Configuration

Once the SCSI ID has been set on the device itself, the system must be reconfigured using the reference diskette. This will tell the IBM SCSI subsystem which devices it has attached and how to address them.

When the SCSI configuration is viewed it will show for each SCSI device a number such as 6,0. The first number indicates the SCSI device ID set on the device itself and the second number is the logical unit number or LUN.

2.4.3 Logical Units (LUs)

For a full definition of logical units see 1.6.2, "Logical Units (LUs)" on page 7.

The IBM SCSI subsystem allows each SCSI device to have up to eight Logical Units (LUs) attached to it. These LUs are controlled by the SCSI device.

Note: The IBM SCSI Subsystem will only support a total of 15 LUs at any one time through its BIOS. If there are more than 15 LUs attached to one IBM SCSI Subsystem the 15 LUs used are determined as follows:

The BIOS scans the SCSI bus to locate SCSI devices. It scans the bus in numeric order, from the highest SCSI device ID to the lowest SCSI device ID. After each SCSI device has been located on the SCSI bus it checks to see if that device has any LUs attached. If the device has some LUs, these are set up immediately. The BIOS then moves to the next SCSI device and so on until a maximum 15 LUs have been configured. The additional LUS will not be accessible through the SCSI BIOS.

IBM does not presently market any SCSI devices that allow multiple LUs to be attached. All of the IBM SCSI devices are single LU devices.

The following diagram will serve as an example of how the IBM SCSI subsystem would address a target fixed disk.

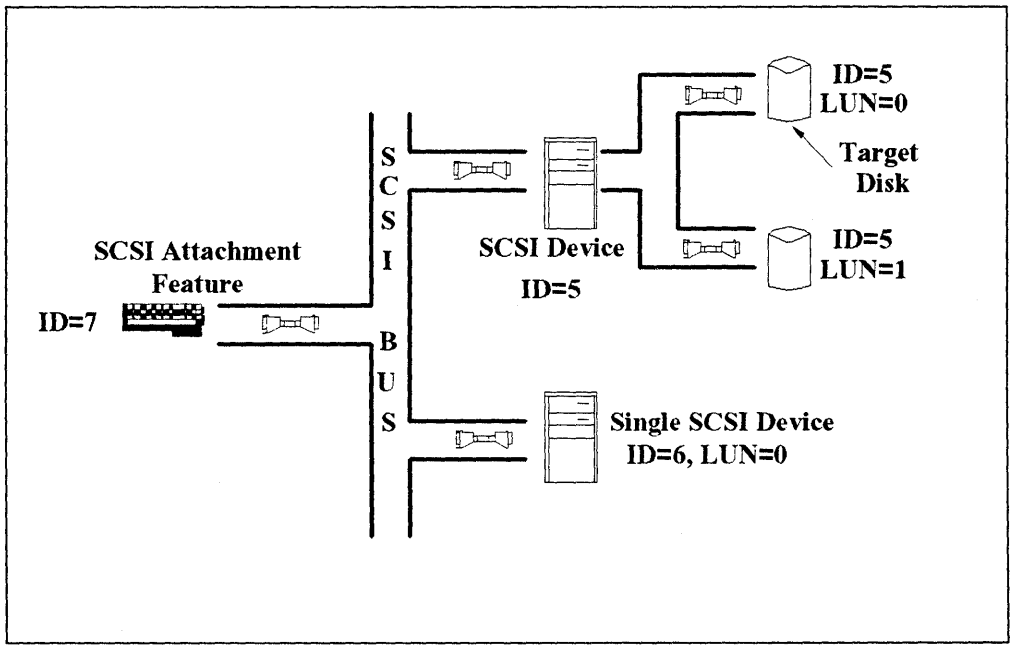

Figure 15. SCSI Logical Units

1. The IBM SCSI subsystem selects the target fixed disk using the SCSI ID, which in this case is 5.
2. It then sends an identify message to select LU 0.
3. Then, it sends a command to the target fixed disk. In this case the 3-bit field would contain the number 0.
4. When the SCSI device receives the command it passes on the instructions to the logical unit, in this case LU 0.
5. The drive will then perform its read or write as specified by the SCSI device.

For a layout of the SCSI commands see Figure 8 on page 11.

2.5 Other Features of the IBM SCSI Subsystem

This section describes other functions of the IBM SCSI Subsystem. For detailed explanations on any points please refer to Chapter 1, "What is SCSI" on page 1.

2.5.1 Initiators and Targets

When two SCSI devices talk to each other on the SCSI bus, one sends out a command and one acts upon it. The SCSI device that sends out the commands (which is most likely to be the IBM SCSI subsystem) is called an *initiator*. The SCSI device that processes the command is called the *target*. All of the IBM SCSI devices available at the moment are targets.

The IBM SCSI subsystem supports the ability to have multiple initiators on its SCSI bus. This allows for functions such as device level copying. None of the current IBM SCSI devices support this function.

The IBM SCSI subsystem cannot be accessed as a target by another initiator.

2.5.2 SCSI Bus Arbitration

Details on arbitration can be found in 1.6.5, "SCSI Bus Arbitration" on page 9.

On the SCSI bus, arbitration is controlled by logic on the IBM SCSI subsystem. Arbitration on the SCSI bus can be initiated by any SCSI device on the bus provided that it has the capability to do so. The SCSI device ID is used as the arbitration level.

2.5.3 Disconnect/Reconnect and Overlapped Command Processing

All of the IBM SCSI devices have the ability to arbitrate for the SCSI bus. This is so that they can perform the disconnect/reconnect function. This means that as soon as a SCSI device (for instance, a IBM 320 MB SCSI fixed disk) has received a command it can disconnect from the SCSI bus. The IBM SCSI subsystem can then send a command to another SCSI device. This means multiple devices can be working concurrently. When the IBM 320 MB SCSI fixed disk has completed the command it arbitrates for the SCSI bus and reconnects to tell the IBM SCSI subsystem that it has finished.

This processing of multiple commands at a time is known as overlapped command processing. The IBM SCSI subsystem supports overlapped command processing for up to 15 logical units.

2.5.4 Synchronous and Asynchronous

There are two modes of data transfer across the SCSI interface. These are asynchronous and synchronous modes.

The IBM SCSI subsystem supports both of these data transfer modes. It intelligently checks, before doing a data transfer, which mode the SCSI device can use. The type of transfer and speed of transfer is not set during configuration of the device. It is done during the message phase of the SCSI bus. Please refer to Figure 7 on page 9 for more details.

For example, the IBM CD-ROM drive, the 60 MB and the 120 MB SCSI disk drives are all asynchronous devices. The 320 MB SCSI disk is a synchronous device.

2.5.5 Multiple SCSI Subsystems In One System

A maximum of four IBM SCSI subsystems are supported in the PS/2 system units.

In order to determine which subsystem will have the bootable drive attached to it the system scans the subsystems and searches for the SCSI device with the most up-to-date software, and will boot off this drive. This is determined by the date and time stamp on each partition.

2.5.6 Installing a SCSI Subsystem in Current PS/2s

When the IBM SCSI subsystem is installed in a PS/2 system, it may be installed in addition to the already installed ESDI or ST-506 controller and drive(s).

If the ESDI or ST-506 subsystem and drive(s) remain installed, the bootable drive attached to that subsystem will remain as the bootable drive. It will not be possible to make any of the SCSI fixed disk drives the bootable C: drive.

2.6 Operating System Support

2.6.1 Device Drivers

IBM has developed many device drivers for the SCSI interface for the various operating systems available. The device drivers are class specific as opposed to device specific. IBM will develop a fixed disk driver, or a CD-ROM driver, or a printer driver, as opposed to a device specific driver, for example a 320 MB SCSI disk driver. Where a device driver does not function correctly, then IBM should be notified as soon as possible for the problem to be analyzed.

2.6.2 BIOS

The IBM SCSI subsystem contains both CBIOS and ABIOS routines. This means that it is supported under both DOS and OS/2*. The BIOS gives support more specifically to hard disks. It also contains a generic BIOS that can be used by other devices such as the IBM CD-ROM in conjunction with a device driver.

Currently support is provided by :

- Operating System/2*
- Disk Operating System (DOS)
- Advanced Interactive Executive PS/2 (AIX* PS/2)

2.6.3 How the Operating System Views SCSI

The following section explains how the IBM SCSI Subsystem is addressed by the operating system and how each SCSI device is addressed.

1. Operating system sends BIOS call. The operating system makes a call to BIOS for data to be read from a fixed disk into memory. The SCSI BIOS for the fixed disks is compatible with that used for other PS/2 disk systems. Therefore any application that uses BIOS to address the fixed disks will work on the SCSI drives.

2. The SCSI BIOS (which has been mapped into a memory address space) builds a subsystem control block (SCB) that defines all of the information necessary to perform the request, such as memory location for data, the actual data requested etc.

   It also contains a logical device number which translates to the SCSI device ID and logical unit number which the command is for.

3. The SCB is then requested by the IBM SCSI subsystem and sent across the Micro Channel bus by the bus master controller on the IBM SCSI subsystem (for more details on subsystem control block architecture please refer to the related PS/2 hardware interface technical reference manuals).

4. The IBM SCSI Subsystem then decodes certain parts of this subsystem control block and the logical device number, and sends a command descriptor block (CDB) across the SCSI bus to the appropriate SCSI device.

5. The SCSI device then reads the CDB and requests the LU specified in the 3-bit field of the CDB to perform the task.

   For an example of a command descriptor block please see Figure 8 on page 11.

2.7 SCSI Security

Small Computer System Interface (SCSI), as defined in the American National Standard Institute (ANSI) standard X3.131-1986 provides a port for the attachment of external devices. The IBM PS/2 SCSI subsystem is in conformance with this standard and has an external port.

A data security exposure exists, even with power-on password installed, since external SCSI controllers can attach through the external SCSI port and gain undetected read or write access to data stored on internal and external SCSI devices.

Physical access to the system and external SCSI devices must be controlled to limit this exposure. Please refer to 8.3.4, "Secure I/O Cables" on page 105 for a description of such an access limitation available in PS/2 systems.

However, certain organizations may find this feature useful for managing their SCSI resources.

2.7.1 Benchmarks

Many different utilities are available to perform benchmarks on disk subsystems. In doing benchmarks the final configuration and environment should be emulated as closely as possible for testing.

Most of these utilities test the amount of time it takes to perform a series of seeks on the drive as against measuring the time it takes to read or write the data. The benchmarking utility will send repetitive *seek* commands, moving the arm back and forth across the disk and observing the time it takes to process each command or averaging the time over a number of such commands.

In normal read/write operations, hard disks seek to a given cylinder after which the arm does not move for some period of time while the read or write takes place. As soon as the read or write has completed, the drive is then ready to

process the next command, which may or may not require a seek to a different cylinder.

This "rest period" that occurs after a seek has completed and the reading or writing operation is taking place allows the arm drive mechanism (voice coil) to cool down somewhat after being heated up by the current necessary to perform the task.

The IBM SCSI implementation takes advantage of this natural cooling action to boost the amount of current that can be used by the voice coil during seeks. The more current used, the faster the seek.

If the command ends when the seek is completed, and the next command to be processed is also a seek, then the natural cooling action to keep the voice coil at an acceptable temperature is no longer available.

To prevent the drive from overheating from consecutive *seek* commands while maintaining a maximum current for fast seeks, a delay of several milliseconds is added after the successful completion of the seek operation. This delay simulates an average latency plus the read or write time. This is why *seek*-based benchmarks are not suitable for measuring the performance of SCSI disk drives as they simulate a situation that doesn't occur in the normal operation of the disk and, as a result, show performance figures that do not represent the "real life"-performance of the drive.

Many *seek*-based benchmarks would probably measure a non-SCSI device as being quicker than a SCSI device, even if it were actually slower. Most non-SCSI devices will run at the speed of the processor for all I/O operations. This would tie down the processor for the period of I/O, but in turn would make the non-SCSI device perform well in the benchmark. SCSI devices are normally bus masters, and often detach from the main processor and perform I/O transfers at the speed of the SCSI processor, which is much slower than the main processor.

When actual applications are loaded into the system, especially in a multitasking environment, the SCSI devices normally outperform non-SCSI devices. This is because the system processor has to wait for I/O processes to complete with non-SCSI devices. With SCSI, however, the bus-mastering capability allows the SCSI controller to release itself from the main processor (allowing it to perform other tasks) while allowing the SCSI controller to perform disk operations at the same time.

Benchmark Summary: Overall, any benchmarks must be carefully analyzed and the other benefits of SCSI taken into consideration before a decision is made on which system will best suit the user. Different tests test different parameters, and the only valid and relevant data would be obtained when the actual application is tested on the final configuration. A pilot test period with real applications and real data is strongly recommended in any benchmark test.

2.8 IBM SCSI Subsystem Performance

The IBM SCSI subsystem is a 16-bit Micro Channel bus master. The figures relating to its performance are shown in Table 2 on page 29. What each of the figures means is explained below the table. These figures are valid for the SCSI-I implementation, and would vary from device to device.

Table 2. IBM SCSI Subsystem Specifications.	
System bus Interface	16-bit data bus width
System Data Transfer Rate	16.6 MBps (burst mode - newer models) 8.3 MBps (burst mode - older models)
SCSI Interface Transfer Rate	5 MBps (maximum)
SCSI Device Data Transfer Rate	Dependent on device

System Bus Interface: This indicates the maximum data bus width supported by the IBM SCSI subsystem. It is the maximum width at which data can be transferred from Subsystem to real memory in the system unit.

System Data Transfer Rate: This figure indicates how quickly data can be transferred from the IBM SCSI subsystem across the Micro Channel bus. This figure relates to the subsystem and not SCSI itself. This figure is achieved when the bus master controller on the IBM SCSI subsystem is performing a burst transfer across the Micro Channel bus.

SCSI Interface Data Transfer Rate: This figure indicates how quickly data can be transferred between the IBM SCSI subsystem and the SCSI devices that are attached to it. The maximum supported by the SCSI interface is 5 MBps. This is the figure that the IBM SCSI subsystem supports.

Note: The SCSI device itself determines this rate. This may not always be the SCSI bus maximum of 5 MBps. This means that data is transferred from the buffer on the SCSI device across the SCSI bus to the IBM SCSI subsystem at different speeds.

SCSI Device Data Transfer Rate: The SCSI device transfers its data into its own buffer before transferring it across the SCSI bus.

It is important to note that the figures quoted are all parts of one overall data transfer.

2.8.1 Bus Master Subsystem

There are many advantages that a bus master subsystem has over a DMA slave in the Micro Channel environment. The main advantage is that of system processor relief. As the bus master is an intelligent device it can perform its data and command transfers without the help of the main central processor. This means that the processor will be free to perform other tasks. Other advantages can be found in the various PS/2 hardware interface technical reference manuals.

2.9 Quick Installation Guide

This section gives a quick overview of how SCSI devices are installed in a PS/2 system.

Installing Subsystem: To use the IBM SCSI subsystem the PS/2 system should be configured using the latest reference diskettes. There is no option diskette for the IBM SCSI subsystem.

Internal or External Devices: The IBM SCSI subsystem allows both internal and external devices to attach. Internal devices can be attached externally to a PS/2 by means of an External SCSI Enclosure.

On floor-standing PS/2 systems there are sometimes 5.25-inch internal DASD bays. Each of these can take two SCSI fixed disks. Alternatively the front bay can take one internal CD-ROM drive.

To install an internal SCSI fixed disk a mounting bracket is required. One mounting bracket will enable two SCSI fixed disks to be installed in one 5.25-inch bay. Certain PS/2s come standard with one bracket. Additional brackets come with the installation kits.

Installing SCSI Devices: Before installing any SCSI device, its SCSI ID must be set. The reference diskette can be used to see which SCSI ID numbers are not being used. Read/write devices should be set to a high SCSI ID and read-only devices to a low SCSI ID.

When the SCSI ID is set, the terminators should be checked to ensure they are installed correctly. When the PS/2 is next booted a 162 POST error code will appear. An automatic configuration should be run with the new reference diskette.

Which Drive Will Boot: The PS/2 will boot off the SCSI device that has the newest boot partition as determined by the date and time stamp on that partition.

Chapter 3. Integrated Drive Electronics (IDE)

3.1 IDE(ATA) Standards Introduction

Sometime after the IBM PC AT* was born, the term Integrated Drive Electronics (IDE) interface was introduced into the computer industry by marketing and retailers. It is generally known throughout the engineering community as the AT Attachment (ATA) Interface or in IBM circles as the AT Direct Bus Attach (AT-DBA) interface. This chapter provides a short overview of the major functions and features of IDE as it applies to the PS/ValuePoint* family. As background, a brief history of the American National Standard for Information Systems (ANSI) ATA standard is described, as well as a comparison between IDE and SCSI interfaces.

When the first IBM PC (Personal Computer) was introduced, there was no hard disk capability. These early systems used floppy disk drives as external storage. Successive generations of products resulted in the inclusion of a hard disk as the primary external storage device. When the IBM PC AT was developed, a hard disk was the key to system performance, and the controller interface became a de facto standard interface for the inclusion of hard disks in PC ATs.

The price of desktop systems has declined rapidly because of the degree of integration to reduce the number of components and interconnects required to build a product. A natural outgrowth of this integration was the inclusion of controller functionality into the hard disk.

In October 1988 a number of peripheral suppliers formed the Common Access Method Committee (CAMC) to encourage an industry-wide effort to adopt a common software standard interface to dispatch input/output requests to SCSI peripherals. Although this was the primary objective, a secondary goal was to specify what is known as the AT Attachment interface (also know as IDE).

This standard was processed and approved for submittal to ANSI by the Accredited Standards Committee on Information Processing Systems, X3. Committee approval of this standard does not necessarily imply that all committee members voted for its approval. The subcommittee X3T9 on I/O interfaces, and the Task Group X3T9.2 on Lower-Level Interfaces also reviewed and approved the standard.

The initial development work on this standard was done by the CAMC. The membership of the CAMC consisted of forty computer and peripherals manufacturers.

Note: Throughout this chapter the terms AT Attachment (ATA) and IDE will be used interchangeably and refer to the same ANSI standard.

3.2 General Description

The application environment for the AT Attachment Interface is any computer which uses an AT bus or 40-pin ATA interface.

The PC AT bus is a widely used and implemented interface for which a variety of peripherals have been manufactured. As a means of reducing size and cost, a class of products has emerged which embed the controller functionality in the drive. These new products utilize the AT bus fixed disk interface protocol, and a subset of the AT bus. Because of their compatibility with existing AT hardware and software this interface quickly became a de facto industry standard.

The purpose of the ATA standard is to define and clarify the hard disk and peripherals input/output (I/O) implementations. Software in the PC operating system dispatches I/O requests via the AT Bus to peripherals which respond to direct commands.

3.2.1 IDE Structure

The IDE structure relies upon specifications of the mechanical and electrical characteristics of the AT bus and a subset of the AT bus specifically developed for the direct attachment of peripherals. Also defined are the methods by which commands are directed to peripherals, the contents of registers and the method of data transfers.

3.2.2 ATA Definitions

The following definitions apply to the ATA standard:

ATA (AT Attachment)
This defines a compatible register set and a 40-pin connector and its associated signals. This is broadly known as IDE throughout the marketing/retail sectors of the PC industry.

CHS (Cylinder Head Sector)
This term defines the addressing mode of the drive as being by physical address.

Data block
This term describes a data transfer (typically a single sector) except when declared otherwise by use of the Set Multiple command.

DMA (Direct Memory Access)
A means of data transfer between peripheral and host memory without processor intervention.

LBA (Logical Block Address)
This term defines the addressing mode of the drive as being by the linear mapping of sectors from 1 sector to a maximum number of sectors.

PIO (Programmed Input/Output)
A means of data transfer that requires the use of the host processor.

VU (Vendor Unique)
The ATA standard uses this term to describe bits, bytes, fields, code values and features which are not described in the standard, and may be used in a way that varies between vendors.

3.2.3 Conventions

In the ANSI standard, the proper names of signals are printed in uppercase to avoid possible confusion with other uses of the same words. A number of conditions, commands, sequence parameters, events, English text, states or similar terms are printed with the first letter of each word in uppercase and the rest lowercase. The American convention of numbering is used, that is the thousands and higher multiples are separated by a comma and a period is used as the decimal point.

3.3 Physical Interface Description

3.3.1 Configuration

The ATA standard provides the capability of operating on the AT bus in a daisy chained configuration with a second drive that operates in accordance with the standards. One drive (selected as Drive 0) has been referred to as the *master* in industry terms and the second (selected as Drive 1) has been referred to as the *slave*. Refer to Figure 18 on page 34. The designation as Drive 0 or Drive 1 may be made in a number of ways:

- A switch on the drive
- A jumper plug on the drive
- Use of the Cable Select (CSEL) pin

Data is transferred in parallel (8 or 16 bits) either to or from host memory to the drive's buffer under the direction of commands previously transferred from the host. The drive performs all of the operations necessary to properly write data to, or read data from, the disk media. Data read from the media is stored in the drive's buffer pending transfer to the host memory and data is transferred from the host memory to the drive's buffer to be written to the media. Figure 16 shows the ATA interface to embedded bus peripherals. In this example the peripheral devices are directly attached to the system board AT bus. No adapter cards are necessary for this type of interface connection. Figure 17 on page 34 shows how peripheral devices interface to the host computer via an adapter card connection. Figure 18 on page 34 shows the ATA standard with the peripherals interfacing directly to a controller which is attached to the host computer. These figures are illustrated below.

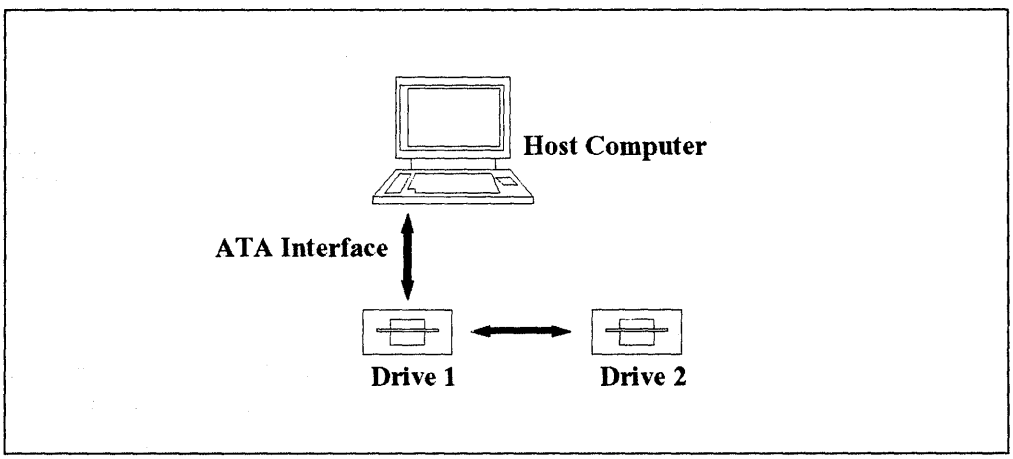

Figure 16. ATA Interface To Embedded Bus Peripherals

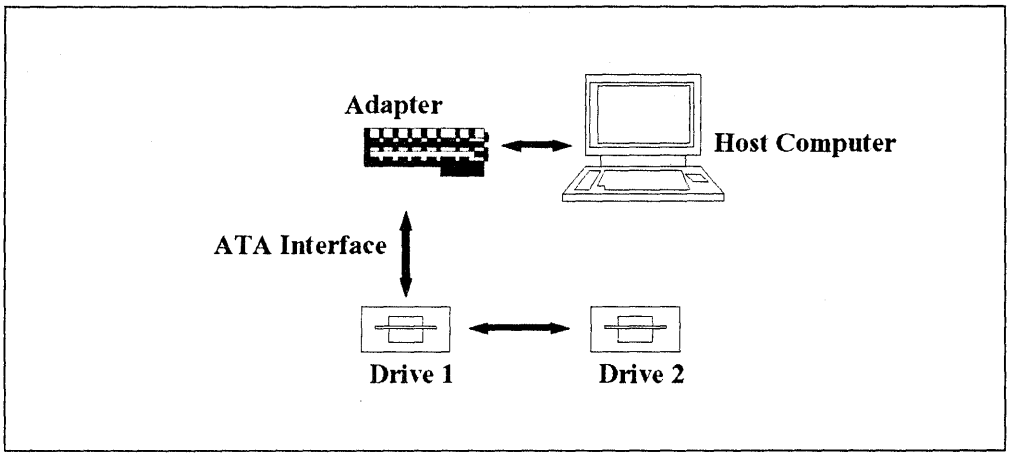

Figure 17. ATA Host Bus Adapter and Peripheral Devices

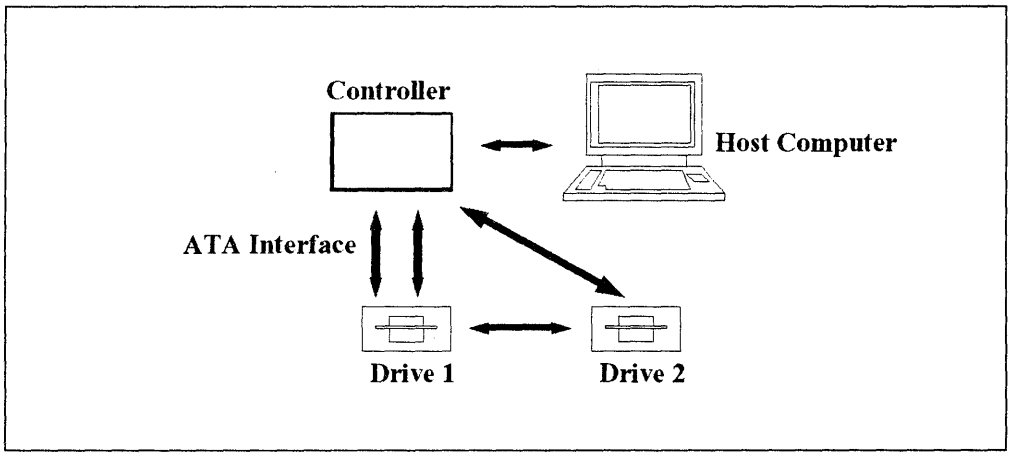

Figure 18. ATA Interface To Controller and Peripheral Devices

3.3.2 Addressing Considerations

In traditional controller operation, only the selected controller receives commands from the host following selection. In the ATA standard, the register contents go to both drives (and their embedded controllers). The host discriminates between the two by using the DRV bit in the Drive/Head Register.

3.3.3 DC Cable and Connector

The drive receives DC power through a 4-pin or a low-power application 3-pin connector. All the PS/ValuePoint models use a 4-pin connection.

3.3.4 I/O Connector Description

The I/O connector used within the the PS/ValuePoint family adheres to the ATA X3 Standard.

The physical interface consists of single ended TTL compatible receivers and drivers communicating through a 40-conductor flat ribbon non-shielded cable using an asynchronous interface protocol. Reserved signals are left unconnected. The I/O connector is a 40-pin connector as shown in Figure 4, with PS/ValuePoint I/O connector pin number assignments and signal names as shown in Table 3 on page 35.

The ribbon cable connector is keyed to prevent the possibility of installing it upside down. A pin key is also provided by the removal of pin 20. The corresponding pin on the cable connector is plugged. The pin locations are governed by the cable plug, not the receptacle. The header receptacle is not polarized, and all the signals are relative to pin 20, which is keyed.

By using the plug positions as primary, a straight ribbon cable connects the drives. As shown in Figure 4, conductor 1 on pin 1 of the plug is in the same relative position. Because the standard receptacle numbering is followed, the cable is twisted 180 degrees between a drive with top-mounted receptacles, and a drive with bottom-mounted receptacles.

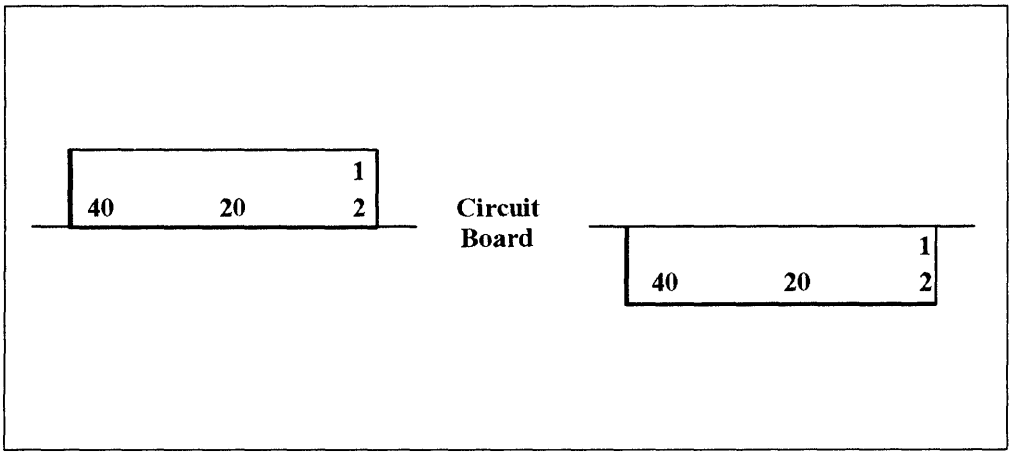

Figure 19. ATA Interface To Controller and Peripheral Devices

3.3.5 Connector

The following figure shows the drive and controller connector and interface specifications.

Table 3 (Page 1 of 2). PS/ValuePoint Connector Signals

Pin	I/O	Signal	Pin	I/O	Signal
1	I	-RESET	**2**	N/A	Ground
3	I/O	D7	**4**	I/O	D8
5	I/O	D6	**6**	I/O	D9
7	I/O	D5	**8**	I/O	D10
9	I/O	D4	**10**	I/O	D11
11	I/O	D3	**12**	I/O	D12
13	I/O	D2	**14**	I/O	D13
15	I/O	D1	**16**	I/O	D14
17	I/O	D0	**18**	I/O	D15
19	N/A	Ground	**20**	N/A	Key
21	N/A	Reserved	**22**	N/A	Ground
23	I	-IOW	**24**	N/A	Ground
25	I	-IOR	**26**	N/A	Ground
27	O	IORDY	**28**	N/A	Reserved
29	N/A	Reserved	**30**	N/A	Ground

Table 3 (Page 2 of 2). PS/ValuePoint Connector Signals					
Pin	**I/O**	**Signal**	**Pin**	**I/O**	**Signal**
31	O	IRQ	**32**	O	-IO16
33	I	A1	**34**	I/O	-PDIAG
35	I	A0	**36**	I	A2
37	I	-CS0	**38**	I	-CS1
39	I/O	-DASP	**40**	N/A	Ground

3.4 Logical Interface Description

3.4.1 Logical Environment

The PS/ValuePoint IDE drives all use the ATA standard logical interface. The drives are programmed by the host computer to perform commands and return status to the host at command completion. When two drives are daisy chained on the interface, commands are written in parallel to both drives, and for all except the Execute Diagnostics command, only the selected drive executes the command. On an Execute Diagnostics command addressed to Drive 0, both drives execute the command, and Drive 1 posts its status to Drive 0.

3.4.2 Drive Selection

Drives are selected by the DRV bit in the Drive/Head Register, and by a jumper or switch on the drive designating it as either Drive 0 or as Drive 1. When DRV=0, Drive 0 is selected. When DRV=1, Drive 1 is selected. When drives are daisy chained, one is set as Drive 0 and the other as Drive 1. When a single drive is attached to the interface it is set as Drive 0.

3.5 PS/ValuePoint IDE Family Specifics

3.5.1 Description

This section describes the IDE interface to the PS/ValuePoint 80MB, 120MB, 170MB, and 212MB fixed disk drives. The PS/ValuePoint systems provide a specialized connector for directly attaching the drive to the channel. This interface complies with the ANSI standard for *AT Attachment (ATA), revision 3.0*, dated November 22,1991.

The drives provide automatic error checking and correction (ECC).

The device-level control for the fixed disk is in the system Basic Input Output System (BIOS). The last cylinder on the fixed disk drive is reserved for diagnostic use. The diagnostic-write test destroys any data on this cylinder.

Important

IBM provides a BIOS interface to insulate the programmer from hardware dependencies. IBM recommends that all applications use the BIOS interface or the operating system interface to prevent incompatibilities caused by differences in hardware.

Note: For detailed programming information on the IDE/ATA interface, please refer to IBM Part No. 53G2161, entitled *ATA/IDE Fixed Disk Drives Technical Reference*, dated 1992.

3.5.2 Features

The PS/ValuePoint fixed disk drives have the following features:

- Integrated controllers
- Task File Architecture
- Implied seeks
- Media data transfer rate is 10.8 Mbps
- 32 KB (1 KB equals 1024 bytes) data buffer
- Self-diagnostics at power-on
- Read look-ahead buffer
- Automatic retry and data correction on read errors.

3.5.3 Task File Architecture

The system addresses the drive through a set of registers called the *Task File*. The registers in the Task File are mapped into the I/O space of the system. The following is a block diagram of the fixed disk drive and the Task File.

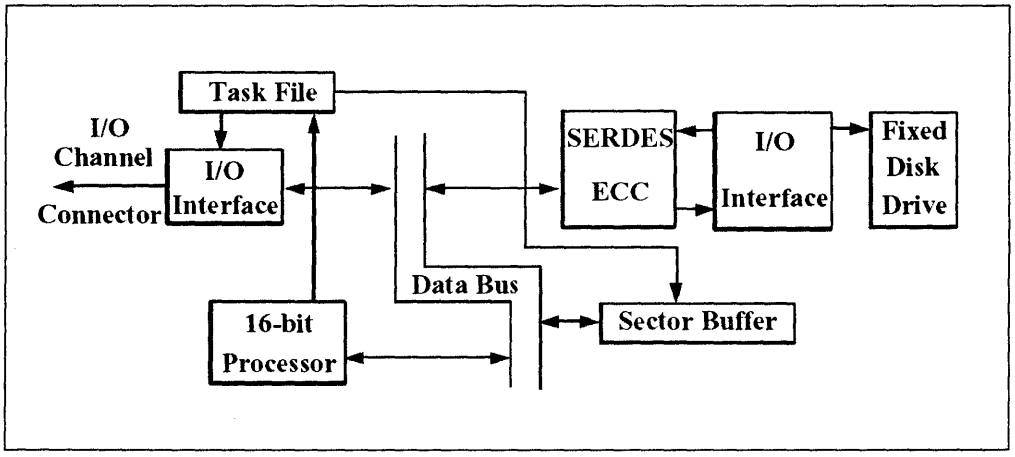

Figure 20. PS/ValuePoint Fixed Disk and Task File Block Diagram.

SERDES = serializer/deserializer

3.5.4 ATA Addressing

ATA/IDE Addressing is controlled by the use of ten registers: eight *Command Block* registers and two *Control Block* registers. Command block registers are used for sending commands to the drive or receiving status from the drive. Control block registers are used for controlling the drive or giving alternate status. A short description of each register follows.

Two chip-select lines (-CS0 and -CS1) and three address lines (A0, A1, and A2) are used to select registers. The I/O address is decoded by the system board to determine which chip select signal is driven active.

The following figure shows the relationship between the I/O address, the state of the chip select signals, and the register that is selected.

Table 4. ATA I/O Addressing

Register	Read/ Write	I/O Addr. (Hex)	Chip Select Signals		Address Signals		
			-CS0	-CS1	A2	A1	A0
Command Block Registers							
Data	R/W	01F0	L	H	L	L	L
Error	R	01F1	L	H	L	L	H
Features	W	01F1	L	H	L	L	H
Sector count	R/W	01F2	L	H	L	H	L
Sector number	R/W	01F3	L	H	L	H	H
Cylinder low	R/W	01F4	L	H	H	L	L
Cylinder high	R/W	01F5	L	H	H	L	H
Drive/head	R/W	01F6	L	H	H	H	L
Status	R	01F7	L	H	H	H	H
Command	W	01F7	L	H	H	H	H
Control Block Registers							
Alternate status	R	03F6	H	L	H	H	L
Device control	W	03F6	H	L	H	H	L
Drive address	R	03F7	H	L	H	H	H

Note:

L = Low level signal

H = High level signal

3.5.5 ATA Addressing Registers

3.5.5.1 Data Register (Hex 1F0)

The data register is a read/write register. It is used to transfer data blocks between the device data buffer and the system. All transfers through this register are 16-bit, except for ECC bytes during read-long and write-long operations where the data transfers are 8-bits wide.

The state of this register is undefined after a reset. This register contains valid data only when the data-request bit in the status register is set to 1.

3.5.5.2 Error Register (Hex 1F1)—Read-Only

The error register is a read-only register. It contains status from the last command executed by the drive or diagnostics information. After completion of any command except Execute Diagnostic, this register contains valid data only when the error bit in the status register is set to 1. After completion of a power-on self test, a reset, or an Execute Diagnostic command, this register contains diagnostic results rather than status.

3.5.5.3 Features Register (Hex 1F1)—Write-Only

The features register is a write-only register and is used only with the Set Feature command. This register may be ignored by some drives.

3.5.5.4 Sector Count Register (Hex 1F2)

The sector count register is a read/write register and is used by the system to define the number of sectors to be transferred. If the value in this register is 0, the number of sectors is 256. This register is decremented by the drive after each sector is transferred to or from the system so that the value in this register shows the number of sectors remaining to be transferred.

This register is also used to define the number of sectors per track when executing a Format Track command or an Initialize Parameters command.

3.5.5.5 Sector Number Register (Hex 1F3)

The sector number register is a read/write register and is used by the system to define the starting sector number for all disk-access commands. At the completion of each sector access, this register is updated to indicate the last sector accessed, whether successful or not.

3.5.5.6 Cylinder Low Register (Hex 1F4)

The cylinder low register is a read/write register and is used by the system to indicate the least significant 8-bits of the starting cylinder address for all disk-access commands. At the completion of each sector access, this register is updated to indicate the current cylinder number.

3.5.5.7 Cylinder High Register (Hex 1F5)

The cylinder high register is a read/write register and is used by the system to indicate the most significant 8-bits of the starting cylinder address for all disk-access commands. At the completion of each sector access, this register is updated to indicate the current cylinder number.

3.5.5.8 Drive/Head Register (Hex 1F6)

The drive/head register is a read/write register and is used by the system to select the drive and the head number for disk operations. After initialization, the drive number is set to 0 and the head number is set to 0.

3.5.5.9 Status Register (Hex 1F7)—Read-Only

The status register is a read-only register. It contains drive-status information. The content of this register is updated by the drive when each command is completed or whenever an error has occurred. When the busy bit is set to 1, the other bits in this register, as well as all other registers, are invalid. A read of this register automatically clears a pending interrupt request.

3.5.5.10 Command Register (Hex 1F7)—Write-Only

The command register is a write-only register that is used to specify a command and to initiate command execution. Because the command is performed immediately after writing to this register, the appropriate values must be loaded into the other registers before writing to the command register.

3.5.5.11 Alternate Status Register (Hex 3F6)—Read-Only

The alternate status register is a read-only register. It contains the same information as the status register. This register can be read at any time without clearing a pending interrupt.

3.5.5.12 Device Control Register (Hex 3F6)—Write-Only

The device control register is a write-only register.

3.6 IDE versus SCSI — A Brief Comparison

3.6.1 Introduction

In the past, many different types of hard disk interfaces were used in personal computer systems. Since the introduction of the first IBM PC, hard disk subsystems have changed from the original Seagate Technology model ST-506, to the Enhanced Small Device Interface (ESDI), to the Direct Bus Attach (DBA) interfaces, to the ATA/IDE interface, or finally, to the Small Computer System Interface (SCSI). Currently, the IBM PS/ValuePoint family of computer systems utilizes the ATA/IDE interface for its hard disk subsystems. The IBM PS/2 family uses both IDE and SCSI interfaces. To help the reader understand the differences between IDE and SCSI, this section provides a brief comparison between IDE and SCSI interfaces, and notes the families or models in which they are employed.

For a comparison between SCSI and ESDI, refer to 1.10, "SCSI versus ESDI" on page 14.

3.6.2 IDE/ATA Hard Disk Subsystem Summary

The ATA, or AT-DBA is the 16-bit controller developed for the AT-Bus (plus some enhancements) integrated onto the hard disk. This interface is the standard for the PS/ValuePoint line, and is a favorite among other PC manufacturers and most hard disk manufacturers. Hard disks interface directly with the AT bus and connect directly to the system board with a single ribbon cable that transmits commands and data, but receive power directly from the PC power supply by a four conductor cable. However, the low-power, 2.5-inch hard disks that are used in laptop PCs use a single ribbon cable that transmits commands, data and power.

IDE Subsystem Models

IBM uses ATA or IDE type of hard disk subsystems in PS/2 Models 35, 40, L40 SX and on all of the PS/ValuePoint family models.

IBM's implementation of the ATA interface takes advantage of the Identify command where the AT-DBA hard disk informs BIOS of its drive geometry, thus superseding the need for subsystems like the ST506 types. The PS/ValuePoint

systems' ATA/IDE hard disk subsystem support two hard disks (if one is set as master, and the other is set as slave).

3.6.3 SCSI Hard Disk Subsystem Summary

An interface that has recently become very popular with PCs is the Small Computer System Interface (SCSI). SCSI hard disks interface with the system via a SCSI host adapter, which is usually in the form of a card that plugs into an expansion slot on the system board. The SCSI host adapter serves as the interface between the PC bus and the SCSI bus. The SCSI bus is a 50-conductor-wide bus that allows up to eight SCSI devices to be connected.

One of the biggest advantages of SCSI is the ability to attach devices other than hard disks, such as CD-ROM drives, read/write optical drives, tape drives, and even printers, to the same SCSI bus. SCSI devices that are installed internally receive power from the PC power supply by a four-conductor cable. SCSI devices that are installed externally to the PC receive power from the enclosure that they are mounted in.

Data is transferred on the SCSI bus in 8-bit wide blocks. This can be done asynchronously or synchronously and at the fastest data rate that both the device and host adapter are capable of (up to 5 MBps). This information is negotiated by the device with the host adapter before the first data transfer.

SCSI Subsystem Models

IBM uses this interface on an adapter card in PS/2 Models 65, 80, 90, and 95. PS/2 Models 57SX and M57 SLC* have a SCSI chip set on the system board. Table 19 on page 118 lists the PS/2 models with SCSI.

Note: See Chapter 1, "What is SCSI" on page 1 for more details.

3.6.4 Hard Disk Subsystems — A Future Look

The future for hard disk interfaces appears to be in the ATA/IDE for low-end to midrange systems (PS/ValuePoint line) because of its cost/performance benefits, and SCSI for the midrange to high-end systems (PS/2s) because of its versatility. Also, SCSI will continue to be enhanced.

For the top-of-the-line file servers, a disk array can be built on the SCSI bus using special software drivers. In a disk array, each byte of data, along with control data, is usually spread among three to seven hard disks, allowing the data to be reconstructed in the event of a hard disk failure.

Chapter 4. XGA-2 Video Subsystem

4.1 Introduction

This chapter describes the IBM Extended Graphics Array-2 (XGA*-2) video subsystems. These replace the previous XGA versions from IBM. The XGA-2 subsystem also offers enhanced color features and support for the new 9518, 9515 and 9517 and the current PS/2 displays, such as the 8514, 8515, 8516 and 8518. It assists users who wish to begin complying with new industry and government standards, such as the International Organization for Standardization (ISO) standard 9241/3. It is a high-performance graphics subsystem with a powerful graphics coprocessor.

The IBM Extended Graphics Array-2 (XGA-2) is the video subsystem that is available for use with IBM Micro Channel machines. It is available either as an integrated component on a PS/2 motherboard, or as as an adapter card, which plugs into a Micro Channel slot.

Both systems consist of a video subsystem similar to the VGA, but with the addition of a coprocessor, which provides high-speed display update functions and extended graphics mode.

Both systems are 32-bit bus masters designed to support high-resolution screens (1024 x 768 pels with 256 colors, or even higher). They can fetch and store data that an application requires for display purposes in main system memory without the assistance of the main processor. This frees the main processor to handle other system activity. Both systems have 1 MB of video display buffer or video random access memory (VRAM).

Memory Differences

In certain countries IBM sold the XGA-1 adapter with only 512 KB of VRAM memory, which was upgradeable to 1 MB. All of the XGA-2 devices will have 1 MB of VRAM memory.

In this chapter, both the XGA-2 and the XGA-2 Adapter/A are treated as the same. Where there are differences, they are pointed out.

IBM makes the XGA-2 chip set available to Original Equipment Manufacturers (OEMs)[1].

[1] The Radius** XGA-2 Display Adapter for AT Bus systems is available from Radius, Inc.

4.2 Standards

4.2.1 XGA Standard

The Video Electronics Standards Association (VESA) has a sub-committee with responsibility for the XGA architecture. This has defined a hardware architecture for XGA. IBM is a member of VESA and will continue to implement various VESA standards.

The VESA XGA Extensions Standard defines its purpose as:

> "To standardize a software interface to XGA compatible subsystems, independent of which bus standard is implemented by the system, in order to provide uniform driver and application access to XGA compatible products."

The XGA standard defines a set of video calls that can be issued from a program to the video hardware subsystem. These calls are normally executed by the video subsystem itself, and usually do not require the assistance of the system processor. If a developer ensures that programs are written to this standard, then the underlying hardware support should be irrelevant to that developer.

Other details specify bus master, Direct Memory Access (DMA) and identification methods, as well as specifics for ISA, EISA and Micro Channel.

4.2.2 ISO Standard

The International Organization for Standardization (ISO) has published a number of standards dealing with personal computer environments. ISO standard 9241 details workstation ergonomics, and this standard includes more than just the personal computer itself. Please refer to Chapter 9, "Standards" on page 109 for more details. Examples include:

- User seating, posture and comfort (ISO 9241, Parts 5 and 6)
- Keyboard (ISO 9241, Part 4)
- Screen Image and Characters (ISO 9241 Part 3, Section 8)

The XGA-2 Adapter/A conforms to certain requirements of the relevant parts of ISO 9241, and can be used in those countries where this standard is a legal requirement. Compliance with one part of the standard does not imply that the standard has been implemented, and it should be emphasized that for the rest of the standard to be complied with the entire collection of various subsystems has to be reviewed for ISO compliance. This would imply the use of the correct displays, software, and environment in association with the XGA-2 Adapter/A. It also implies that the environment is used correctly, even if it is capable of using other features. For example the display must be used at a minimum of 72 Hz, which is an ISO standard.

4.3 Video Subsystem

Certain PS/2 machines may already have a video subsystem. This system video could be one of a Type 1, Type 2, or Type 3 video subsystem:

- Type 1 video — Video Graphics Array (VGA)
- Type 2 video — Extended Graphics Array (XGA-1)
- Type 3 video — Extended Graphics Array-2 (XGA-2)

4.3.1 Type 1 Video

The Type 1 video provides VGA function. Only one video subsystem within a PS/2 can be enabled into VGA or 132-column text mode at any one time.

4.3.2 Type 2 Video

The Type 2 video contains the XGA-1 function, which supports the VGA mode, 132-column text mode, and extended graphics mode. One to eight Type 2 video subsystems are allowed in a system.

4.3.3 Type 3 Video

The Type 3 video contains all the functions of the Type 2 video, along with other enhancements. This video type is implemented in XGA-2.

4.4 Type 2 Video Subsystems

The Base XGA function (including the VGA function) is generated by the Type 2 video subsystem. This video subsystem was delivered by IBM in the first XGA implementation (XGA-1).

The XGA function has three modes.

- VGA
- 132-column text
- Extended Graphics.

4.4.1 VGA Mode

In VGA mode, the XGA video subsystem is VGA register compatible with previous IBM VGA implementations.

4.4.2 132-Column Text Mode

In this mode, text is displayed in 132 vertical columns, and is accessible through BIOS mode 14 in the PS/2 Models 90 and 95.

4.4.3 Extended Graphics Mode

Extended Graphics mode provides the following software and hardware support.

1. IBM PS/2 8514/A Adapter Interface Compatibility

   Compatibility is provided through the XGA adapter interface, a device driver supplied with the subsystem as programming support for applications operating in the Disk Operating System (DOS) environment.

2. High Resolution Support

   Depending on the display attached and the size of video memory installed, the image on a screen can be defined using 1024 pels and 768 scan lines with 256 colors.

3. Direct Color Mode

   In this mode, each 16-bit pel in video memory specifies the color of the pel directly. This allows 65,536 colors to be displayed using 640 pels and 480 scan lines.

4. Packed Pel Format

   In the packed pel format, reads and writes to the video memory access all the data that defines a pel (or pels) in a single operation.

5. Hardware Sprite

   The sprite is a 64 x 64 pel image. When enabled, it overlays the picture that is being displayed. It can be positioned anywhere on the display without affecting the contents of video memory. For example, this feature can be used for a mouse pointer.

6. Display Identification

   Signals from the attached display identify its characteristics. Applications use this information to determine the maximum resolution and whether the display is color or monochrome. See Table 8 on page 58 for a list of supported IBM displays.

7. Coprocessor

   The coprocessor provides hardware drawing-assist functions throughout real or virtual memory. The following functions can be used with the XGA adapter interface.

   - Pel-block and bit-block transfers (PxBlt)
   - Line drawing
   - Area filling
   - Logical and arithmetic mixing
   - Map masking
   - Scissoring
   - X and Y axis addressing

   See 4.8.1.3, "Coprocessor" on page 50 for a brief description of each of the above fields.

4.5 Type 3 Video Subsystems

All functions of the Type 2 video subsystem are included in the Type 3 video subsystem. The Type 3 video subsystem is an enhanced version of the Type 2 Video subsystem that is delivered by IBM in the XGA-2 Subsystem. These enhancements include the following functions.

- Higher refresh rates, such as 75 Hz and 72 Hz, non-interlaced, for improved screen stability, even at higher resolution (1024 x 768). These higher refresh rates (72 Hz) are required for ISO compliance.
- Coprocessor support for Direct Color mode operation.
- The digital-to-analog converter (DAC) has been expanded from 18 bits to 24 bits, which allows up to 256 colors available from a palette of more than 16 million colors.
- Supports both VGA and mainframe interactive (MFI) character attributes in text mode.
- 1 MB of VRAM is standard in all countries.

4.6 Multiple XGA-2 Adapter/A Support

Up to six adapters can be installed, each driving a different display simultaneously and individually. On machines which have a built-in VGA, XGA-1, or XGA-2, there can be a maximum of five XGA-2 Adapter/A adapters. The number of adapters that can actually be installed depends on whether there are enough available slots. As a result, software developers can satisfy the demand for multiple independent display applications.

Note: Only one real VGA, VGA mode or 132-column text mode can be enabled at any one time. This is because all of these modes have only one set of addresses allocated - the VGA addresses. Multiple screens attached to multiple adapters can display VGA or 132-column text mode at once. The address decoding mechanism can be independently enabled and disabled for each adapter. A program can write to a screen, disable its address decoding mechanism, enable another adapter's decoding mechanism, and write to it in turn.

The XGA-2 Display Adapter/A can be installed in either a 16-bit or 32-bit Micro Channel slot that does not have an auxiliary video extension (AVE). One XGA-2 subsystem can coexist with the following video subsystems :

- VGA on a PS/2 planar
- XGA on a PS/2 planar
- XGA-2 on a PS/2 planar
- Up to three IBM Image Adapter/A or Image Adapter/A 1MB, 3MB, or 3MB 6091 adapters
- Up to five XGA Display Adapter/A adapters
- An IBM Display Adapter 8514/A card
- Adapters that utilize the Auxiliary Video Extension (AVE)

In PS/2 systems with no planar video, one video subsystem should occupy a slot with a Base Video Extension (BVE) in order to activate the Auxiliary Video Extension.

4.7 Video BIOS

The IBM Video BIOS has support for a number of different video modes. The different modes are selected through software calls. Most of these calls are included in the operating system that is executing on the PS/2, and therefore the user does not need to be concerned about various mode switching methods. The information in this section is for reference purposes only. More detailed information can be found in the *IBM Personal System/2 Video Technical Reference* (S42G-2193).

The video function is classified by BIOS mode numbers, which in turn define the screen size, colors, and associated parameters of the specific mode.

Table 5 on page 48 describes the alphanumeric (A/N) and all points addressable (APA) graphics modes supported by BIOS. Each color is selected from 256K (256 x 1024 = 262144) possibilities, and gray shades are selected from 64 possibilities. The variations within the basic BIOS modes are selected through

BIOS calls that set the number of scan lines. The scan line count is set before the mode call is made.

BIOS should be used to determine the modes that are supported on a given subsystem.

Table 5. XGA-2 BIOS Video Modes

Mode (hex)	Type	Colors	Alpha Format	Buffer Start	Box Size	Max. Pgs.	Vert. Pels
0,1	A/N	16	40x25	B8000	8x8	8	320x200
0*,1*	A/N	16	40x25	B8000	8x14	8	320x350
0+,1+	A/N	16	40x25	B8000	9x16	8	360x400
2,3	A/N	16	80x25	B8000	8x8	8	640x200
2*,3*	A/N	16	80x25	B8000	8x14	8	640x350
2+,3+	A/N	16	80x25	B8000	9x16	8	720x400
4,5	APA	4	40x25	B8000	8x8	1	320x200
6	APA	2	80x25	B8000	8x8	1	640x200
7	A/N	–	80x25	B0000	9x14	8	720x350
7+	A/N	–	80x25	B0000	9x16	8	720x400
D	APA	16	40x25	A0000	8x8	8	320x200
E	APA	16	80x25	A0000	8x8	4	640x200
F	APA	–	80x25	A0000	8x14	2	640x350
10	APA	16	80x25	A0000	8x14	2	640x350
11	APA	2	80x30	A0000	8x16	1	640x480
12	APA	16	80x30	A0000	8x16	1	640x480
13	APA	256	40x25	A0000	8x8	1	320x200
14	A/N	16	132x25	B8000	8x16	4	1056x400
14+	A/N	16	132x25	B8000	9x16	4	1188x400

Note:

* and + represent Enhanced Modes

Mode 14 character box size is determined by hardware.

In the 200-scan-line modes, the data for each scan line is scanned twice. This double scanning allows the 200-scan-line image to be displayed in 400 scan lines.

Certain modes on previous IBM display adapters distinguished between monochrome and color displays. For example, mode 0 was the same as mode 1 with the color burst turned off. Because color burst is not supported by the PS/2 video, the mode pairs are exactly the same. The support logic for the VGA function recognizes the type of display, and adjusts the output accordingly. When a monochrome display is attached, the colors for the color modes appear as shades of gray.

Mode 3+ is the default mode with a color display attached and mode 7+ is the default mode with a monochrome display attached.

Border support and double scanning depend on the mode selected. The following table shows which modes use double scanning and which support a border.

Table 6. XGA-2 Double Scanning and Border Support

Mode (Hex)	Double Scan	Border Support
0, 1	Yes	No
0*, 1*	No	No
0+, 1+	No	No
2, 3	Yes	Yes
2*, 3*	No	Yes
2+, 3+	No	Yes
4, 5	Yes	No
6	Yes	Yes
7	No	Yes
7+	No	Yes
D	Yes	No
E	Yes	Yes
F	No	Yes
10	No	Yes
11	No	Yes
12	No	Yes
13	Yes	Yes
14	No	Yes
14+	No	Yes

Note:

* and + represent enhanced modes

4.8 XGA Components

The XGA video subsystem components include:

- System bus interface
- Memory and CRT controller
- Coprocessor
- Video memory
- Attribute controller
- Sprite controller
- Alphanumeric (A/N) font and sprite buffer
- Serializer
- Palette
- Video digital-to-analog converter (DAC)

The following diagram represents the structure of the XGA subsystem and how the various components of the subsystem interrelate.

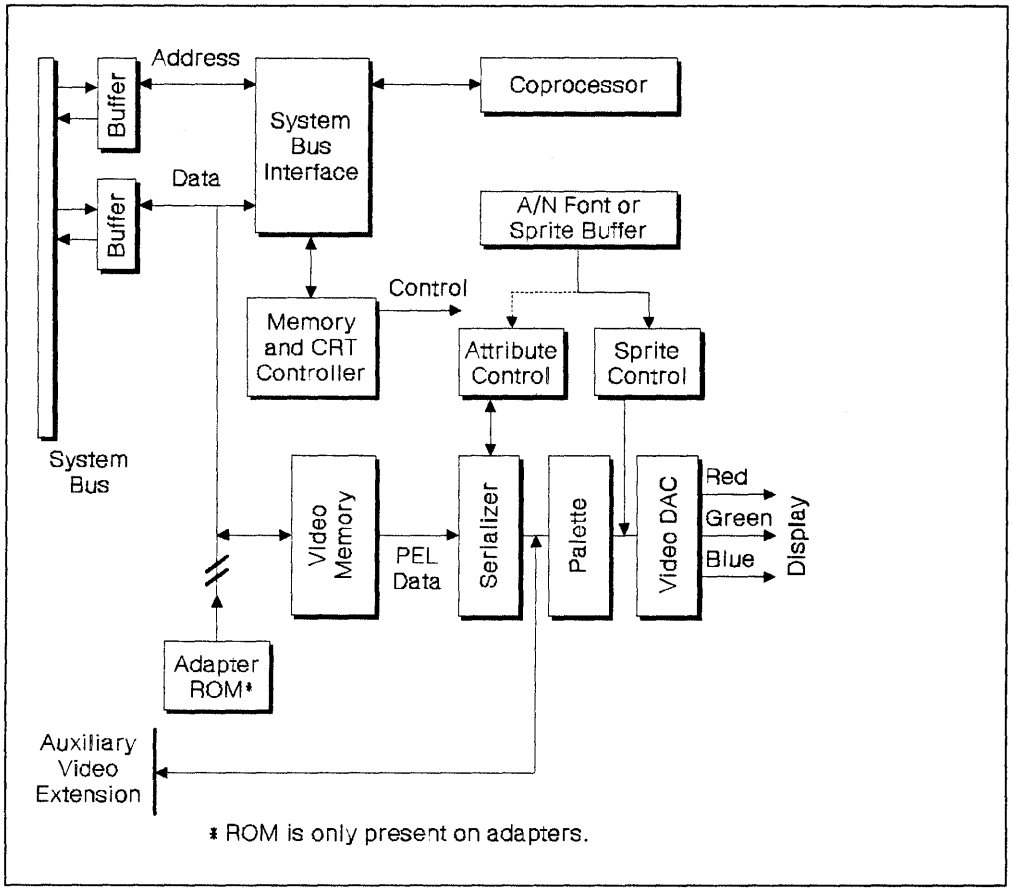

Figure 21. XGA Video Subsystem

4.8.1.1 System Bus Interface

The system bus interface controls the interface between the video subsystem and the system microprocessor. It decodes the addresses for VGA and XGA I/O registers, the memory addresses for the coprocessor memory-mapped registers, and video memory.

It also provides the bus master function, and determines whether the system data bus is 16 or 32 bits wide.

4.8.1.2 Memory and CRT Controller

The memory and CRT controller controls access to video memory by the system microprocessor, displays the contents of video memory on the display, and provides support for the VGA and 132-column text modes.

4.8.1.3 Coprocessor

The coprocessor provides hardware drawing-assist functions. These functions can be performed on graphics data in video memory and system memory.

The coprocessor updates the video memory independently of the system microprocessor. Instructions are written to a set of memory-mapped registers; the coprocessor then executes the drawing function.

The coprocessor functions are:

Pel-Block or Bit-Block Transfers
Transfers a bit map, or part of a bit map, from one location to another:

- Within video memory
- Within system memory
- Between system and video memory

Line Drawing
Draws lines, with a programmable style, into a bit map in video memory or system memory.

Area Fill
Fills an outlined area in video memory or system memory with a programmable pattern.

Logical and Arithmetic Mixing
Provides logical and arithmetic operations for use with data in video memory or system memory.

Map Masking
Controls updates to each pel for all drawing functions.

Scissoring
Provides a rectangular-mask function for use instead of the mask map.

X and Y Axis Addressing
Allows a pel to be specified by its X and Y coordinates within a pel map, instead of by its linear address in memory.

4.8.1.4 Video Memory
The video subsystem uses a dual-port video memory to store on-screen data, so that video memory can be read serially to display its contents as the data is being updated.

4.8.1.5 Attribute Controller
The attribute controller works with the memory and CRT controller to control the color selection and character generation in the 132-column text mode and VGA text modes.

4.8.1.6 Sprite Controller
The sprite controller is used to display and control the position and image of the sprite (cursor). The sprite is not available in 132-column text mode or VGA modes.

4.8.1.7 Serializer, Palette, and Video DAC
The serializer takes data from the serial port of video memory in 16- or 32-bit widths (depending on the size of video memory) and converts it to a serial stream of pel data. The pel data addresses a palette location, which contains the color value. The color value is passed to the DAC, which converts the digital information into red, green, and blue analog signals for the display.

4.8.1.8 Alphanumeric (A/N) Font and Sprite Buffer

This buffer holds the character fonts in 132-column text mode and VGA modes. It also stores the sprite image in Extended Graphics mode.

4.8.2 8514/A Compatibility

The XGA function is *not* hardware register compatible with the 8514/A adapter interface. Applications written directly to the register-level interface of the 8514/A adapter interface do not run.

The XGA function is 8514/A adapter interface compatible in the DOS environment through a DOS adapter interface driver supplied with the XGA video subsystem.

Applications written to the 8514/A DOS adapter interface should run unchanged with the XGA adapter interface. The following differences, however, should be noted:

OS/2 protected mode adapter interface
An XGA adapter interface driver is not available for the OS/2 protect mode.

640 x 480, 4 + 4 mode with 512KB display buffer
This is not an Extended Graphics mode, but applications using this mode and written to the rules for the 8514/A adapter interface will run.

Dual-display buffer applications
8514/A applications using VGA or other advanced function modes that rely on two separate video display buffers do not run on a single-display configuration. These applications run correctly with two video subsystems when one is an XGA-2 and each has a display attached.

Nondisplay memory
The XGA and 8514/A nondisplay (off-screen) memory are mapped differently. Applications using areas of the off-screen memory for storage might not run.

Adapter interface code size
The XGA adapter interface code size is larger than that for the 8514/A. This reduces the amount of system memory available to applications.

Adapter interface enhancements
The XGA adapter interface is a superset of that provided with the 8514/A. Any 8514/A applications using invalid specifications of parameter blocks might trigger some of the additional functions provided by the XGA adapter interface.

Use of LIM EMS drivers
Applications written to the 8514/A adapter interface that locate resources, such as bit maps or font definitions, in LIM EMS memory, and pass addresses of these resources to the adapter interface, require an EMS driver that has implemented the Physical Address Services Interface for bus masters.

Time-dependent applications
Some XGA and 8514/A functions run at different speeds. Applications that rely on a fixed performance might be affected by these differences.

XGA adapter interface directory and module name

The directory and module name of the XGA adapter interface, namely:

\XGAPCDOS\XGAAIDOS.SYS

is different from that of the 8514/A, namely:

\HDIPCDOS\HDILOAD.EXE.

Applications written to rely on the existence of either the specific 8514/A module name or directory do not run on the XGA Adapter Interface.

8514/A and XGA adapter interface code type

The XGA adapter interface is implemented at startup time as a device driver within the CONFIG.SYS file, and has the extension .SYS. The 8514/A adapter interface is implemented as a terminate and stay resident program (TSR). Applications written to rely on the adapter interface as a terminate and reside program do not run on the XGA adapter interface.

4.9 AVE Disabled

The AVE will be disabled when extended graphics mode is selected. It will also be disabled when a 95XX display is attached to the XGA-2 Subsystem, due to the higher refresh rate. This is important, especially where applications that use multiple screens are used, for example IBM ImagePlus*. Any displays that were displaying a VGA or 132 Column Text mode screen will freeze, and will continue to display the last screen of information displayed. They will only be updated again either when extended graphics mode is deselected, or when the software in the machine specifically addresses them.

4.10 XGA-2 Adapter/A Installation

Before the installation of the XGA-2 Adapter is attempted, the following installation manuals should be read :

- *IBM PS/2 XGA-2 Display Adapter/A Installation Instructions*, Part Number 53G2308
- *IBM Personal System/2 XGA Device Driver Installation Instructions*, Part Number 53G2122

In this section, the term "connector" refers to that part of an adapter that plugs into the Micro Channel. The term "slot" refers to that part of the Micro Channel into which the connector plugs.

4.10.1 XGA-2 Adapter/A Description

The following is an example of the XGA-2 Adapter/A.

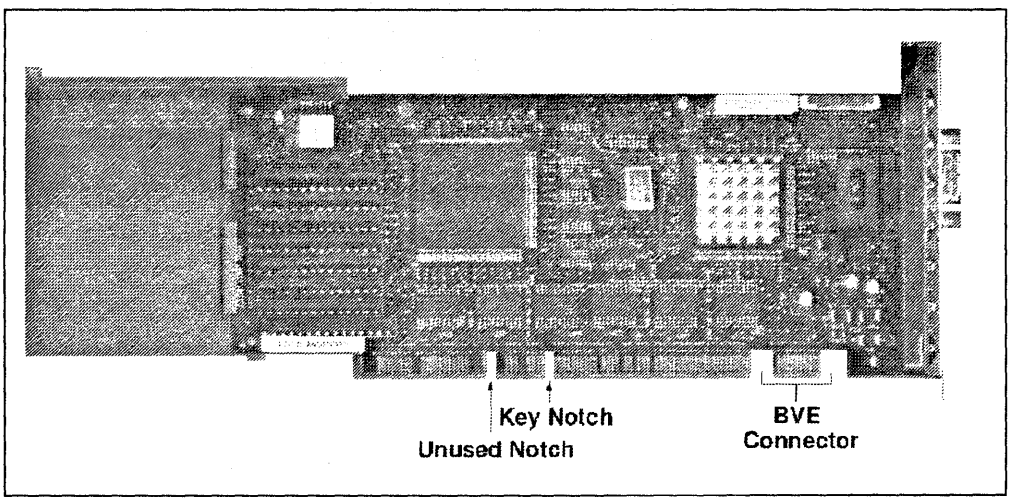

Figure 22. XGA-2 Adapter/A

Place the XGA-2 Adapter/A flat on a desktop with the blue plastic to the left, and the components facing up. The Micro Channel connector has four notches cut into it, two narrow ones on the left, and two wider ones to the right. The left most notch is not used. The second narrow notch from the left is the key notch that must be aligned with the primary datum as described in Figure 23 on page 56.

The metal contacts between the two large notches are the connectors that would plug into the BVE section of a Micro Channel slot, if one exists. If a BVE does not exist in a slot, then do not be concerned if these connectors hang over the edge of the slot. This is normal.

The XGA-2 planar subsystem interfaces to the Auxiliary Video Extension (AVE), whereas the XGA-2 Adapter/A interfaces to the Base Video Extension (BVE), which in turn drives the Auxiliary Video Extension. The XGA-2 Adapter/A can therefore drive a secondary screen through its connection to the Auxiliary Video Extension (AVE). Some machines have a Base Video Extension (BVE), as well as the Auxiliary Video Extension (AVE). The BVE is connected to the AVE, and has control over it. See Figure 23 on page 56 for a description of the Video Extensions. The planar version of XGA-2 is attached to the AVE on the planar.

4.10.2 Installation Process

The XGA-2 Adapter/A plugs into most standard Micro Channel 16-bit or 32-bit slots. It will perform faster in a 32-bit slot, but if there are only 16-bit slots left, it will still run there. However, for 32-bit operations, it will require two bus cycles instead of one, and memory addressability will be limited to 16 MB.

On some machines, there is a slot especially designed for the XGA-2 Adapter/A. This is called the Base Video Extension (BVE) slot. The XGA-2 Adapter/A should be plugged into the BVE if it is present.

Warning

On PS/2s that do not have a planar video subsystem there must be at least one instance of a video subsystem installed into a slot with BVE support. Otherwise there will be no video support on the AVE. The XGA-2 Adapter/A itself will still generate a video signal.

For example, on a PS/2 Model 95 there should be an XGA-1 or an XGA-2 card plugged into slot 5, which has the BVE extension.

There are five kinds of Micro-Channel slots. Various PS/2s will have have different combinations of these slots. These are:

- 32-bit slot
- 16-bit slot
- 16-bit or 32-bit slot with Matched Memory Extension
- 16-bit or 32-bit slot with Auxiliary Video Extension
- 16-bit or 32-bit slot with Base Video Extension

A Micro Channel slot with BVE can be recognized by the fact that it is the longest slot in a Micro Channel machine. A slot with an AVE is the second longest slot, while all others are shorter. The lengths of each type of slot are shown in this next figure. The Primary Datum in this diagram is the notch in the middle of an adapter connector. All measurements are shown from this notch to the end of the connector at the back of the PS/2.

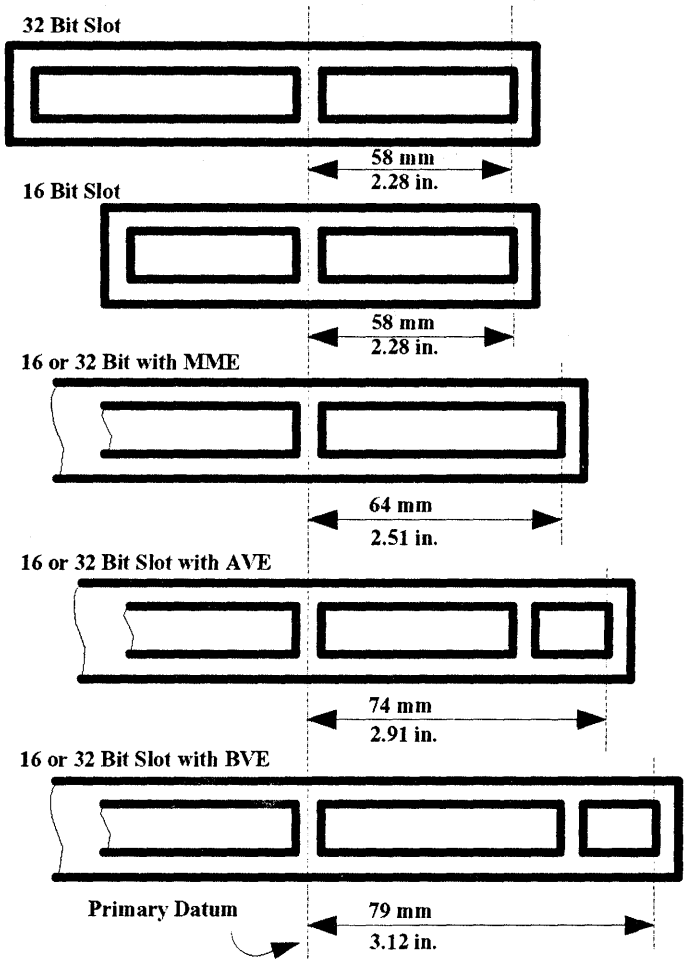

Figure 23. PS/2 Micro Channel Connectors (not to scale)

Caution

The one slot that the XGA-2 Adapter/A can *not physically* plug into is one designed for the 8514/A adapter, that is, a slot with an AVE connector. Do not force the adapter into such a slot.

The reason is that the 8514/A adapter has an extra set of connectors where it connects into the Micro Channel Slot. These can fit into a matching slot (AVE slot) on the Micro Channel bus. The XGA-2 Adapter/A has a Base Video Extension connector, and was designed to exploit a 32-bit slot. There are some connectors, used for matched memory, which would conflict with the position of the AVE. In summary then, the process for the installation of an XGA/2 card is:

- Review the installation instructions for the adapter.
- Determine what kinds of slots are in the PS/2.

- Where a system has available a Base Video Extension slot then it should be used.
- Next a 32-bit Micro Channel slot for optimum performance should be used.
- If neither of these are available, a 16-bit Micro Channel slot will suffice.

4.11 Graphic Modes

The following table shows the key resolutions available with the XGA-2 subsystem when running XGA applications and device drivers that exploit Display Mode Query and Set (DMQS). There is no "top" resolution as such. The XGA-2 subsystem is a programmable system and provided the 90 MHz pixel clock rate or the maximum values of the registers are not exceeded then almost any resolution is possible. For example, 1360 x 1024 is possible, but it would be 45Hz, interlaced, and certainly would not meet ISO requirements due to the flickering of the screen.

The maximum ISO capable resolution that is supported with IBM monitors is 1024 x 768, 75Hz non-interlaced. DMQS files are supplied for other (non-ISO) monitors to support 1280 x 1024 at 45Hz interlaced (16 colors).

Table 7. XGA-2 Resolutions Supported

Resolutions	Scan Frequency		I/NI	Max. Colors/Gray Shades	VESA
	Vertical (Hz)	Horizontal (KHz)			
640 x 480	60	31.5	NI	65536 / 256	
640 x 480	72	37.8	NI	65536 / 256	VS
640 x 480	75	39.4	NI	65536 / 256	
800 x 600	56	35.2	NI	65536 / 256	VG
800 x 600	60	37.9	NI	65536 / 256	VG
800 x 600	72	48.1	NI	65536 / 256	VS
800 x 600	75	50.0	NI	256 / 256	
1024 x 768	43.5	35.5	I	256 / 256	
1024 x 768	60	48.4	NI	256 / 256	VG
1024 x 768	70	56.5	NI	256 / 256	VS
1024 x 768	72	58.1	NI	256 / 256	
1024 x 768	75	61.1	NI	256 / 256	
1280 x 1024	45	48.8	I	16 / 16	

Note:

I = Interlaced

NI = Non-interlaced

VS = Video Electronic Standards Association (VESA) Standard

VG = VESA Guideline

The following table shows which IBM displays are supported at various resolutions. The monitor to be used should be chosen on the basis of which resolution will be used for most of the time. For example an IBM 9517 display is not suitable for 800 x 600 operation, whereas the 6312 would be an excellent choice in this environment. Some XGA-2 modes are shown with no displays. Although these modes are produced by the XGA-2 subsystem, it is recommended that another mode be used, or alternatively a non-IBM display.

Table 8. XGA-2 Supported IBM Displays

Resolutions	Scan Frequency		I/NI	Supported IBM Display
	Vertical (Hz)	Horizontal (KHz)		
640 x 480	60	31.6	NI	8503, 8504, 8507, 8511, 8512, 8513, 8514, 8515, 8516, 8517, 8518, 7544, 7554
640 x 480	72	37.8	NI	
640 x 480	72	37.8	NI	6312, 6314, 6319
640 x 480	75	39.4	NI	9515, 9517, 9518
800 x 600	56	35.2	NI	
800 x 600	60	37.9	NI	6312, 6314, 6319
800 x 600	72	48.1	NI	6312, 6314, 6319
800 x 600	75	50.0	NI	
1024 x 768	43.5	35.6	I	8507, 8514, 8515, 8516, 8517, 7554
1024 x 768	60	48.4	NI	6312
1024 x 768	70	57.0	NI	8517
1024 x 768	70	56.5	NI	
1024 x 768	72	58.1	NI	6314, 6319, 9517
1024 x 768	75	61.1	NI	9515
1280 x 1024	50	53.4	I	

Note:

I = Interlaced

NI = Non-interlaced

VS = Video Electronic Standards Association (VESA) Standard

VG = VESA Guideline

Displays Support

Many non-IBM displays, as well as the PS/ValuePoint 63XX displays report themselves as 8514 displays when queried by the XGA subsystem. This could limit the display only to 8514 capabilities, even if that display supports some of the enhanced features of the XGA-2 subsystem, and could even damage the equipment. The DMQS file should be updated to avoid this.

The DMQS file can be updated by executing the DMQS Configuration program. This process is described in the *IBM Personal System/2 XGA Device Driver Installation Instructions* (Part Number 53G2122).

4.12 Display Mode Query and Set

Display Mode Query and Set (DMQS) has been introduced so that device drivers written for the XGA Subsystem will work regardless of what display is attached. DMQS is needed so that device drivers and applications can determine screen size, ISO font compliance, and also screen characteristics, such as Color/Mono or LCD/CRT.

The XGA subsystem has a programmable frequency generator. This means that many different frequencies can be generated by the same subsystem. Displays attached to the subsystem limit the number of video modes available to the user. This limitation was previously imposed by the video subsystem, and not the display that was attached.

There are a number of ways that DMQS can determine the environment in which it is operating:

- Ask the user to key the information in
- Obtain the information from the BIOS of the XGA subsystem
- Read the information from a file

All these methods can be used to determine the environment. The file method can easily be used for those features not specifically supported on a particular system.

There are a number of benefits that result from DMQS. Device driver updates can be released independently of display or adapter releases. It also means that the XGA subsystem is not released with specific modes, rather the mode is dependent on the display. Most importantly, many more displays, including non-IBM displays, can be attached to the XGA subsystem.

4.13 Identification of an XGA Subsystem

An XGA subsystem and its manufacturer can be determined by examining the BIOS. Using the POS (Programmable Option Select) ID method, the manufacturer can be determined. The following IDs have been reserved (in hexadecimal):

- 8FD8 to 8FDB, and 8FD0 to 8FD3 reserved for IBM
- 0240 to 027F, 0830 to 0A7F and 0A90 to 0BFF reserved for non-IBM

Programmable Option Select (POS) extensions have been created to provide further information. These use a non-zero value in POS 6 as well as POS 7:

- Index 1 - 8-bit chip manufacturer ID (Assigned by VESA)
- Index 2 - 8-bit revision code (this is optional)

There is further information that can be gathered about the manufacturer of the subsystem motherboard. 6 bytes have been allocated in indexed input/output (I/O) space. These are bytes 72 to 77 hexadecimal. Using index 75 hex returns either:

- 8-bit board manufacturer ID (as assigned by the silicon vendor) or
- 16-bit board manufacturer ID (as assigned by VESA)

4.14 XGA-2 and Operating Systems

There are a number of prerequisites for operating systems before they will support the XGA-2 subsystem:

- OS/2 Standard Edition V1.3 requires the installation of CSD XR05101 or higher
- OS/2 Extended Edition requires the installation of CSD WR05101 or higher
- OS/2 Version 2.00 requires ServicePac* XR06055 or higher
- Preinstalled OS/2 Version 2 must be OS/2 V 2.00.1 or higher
- Windows 3.0 and Windows 3.1 require the XGA Device Driver diskette V2.0 or higher
- DOS 3.3 or higher requires the XGA Device Driver diskette V2.0 or higher

Note: The XGA-2 DOS adapter interface does not support 132 column text mode or direct color mode.

4.15 Benchmarks

Many of the benchmarks in use today were designed a few years ago when hardware-assisted display adapters were not available. They were designed to test the speed of adapters in a windowed environment. Many of these benchmarks analyze the calls that are being used, and give each of these calls a weighting factor. Calls that are used frequently have a higher factor than those used infrequently. Due to the fact that hardware assist did not exist, many hardware assist calls have a low factor.

An example of this scenario would be drawing the border of a window on the screen, that is, a rectangle. Due to the fact that there is no hardware assist the device driver is forced to issue a stream of pixel calls and paint each pixel of the rectangle individually. Hardware assist subsystems would simply issue a rectangle call. Many of the older benchmarks would measure the many pixel calls, and ignore the rectangle call totally. The same argument can be used for circles, arcs, lines, etc.

The best benchmark for any situation is to use the entire PS/2 system, as it would be actually configured at implementation time, with the actual application and operating system that would be used in production. This would provide the most reliable results for any benchmark situation.

4.16 Non-Interlaced Support

The XGA subsystem provides non-interlaced support. To use this feature, the user must have the XGA-2 subsystem, a display capable of non-interlaced support as well as new device drivers. A number of problems could occur:

- If the new XGA-2 subsystem is purchased, and the monitor is not upgraded then the front of screen is not changed. This means that it will still flicker.
- If an OEM display is purchased with the XGA-2 subsystem, then the DMQS display configuration profile often needs to be changed for the OEM display to take advantage of non-interlaced support. Many non-IBM displays, as well as the PS/ValuePoint displays tend to default as 8514 displays.
- If only the new 95XX displays is ordered, and not the XGA-2 subsystem as well, then problems could occur. This is because the 95XX displays do not work on existing XGA or VGA subsystems.
- The new hardware will not operate correctly without the new device drivers.

Chapter 5. Programming the XGA

5.1 Introduction

The XGA subsystem programs should use the XGA Device Driver, especially DMQS for mode setting. It is recommended that programs use the device drivers and do not access the hardware directly. This would ensure compatibility for future releases. See 4.8.2, "8514/A Compatibility" on page 52 for an example of some of the potential problems.

This section briefly looks at some of the programming issues. More detailed information on programming can be found in the *IBM Personal System/2 Video Technical Reference* (S42G-2193).

In the chapter that follows, the term "host processor" refers to the main processor in the PS/2. The term "coprocessor" refers to the processor within the IBM XGA that manipulates pixels.

This chapter refers to both the XGA-1 and the XGA-2 subsystems as described in Chapter 4, "XGA-2 Video Subsystem" on page 43. Where there are differences, they are pointed out.

5.2 Developer Assistance Program

Users should consider contacting their IBM representative for information on the Developer Assistance Program (DAP), or the OS/2 Expedite Program. IBM provides a number of services to assist users in developing software for the IBM PS/2 subsystems.

5.3 Registers

The XGA subsystem is controlled using a combination of input/output (I/O) mapped and memory mapped registers. I/O mapped registers are those that appear in the I/O address space of an Intel** 80x86 processor, and are accessed by using the I/O instruction set. Memory mapped registers are accessed with memory operations, and appear in the 80x86 memory address space. Memory operations are executed using combinations of registers and addressing modes. Memory mapped registers are generally used to control a coprocessor.

Where multiple XGA adapters have been installed (multiple instances), then each adapter has an instance number, and has its registers mapped at different addresses. These memory mapped registers will be located at some point in the address range C0000 and DFFFF, and is established during the PS/2 configuration process. The memory mapped registers for all adapters can be mapped within the same 8 KB block of address space. The configuration process should ensure that there are no conflicts between the XGA subsystem and other subsystems in the PS/2.

Memory mapped registers are used for the XGA coprocessor due to the fact that accesses are frequent and good performance is desired. The I/O address space of an 80x86 is limited to only 64 KB, which restricts the number of addresses

available to a coprocessor. Indexing is sometimes used to control this address area, especially to avoid conflicts with other adapters. Memory address space is much larger, and so the use of indexing is not needed. This means that processing time is reduced as the index does not have to be processed first before the XGA adapter is addressed.

An 80386 cannot do security checking on I/O accesses by applications trying to access the XGA Adapter, due to the fact that the XGA Adapter uses memory mapped registers. Caution should be used when an operating system allows this to be done easily, such as DOS, in order to ensure that the device driver is not compromised.

There is an optional real mode BIOS that uses mode tags rather than mode numbers. By using this feature (interrupt 10 and function 4E), certain information can be updated or obtained:

- XGA environment information, for example BIOS version, number of XGA subsystems
- XGA subsystem information, for example apertures and mode tags
- XGA mode information, such as resolutions.

5.4 LIM EMS Drivers

The XGA coprocessor memory-mapped registers are located in system memory address space. They reside in the top 1 KB of an 8 KB block of memory assigned to the XGA subsystem. The lower 7 KB of this block is used to address the ROM of an XGA subsystem on an adapter card.

Although an XGA subsystem integrated on the system board does not have a subsystem ROM, an 8 KB block of memory is allocated to it to support the coprocessor memory-mapped registers. While the lower 7 KB of this 8 KB block do not contain any memory, the memory-mapped registers are accessed in the top 1 KB of the block.

Applications or drivers, such as LIM EMS drivers that scan memory addresses looking for RAM or ROM signatures, might assume incorrectly that all 8 KB of memory is available for use.

The location of the 8 KB block of memory assigned to the XGA subsystem can be determined by using the system unit reference diskette. See the installation instructions for your EMS driver for details on how to avoid address conflicts.

5.5 XGA Applications (Written to the Hardware Interface)

If an XGA application is dependent on specific display IDs or characteristics, it might not function on an XGA subsystem. Applications written using Display Mode Query and Set (DMQS) will be insulated from the differences in the displays. Applications not written using DMQS should use only the displays supported by XGA-1.

5.5.1 Typical Coprocessor Operation

The typical operation of the coprocessor involves these steps:

1. The host processor loads the coprocessor registers to perform a particular operation.
2. The host system processor writes the definition of the operation in a "pixel operation register" to start the coprocessor.
3. The coprocessor performs the operation defined. The host system processor can perform other functions at this time.
4. The coprocessor completes the operation, informs the host processor, and becomes idle.
5. The process repeats.

5.5.2 Pixel Interface Overview

The pixel interface provides autonomous drawing functions. In brief, what happens is this:

In one sentence

Pixels from a source are combined with pixels from a destination under the control of a pattern and a mask, and the result is written back to a destination.

After each access the source, destination, pattern and mask addresses are updated according to the function being performed, and the operation is repeated until a programmed limit is reached.

This address update function takes place for a pixel block transfer (PxBlt), Bresenham line draw, or draw and step.

The function performed to combine the source and destination data can be a logical or an arithmetic operation. One of two possible operations is selected for each pixel by the value of the corresponding pattern pixel. Also, a mask pixel for each pixel allows the destination to be protected from update.

To simplify the process, the pattern data can be generated automatically from the source data. This is done by detecting pixels in the source that have a zero value.

A color compare function is provided. This allows the modification of the destination pixel to be dependent on the result of the comparison of the destination pixel with a programmable value.

Three general-purpose pixel maps (A, B and C) can be defined in memory. For each map a start address, height in pixels, width in pixels, and number of bits per pixel must be defined. Source, destination and pattern data can reside in any combination of these maps. There is also a mask map that has its own defined start address, height, width and format. Mask data is always taken from this map.

Source, destination and pattern data are each addressed by unique X and Y pointers. Should the source or pattern X and Y pointers move outside the extremities of their pixel maps, they automatically wrap around to the opposite

side of the pixel map. However, if the destination X and Y pointers move outside the extremities of the destination map, no update of the destination map takes place until the pointers move back inside the map. Figure 24 on page 66 shows a simplified representation of the coprocessor graphics data flow.

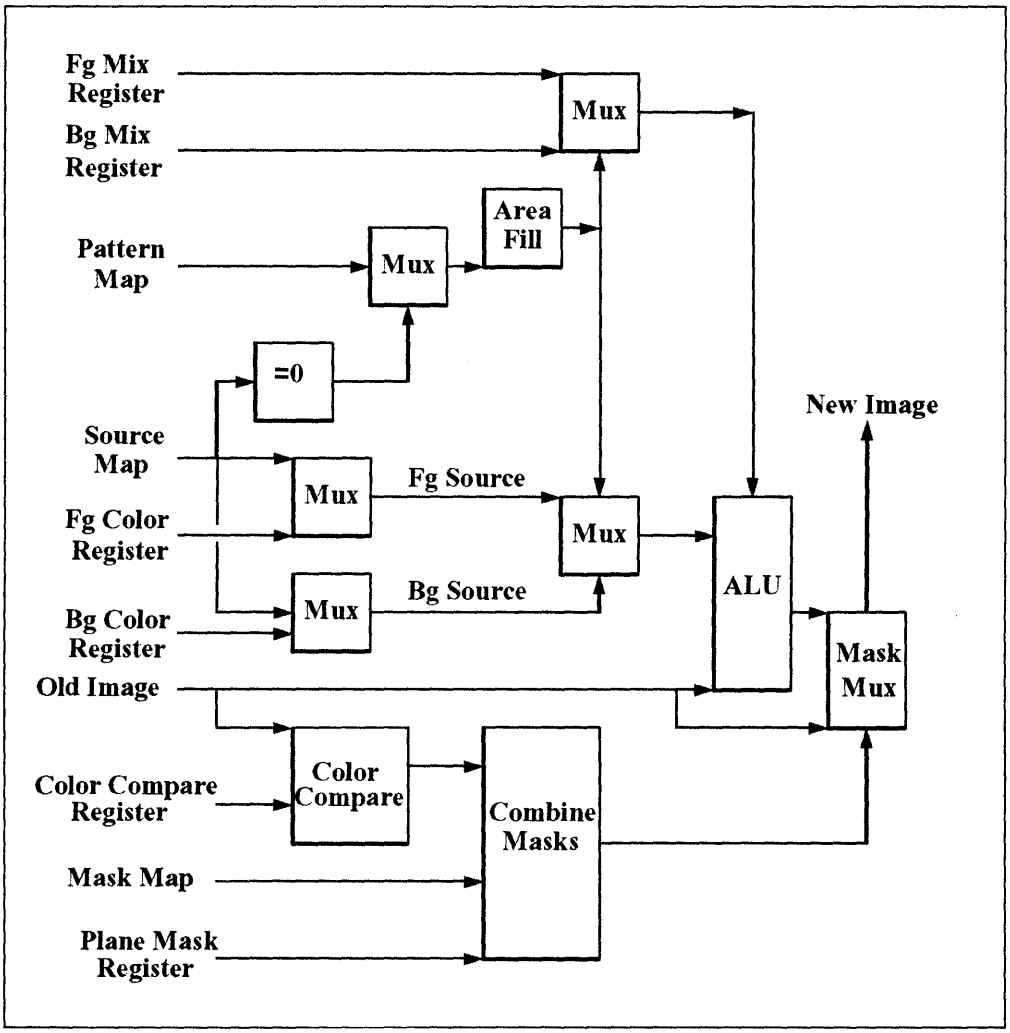

Figure 24. XGA Coprocessor Data Flow.

The diagram shows some of the elements of data flow logic. The abbreviations are:

Fg - Foreground

Bg - Background

Mux - multiplexor

ALU - arithmetic and logic unit

5.5.3 Purpose of the Mask Map

Besides the three general-purpose maps, the IBM XGA also defines a mask map. This map is closely related to the destination map. It allows the destination to be protected from update on a pixel-by-pixel basis. Therefore, it can provide a scissoring or clipping function. Furthermore, it can do so on any arbitrary shaped area.

The size of the mask map must be less than or equal to that of the destination map. If it is smaller than the destination map, its location relative to the destination map must be indicated. Two pointers, called the Mask Map Origin X Offset and Mask Map Origin Y Offset, are loaded into memory. Figure 25 on page 67 illustrates the mask map and its offset pointers.

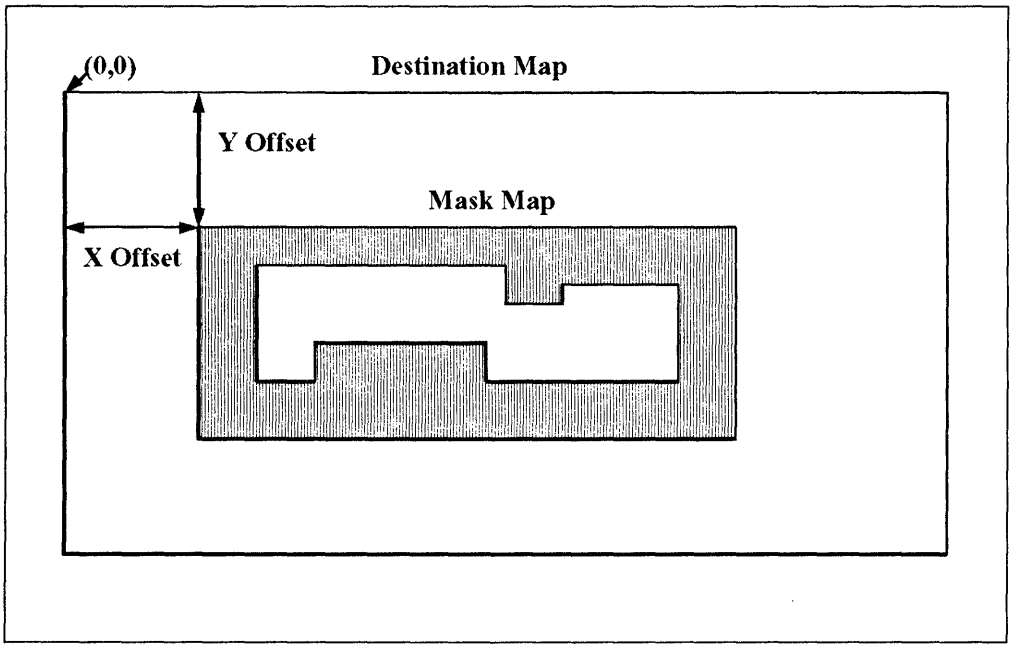

Figure 25. XGA Mask Map Origin X and Y Offsets.

The shaded area indicates that a destination pixel is masked. Note that the mask map is located within the destination map.

For any operation, there are three ways that the mask can be used.

Disabled The map and its contents are ignored.

Boundary Enabled The contents of the map are ignored, but the boundary acts as a rectangular scissor window on the destination map.

Enabled The contents of the mask map act as a possibly non-rectangular window. The extremities of the mask map also provide a rectangular scissor window.

Figure 26 on page 68 shows the effect of a mask map enabled operation. In this illustration, horizontal lines of pixels are transferred to the destination map. Pixels have been scissored because they are either outside the destination map, outside the mask map boundary, or masked by the mask map.

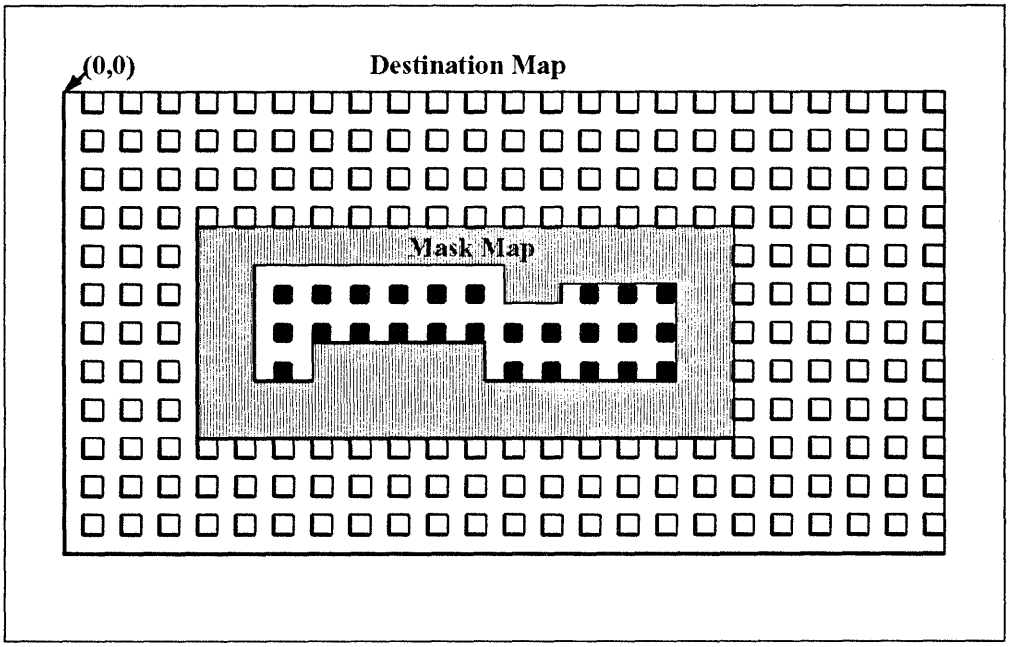

Figure 26. XGA Mask Map Enabled.

Solid blocks indicate that the pixel is drawn. Empty blocks indicate that the pixel is not drawn.

The entire operation illustrated in Figure 26 would be performed by the coprocessor without any use of the host system processor until the operation was complete.

5.5.4 Mask Map Example

The Pixel Block transfer (PxBlt or "pixel blit") can be extremely powerful. An example of such an application would be one that edited photographs, for example a photograph of a crowd. The photograph has been scanned and placed in memory, but only a portion of it is to be included in a document. To isolate the part of the image that is needed, a mask can be created that covers the unwanted area. A pointing device could be used to "cut out" the portion needed. The mask can be placed in the center of a destination area, and the PxBlt procedure can be used to transfer the source so that the background is cleared and just the needed portion remains.

5.5.5 Purpose of the Pattern Map

The purpose of the pattern map can be described by extending the previous example, where a pattern effect can be applied to the image that was extracted from the photograph background. The application may have a draft printing mode for example, and so there would be a need to make the picture appear less distinct than it really is. One way to achieve this is to turn off every second pixel of the image. Here a selective pattern is used where the pixels are a single bit, and alternate between on and off. Two valid possibilities for this pattern map are shown in Figure 27 on page 69.

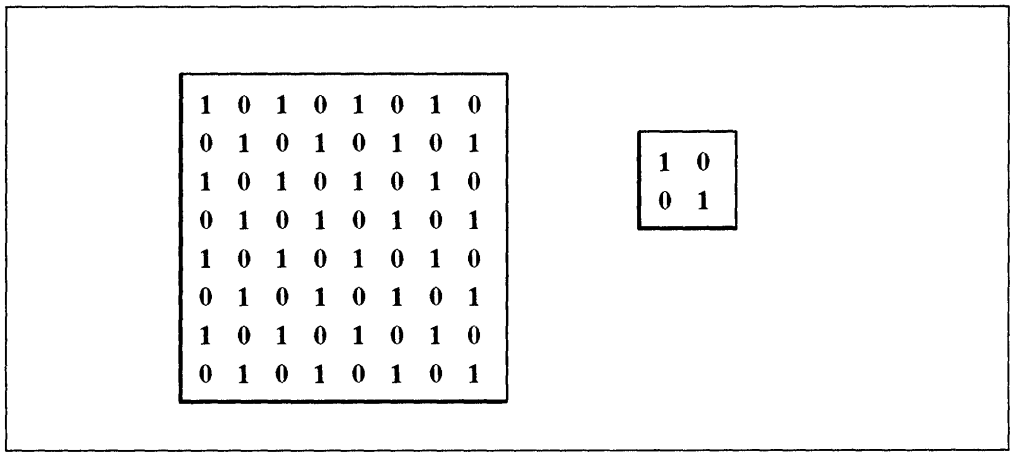

Figure 27. XGA Pattern Map Example.

The diagram shows two examples of a pattern map. Since the pattern is regular, and the X and Y pointers wrap around, both examples achieve the same result.

Because the pattern X and Y pointers automatically wrap around to the opposite side when they move outside the extremities of their map boundaries, and because the pattern map is so regular, either pattern map will suffice.

These tasks are accomplished without the use of the host processor's resources.

5.6 Pixel Operation Summary

Where applicable, the possible address and data modifiers are listed under each combination.

Pixel Data Combinations

- Source Pixels (1, 2, 4 or 8 bits/pixel)
  - Map A, B, or C
  - Foreground color register (fixed)
  - Background color register (fixed)
- Pattern Pixels (1 bit/pixel)
  - Pattern forced to foreground
  - Map A, B or C
  - Pattern generated from source
- Destination Pixels (1, 2, 4 or 8 bits/pixel)
  - Map A, B or C
- Mask Pixels (1 bit/pixel)
  - Mask map disabled
  - Mask map boundary enabled
  - Mask map enabled
- All Maps
- Specified width and height

Address Update Functions

- Read Draw and Step
- Write Draw and Step
- Read Bresenham Line Draw
- Write Bresenham Line Draw
- Pixel Block Transfer (PxBlt)
- Inverted Pixel Block Transfer
- Area-Fill Pixel Block Transfer

Update Masking

- Drawing Mode (for Draw and Step and Bresenham Line Draw)
  - Normal
  - First pixel null
  - Last pixel null
  - Area outline
- Scissoring
  - Fixed destination boundary scissor
  - Mask map rectangular or non-rectangular scissor
- Color Compare
- Plane Masking

Data Modifiers

- ALU mixes (foreground and background)
  - All 16 logical
  - 6 arithmetic
- ALU Sources
  - Fixed color (foreground or background)
  - Source pixel map data

Chapter 6. SVGA Video Subsystems

6.1 Introduction

This chapter describes the IBM Super Video Graphics Adapter (SVGA) video subsystems. These replace the previous VGA versions from IBM. These SVGA subsystems offer enhanced color features and support for the new 6312, 6314 and 6319 and the current PS/2 monitors, such as the 8503, 8504, 8512, 8513, 8514, 8515, 8516, and 8518. All IBM SVGA Subsystems conform to industry and government standards, such as the Video Electronic Standards Association (VESA), the Federal Communication Commission (FCC), Swedish magnetic test specifications (VLMF), International Organization for Standardization's (ISO) standard 9241 (see 9.3, "ISO and the European Community" on page 109 for more information), and others. It is a high-performance graphics subsystem that operates in CGA, EGA, VGA or SVGA modes.

The IBM Super Video Graphics Adapter (SVGA) is the video subsystem that is available for use with IBM AT-Bus machines. This is a brand new line of personal systems know as the IBM PS/ValuePoint systems. For more information on PS/ValuePoint, please refer to 6.2, "IBM Personal System/ValuePoint" on page 72, or contact the IBM representative in your area. The SVGA subsystem is available as an integrated component, Very Large Scale Integration (VLSI), on PS/ValuePoint motherboard, and comes in two versions - one for 386** systems and one for 486** machines. The SVGA subsystem for the PS/ValuePoint 386-based systems is the CL-GD5422 provided by Cirrus Logic** Corporation, and is remarketed by IBM. The SVGA subsystem for the 486 based ValuePoint systems uses the ET4000 chip provided by Tseng** Labs Inc. on behalf of IBM.

Note: For the remainder of this chapter, SVGA-386 refers to the CL-GD5422 Cirrus Chip Set, and SVGA-486 refers to the ET4000 Tseng Labs Chip Set. Because of the differences between the Cirrus and the Tseng SVGA chips, technical portions of this chapter are subdivided by the SVGA-386 (PS/ValuePoint 386 video subsystems) or SVGA-486 (PS/ValuePoint 486 video subsystems) topics.

Both PS/ValuePoint SVGA subsystems consist of a greatly improved video subsystem which is similar to the previous PS/2 VGA subsystem under MCA, but with a broader capability of modes and frequencies which is described in detail in Table 9 on page 78, and in Table 12 on page 89.

Both subsystems support higher resolution, interlaced and non-interlaced monitors, with a maximum resolution of 1280 x 1024 (interlaced) pels. The popular 1024 x 768 pels is supported in both non-interlaced and interlaced modes. The 800 x 600 and 640 x 480 displays are also supported in non-interlaced mode. For a complete list of all available modes, refer to Table 9 on page 78, and Table 12 on page 89. Both subsystems contain 1 MB of video display buffer or video random access memory (VRAM).

6.2 IBM Personal System/ValuePoint

To further satisfy customer needs IBM announced a new brand product family, the Personal System/ValuePoint (PS/ValuePoint), a value-priced offering complete with new displays, which complements the PS/1* and PS/2 families of Personal Systems. This new family of desktop/client systems and compatible displays provides excellent value at an attractive price. The objective is an industry-compatible system with IBM value added, for example: function, technology, and performance, to be equal or better than similar industry products with quality, reliability, service, and support.

6.2.1 PS/ValuePoint In Brief

Some of today's customers have everyday business tasks which can be adequately accomplished at typical industry performance levels, from systems built with readily available industry technology. For these customers IBM introduces the PS/ValuePoint:

- A high quality value-priced IBM system engineered by IBM with the objective being to meet or exceed typical industry standard function and performance levels ("industry standard" means product characteristics which have become accepted as the current norm in the personal computer industry for a given price range product).
- Based on the best technology and component values in the industry
- Developed to meet high standards of quality and reliability
- Manufactured to high quality standards
- Tested to standards which exceed industry norms
- Compatible with readily available upgrade options
- Serviced and supported by IBM's quality service organization

The IBM PS/ValuePoint systems are "ISO capable" as described in Chapter 9, "Standards" on page 109.

6.3 SVGA-386 Introduction

The SVGA-386 VSLI Video Graphics Controller chip is remarketed by IBM from Cirrus Logic for the Personal Systems 386 ValuePoint family. The chip is the Cirrus Logic TrueColor CL-GD5422 which is designed to optimize cost/performance trade-off considerations, providing a cost-efficient solution to IBM's latest generation of 386 ValuePoint display controllers. The CL-GD5422 is specifically designed for the IBM PS/ValuePoint, and compatible systems offering 100% register-level compatibility in all video standards using VGA, EGA, CGA, MDA, and Hercules** modes, and is VESA standard compatible as well. Refer to 9.5, "Video Electronics Standards Association" on page 112 for information about the VESA and the VESA standards.

The SVGA-386 video graphics controller supports high resolution graphics and text display modes for a variety of color CRT monitors using industry standard 15 pin analog video and VESA interfaces. This highly integrated chip includes a programmable Dual-frequency Synthesizer and Digital to Analog Converter (DAC). The SVGA-386 chip implements all control and data registers in the standard VGA controller, and implements all data manipulation capabilities and data paths in the standard VGA adapter.

6.3.1 SVGA-386 Overview

The following figure presents a graphical overview of the SVGA-386 Graphics Controller chip.

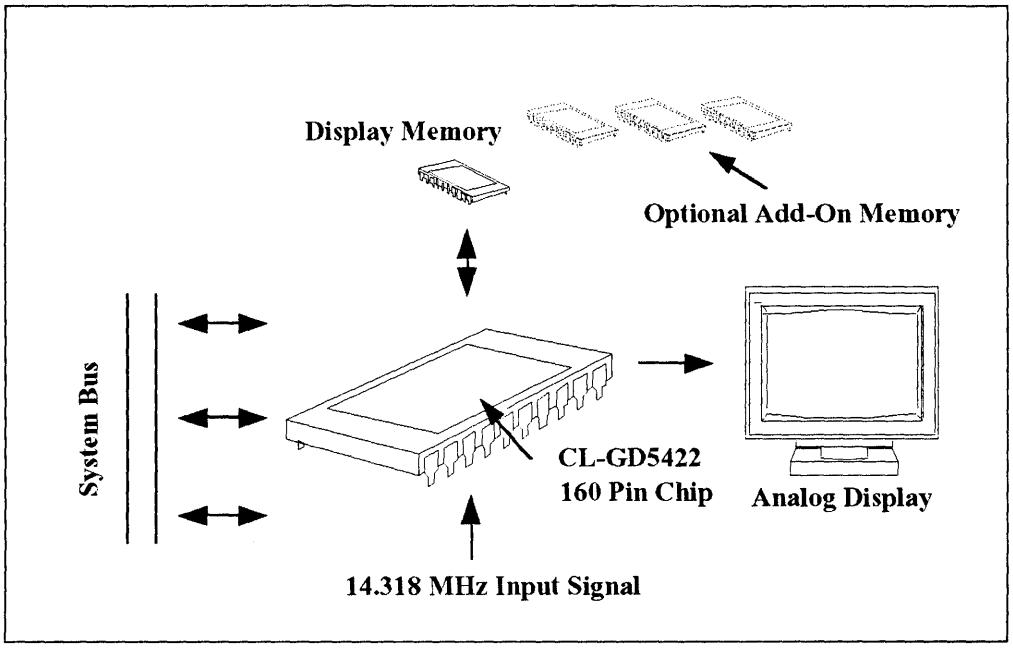

Figure 28. PS/ValuePoint SVGA-386 Single Chip Controller

The SVGA-386 video graphics controller is hardware-compatible with the IBM VGA standard and provides improved performance with additional functionality. It is ideally suited to highly integrated systems; the CL-GD5422 chip requires no external support other than display memory and a 14.31818-MHz frequency reference. The chip connects directly to the ISA bus, and can connect to the local bus in the future (should this arrangement be accepted as an industry standard), allowing a minimum adapter solution. The chip operates at dot clock rates programmable up to 75 MHz supporting standard VESA high resolution along with extended modes. The internal Palette DAC may be configured to provide a palette of 256K colors, or true-color displays of 32K, 64K, and 16.8M colors. The dual-frequency synthesizer requires a single crystal or reference for all supported screen resolutions, as well as all standard memory speeds and formats. The chip supports all control and data registers according to current VGA standard data path and data manipulation functions which provides complete hardware compatibility.

In addition, the SVGA-386 supports extended registers and compatibilities to provide functional and performance enhancements beyond standard VGA. The chip supports a 16-bit host interface in all operations, including I/O and memory operations in planar modes. All write cycles to memory are optimized with zero-wait-state capability.

6.3.2 SVGA-386 Features

The following is a list of the major features of the SVGA-386 CL-GD5422 VSLI Video Graphics Controller.

- 100% hardware and BIOS IBM VGA compatible
- Motherboard VGA solution with only two ICs
- Resolutions up to 1280 x 1024
- Video Overlay and Color Key Support
- 24-bits/pixel 640 x 480 True-color Interface
- Integrated Palette DAC and Dual-Frequency Synthesizer
- 32 x 32 Hardware Cursor
- 64 x 64 Hardware Cursor
- 1 MB Maximum Display Memory
- 16-bit Video Bus Interface
- 32-bit Video Bus Interface Capability
- 8-bit wide DRAMs
- Programmable Dot Clock up to 75MHz
- Up to 12.5 MHz ISA Interface
- Zero wait state
- 16-bit Host Bus I/O Memory
- VESA pass-through feature connector
- Low-power CMOS, 160-pin package

6.3.3 SVGA-386 Brief Description

The SVGA-386 Cirrus CL-GD5422 includes all the hardware required to implement CPU updates to display memory, screen refresh, and DRAM refresh. It interfaces directly with the HOST system, display memory, and the monitor. The host interface is 16 bits wide for memory and PS/ValuePoint I/O. The chip requires no glue logic for address decoding and control handshaking.

Four major functions supported by the SVGA-386 chip are:

- Host Access to Registers
- Host Access to Display Memory
- Display Access to Display Memory (screen refresh)
- Display Memory Refresh

For programming information or a more complete description of the SVGA-386 subsystem, please refer to the *TrueColor VGA Family - CLGD5422, Technical Reference Manual* dated June 1992 and published by Cirrus Logic, Inc., Fremont, CA 94538.

6.3.3.1 Host Access to Registers

The ISA host can access the SVGA-386 chip's registers by setting up a 16- or 24-bit address and generating I/O control signals to read or write 16-bit data. Other activities such as screen refresh and delayed CPU writes to display memory can take place concurrently with accesses to registers. These registers include all the standard VGA registers, and are host-readable to allow BIOS and driver software to determine the state of the graphics adapter.

6.3.3.2 Host Access to Display Memory

The SVGA-386 chip handles the host access to display memory. The host effects memory accesses in the VGA address range to transfer data to or from one or more of the four display memory planes. All of the required video handshake interface signals are internally generated by the CL-GD5422 with no requirement for external logic decoding.

The chip takes 24-bit addresses from the ISA host, and transforms them according to the selected addressing mode and address space mappings, then issues multiplexed addresses to the planes via the memory address (pins 9:0) bus. Row Address Strobe (RAS), Column Address Strobe (CAS), Output Enable (OE), and Write Enable (WE), pins 3:0, provide timing and control to the display memories. When interfacing to DRAMs that have dual-CAS signals, the CAS pin becomes WE, and the WE (pins 3:0) pins become CAS (pins 3:0).

A write buffer is logically located at the CPU interface to isolate the CPU from the display memory. The CPU write access to display memory takes place immediately until the write buffer is full. The address and the data are written into the cache, and the actual write into display memory occurs later. If the write buffer is full, wait states will be inserted until there is space.

6.3.3.3 Display Access to Display Memory (Screen Refresh)

The chip contains an Intelligent Address Sequencer (IAS) that allocates display memory cycles not only to the host, but also to the display CRT controller for screen refresh. A First In First Out (FIFO) memory between the memory sequencer and the Attribute Controller (ATC) decouples the memory speed from the display speed, allowing the execution of fast page mode accesses for screen refresh. This minimizes the memory bandwidth required. The display is blanked during horizontal and vertical retrace intervals, freeing additional memory bandwidth for host access. The chip improves the performance of the IBM VGA implementation, especially for lower resolution displays.

6.3.3.4 Display Memory Refresh

Display memory refresh is handled by the chip's refresh of the DRAMs used for display memory. During each horizontal blanking period, a selectable number of CAS-before-RAS refresh cycles are executed.

6.3.4 SVGA-386 Components

The SVGA-386 incorporates all major subsections of the IBM VGA/EGA into a single circuit. The following information lists the major SVGA-386 video subsystem components with a short description following.

- Sequencer
- CRT Controller
- Graphics Controller

- Attribute Controller
- Programmable Dual-Frequency Synthesizer
- DAC Palette

6.3.4.1 Sequencer

The sequencer controls access to the display memory. It ensures that the necessary screen refresh and dynamic memory refresh cycles are executed, and that the remaining memory cycles are made available for CPU and Block Logical Transfer (BLT) read/write operations. The sequencer consists of a memory arbitrator and memory controller. It accepts requests from memory address counters associated with the CRTC, and address transformation logic associated with the graphics controller. It uses the video FIFO to deliver data to the ATC, and the write buffer to transfer data to the graphics controller.

The memory controller is driven by the Memory Clock (MCLK) that is optimized for the speed of the DRAM used independent of the video clock. It generates the signals and addresses necessary for accessing the display memory. The memory arbitrator is also driven by the MCLK. It implements a procedure that selects from either the CPU or the CRT on a dynamic priority.

6.3.4.2 CRT Controller

The CRT controller generates the horizontal and vertical synchronization signals for the CRT display. It includes various registers that allow flexible configuration options. These options include user configurable horizontal and vertical timing and polarity, cursor position, horizontal scanlines, and other display related characteristics.

The CRT controller is the equivalent of the IBM CRTC as implemented in the IBM VGA hardware. The CRT controller also provides split screen capability and smooth scrolling.

6.3.4.3 Graphics Controller

The graphics controller operates in either text or graphics modes and has the following major functions:

- Provides to the host CPU a read/write path to display memory
- Controls all four memory planes
- Allows data to be manipulated prior to being written to display RAM
- Formats data for use in various backward compatible modes
- Provides color comparators for use in color painting modes
- Reads/writes 32-bit words through the 32-bit display memory interface
- Combines display RAM data and attribute data for output to the pixel bus

The graphics controller directs data from the display memory to the ATC and the CPU. For write operations, the data from the CPU bus are combined with the data from the SET/RESET logic, depending on the write mode. In addition, the data may be combined with the contents of the read latches, and some bits or planes may be masked (prevented from being changed).

The graphics controller is also involved when the CPU is reading data from display memory. Depending on the read mode, the data returned may be the

actual contents of the display memory, or it may reflect the outcome of comparisons with the color value in one of the graphics controller registers.

6.3.4.4 Attribute Controller (ATC)

The ATC controls blinking and underline operations in alphanumeric modes. It also provides the horizontal pixel panning capability in both alphanumeric and graphics modes.

6.3.4.5 Programmable Dual-Frequency Synthesizer

The SVGA-386 chip includes an integrated Dual-frequency Synthesizer that can be programmed to generate the Video Clock (VCLK) for many standard screen formats, and the MCLK used by the sequencer. The synthesizer requires a single-reference frequency of 14.31818 MHz that can be supplied by the on-chip oscillator, or injected from an external source.

6.3.4.6 DAC Palette

The integrated DAC palette interfaces directly to the monitor connector via appropriate RFI filters. The DAC palette can be programmed for 256 simultaneous colors from a palette of 256K, or it can be programmed for direct color mode. In direct color mode, three bytes from display memory are combined for each pixel. This allows 32K, 64K, or 16.8M simultaneous colors on the screen depending, of course, on the display monitor.

With this type DAC palette configuration, the pixel bus, Video Dot Clock (DCLK), and BLANK can be driven into the chip. This allows it to operate in the VESA standard VGA Pass-through Connector Mode. Fifteen, sixteen-bit data can also be inserted from an external source through the p<7.0> pins. In addition to the VESA standard, the enable video (EVIDEO) input is capable of switching at the pixel rate. In overlay mode, the 24-bit data cannot be driven through the connector.

6.3.5 Hardware/Software Compatibility

The SVGA-386 is CGA, EGA, MDA, and VGA compatible. This allows a selection of a broad range of display monitors. The chip includes all register and data paths required for VGA controllers. Enhancements include 1024 x 768 8-bit pixel mode, and internal color palette, eight simultaneously loadable text fonts, write mode 3, and readable registers. Extended resolution display modes are made possible by the high video clock rates and high display memory bandwidth. Extended text and graphics resolutions beyond 640 x 350 (IBM EGA), and 640 x 480 (VGA standards) are also supported by the Cirrus Logic BIOS on:

- Fixed frequency PS/2 compatible monitors such as the IBM 85XX monitors
- PS/ValuePoint 6312, 6314, and 6319 multi-frequency compatible monitors
- Non-IBM multi-frequency monitors such as the NEC MultiSync**

In addition, 132-column and 60-line text modes are supported, with 640 x 480 and 800 x 600 32K- and 64K-color graphics modes. Also, the 800 x 600 16-color VESA mode and the 640 x 480 16.8M TrueColor graphics mode are supported. The extended resolution display capabilities are listed in Table 9 on page 78.

6.3.6 SVGA-386 Display Modes

The following table lists the display modes provided by the SVGA-386.

Table 9 (Page 1 of 2). SVGA-386 Display Modes Table - Graphics and Text

Mode (hex)	Type	Colors	Alpha Format	Box Size	Pels	H Freq KHz	V Freq Hz
0,1	A/N	16/256K	40x25	9x16	360x400	31.5	70
2,3	A/N	16/256K	40x25	9x16	720x400	31.5	70
4,5	APA	4/256K	40x25	8x8	320x200	31.5	70
6	APA	2/256K	80x25	8x8	640x200	31.5	70
7	A/N	Monochr.	80x25	9x16	720x400	31.5	70
D	APA	16/256K	40x25	8x8	320x200	31.5	70
E	APA	16/256K	80x25	8x14	640x200	31.5	70
F	APA	Monochr.	80x25	8x14	640x350	31.5	70
10	APA	16/256K	80x25	8x14	640x350	31.5	70
11	APA	2/256K	80x30	8x16	640x480	31.5	60
12	APA	16/256K	30x30	8x16	640x480	31.5	60
12+	APA	16/256K	30x30	8x16	640x480	37.9	72
13	APA	256/256K	40x25	8x8	320x200	31.5	70
14	A/N	16/256K	132x25	8x16	1056x400	31.5	70
54	A/N	16/256K	132x43	8x8	1056x350	31.5	70
55	A/N	16/256K	132x25	8x14	1056x350	31.5	70
58,6A	APA	16x256K	100x37	8x16	800x600	35.2	56
58,6A	APA	16x256K	100x37	8x16	800x600	37.8	60
58,6A	APA	16x256K	100x37	8x16	800x600	48.1	72
5C	APA	256x256K	100x37	8x16	800x600	35.2	56
5C	APA	256x256K	100x37	8x16	800x600	37.9	60
5C	APA	256x256K	100x37	8x16	800x600	48.1	72
5D	APA	16x256K	128x48	8x16	1024x768	48.3	60
5D	APA	16x256K	128x48	8x16	1024x768	56	70
5Di	APA	16x256K	128x48	8x16	1024x768	35.5	87i
5F	APA	256/256K	80x30	8x16	640x480	31.5	60
5F	APA	256/256K	80x30	8x16	640x480	31.5	70
60i	APA	256/256K	128x48	8x16	1024x768	35.5	87i
60	APA	256/256K	128x48	8x16	1024x768	48.3	60
60	APA	256/256K	128x48	8x16	1024x768	56	70
64	APA	64K			640x480	31.5	60
64	APA	64K			640x480	37.9	72
65	APA	64K			800x600	35.2	56
66	APA	32d			640x480	31.5	60
66	APA	32d			640x480	37.9	72
67	APA	32d			800x600	31.5	56

Table 9 (Page 2 of 2). SVGA-386 Display Modes Table - Graphics and Text

Mode (hex)	Type	Colors	Alpha Format	Box Size	Pels	H Freq KHz	V Freq Hz
6Ci	APA	16/256K	160x64	8x16	1280x1024	48	87i
6Di	APA	256/256K	160x64	8x16	1280x1024	48	87i
6F	APA	64K	40x25	8x8	320x200	31.5	70
70	APA	16M	40x25	8x8	320x200	31.5	70
71	APA	16M	80x30	8x16	640x480	31.5	60
74i	APA	64K			1024x768	35.5	87i

Note:

A/N = Alphanumeric modes (text) text modes with 350 scan lines.

APA = All points addressable modes (graphics)

d = 32K Direct Color/256 color mixed mode

i = interlaced modes

Some modes are not supported by all Cirrus CL-GD5422 controllers. Refer to CL-GD5422 Data Sheet and the Software Release Kit for further information.

Some modes are not supported by all monitors. In that case, the best quality vertical refresh rate for the monitor type selected will be automatically used.

6.3.7 Choosing the Video Mode (CLMODE)

The CLMODE utility allows the user to define the type of monitor attached and set the video modes supported by your computer. CLMODE.EXE is preinstalled on PS/ValuePoint 386 systems; it also comes with the 386 SVGA Drivers/Utilities diskette.

CLMODE allows you to do the following tasks:

1. Choose the attached monitor type.

   Selecting the proper monitor type will allow your computer to display the highest quality output that it is capable of with the attached display. The monitor type also determines what video modes will be available to your system.

2. High or low VGA refresh rate
3. Set the video mode
4. Review the current VGA controller status

   This options displays the Cirrus Logic VGA type, the BIOS version number and the amount of video memory present

These options can be set by either using through CLMODE's menu-driven interface or by issuing the CLMODE command with command line options. For a detailed description of CLMODE, refer to *IBM PS/ValuePoint 386 SVGA Drivers/Utilities User's Guide.*

6.3.8 SVGA-386 Graphic Modes

The following table shows the key resolutions available with the SVGA-386 subsystem when running graphics applications and device drivers that exploit display modes. It is followed by a table showing the IBM monitors at their highest refresh rates and resolutions supported by SVGA-386.

Table 10. SVGA-386 Resolutions Supported

Resolutions	Scan Frequency		I/NI	Max. Colors/Gray Shades	VESA
	Vertical (Hz)	Horizontal (Hz)			
640 x 480	60	31.5	NI	16M / 256	
	72	37.9	NI	256 / 256	VS
800 x 600	56	35.2	NI	64K / 256	VG
	60	37.9	NI	256 / 256	VG
	72	48.1	NI	256 / 256	VS
1024 x 768	60	48.3	NI	256 / 256	VG
	70	56	NI	256 / 256	VS
	87	35.5	I	256 / 256	
1280 x 1024	87	48.1	I	16 / 16	

Note:

I = Interlaced

NI = Non-interlaced

VS = Video Electronic Standards Association (VESA) Standard

VG = VESA Guideline

Table 11. SVGA-386 Supported IBM Monitors (Including Refresh Rates)

Monitor	640 x 480	800 x 600	1024 x 768
8503, 8512, 8513, 8518	60 Hz (NI)	N/A	N/A
8514, 8515, 8516	60 Hz (NI)	N/A	43.5 Hz (I)
6312	60, 70, 72 Hz (NI)	56, 60, 72 Hz (NI)	60 (NI), 87 Hz (I)
6314	60, 70, 72 Hz (NI)	56, 60, 72 Hz (NI)	60, 70 (NI), 87 Hz (I)
6319	60, 70, 72 Hz (NI)	56, 60, 72 Hz (NI)	60, 70 (NI), 87 Hz (I)

Note:

Supported resolutions, like 1280 X 1024 are available for non-IBM (OEM) monitors provided the scanning frequencies match the SVGA-386 graphics controller.

N/A = not available.

6.3.9 SVGA-386 DOS 5.0 Device Drivers

The following is a brief listing of the DOS 5.0 compatible device drivers that are shipped with the SVGA-386 PS/ValuePoint systems. If you don't see the device driver you need listed here, or you have further questions refer to IBM Part Number 53G0178, *IBM PS/ValuePoint 386 SVGA Drivers/Utilities User's Guide* or call your local IBM technical support representative.

- Microsoft** Windows** 3.1
- Autodesk** Device Interface (ADI) Drivers
- Framework** II
- Framework III
- GEM/3**
- Generic CADD
- Locus Computing PC Xsight**
- Lotus** 1-2-3**, Symphony**, and Report Writer v2.x
- Lotus 1-2-3 v3.0
- OrCAD**
- Personal CAD (PCAD**)
- Ventura Publisher**
- VERSACAD 386
- VERSACAD 2D
- Microsoft Word** 5.0 and 5.5
- WordPerfect** 5.x
- WordStar** 5.5, 6.0+
- WordStar 2000 3.5

6.4 SVGA-486 Introduction

The SVGA-486 ET4000 video graphics controller chip has been designed to optimize cost/performance trade-off considerations, providing a cost-efficient solution to IBM's next generation of 486 ValuePoint display controllers. The ET4000 is specifically designed for the IBM PS/ValuePoint, and compatible systems offering 100% register-level compatibility in all video standards using VGA, EGA, CGA, MDA, and Hercules modes.

The ET4000 is a single 0.8 micron VSLI chip which is distinguished from the previous generation of VGA controllers by its high level of intelligence and flexibility in managing memory resources. Recently, memory technology has changed from wider (more available pins) to deeper (more memory) configurations. This characteristic places greater importance on graphics controller Application Specific Integrated Circuits (ASIC).

The SVGA-486 has created a completely new design which initiates a new generation of design techniques particularly relating to memory resource management capabilities. The ET4000 has:

- Multiple blocks of Cache Memory
- Multiple blocks of First In First Out memory (FIFO)
- A Memory Management Unit (MMU)
- A System Priority Controller (SPC)

These added capabilities translate to minimum memory requirements and higher system performance. There are two other performance features worth mentioning. One has to do with the VGA speed, and the other with memory resources.

In a VGA display controller, only two 1 MB memory devices are needed to maintain comparable VGA performance. The faster, or additional memory chip installed with the SVGA-486 provides performance up to 17 times that of the VGA while achieving zero wait state during memory write access.

Another interesting aspect of the SVGA-486's memory resource management features is its capability to be reconfigured for the amount of useable memory on board. For example, in maximum memory implementation, defective memory detected during diagnostic procedures is ignored and ET4000's memory is reconfigured for minimum video memory execution with an understandable loss of performance.

6.4.1 SVGA-486 Overview

The following figure presents a graphical overview of the SVGA-486 Controller Subsystem Block Diagram.

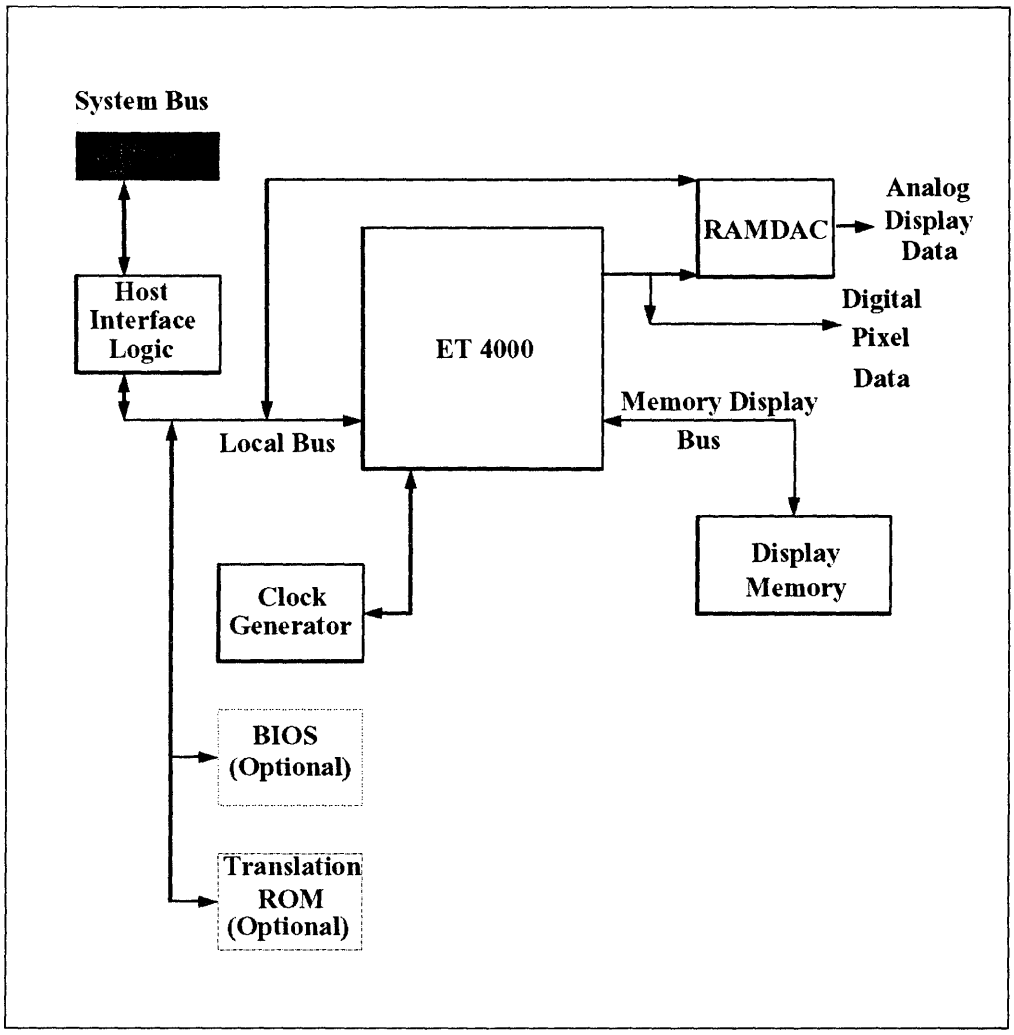

Figure 29. PS/ValuePoint SVGA-486 Subsystem Block Diagram

The SVGA-486 input interface uses an 8 or 16-bit programmable data bus via an internal system configuration register consisting of a 20-bit linear address and a 4-bit segment address. The bus is controlled by the PS/ValuePoint AT bus interface. The output monitor interface can be interlaced or non-interlaced vertical synchronization (V-SYNC) and horizontal synchronization (H-SYNCH) with polarity control and 8-bit palettes. There is an external Digital to Analog Converter (DAC) for look-up, pixel clock, blanking, and read/write decode control. Resource management has six primary functions. A brief description follows.

Memory Management

Memory management contains a VGA graphics controller, and least recently used (LRU) cache, up to two FIFOs, and a memory control unit (MCU) of 1MB of VRAM.

System Priority Controller (SPC)

An intelligent SPC is used to resolve multiprocessor and ET4000 request to optimize MCU utilization.

Cathode Ray Tube (CRT) Control

The CRT controller contains a 8-bit horizontal H-SYNCH, and an 11-bit vertical V-Synch counter.

Display Address Control

Display address control is achieved via a 18-bit linear address and a 5-bit row address generator.

Attribute Control (ATC)

The attribute controller provides text mode support of up to 256 character sets with IBM-compatible text attribute and cursor blink/underline control. Programmable font widths are 8, 9, 10, 12, and 16 pixels.

Timing Interface (TI)

The timing interface selects up to 8 Memory Clock (MCLK) cycles for pixel clock, 80 MHz for graphics, 56 MHz for text, and 50 MHz for the system clock. Plane, linear byte, linear word graphics, and VGA-compatible text formatting with up to 16-bit wide characters. The maximum display resolution is 1024 x 768 in 256 and 1280 x 1024 in 16 colors interlaced or non-interlaced in graphics mode. The display pixel clock rate in graphics is 65 MHz and 56 MHz in text modes.

6.4.2 SVGA-486 Compatibility

- The SVGA-486 is *register level* compatible with:

  CGA, MDA, HERC, EGA, VGA, SVGA.

- The SVGA-486 is *display level* compatible with:

  the 8514/A.

- The SVGA486 is *monitor level* compatible with:

  IBM 8503, 8512, 8513, 8514, 8514, 6312, 6314, 6319, NEC Multisync, Multisync Plus, XL, and others with up to 1280 x 1024 resolution.

6.4.3 SVGA-486 Features

The following is a list of the important features of the SVGA-486 ET4000 VSLI Video Graphics Controller.

6.4.3.1 Compatibility Features

- IBM CGA, EGA, MDA, VGA compatible
- Easy interface with all popular microprocessors, including: Intel 8086, 80286, 80386, Motorola 68000, and Zilog** Z8000 families.

6.4.3.2 Cursor Control Features

- Full cursor text and APA graphics capabilities
- Text mode cursor supports underline and full cursor height
- 18-bit linear start and cursor address
- Cursor, horizontal display enable, and horizontal synch signals may be skewed independently

6.4.3.3 Display Features

- Up to 64-bit color comparison function, allows byte-wide pixel-to-color comparison facilitating area fill operations
- Interlaced or non-interlaced display screen
- Dot frequency response to 80 MHz
- Plane-wide and linear byte-wide data structures to support dot 16 and 256 color formats
- Color and monochrome support

6.4.3.4 Display Memory Features

- All display memory can be read from or written to with minimum wait states and are fully 8 or 16-bit data bus compatible.
- Up to 64-bit display memory modification in plane graphics mode
- Bit-masking of CPU data, software-selectable, enabling pixel-specific manipulation of display memory.
- Software selectable X-first, Z-first, and block move write access to display memory
- Byte-wide software-selectable Boolean functions of CPU data and latched display memory data
- Addressing may be linear byte, linear word, double word, or with memory planes paired into double-sized planes
- 1 MB display memory addressing to support up to 1024 x 768 256 color formats
- Programmable CAS before RAS refresh, providing memory refresh during blanking
- X-Y memory addressing allowing definition of virtual display area wider than the CRT surface
- Programmable display memory start address for virtual panning/scrolling applications around a virtual screen higher than the CRT surface
- Split-screen feature allows second independent window starting at display memory address zero

6.4.3.5 Scanning and Scrolling Features

- 5-bit raster scan addressing supporting 32-scan-line fonts with double scanning as software selectable
- Completely independent software control of horizontal display enable, blanking, and synch signal and vertical display enable, blanking, and synch signals
- Raster address presetting allows smooth single scan line scrolling even in text mode
- Split-screen window occupies full width of screen with starting scan line software-selectable

6.4.3.6 Panning Features

- Horizontal panning supported by the attribute controller permits smooth movement around the virtual display area
- Supports both PEL and byte panning
- Panning can be disabled within a split screen

6.4.3.7 Programmable Features

- Programmable character width up to 16-dot-per-character modes
- Programmable internal color lookup table with 16 x 6-bit entries
- Supports external palette RAM interface
- Border color programmable to 1 of 256 colors

6.4.3.8 Miscellaneous Features

- Single +5V power supply
- 7 times faster than previous ET3000 version
- I/O register translation in both read and write operation
- Single-cycle software-selectable data rotation of CPU data
- Programmable memory timing control for any-speed DRAM interfaces
- Graphics mode blinking allows full emulation of text mode in bit-mapped graphics mode; intensity, reverse-video, and cursor can all be simulated by software
- Supports up to two simultaneous soft fonts
- Software selectable CPU interrupt generated on vertical retrace

6.4.4 SVGA-486 Brief Description

The SVGA-486 is a highly integrated, highly flexible single-chip controller that can propel a video design using a minimum number of components. A complete VGA-486 video design uses a chip configured with only two 1 MB DRAMs. The SVGA-486 requires no additional support chip to interface to the PC/AT bus. This means it uses less space and fewer overall components (as compared with similar controllers), provides high performance, and high reliability, at a reduced cost. These attributes make the SVGA-486 ideal for system motherboard integration. The chip set delivers resolutions up to 1024 x 768 with 256 simultaneous colors, interlaced or non-interlaced; and resolutions up to 1280 x 1024 with 16 colors, interlaced. This provides interfacing compatibility with a wide variety of non-IBM monitors as well.

The SVGA-486 is easily programmed and configured to function as a SVGA/VGA/EGA/CGA/MDA controller with only two 100ns 1MB DRAMs on typical board-level configuration. The standard AT-bus configuration consists of a single memory bank as display buffer, the ET4000 VSLI chip, and external color look-up DAC (Digital to Analog Converter), and data, address buffers, and multiplexors as support logic.

The PS/ValuePoint video connector allows interfacing to a color or monochrome monitor. The CPU bus interface is based on the IBM PC/XT* bus timing. This video configuration can be programmed by a single register to be 100% register-level compatible with VGA/EGA/CGA, or monochrome display adapter (MDA) controller. All of the VGA/EGA text and graphic modes are supported, as

well as all of the VGA/EGA hardware assist features, including data latching, bit masking, rotation, logical functions and plane-selects which are provided at register-compatible level.

6.4.5 SVGA-486 Components

The following information lists the major SVGA-486 video subsystem components with a short description following.

- CRT Controller (CRTC)
- Memory Control Unit (MCU)
- System Priority Control (SPC)
- Timing Sequencer (TS)
- Graphics Display Controller (GDC)
- Attribute Controller (ATC)
- ROM BIOS (RB)

  For detailed programming or more in-depth information, refer to the *ET4000 Graphics Controller, High Performance Video Technology* manual from Tseng Labs, Inc., Newton, PA 18940, or contact your local IBM technical support representative.

6.4.5.1 CRT Controller (CRTC)

The SVGA-486 CRTC provides an 18-bit linear address cursor control and Vertical Scan (VS) and Horizontal Scan (HS) controls to external raster-scan CRT displays. Internally, CRTC derives all reference timings in two dimensions:

- Horizontal display/blanking/synchronization
- Vertical display/blanking/synchronization.

Each horizontal cycle and vertical cycle centers around character and line reference log. Each character is based on multiples of an 8 or 9 MCLK. Both character and line reference logic can be asynchronously initialized via the SYNR input pin.

6.4.5.2 Memory Control Unit (MCU)

The Memory Control Unit consists of four parts:

Memory Control
RAS/CAS/MW/DTE/SCC timing/sequence control; the trp (RAS pre-charge), trcd (RAS to CAS delay), tcas (CAS pulse width), and tcp (CAS pre-charge) are programmable via register RCONF.

Memory Address
provides up to 1 MB addressing space via AB<8.0> and AA<8.0>.

Memory Data
provides from 8-bit display memory data width to 32-bit data width via MD<31.0> data interface.

Memory Refresh
programmable refresh frequency via CRTC Indexed Register 36.

6.4.5.3 System Priority Control (SPC)

The System Priority Controller's main task is to orchestrate the internal resource requests, including: the FIFOs, Graphics Data Controller, Cache Controller, and RAM refresh. The system performance is based on two major factors:

- The ATC demand - the display resolution and color
- The memory bandwidth - the memory bus width and access time.

Other factors also can contribute to the overall performance. For example, the cache controller can be optimized for sequential access and CPU write operations. The 16-bit CPU bus interface also results in a faster data transfer, particularly in the plane graphics mode (a 16-bit CPU write = up to a 64-bit data transfer).

6.4.5.4 Timing Sequencer (TS)

The Timing Sequencer is a set of registers responsible for providing basic timing control for both the CRTC and ATC. Seven of these eight registers are internally indexed, which means they are accessed via a common I/O address, with one of the seven registers that is selected by the timing sequencer index register. Timings controlled by the TS registers include:

- Horizontal count resolution: 8 or 9 dots/character
- SCLK/2, MCLK/2, MCLK/4, and DCLK/2 (dotclock)
- Video load control: every 8, 16, or 32 dot clocks

6.4.5.5 Graphics Display Controller (GDC)

The Graphics Display Controller optimizes bit-mapped display memory data manipulation by assisting the CPU in the operation of displaying memory data-related functions. This includes: rotate/mask/z-plane with any of the four Boolean functions in response to a single CPU write. By placing basic bit map operations in high-speed hardware, the SVGA-486 dramatically increases graphics processing throughput over software-driven solutions. The data manipulation capability implemented in the GDC is, however, applicable only for plane systems and not for linear byte systems. This is because all the processing functions are designed to manipulate pixel data with one bit sourced from each plane. For example, the color compare function allows four bits across four planes (one pixel) to be compared to a pre-defined color, therefore allowing eight pixels to be color-compared simultaneously by processing 32 bits of video data (one byte from each plane).

6.4.5.6 Attribute Controller (ATC)

The Attribute Controller provides flexible high-speed video shifting and attribute processing, designed for both text and graphics video display applications. The ATC can process up to 16-bits of display at the rate of 45 MHz or 8-bits at the rate of 84 MHz. In graphics mode, memory bits are reformatted into pixel color data groups of 16, 8, 2, or 1 adjacent bits. Next, they are translated through a 16-element color look-up table, and sent out serially to the video display. Through this pixel mapper, the ATC supports:

- PLANE oriented pixel structures for 16 colors
- BYTE oriented pixel structures for 256 colors
- WORD oriented pixel structures for 64K colors

In text mode, 8 bits of character code data and 8 bits of attribute data are loaded. The character code is used to look up a font table that is then loaded as the corresponding 16 bits of font data. The attribute is then applied to the font/cursor data, translated through the color lookup table, and sent out serially to produce 16 colors of text data at speeds of up to 56 MHz. In high resolution modes, the SRC<0> bit in the ATC auxiliary register will, when set to 1, process the pixel at half the MCLK rate internally and provide the full pixel clock (PCLK) at the same rate as MCLK. The high resolution modes should be used when the desired PCLK is greater than 45 MHz.

6.4.5.7 ROM BIOS (RB)

The SVGA-486 ROM BIOS contains modules that provide video BIOS functions to support both VGA and EGA compatible modes. Please refer to the following MODE and Extended MODE tables and sections for a detailed list of all supported scanning frequencies and color modes. When the RB is employed, the CPU reads the ROM BIOS during the bootstrap operation, and the ROM enable signal (ROMEL) will be activated to enable the ROM data onto the BD bus with the DIR signal driven high to allow the ROM data to be read by the host processor.

6.4.6 SVGA-486 Display Modes

The following table lists the display modes provided by the SVGA-486.

Table 12 (Page 1 of 2). SVGA-486 Display Modes Table - Graphics and Text

Mode (hex)	Type	Colors	Alpha Format	Box Size	Pels	H Freq KHz	V Freq Hz
0	A/N	16/256K	40x25	8x8	320x200	31.5	70
0*	A/N	16/256K	40x25	8x14	320x350	31.5	70
0+	A/N	16/256K	40x25	9x16	360x400	31.5	70
1	A/N	16/256K	40x25	8x8	320x200	31.5	70
1*	A/N	16/256K	40x25	8x14	320x350	31.5	70
1+	A/N	16/256K	40x25	9x16	360x400	31.5	70
2	A/N	16/256K	80x25	8x8	640x200	31.5	70
2*	A/N	16/256K	80x25	8x14	640x350	31.5	70
2+	A/N	16/256K	80x25	9x16	720x400	31.5	70
3	A/N	16/256K	80x25	8x8	640x200	31.5	70
3*	A/N	16/256K	80x25	8x14	640x350	31.5	70
3+	A/N	16/256K	80x25	9x16	720x400	31.5	70
4	APA	4/256K	40x25	8x8	320x200	31.5	70
5	APA	4/256K	40x25	8x8	320x200	31.5	70
6	APA	2/256K	80x25	8x8	640x200	31.5	70
7	A/N	Monochr.	80x25	9x14	720x350	31.5	70
7+	A/N	Monochr.	80x25	9x16	720x400	31.5	70
D	APA	16/256K	40x25	8x8	320x200	31.5	70
E	APA	16/256K	80x25	8x8	640x200	31.5	70
F	APA	Monochr.	80x25	8x14	640x350	31.5	70
10	APA	16/256K	80x25	8x14	640x350	31.5	70

Table 12 (Page 2 of 2). SVGA-486 Display Modes Table - Graphics and Text

Mode (hex)	Type	Colors	Alpha Format	Box Size	Pels	H Freq KHz	V Freq Hz
11	APA	2/256K	80x30	8x16	640x480	31.5	60
11,72h	APA	2/256K	80x30	8x16	640x480	37.76	72
12	APA	16/256K	80x30	8x16	640x480	31.5	60
12,72h	APA	16/256K	80x30	8x16	640x480	37.76	72
13	APA	256/256K	40x25	8x8	320x200	31.5	70
21	A/N	16/256K	132x60	8x8	1056x480	30.5	60
22	A/N	16/256K	132x44	8x9	1056x396	30.5	70
23	A/N	16/256K	132x25	8x16	1056x400	30.5	70
24	A/N	16/256K	132x28	8x14	1056x392	30.5	70
25	APA	16/256K	80x60	8x8	640x480	31.5	60
25,72h	APA	16/256K	80x60	8x8	640x480	37.76	72
26	A/N	16/256K	80x60	9x8	720x480	31.50	60
29,35k	APA	16/256K	100x37	8x16	800x600	35.5	56
29,38k	APA	16/256K	100x37	8x16	800x600	38	60
29,48k	APA	16/256K	100x37	8x16	800x600	48.4	72.7
2A,35k	A/N	16/256K	100x40	8x15	800x600	35.5	56
2A,38k	A/N	16/256K	100x40	8x15	800x600	38	60
2A,48k	A/N	16/256K	100x40	8x15	800x600	48.4	72.7
2D	APA	256/256K	80x25	8x14	640x350	31.5	70
2E	APA	256/256K	80x30	8x16	640x480	31.5	60
2E,72h	APA	256/256K	80x30	8x16	640x480	37.76	72.7
2F	APA	256/256K	80x25	8x16	640x400	31.5	70
30,35k	APA	256/256K	100x37	8x16	800x600	35.5	56
30,38k	APA	256/256K	100x37	8x16	800x600	38	60
30,48k	APA	256/256K	100x37	8x16	800x600	48.4	72.7
37i	APA	16/256K	128x48	8x16	1024x768	35.5	87
37n	APA	16/256K	128x48	8x16	1024x768	49	60.5
37,72m	APA	16/256K	128x48	8x16	1024x768	56.48	70
38i	APA	256/256K	128x48	8x16	1024x768	35.5	87
38n	APA	256/256K	128x48	8x16	1024x768	49	60.5
38,72m	APA	256/256K	128x48	8x16	1024x768	56.48	70
3Di	APA	16/256K	160x64	8x16	1280x1024	48.1	87

Note:

A/N = Alphanumeric modes (text) text modes with 350 scan lines.

APA = All points addressable modes (graphics)

* Extended Graphics Adapter

+ 9x16 character cell enhanced text modes with 400 scan lines.

i = interlaced modes

n = non-interlaced modes

6.4.7 Using the Extended-Column Modes (VMODE)

SVGA-486 provides the capability to utilize extended column modes with text applications. This means that your computer, when interfaced with appropriate color displays, can produce 132 x 44, 132 x 28, 132 x 25, 100 x 40, and 80 x 60 modes in addition to the standard 80 x 25 and 40 x 25 modes. With the appropriate software, the 132-column display capability allows the emulation of terminals that require 132 columns of text.

You can switch back and forth between the 80-column display modes and the various extended-column display modes. To use VMODE, follow these steps:

1. First, be sure that the VMODE.COM utility is present on the disk you are using. This file is installed on PS/ValuePoint 486 sytems; it also comes with the SVGA 486 Drivers/Utilities diskette.
2. To switch to a different mode, type the mode you wish to use and then press the Enter key:

```
VMODE 25      - to switch to 132x25 mode
VMODE 28      - to switch to 132x28 mode
VMODE 44      - to switch to 132x44 mode
VMODE 40      - to switch to 40x25 mode
VMODE 60      - to switch to 80x60 mode*
VMODE 80      - to switch to 80x25 mode
VMODE 100     - to switch to 100x40 mode*
```

* Note: Not all modes are supported by all monitors. Attempting to use modes that your monitor does not support will produce unsatisfactory results.

Three additional modes are provided to enable you to change the scan line resolution. This is to accommodate some software that specifically looks for a particular number of scan lines. The 400 scan line mode provides the most pleasing text resolution.

```
VMODE 200 - to provide 200 scan lines in 40- or 80x25 text modes
VMODE 350 - to provide 350 scan lines in 40- or 80x25 text modes
VMODE 400 - to provide 400 scan lines in 40- or 80x25 text modes
```

6.4.8 VMODE Scan Rates

Additional modes are available to provide additional scan rates that may improve synchronization with a variety of monitors. Normally, the default scan rates are effective, but some monitors may require different scan rates for the most satisfactory display results. By setting these modes, frequencies are adjusted that affect displayed graphic modes.

The following modes are available via the VMODE command.

```
VMODE x
```

VMODE x Value	Modes affected	Vertical Refresh Rate	Horizontal Frequency	Resolution
35K	29,2A,30	56Hz	35KHz	800x600
38K	29,2A,30	60Hz	38KHz	800x600
48K	29,30	72.7Hz	48.4KHz	800x600
45M	37i,38i	86.5Hz	35.5KHz	1024x768 [1]
65M	37n,38n	60.5Hz	49KHz	1024x768 [2]

[1] interlaced
[2] non-interlaced

6.4.9 72 Hz Modes

The following graphic (not text) modes can be displayed after setting the vertical refresh rate to 72 Hz. The 72 Hz mode will provide a clearer display with less flicker on some monitors. Set the VMODE parameter to VMODE 72HZ. After this is done you can use VMODE to set the display to any of the graphic modes listed below.

VMODE x Value	Modes Affected	Vertical Refresh Rate	Horizontal Frequency	Resolution
72HZ	11	72.00Hz	37.76KHz	640x480*
72HZ	12	72.00Hz	37.76KHz	640x480*
72HZ	25	72.00Hz	37.76KHz	640x480*
72HZ	2E	72.00Hz	37.76KHz	640x480*

* monitor must be capable of 72.00Hz vertical and 37.76KHz horizontal frequency.

6.4.10 70 MHz Modes

The following graphic (not text) modes can be displayed after setting the video clock speed to 70 MHz. The 70MHz mode will provide a clearer display with less flicker on some monitors. Set the VMODE parameter to VMODE 70M. After this is done you can use VMODE to set the display to any of the graphic modes listed below.

VMODE x Value	Modes Affected	Vertical Refresh Rate	Horizontal Frequency	Resolution
72M	37	70.00Hz	56.48kHz	1024x768*
72M	38	70.80Hz	56.48kHz	1024x768*

* monitor must be capable of 70Hz vertical and 56.48KHz horizontal frequency.

Typing VMODE ? will display the full array of mode possibilities. Users that are familiar with the characteristics of their monitors will find these modes more useful. See Appendix A, "Video Comparison" on page 115 for definitions of available modes. Note that choosing VMODE 60HZ *will return the adapter to normal operation*.

Note: Choose modes/resolutions that are compatible with your video configuration and monitor capabilities.

6.4.11 Using the Compatibility Modes

Some programs are written to be run using specific modes or are written according to particular video standards. For example, there are programs that require a monochrome adapter or those that are written exclusively for a Color Graphics Adapter (CGA). When these programs are used, it is necessary to make your computer appear to be what the program requires. This is easily accomplished. In order to select a mode that will change the "appearance" of the video adapter to the software, you need only select the appropriate VMODE parameter. When another mode is needed or desired, you can simply select the mode using another VMODE parameter. In order to return to the default mode (VGA), type VMODE VGA or power down. The following is a list of modes and their uses.

```
VMODE CGA       -  Set adapter for compatibility with the Color Graphics Adapter
VMODE MDA       -  Set adapter for compatibility with the Monochrome Display Adapter
VMODE HERCULES  -  Set adapter for compatibility with the Hercules card
VMODE EGA       -  Set adapter for compatibility with the Enhanced Graphics Adapter
VMODE VGA       -  Set adapter for compatibility with the Video Graphics Array
```

A typical use might be using game software that requires CGA resolution. Using VMODE CGA will put the computer in CGA mode. (If the software needs to be started in order to work, you simply place the VGA in CGA-compatible mode with VMODE CGA, and restart with your game diskette in the A: drive.)

You may switch modes in this manner as often as you wish. VMODE ? will display a list of the available modes. Entering VMODE with no parameter will display a menu screen from which to choose a text mode.

6.4.12 SVGA-486 Graphic Modes

The following table shows the key resolutions available with the SVGA-486 subsystem when running graphics applications and device drivers that exploit display modes. It is followed by a table showing the IBM monitors at their highest refresh rates and resolutions supported by SVGA-486.

Table 13. SVGA-486 Resolutions Supported

Resolutions	Scan Frequency		I/NI	Max. Colors/Gray Shades	VESA
	Vertical (Hz)	Horizontal (KHz)			
640 x 480	60	31.5	NI	256 / 256	
	70	31.5	NI	256 / 256	
	72	37.76	NI	256 / 256	VS
800 x 600	56	35.5	NI	256 / 256	VG
	60	38	NI	256 / 256	VG
	72.7	48.4	NI	256 / 256	VS
1024 x 768	60.5	49	NI	256 / 256	VG
	70	56.48	NI	256 / 256	VS
	87	35.5	I	256 / 256	
1280 x 1024	87	48.1	I	16 / 16	

Note:

I = Interlaced

NI = Non-interlaced

VS = Video Electronic Standards Association (VESA) Standard

VG = VESA Guideline

Table 14. SVGA-486 Supported IBM Monitors (Including Refresh Rates)			
Monitor	**640 x 480**	**800 x 600**	**1024 x 768**
8503, 8512, 8513, 8518	60 Hz (NI)	N/A	N/A
8514, 8515, 8516	60 Hz (NI)	N/A	43.5 Hz (I)
6312	60, 70, 72 Hz (NI)	56, 60, 72 Hz (NI)	60 (NI), 87 Hz (I)
6314	60, 70, 72 Hz (NI)	56, 60, 72 Hz (NI)	60, 70 (NI), 87 Hz (I)
6319	60, 70, 72 Hz (NI)	56, 60, 72 Hz (NI)	60, 70 (NI), 87 Hz (I)
Note: Supported resolutions, like 1280 X 1024 are available for non-IBM (OEM) monitors provided the scanning frequencies match the SVGA-486 graphics controller. N/A = not available.			

6.4.13 SVGA-486 DOS 5.0 Device Drivers

The following is a brief listing of the DOS 5.0 compatible device drivers that are shipped with the SVGA-486 PS/ValuePoint subsystems. If you don't see the device driver you need listed here, or you have further questions refer to IBM Part Number 53G0165, *IBM PS/ValuePoint 486 SVGA Drivers/Utilities User's Guide* or call yout local IBM technical support representative.

- AutoCAD** ADI Driver
- GEM 3.1
- Lotus 1-2-3 Release 2, 2.01, 2.2
- Lotus Symphony 1.1
- Ventura Publisher 1.1 - 2.0; 800 x 600 and 1024 x 768
- IBM 8514/A Emulation Driver
- VESA Super VGA BIOS Extension
- WordPerfect 5.0 - 5.1 Drivers for High Resolution Modes
- WordPerfect 5x Drivers for 132-Column Text Modes
- WordStar 6.0 (a-d) High Resolution Drivers for Page Review
- WordStar 4.0 132-Column Text Modes Drivers
- Microsoft Windows 3.1

Chapter 7. Processor Complexes

7.1 Introduction

This chapter describes processor upgrades that were available for various PS/2 models at the time of publication. These options will change over time. A more detailed description of how the processor complex is structured can be found in *Personal System/2 Models 95 XP 486, 90 XP 486, 55 LS and P75 486 Fundamentals* (Form Number GG24-3616).

At the end of this chapter is a description of the upgrade options for the PS/ValuePoint range.

7.2 Background to PS/2 Processor Complexes

In the first PS/2 models that IBM produced, most components were integrated into the planar of the system. This severely limited upgrade options and upgrade flexibility. While one component was perhaps upgraded, for example the processor, the other components such as the I/O controller and the memory controller were not. This created combinations of fast and slow components, which created unbalanced systems. Unbalanced systems are not as efficient as balanced systems where every component's performance is matched against other components' performances.

On Model 90s and 95s, the input/output (I/O) controller, processor and memory controller have been grouped together on a separate card known as a processor complex. This card attaches to the planar through a proprietary interface. On smaller PS/2 models, such as the Models 56 and 57, provision has been made for the processor to be upgraded, and therefore some of the subsystems of the Models 56 and 57 already have support for future processors still to be announced.

7.3 Model 90 and 95 Processor Complexes

Three types of processor complexes have been developed for the PS/2 Model 90 and 95:

- Base 1
- Base 2
- Base 3

Base 1: The Base 1 complexes were the first processor complexes produced by IBM for the Model 90 and 95. They come with a Level 2 cache socket, and have a 24-bit Direct Memory Access (DMA) controller. The DMA controller typically operates at 10 to 12 MHz. There are no math coprocessor sockets, as the Intel 80486 DX or larger has a math coprocessor integrated into the processor itself. The following complexes have been announced:

- 20 MHz 486SX** "G", announced October 1990
- 25 MHz 486DX "J", announced October 1990

- 33 MHz 486DX "K", announced October 1990
- Upgrade Complex 486DX 50 MHz, announced June 1991
- Upgrade Complex 486DX2 66/33 MHz, announced August 1992

Base 2: The Base 2 complexes have no Level 2 cache socket, and the "H" model has a math coprocessor socket into which an 80487 math coprocessor or a 486 DX 50/25 MHz upgrade chip can be installed. The 24-bit Direct Memory Access (DMA) controller operates at 25 MHz, and is therefore balanced with the processor itself. Bus arbitration is faster than on Base 1 complexes, and there is also support for both interleaved (memory pairs) and non-interleaved (single memory chips) memory. The Base 2 complexes are:

- 25 MHz 486 SX** "H", announced October 1991
- 50/25 MHz 486 DX2 "L", announced April 1992

Base 3: Only one Base 3 complex is currently available:

- 50 MHz 486 DX "M", announced April 1992

There are a number of features of the Base 3 complexes. While they are present on the processor complex, they must be enabled by software.

1. **VPD** - Vital Product Data (VPD) support is included in the ROM of the processor complex. This allows software to obtain unique information about the processor complex, for example the serial number.
2. **Cache** - Memory Level 2 cache of 256 KB is standard on this complex.
3. **ECC** - The memory controller supports Error Checking and Correcting (ECC) memory. This will automatically correct single bit memory errors, which make up 98% of memory errors. All 2-bit errors and most 3 and 4-bit errors will be found by the same.
4. **Logs** - A logging facility is provided for ECC memory errors to be logged, as well as other system errors.
5. **Dual Path Memory** - There are buffers on both paths to memory. Dual Path memory is also known as Dual Bus Interleave. Base 1 complexes also support this feature, but do not have buffers. Base 2 complexes do not support Dual Path Memory. Packet Data Transfers are used by the I/O buffer for writes to memory. This means that 16 bytes are written to memory in one processor cycle. In unbuffered systems a write to memory is performed every 4 bytes.
6. **Subsystem Control Block (SCB)** - This feature allows for communication between bus masters and also between bus masters and the processor complex over the Micro Channel. Examples of SCB operations include command chaining, data chaining, block data moves, and status information. This capability allows the processor and other bus masters to continue with other tasks instead of waiting for a command to complete. This implies parallel processing, and hence this feature must be supported by software.
7. **Streaming Data Support** - The I/O controller allow for streaming data transfer at up to 40 MB per second. The two subsystems that communicate over the Micro Channel must both be able to support the same speed. If not, then communication takes place at the speed dictated by the slower of the two subsystems.

8. **Synchronous Channel Check** - This allows errors to be sent at the same time as the data is being transferred across the Micro Channel.
9. **Data Bus Parity** - Data Bus Parity allows for the verification of data transmission over the Micro Channel. This ensures that all data is transferred correctly across the channel. All of the components on the complex itself support this feature, and is also supported by various bus master adapters.

7.4 PS/2 Upgrade Options

The following processor upgrade paths were available at the time of publication.

7.4.1 PS/2 Model 56 and 57 386 SX Models

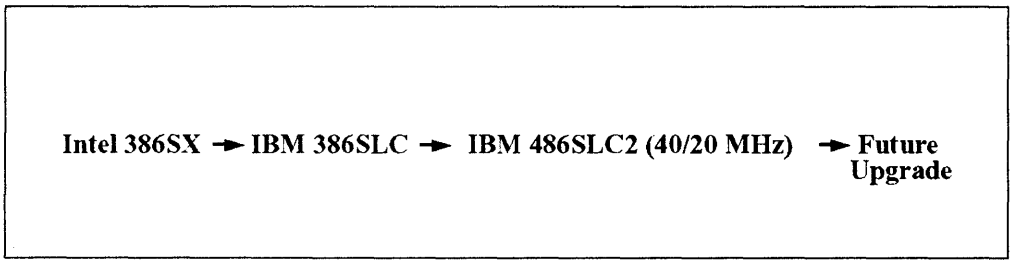

Figure 30. PS/2 Model 56 and 57 386 SX Upgrade Path

All Model 56s and 57s with an Intel 80386 SX can be upgraded to an 80386 SLC at 20 MHz or a 80486 SLC2 at 40/20 MHz. Both of these upgrade options plug into the coprocessor socket on the planar. They are in the form of a daughter card, and have their own coprocessor socket.

7.4.2 PS/2 Model 56 and 57 386 SLC Models

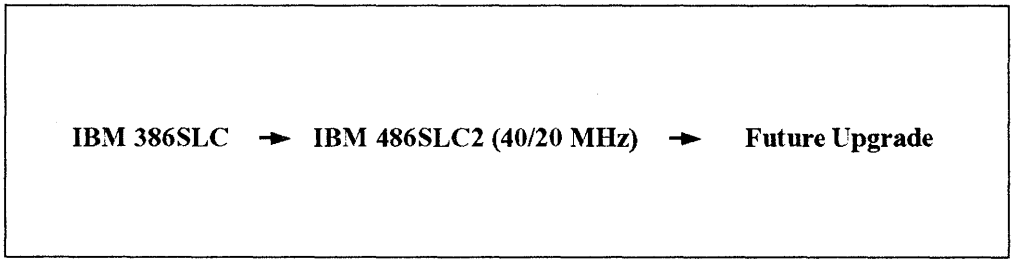

Figure 31. PS/2 Model 56 and 57 386 SLC Upgrade Path

All Model 56s and 57s with a 80386 SLC can be upgraded to an 80486 SLC2 at 40/20 MHz. The upgrade is in the form of a daughter card, and has its own coprocessor socket. The upgrade is plugged into the coprocessor socket on the planar.

7.4.3 PS/2 Model 56 and 57 486 SLC2 Models

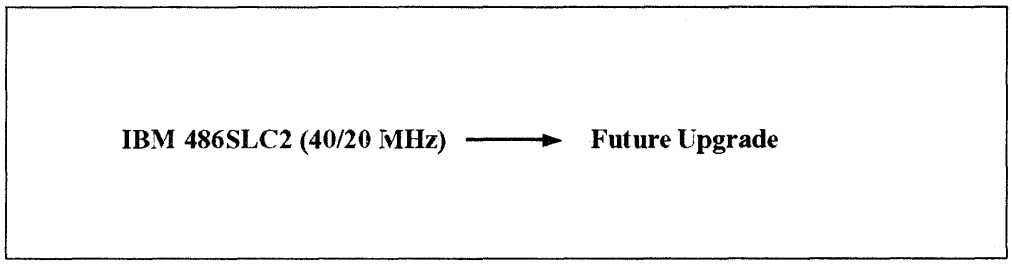

Figure 32. PS/2 Model 56 and 57 486 SLC2 Upgrade Path

IBM has issued a statement of direction (SOD) that a new processor will be provided for the Model 56 and Model 57.

7.4.4 PS/2 Model 70 386 Models

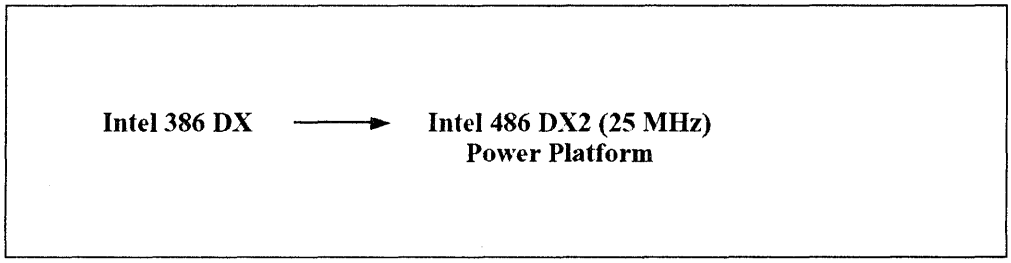

Figure 33. PS/2 Model 70 386 Upgrade Path

The PS/2 Model 70 386 can be upgraded by installing the PS/2 486/25 Power Platform. The 386 processor is removed and replaced by the Power Platform. In addition to that, two EPROM modules on the PS/2 70 motherboard need to be exchanged for the system to support the new processor.

7.4.5 PS/2 Model 76 and 77 486 SX Models

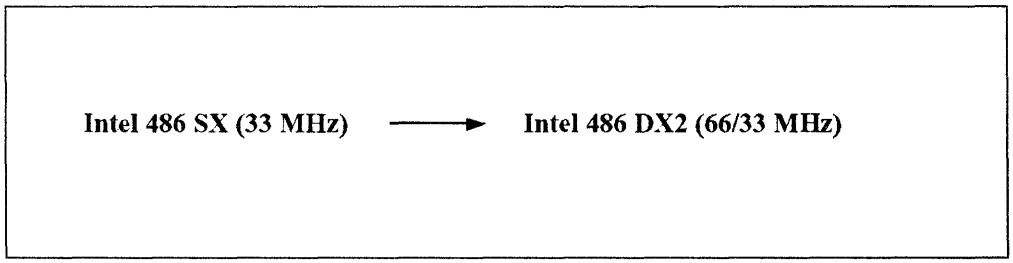

Figure 34. PS/2 Model 76 and 77 486 SX Upgrade Path

There is an open socket on the planar of the Model 76s and the Model 77s. This socket can be used to receive the 486 DX2 66/33 MHz upgrade option.

7.4.6 PS/2 Model 90 and 95

The following table shows the various upgrade paths available for the various processor complexes on the Models 90 and 95.

Table 15. PS/2 Model 90, 95 Processor Upgrade Paths

Old Processor Complex	New Processor Complex	New Base Level
486SX 20 MHz "G"	486SX 25 MHz "H"	Base 2
486SX 20 MHz "G"	486DX2 50/25 MHz "L"	Base 2
486SX 20 MHz "G"	486DX 50 MHz "M"	Base 3
486SX 20 MHz "G"	486DX2 66/33 MHz	Base 1
486SX 25 MHz "H"	486DX2 50/25 MHz (chip)	Base 2
486SX 25 MHz "H"	486DX 50 MHz "M"	Base 3
486SX 25 MHz "H"	486DX2 66/33 MHz	Base 1
486DX 25 MHz "J"	486DX2 50/25 MHz "L"	Base 2
486DX 25 MHz "J"	486DX 50 MHz "M"	Base 3
486DX 25 MHz "J"	486DX2 66/33 MHz	Base 1
486DX 33 MHz "K"	486DX2 50/25 MHz "L"	Base 2
486DX 33 MHz "K"	486DX 50 MHz "M"	Base 3
486DX 33 MHz "K"	486DX2 66/33 MHz	Base 1
486DX2 50/25 MHz "L"	486DX 50 MHz "M"	Base 3
486DX2 50/25 MHz "L"	486DX2 66/33 MHz	Base 1
486DX 50 MHz (Chip)	486DX 50 MHz "M"	Base 3
486DX2 66/33 MHz	486DX 50 MHz "M"	Base 3

All of the complexes mentioned have not necessarily been announced in all countries.

7.5 Processor Differences

The following table describes some of the key features of the various microprocessors that are found in IBM Personal Computer systems.

Table 16 (Page 1 of 2). Personal Computer Processor Features

Processor Name	Clock Rate MHz	Data Path Size	Internal Path Size	Address Path Size	Other
Intel 8086	8	16 Bit	16 Bit	20 Bit	
Intel 80286	8,10	16 Bit	16 Bit	24 Bit	
Intel 80386 SX	16,20	16 Bit	32 Bit	24 Bit	
Intel 80386 SL	25	16 Bit	32 Bit	24 Bit	PM
Intel 80386 DX	16,20,25	32 Bit	32 Bit	32 Bit	
IBM 80386 SLC	16,20,25	16 Bit	32 Bit	24[1] Bit	8 KB Cache, PM, OI
IBM 80486 SLC	25	16 Bit	32 Bit	24[1] Bit	16 KB Cache, PM, OI

Table 16 (Page 2 of 2). Personal Computer Processor Features

Processor Name	Clock Rate MHz	Data Path Size	Internal Path Size	Address Path Size	Other
IBM 80486 SLC2	40/20, 50/25	16 Bit	32 Bit	24[1] Bit	16 KB Cache, PM, OI
Intel 80486 SX	20,25,33	32 Bit	32 Bit	32 Bit	8 KB Cache,OI, BRI
Intel 80486 DX	25,33,50	32 Bit	32 Bit	32 Bit	Math, 8 KB Cache,OI,BRI
Intel 80486 DX2	50/25, 66/33	32 Bit	32 Bit	32 Bit	Math, 8 KB Cache,OI,BRI

Note:

[1] = 32 Bit Path between Cache and Processor

PM = Power Management Feature

OI = Optimized Instructions

BRI = Burst Read Instructions

Math = Math Coprocessor Included

7.6 PS/ValuePoint Upgrade Options

The PS/ValuePoint range does not have an equivalent level of processor integration to form a processor complex. Provision has been made, however, for the processor to be upgraded.

The following processor upgrade paths were available at the time of publication.

7.6.1 PS/ValuePoint Model 425 SX

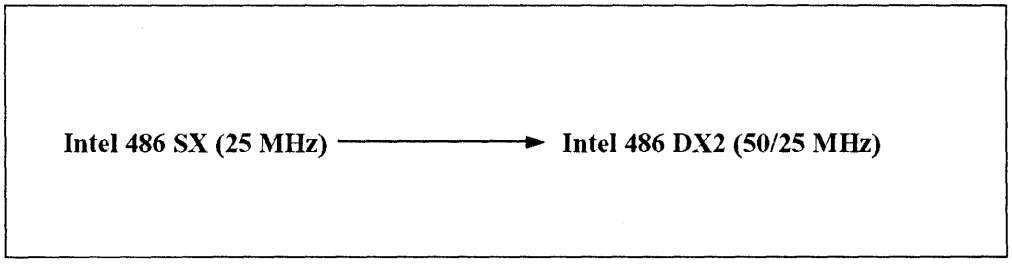

Figure 35. PS/ValuePoint Model 425 SX Upgrade Path

All Model 425 SXs with an Intel 80486 SX at 25 Mhz can be upgraded to an Intel 80486 DX2 at 50/25 MHz. This upgrade option plugs into the coprocessor socket on the planar.

7.6.2 PS/ValuePoint Model 433 DX

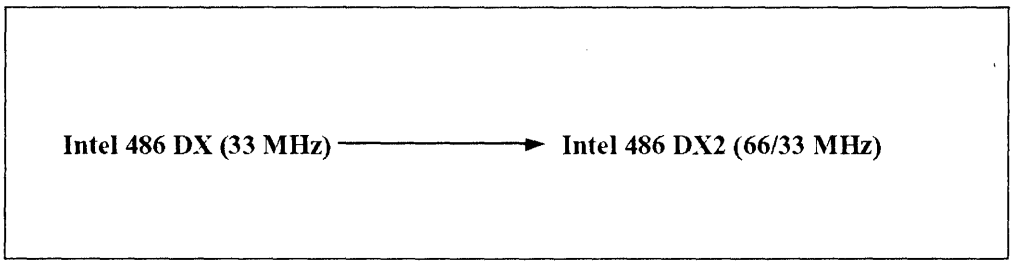

Figure 36. PS/ValuePoint Model 433 DX Upgrade Path

All Model 433 DXs with an Intel 80486 DX at 33 Mhz can be upgraded to an Intel 80486 DX2 at 66/33 MHz. This upgrade option replaces the existing processor chip.

Chapter 8. C2 Security

This section briefly discusses certain aspects of PS/2 security. Operating system-specific information is not included here, only features related to specific IBM PS/2 models have been included.

8.1 Introduction

The trend toward downsizing from large systems that are located in controlled access areas and staffed by authorized personnel, to personal computers that are located in unsecured areas with potential access by unauthorized users, has created security exposures and challenges for security management. In contrast to the medialess and non-programmable terminals used with larger systems, personal computers provide local media, local software, local memory, and - perhaps most important - local data. In a highly connected environment, personal computers also provide the opportunity for access to a major portion of the data processing assets of an organization.

8.2 Government Requirements and Legislation

United States Department of Defense (DoD) security requirements have been influential in defining security legislation and computer hardware and software implementations around the world. The source for these requirements is the *Department of Defense, Trusted Computer System Evaluation Criteria, DoD 5200.28 STD*, dated 12/85. The essence of the requirements is contained in the Assurance section, Requirement 6: a "trusted mechanism must be continuously protected against tampering and/or unauthorized changes...". The National Computer Security Center (NCSC) evaluates computer system security products with respect to the criteria defined by the U.S. Department of Defense.

There are seven computer system security product classifications in the DoD requirements: A1, B3, B2, B1, C2, C1, and D. The requirements for these classifications fall into four basic groups: security policy, accountability, assurance, and documentation. Several criteria, which vary by security classification, are specified in each of these groups. Currently, A1 is the highest classification, followed by B3, B2, and so on. The C2 classification satisfies most security requirements for personal computing environments.

The importance of the C2 security criteria extends far beyond that of the U.S. Department of Defense requirements. The issue of individual privacy and confidential personal information is very much a part of contemporary computer security requirements. A great deal of legislation in effect or pending is either directly or indirectly linked to the DoD requirements. For example, the criteria have been applied to other federal agencies and to prime contractors handling confidential information. The Computer Security Act of 1987 requires C2 security compliance for this type of information in the United States.

Many European countries have requirements similar to those of the U.S. Department of Defense. In the United Kingdom, the 1984 Data Protection Act places responsibility for compliance with its terms on those who control the contents and use of personal data files. One of the principles of this act is that "appropriate security measures shall be taken against unauthorized access to, or alteration, disclosure or destruction of, personal data and against accidental

loss or destruction of personal data." The single European market is also driving a piece of legislation designed to standardize the data protection laws of Europe.

IBM has interpreted the DoD requirements for C2 security for personal computers based on experience in dealing with government agencies requiring certification. However, the design and implementation of features that meet the C2 evaluation level for security and integrity is, primarily, a software (operating system) issue. However, to maintain a C2 system environment, the user must also provide methods of ensuring that the software cannot be modified or removed. The user can accomplish this by enclosing the computer in isolation rooms with controlled access; using monitoring devices to ensure that system modification is not possible; or employing detection methods to ensure that unauthorized media are not used. These techniques require a great deal of user effort and expense to ensure system integrity, and may impose limitations on how and where personal computers are used.

To help reduce effort and expense for secured workstations, IBM has determined that PS/2 hardware, microcode, and system software can be designed with features that enable a low-cost, convenient system integrity and security solution, and provide a secure platform for any evaluated operating system at all evaluation levels. However, in order to obtain actual security certification by the U.S. Department of Defense, the specific hardware and software configuration must be submitted to the NCSC for testing. The process takes from 12 to 18 months. Notwithstanding the importance of certification, the features of the secured PS/2 systems are independent of the operating system, and they provide a great deal of data and resource protection even if a non-secured operating system is used.

The actual hardware and software configurations are a subset of the total requirements for security certification by the DoD. The total environment and procedures are essential elements of achieving and maintaining computer security and DoD certification. The system security and basic hardware integrity features provide the foundation of a total security program for personal computers.

8.3 Secured PS/2 Models

There are currently three PS/2 systems that have enhanced hardware integrity features. These new models are:

- PS/2 Model 56 486SLC2 (9556)
- PS/2 Model 57 486SLC2 (9557)
- Ultimedia* Model 57 486SLC2 (9557)

The following section discusses some of the security features in the new PS/2 models.

8.3.1 Tie-Down Capability

There are two small holes in the back of the computer that can be used to secure the system to a permanent fixture. A U-bolt can be installed in the holes and a cable or chain can be attached to prevent physical removal or theft.

8.3.2 Tamper Evident Cover

These systems have a keylock for their covers and internal I/O devices. In the locked position, it mechanically prevents the covers from being removed. The key has been changed to a type that can be duplicated only by the manufacturer.

If the covers are forced open, an electro-mechanical switch and perimeter sensor detect the intrusion. If the computer was on during the break-in attempt, it will cease working.

The next time the computer is started, the power-on self test (POST) routine displays a message informing the user of the intrusion, and requires that the automatic configuration program be run before the computer can be used. This is done to flag any configuration changes that may have occurred due to the intrusion - for example, removal of a disk drive. In addition, the system cannot be used without the power-on and security passwords (if they have been set). There is a provision for maintenance that allows the system to be used without the covers in place; however, to use this feature, the key must have been used to remove the covers.

Other systems may have lockable covers. However, it is not that difficult to pry the system unit cover off, disable or unplug the key mechanism, and get inside the system. The tamper evident mechanism is an important feature to flag the intrusion and to prevent operation of the system after a forced entry. This PS/2 detection feature is very valuable for detecting the person most likely to break into the secured workstation - the user. Once the machine has been disabled, the system owner or administrator must be contacted to reset the system.

8.3.3 Secure Access Openings

The basic design of the keylock, cover interlock switch, diskette media lock, and other openings of the new systems prevents this type of intrusion.

In the original PC AT systems the cover lock also locked the keyboard. If the cover lock was deactivated, the keyboard was enabled. One could still insert a tool through the air vent in the front of the AT and deactivate the keylock, thereby gaining access to the system. Even for those systems with keyboard passwords and power-on passwords, if the battery was accessible, it is possible to disable the password protection.

The privileged-access password in the new PS/2 systems is not linked to the battery, and is not disabled even if the battery is disabled, providing an additional measure of protection.

8.3.4 Secure I/O Cables

The rear-panel security option available for the new systems is an enclosure that is secured to the back of the computer by the cover lock. Its function is to prevent the cables from being removed and other cables from being attached. This effectively secures the serial, parallel, and SCSI cables, as well as other ports and cables provided by adapters, because it prevents someone from attaching a device through these connectors and gaining access to the data in the system.

The cable cover also has a tamper evident feature. If the cover is forced open, the system will not operate until the privileged-access password is entered.

The IBM PS/2 Cable Cover 2 option #2863, 32G2430 is provided for the IBM PS/2 Model 56 486SLC2. The IBM PS/2 Cable Cover 3 option #2864, 32G2431 is provided for the PS/2 Model 57 486SLC2 and the PS/2 Ultimedia Model 57 486SLC2.

8.3.5 Privileged-Access Password

All PS/2 systems provide power-on password and keyboard password protection. The power-on password must be entered correctly each time the system is turned on. After three incorrect attempts, the system must be turned off and back on in order to try again. The keyboard password is used to lock the keyboard without turning the computer off. It also prevents rebooting the system by pressing the Ctrl + Alt + Del keys. PS/2 systems also provide what is called an unattended server mode or a network server mode. This mode allows other computers to access a fixed disk drive on a server even though the keyboard is locked. This is useful when there is a power failure for example, the machine recovers but still has a locked keyboard.

Because the power-on and keyboard passwords can be defeated by deactivating the battery inside the system, another level of password protection has been provided in the new system. This security feature is called the privileged-access password. It provides a much higher level of security when used with an operating system that controls access through the use of passwords. Systems are shipped with the privileged-access password disabled. To set this password, a jumper on the system board must be moved in order to put the system in the change state. Once this password is set, it cannot be overridden or removed by an unauthorized person.

Warning - Forgotten Password

If the administrator misplaces or forgets the privileged-access password, the system board will have to be replaced. There is no way to reset a forgotten privileged-access password.

The privileged-access password restricts access to system programs, prevents the IPL source and sequence from being changed, and effectively deters unauthorized modifications to the hardware. After a forced entry is detected by the tamper evident cover switch, the privileged-access password (if it has been set) must be used also in order to make the system operate.

The privileged-access password is stored in a special type of read-only memory called flash EEPROM. EEPROM is an acronym for electrically erasable programmable read-only memory.

8.3.6 System Identification

The new systems provide a wealth of information that is stored in read-only memory. The system board serial number, the model and submodel byte data, the system serial number, the system board part number, the replaceable unit part number, and the manufacturing location are included in the software-readable information. This collection of data about the system is called the Vital Product Data (VPD). The VPD information is accessible using the utility called the System Information Tool, which is part of the OS/2 version that comes preinstalled on the new PS/2 systems. In addition to preventing substitution of an unauthorized system and aiding in matching a system with its authorized

user, VPD capability is extremely beneficial in inventory and asset management. The System Information Tool provides detailed adapter, memory, and disk configuration data for these Micro Channel systems. VPD is used extensively by the IBM LANfocus range of products.

8.3.7 Secure Removable Media

A new, optional 2.88 MB diskette drive with security features is available for the new systems. The new diskette drive is a 3.5-inch, one-inch high drive with media sense capability for the standard diskette capacities of 720 KB, 1.44 MB, and 2.88 MB. It can read and write data up to a formatted capacity of 2.88 MB, while maintaining read and write capability with 720 KB and 1.44 MB diskette drives. A new control signal has been added to the diskette interface that supports LOCK, UNLOCK, and EJECT commands issued by the operating system. If the privileged-access password is not set, the diskette is unlocked during POST. If the password is set, the boot process does not unlock the diskette drive unless it is the designated IPL source. In this case, the LOCK and UNLOCK state is controlled by an operating system utility. For SCSI devices, there is a proposed standard UNLOCK command. In this case, the operating system will control the LOCK command if the privileged-access password is set. Access to the unlocking function with specific user authorization will be controlled by future secured system software.

In the event of power loss, the system retains its state (secured or unsecured) independent of the state of the battery. A diskette can be inserted in the drive, but it cannot be removed if the power is off. When the drive is turned on and locked, the media cannot be inserted or removed.

8.3.8 Secure IPL Source

These new systems allow the system owner or administrator to select the IPL source and sequence. The IPL sequence is stored in a region of the system's EEPROM, and can only be read, but not written, without the privileged-access password. The setup routine ensures that at least one IPL source is specified if the privileged-access password is used. This allows the system owner to control the IPL source, but prevents the user from modifying the source and sequence. For example, the diskette drive can be excluded as an IPL source. This feature helps to ensure that the system owner's specified operating system is loaded.

Earlier PS/2 models with IML (Initial Microcode Load), in which part of the system's microcode is loaded on the disk drive, provided the capability of selecting the IPL source. However, the information was stored in CMOS, which could be disabled by removal of the battery. Storage of the IPL sequence in the EEPROM protects it from being deactivated by removing the battery.

8.3.9 Interface to Security Adapter

The Micro Channel bus in PS/2 systems provide an excellent interface for cryptographic and other security adapters. Some of these adapters are bus masters with on-board processing capabilities. In addition, the data integrity features and high-data transfer rates supported by Micro Channel architecture are important for these applications. The PS/2 Model 56 486SLC2 provides three Micro Channel slots; the PS/2 Model 57 486SLC2 and Ultimedia M57 486SLC2 provide five Micro Channel slots.

IBM currently ships a family of workstation security products called the Transaction Security System. The family of products consists of:

- IBM 4755 Cryptographic Adapter
- IBM 4754 Security Interface Unit
- IBM Personal Security* Card

Several new models of the IBM 4755 Cryptographic Adapter have recently been announced, including enhanced versions for PS/2 systems. These adapters have a much higher performance rate, and they will support a larger number of cryptographic standards, including the Data Encryption Standard (DES) and the Rivest, Shamir and Adleman cipher (RSA).

Warning - Export Regulations

The use of these products is restricted by legislation in the United States. Users can confirm which restrictions are applicable by contacting their IBM representative.

8.3.10 Ability to Disable ROM BASIC

A ROM version of BASIC is not provided for system boot. A full BASIC program is available as a separate software product.

8.3.11 Diagnostic Tests

These are an integral part of the system board diagnostics. The functionality of the security features is assured during the POST routine.

8.3.12 Protection Against Securing Unsecured Systems

A switch under the lockable covers enables the privileged-access password to be written. With the covers locked and the switch in the locked state, an unauthorized person cannot set it.

8.3.13 Disk and Memory Erasing

The erasable disk capability is a feature implemented in the Secured Workstation Manager. In addition, in the new secured systems, the system memory is cleared after the system is powered on and before the operating system is given control.

8.3.14 Lockable I/O Ports

The rear-panel security option provides an "all or none" type of access to I/O ports. In addition to this support, future software will provide I/O port management based on the current signed-on user's authorization.

8.3.15 Security Features User's Guide

The new systems come with publications that describe the security features and their use. These descriptions are included in the *Personal System/2 User's Guide* for the new systems, and in the *Personal System/2 Micro Channel Computer Reference*.

Chapter 9. Standards

9.1 Background

Ergonomics is a term describing the relationship between people and machines. Workstation ergonomics is the science of fitting the workstation to the user.

There is considerable interest in workstation ergonomics for two reasons:

1. Organizations can achieve a high degree of user comfort, and user productivity, with the proper application of good ergonomic principles.
2. Europe is placing a significant emphasis on the legislative aspects of ergonomics as it applies to workstation displays (sometimes referred to as VDTs, Video Display Terminals).

9.2 Ergonomic Factors

For any given workstation environment, there are numerous ergonomic factors which influence overall user comfort, acceptance, and productivity. Examples include:

- The ambient lighting level of the office
- The audio noise level
- Office temperature and humidity
- The height of the display relative to the eyes of the user.

As far as the display itself is concerned, a number of factors can affect the users comfort. Examples include:

- The brightness and contrast ratio of the display
- The absence of reflections on the work surfaces
- The readability of the characters (fonts) being displayed
- Image stability on the display, including the absence of display flicker

All of these factors must be considered for an optimum system solution.

9.3 ISO and the European Community

In May of 1990, the European Community (formerly the European Economic Community) released Council Directive 90/270/EEC on the "minimum safety and health requirements for work with display screen equipment". The directive requires each of the 12 member countries to enact legislation by year end 1992 which sets appropriate standards for new workstation displays. The directive also requires employers to ensure an adequate work environment beyond the workstation itself.

The wording of the directive is very general, which has caused the countries to search for an accepted standard upon which to base their legislation. A consensus is developing among the European countries to use the requirements being developed by existing and widely accepted standards organizations such

as the ISO (International Organization for Standardization) as the basis for their legislation. Independent of the European Community directive, the ISO standard represents an international consensus by 72 nations for workstation ergonomics.

The ISO Standard most often invoked is ISO 9241. Since ISO 9241 does not address electronic emissions from VDTs, a similar consensus is developing to use a Swedish specification (MPR-II) as the basis for this portion of the legislation. IBM is actively participating in establishing and implementing these standards throughout the world.

ISO 9241 and ISO 9000

ISO 9241 is completely unrelated to ISO 9000 and specifies standards for workstation ergonomics. ISO 9000 relates to *quality systems* and is only awarded after a business has had its management process audited.

9.3.1 The Workplace and ISO 9241

The following figure shows the various components of the ISO 9241 standard.

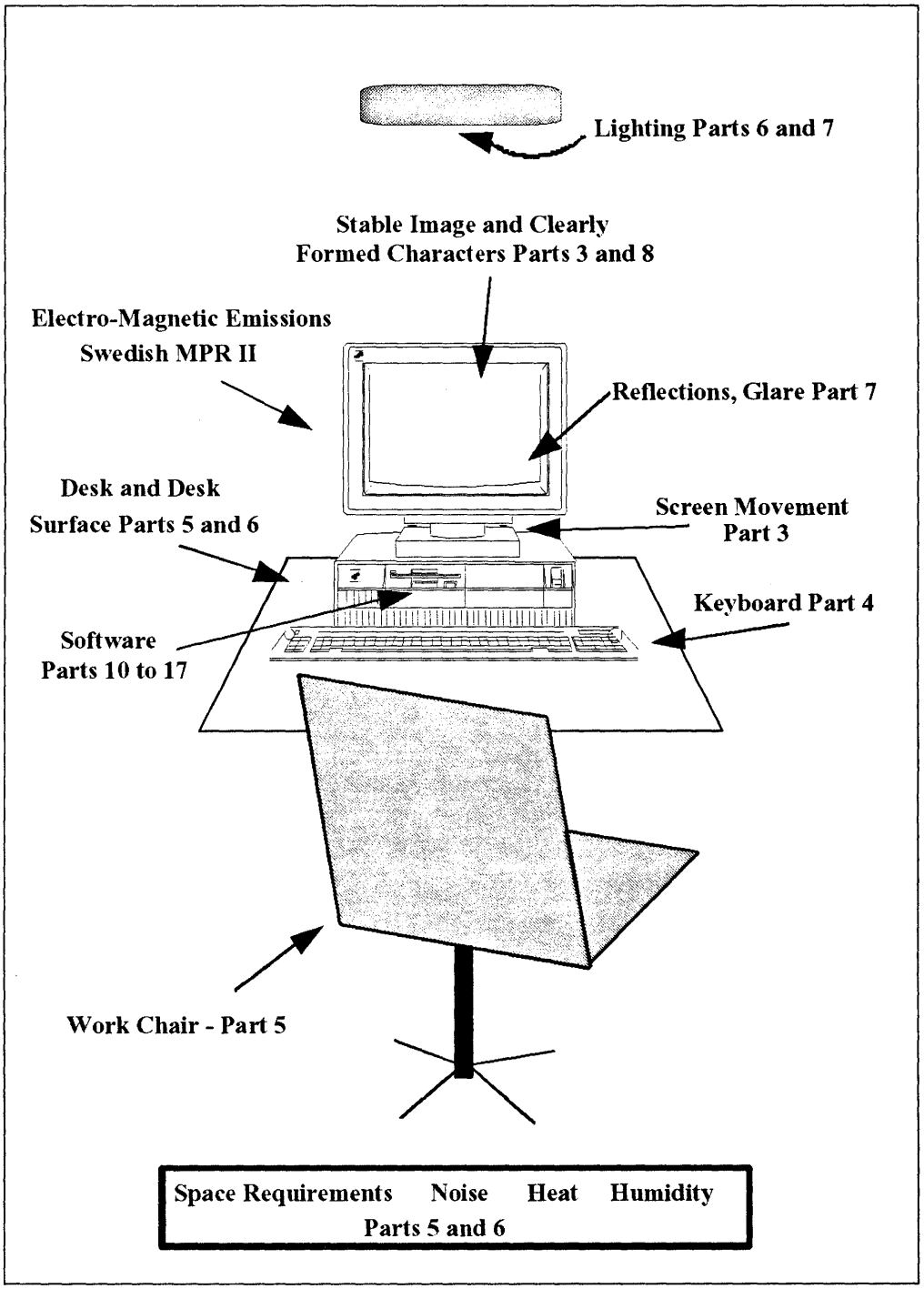

Figure 37. The Workplace and ISO 9241

9.4 ISO Capable versus ISO Compliant

In order to satisfy the requirements of ISO 9241, a complete system must be tested and must comply with all applicable elements of ISO 9241. This system includes, for example, a display which has sufficiently high contrast, a graphics adapter which drives the display at a fast enough rate to avoid flicker, and a CPU which generates satisfactory fonts.

Individual components of the system can be identified as being "ISO capable". ISO capable means that a product will provide performance which meets its portion of the ISO requirements, when used with other compatible "ISO-capable" components, as part of a total system. When all contributing system components satisfy their portion of the requirements, as verified by the required total system testing, an "ISO-compliant" system is then created.

During the project planning phase, it is important to ensure that all components to be purchased are ISO capable. This would be necessary to satisfy the legal requirements of certain countries. A broad approach to this problem is important, as the purchase of just one small non-compliant component will cause the entire installation to fail ISO compliance testing.

9.5 Video Electronics Standards Association

The Video Electronics Standards Association (VESA) is a non-profit organization based in California, United States. It has as its members various organizations in the electronics industry, and facilitates and promotes improved graphics standards. The organization was founded in 1989 to eliminate the confusion surrounding the "Super VGA" modes.

VESA is attempting to achieve compatibility between software and the various Super VGA modes. It is also attempting to achieve compatibility between various display adapters and display monitors.

9.5.1 Committees

Some of the VESA committees include:

- Super VGA
- Monitor
- XGA
- Multimedia
- Local Bus

9.5.2 Monitor Committee

The monitor committee has established certain standards and guidelines. Please refer to Table 7 on page 57 for information on how IBM has implemented these standards and guidelines.

Standards

- 640 x 480 at 72 Hz
- 800 x 600 at 72 Hz
- 1024 x 768 at 70 Hz

Guidelines

- 800 x 600 at 56 Hz
- 800 x 600 at 60 Hz
- 1024 x 768 at 60 Hz

Appendix A. Video Comparison

A.1 PS/2 XGA-2 versus PS/ValuePoint SVGA

Table 17. Video Comparison PS/2 XGA-2 versus PS/ValuePoint SVGA

Feature	IBM PS/2 XGA-2	IBM Value Point SVGA
(1) Hardware Features		
Refresh rate (Hz)	70-75.8	70-72
Std/Max. VRAM	1 MB	1 MB (DRAM)
Hardware Assist	Yes	No (no Coprocessor)
(2) Resolution/Colors		
640x480	Yes. 64 K colors	Yes, 256 colors
800x600	Yes, 64 K colors (60Hz)	Yes, 256 colors
800x600	Yes, 256 K colors (70-75Hz)	
1024x768	Yes, 256 colors	Yes, 256 colors
1280x1024	Yes, 16 colors	Yes, 16 colors (Unsupported)
(3) Non-Interlaced (NI)		
Maximum Resolution	1024 x 768	1024 x 768
(4) Interlaced (I)		
Maximum Resolution	1360 x 1024	1280 x 1024 (Unsupported)
(5) Driver Support		
Operating Systems	OS/2,DOS,Windows	OS/2,DOS,Windows
640x480	Yes, 64 K colors	Yes, 256 colors
800x600	Yes, 64 K colors	Yes, 256 colors
1024x768	Yes, 256 colors	Yes, 256 colors
(6) General		
Photo Image (> 32K Colors)	Yes	No
132 Column Support	Yes	Yes
ISO Capable	Yes	Yes
Multiple Monitor Frequency	Yes	Yes

Appendix B. Feature Comparisons

This appendix compares the various features as found in some IBM PS/2 and PS/ValuePoint computers. Please note that the various models mentioned may not necessarily be available for sale in every country, or may have been sold with different features. Older PS/2 Models are shown for reference purposes only.

All PS/ValuePoint models listed have Industry Standard Architecture (ISA), and all PS/2 models listed have Micro Channel Architecture (MCA).

B.1 PS/ValuePoint Disk and Diskette Options

The following table compares the various disk and diskette features of the PS/ValuePoint range.

Table 18. PS/ValuePoint Disk and Diskette Options

Name	Model No.	Hard File			Diskette Drives 1.44 MB	Internal Bays
		Standard MB	Maximum MB	Type		
325 T	6384-C00	0	424	IDE	1	5
325 T	6384-C20	80	424	IDE	1	5
325 T	6384-C40	170	424	IDE	1	5
425 SX	6384-F00	0	424	IDE	1	5
425 SX	6384-F20	80	424	IDE	1	5
425 SX	6384-F40	170	424	IDE	1	5
433 DX	6384-M00	0	424	IDE	1	5
433 DX	6384-M20	120	424	IDE	1	5
433 DX	6384-M40	212	424	IDE	1	5
466 DX2	6384-W52	212	424	IDE	1	5

B.2 PS/2 Disk and Diskette Options

The following table compares the various disk and diskette features of the PS/2 range.

Table 19. PS/2 Disk and Diskette Options

Name	Model No.	Hard File			Diskette Drives 2.88 MB	Internal Bays
		Standard MB	Max. MB	Type		
56 SX	8556-043	40	40	SCSI[1]	1	2
56 SX	8556-045	80	80	SCSI[1]	1	2
56 LS	8556-14X	0	400	SCSI[1]	0	2
56 LS	8556-24X	0	400	SCSI[1]	0	2
56 SLC	8556-055	80	80	SCSI[1]	1	2
56 SLC	8556-059	160	160	SCSI[1]	1	2
56 SLC LS	8556-15X	0	400	SCSI[1]	0	2
56 SLC LS	8556-25X	0	400	SCSI[1]	0	2
56 SLC2	9556-0B6	104	800	SCSI[1]	1	3
56 SLC2	9556-0BA	212	800	SCSI[1]	1	3
57 SLC	8557-055	80	1.2G	SCSI[1]	1	4
57 SLC	8557-059	160	1.2G	SCSI[1]	1	4
57 SLC	8557-05F	400	1.2G	SCSI[1]	1	4
57 SLC2	9557-0B6	104	1.2G	SCSI[1]	1	4
57 SLC2	9557-0BA	212	1.2G	SCSI[1]	1	4
76	9576-0U6	104	800	SCSI[1]	1	3
76	9576-0UA	212	800	SCSI[1]	1	3
77	9577-0UA	212	1.2G	SCSI[1]	1	4
77	9577-0UF	400	1.2G	SCSI[1]	1	4
77 DX2	9577-0NA	212	1.2G	SCSI[1]	1	4
77 DX2	9577-0NF	400	1.2G	SCSI[1]	1	4
90 XP	8590-0H5	80	1.2G	SCSI[2]	1[3]	4
90 XP	8590-0H9	160	1.2G	SCSI[2]	1[3]	4
90 XP	8590-0L9	160	1.2G	SCSI[2]	1	4
90 XP	8590-0LF	400	1.2G	SCSI[2]	1	4
95 XP	8595-0H9	160	3.2G	SCSI[2]	1[3]	7
95 XP	8595-0HF	400	3.2G	SCSI[2]	1[3]	7
95 XP	9595-0LF	400	3.2G	SCSI[2]	1	7
95 XP	9595-0MF	400	3.2G	SCSI[2]	1	7
95 XP	9595-0MT	1G	3.2G	SCSI[2]	1	7

Note:

[1] = 16 Bit Planar SCSI Subsystem

[2] = 32 Bit Adapter SCSI Subsystem

[3] = Diskette Drive is 1.44 MB 3.5-inch

B.3 PS/ValuePoint Planar Options

The following table compares the various options that can be installed onto the planar for the PS/ValuePoint range.

Table 20. PS/ValuePoint Planar Options

Name	Model No.	Planar Memory			Expansion Slots	
		Standard MB	Maximum MB	Speed ns	16 Bit	32 Bit
325 T	6384-C00	2	16	80	5	0
325 T	6384-C20	2	16	80	5	0
325 T	6384-C40	2	16	80	5	0
425 SX	6384-F00	4	32	80	5	0
425 SX	6384-F20	8	32	80	5	0
425 SX	6384-F40	8	32	80	5	0
433 DX	6384-M00	4	32	80	5	0
433 DX	6384-M20	8	32	80	5	0
433 DX	6384-M40	8	32	80	5	0
466 DX2	6384-W52	8	32	80	5	0

B.4 PS/2 Planar Options

The following table compares the various options that can be installed onto the planar for the PS/2 range.

Table 21. PS/2 Planar Options

Name	Model No.	Planar Memory			Expansion Slots	
		Standard MB	Max MB	Speed ns	16 Bit	32 Bit
56 SX	8556-043	4	16	70	2	0
56 SX	8556-045	4	16	70	2	0
56 LS	8556-14X	4	16	70	2	0
56 LS	8556-24X	4	16	70	2	0
56 SLC	8556-055	4	16	70	2	0
56 SLC	8556-059	8	16	70	2	0
56 SLC LS	8556-15X	4	16	70	2	0
56 SLC LS	8556-25X	4	16	70	2	0
56 SLC2	9556-0B6	8	16	70	3	0
56 SLC2	9556-0BA	8	16	70	3	0
57 SLC	8557-055	4	16	70	5	0
57 SLC	8557-059	8	16	70	5	0
57 SLC	8557-05F	8	16	70	5	0
57 SLC2	9557-0B6	8	16	70	5	0
57 SLC2	9557-0BA	8	16	70	5	0
76	9576-0U6	8	32	70	0	2
76	9576-0UA	8	32	70	0	2
77	9577-0UA	8	32	70	0	4
77	9577-0UF	8	32	70	0	4
77 DX2	9577-0NA	8	32	70	0	4
77 DX2	9577-0NF	8	32	70	0	4
90 XP	8590-0H5	8	64	70	0	3
90 XP	8590-0H9	8	64	70	0	3
90 XP	8590-0L9	8	64	70	0	3
90 XP	8590-0LF	8	64	70	0	3
95 XP	8595-0H9	8	64	70	0	6
95 XP	8595-0HF	8	64	70	0	6
95 XP	9595-0LF	8	64	70	0	6
95 XP	9595-0MF	16[1]	64	70	0	6
95 XP	9595-0MT	16[1]	64	70	0	6

Note:

[1] = Error Checking and Correcting Memory

B.5 PS/ValuePoint Available Ports

The following table shows some of the available ports for connection of external devices for the PS/ValuePoint range.

Table 22. PS/ValuePoint Available Ports

Name	Model No.	Serial Ports	Parallel Ports	Display Type	Keyboard and Mouse Ports
325 T	6384-C00	1	1	SVGA[1]	1
325 T	6384-C20	1	1	SVGA[1]	1
325 T	6384-C40	1	1	SVGA[1]	1
425 SX	6384-F00	2	1	SVGA[2]	1
425 SX	6384-F20	2	1	SVGA[2]	1
425 SX	6384-F40	2	1	SVGA[2]	1
433 DX	6384-M00	2	1	SVGA[2]	1
433 DX	6384-M20	2	1	SVGA[2]	1
433 DX	6384-M40	2	1	SVGA[2]	1
466 DX2	6384-W52	2	1	SVGA[2]	1

Note:

[1] = Cirrus Chipset

[2] = TSENG Chipset.

B.6 PS/2 Available Ports

The following table shows some of the available ports for connection of external devices for the PS/2 range.

Table 23. PS/2 Available Ports

Name	Model No.	Serial Ports	Parallel Ports	Display Type	Network Type
56 SX	8556-043	1	1	VGA	-
56 SX	8556-045	1	1	VGA	-
56 LS	8556-14X	1	1	VGA	Ethernet
56 LS	8556-24X	1	1	VGA	Token Ring
56 SLC	8556-055	1	1	VGA	-
56 SLC	8556-059	1	1	VGA	-
56 SLC LS	8556-15X	1	1	VGA	Ethernet
56 SLC LS	8556-25X	1	1	VGA	Token Ring
56 SLC2	9556-0B6	2	1	XGA-2	-
56 SLC2	9556-0BA	2	1	XGA-2	-
57 SLC	8557-055	1	1	VGA	-
57 SLC	8557-059	1	1	VGA	-
57 SLC	8557-05F	1	1	VGA	-
57 SLC2	9557-0B6	2	1	XGA-2	-
57 SLC2	9557-0BA	2	1	XGA-2	-
76	9576-0U6	2	1	XGA-2	-
76	9576-0UA	2	1	XGA-2	-
77	9577-0UA	2	1	XGA-2	-
77	9577-0UF	2	1	XGA-2	-
77 DX2	9577-0NA	2	1	XGA-2	-
77 DX2	9577-0NF	2	1	XGA-2	-
90 XP	8590-0H5	2	1	XGA-1	-
90 XP	8590-0H9	2	1	XGA-1	-
90 XP	8590-0L9	2	1	XGA-1	-
90 XP	8590-0LF	2	1	XGA-1	-
95 XP	8595-0H9	1	1	XGA-1	-
95 XP	8595-0HF	1	1	XGA-1	-
95 XP	9595-0LF	1	1	XGA-2	-
95 XP	9595-0MF	1	1	XGA-2	-
95 XP	9595-0MT	1	1	XGA-2	-

Note:

All parallel and serial ports are DMA capable.

All models have one keyboard and one mouse port.

Appendix C. POST Error Codes

Most power-on self test (POST) error codes are common to all IBM PS/2s. Some are unique to a specific model of PS/2, for example error number 0086 8200 below, which is unique to machines that implement C2 security standards.

The following table is for reference purposes only, and is unique to the PS/2 model 9556, 9557, 9576, and 9577. However, the majority of the codes listed will be common to most PS/2s.

For a complete listing of POST error codes for a specific PS/2 model, always refer to the documentation for that model.

C.1 Error Code Format

POST returns a message in the form of a multiple-character code to indicate the type of test that failed. Two formats are used for these error messages:

- A 12-character code for all errors that *are* related to SCSI devices:
  - The first four characters identify the device type.
  - The next eight characters identify specifics of the error.

  Please refer to Appendix D, "IBM SCSI POST Error Codes" on page 127 for a complete listing of SCSI POST error codes.
- An 8-character error code for all errors that *are not* related to SCSI devices.

Note: The POST error messages on the following pages are all listed as 8-digit messages. In some cases your messages might appear as 3-, 4-, or 5-digit messages. When this occurs, add two zeros to the last digit and one, two, or three leading zeros before the first digit. This will allow you to look up the error message as an 8-digit number.

Examples

- The following example shows a 5-digit error message that can appear on your screen. When this occurs, add two zeros to the last digit and one leading zero to make it an 8-digit message.

  0 **1 6 6 8 0** 0 0

- The following example shows a 4-digit error message that can appear on your screen. When this occurs, add two zeros to the last digit and two leading zeros to make it an 8-digit message.

  0 0 **1 7 0 1** 0 0

- The following example shows a 3-digit error message that can appear on your screen. When this occurs, add two zeros to the last digit and three leading zeros to make it an 8-digit message.

  0 0 0 **3 0 1** 0 0

Password Prompt

If a privileged-access password prompt (o—╖) appears with a POST message, type the password; then press **Enter** to use the system programs.

C.2 Error Codes Listing

The 8-character error code consists of two 4-character elements: the major error code and the minor error code. The following table lists the failure and the associated error code.

Table 24 (Page 1 of 3). PS/2 POST Error Codes

Major Code	Minor Code	Description
0001		System bus error - system board
	0100	Unexpected interrupt
	0200	Timer failure
	0300	Timer interrupt failure
	0400	Protected mode failure
	0500	Last keyboard command not accepted
	0600	Converting logic test
	0700	NMI test failed
	0800	Timer bus-test failed
	0900	Low MB chip select test failed
	10*xx*	System board memory parity error
	11*xx*	I/O channel-check error
	1200	Watchdog time-out
	1300	DMA arbitration time-out
	1400	Adapter card ROM checksum error
	1500	System board ROM checksum error or DMA error
	1600	System board port read/write failure
	1800	System board parity error
	2000	Microprocessor test error
	2100	System board 256KB ROM error
	6000	System board ID not recognized
	6100	Dead battery
	6300	Clock not updating
	6400	Memory-configuration error
	6500	Adapter ID mismatch
	6600	Adapter-busy error
	6700	Clock not updating
	6900	System board and processor card configuration mismatch
	7000	ASCII Setup Conflict Error
	7100	Rolling-bit-test failure on CMOS shutdown address byte
	7200	Rolling-bit-test failure on NVRAM diagnostic byte
	7300	Bad CMOS/NVRAM checksum
	7400	Bad configuration
	7500	Bad EEPROM

Table 24 (Page 2 of 3). PS/2 POST Error Codes		
Major Code	**Minor Code**	**Description**
	7600	Tamper evident
	7700	Bad EEPROM
	7800	Bad EEPROM
	7900	NVRAM error log full
	8100	Unsupported configurations
	8200	Privileged-access switch (JMP2) is not in the write-enable position
	8300	Privileged-access password required
	8400	Bad power-on password
	8500	Bad startup sequence
	8600	Password protection hardware
	87*xx*	Serial number error
	8800	Bad EEPROM checksum
	8900	Excessive incorrect password attempts
0002		Memory errors
	0*xxx*	Memory error
	1*xxx*	Unrecoverable error in first 1MB
	2100	ROM-to-RAM remapping error
	25*xx*	Unsupported memory-type installed
	2600	Memory kit in incorrect connector
0003		Keyboard
	0100	Keyboard error
	0200	Keyboard locked
	0300	Keyboard-to-system board interface error
	0400	Keyboard clock high
	0500	No keyboard +5 V dc
0006		Diskette
	0100	Diskette drive or controller error
	0200	Diskette IPL boot record not valid
	0400	Non-media sense diskette drive detected
	0500	Diskette drive locked
0011	*xxxx*	Serial port A error
0012	*xxxx*	Serial port B error
0017		Fixed disk error
	8000	Fixed disk 0 failed
	8100	Fixed disk 1 failed
	8200	Disk-controller error
	9000	Fixed disk 0 error
	9100	Fixed disk 1 error
0024	0100	System board video error

Table 24 (Page 3 of 3). PS/2 POST Error Codes

Major Code	Minor Code	Description
0037	*xxxx*	System board SCSI controller error
0086		Mouse
	0100	System-bus error - keyboard/pointing device interface
	0200	Pointing-device error
	0300	Pointing-device or system-bus error
0096	*xxxx*	SCSI adapter with cache error
0112	*xxxx*	SCSI adapter error
0129	0200	Cache error
0208 to 0241	*xxxx*	SCSI device test failure
I999		Special instruction codes
	00*xx*	Initial microcode load (IML) error
	03*xx*	No bootable device
	04*xx*	IML-to-system mismatch

Note:

x denotes variable information. Various numbers may appear in these fields.

Appendix D. IBM SCSI POST Error Codes

This section contains a list of all IBM SCSI POST error codes. Codes here can be used to determine errors that occur on the IBM SCSI adapter and any attached SCSI devices. Further information can be found in the *IBM Hardware Maintenance and Service Manual* for the IBM SCSI adapter and the various SCSI devices.

D.1 Error Code Format

With the new IBM SCSI adapter and SCSI devices come a new set of error codes. The error codes that occur during POST have the format shown in Figure 38.

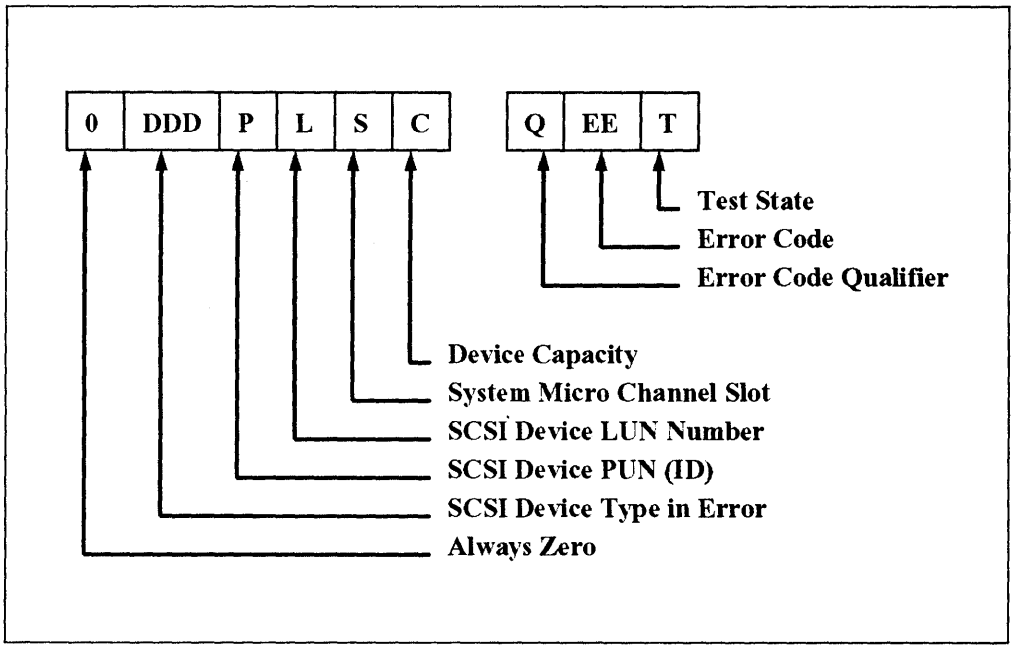

Figure 38. IBM SCSI POST Error Code Format

Figure 38 shows the error code format. The next few sections show what each part indicates.

"0" Always zero: This is the first digit of the error code and is always 0.

"DDD" SCSI device causing error: This part shows the SCSI device which causes the error. For example 112 indicates that a 16-bit non-cached SCSI adapter is causing the error. See D.1.1, "SCSI Device Causing Error" on page 128 for a list of what the device codes are.

"P" SCSI device PUN (ID): This part shows the SCSI device physical unit number or SCSI ID.

"L" SCSI Device LUN: This part shows the SCSI device logical unit number. For a SCSI adapter it will show zero.

"S" System Micro Channel slot: This part shows the Micro Channel slot number. If "S" equals 0 then DDD will be 096 or 112. You must go to D.1.2, "Generic Errors ("S" = 0)" on page 129 to determine the error. If "S" is not equal to 0 there is error on the adapter (or device attached to the adapter) in slot "S".

"Q" Error code qualifier: This part indicates the error code qualifier and can be 0 through 7. Go to D.1.3, "Error Codes with "Q" = 0" on page 129 and choose the section which corresponds to the value of "Q" that you have.

D.1.1 SCSI Device Causing Error

This section decodes the DDD part of the error code.

```
DDD : 096 : 32-BIT CACHED SCSI ADAPTER
      112 : 16-BIT NON-CACHED SCSI ADAPTER

      208 : UNKNOWN SCSI DEVICE TYPE
      209 : DIRECT ACCESS - REMOVABLE MEDIA AND/OR
            OTHER THAN 512 BYTE BLOCKS
      210 : DIRECT ACCESS - NON REMOVABLE MEDIA. 512
            BYTE BLOCKS (FIXED DISK)
      211 : SEQUENTIAL ACCESS (IE. TAPE)
      212 : PRINTER
      213 : PROCESSOR
      214 : WRITE ONCE, READ MULTIPLE (W.O.R.M.)
      215 : READ ONLY (IE. CD-ROM)
      216 : SCANNER
      217 : OPTICAL MEMORY
      218 : CHANGER (IE. MULTIPLE TRAY CD-ROM OR JUKEBOX)
      219 : COMMUNICATIONS
```

Figure 39. SCSI Device Causing Error

D.1.2 Generic Errors ("S" = 0)

When "S" is 0, DDD will be 096 or 112.

```
DDD0100 0000 : NO SETUP DATA AVAILABLE ON SYSTEMS WITH
               NVRAM.  THIS MEANS SCSI SETUP DATA WAS NOT
               LOCATED OR THE CHECKSUM DID NOT VERIFY.
               ON SYSTEMS WITHOUT NVRAM (MODEL 50 FOR
               EXAMPLE) SETUP DATA MUST BE ON 1ST
               NON-SCSI FIXED DISK.

DDD0200 0000 : NO FIXED DISK AT PUN 6. LUN 0 FOR 161,
               162, 165 SYSTEM ERROR PATH

DDD0300 0000 : NO SPACE AVAILABLE IN EXTENDED BIOS DATA
               AREA FOR SCSI DATA TABLE

DDD04Q0 0000 : ROM MODULES NOT FOUND ON ADAPTER

DDD0500 0000 : ROM CHECKSUM ERROR ON 2ND 16K PORTION OF
               32K ROM
```

Figure 40. SCSI Generic Errors (S=0)

D.1.3 Error Codes with "Q" = 0

A value of "-" in any of the following error codes may be any character.

```
 96---- 001- : 80188 ROM TEST FAILURE
 96---- 002- : LOCAL RAM TEST FAILURE
 96---- 003- : EXTERNAL TERMINATOR MISSING OR FUSE BAD
 96---- 004- : 80188 INTERNAL PERIPHERAL TEST FAILURE
 96---- 005- : BUFFER CONTROL CHIP TEST FAILURE
 96---- 006- : BUFFER RAM TEST FAILURE
 96---- 007- : SYSTEM INTERFACE CONTROL CHIP TEST FAILURE
 96---- 008- : SCSI INTERFACE TEST FAILURE

112---- 001- : 8032 ROM TEST FAILURE
112---- 002- : LOCAL RAM TEST FAILURE
112---- 003- : LOCAL RAM ADDRESS TEST FAILURE
112---- 004- : 8032 INTERNAL PERIPHERAL TEST FAILURE
112---- 005- : BUFFER CONTROL CHIP TEST FAILURE
112---- 006- : UNDEFINED ERROR CONDITION
112---- 007- : SYSTEM INTERFACE CONTROL CHIP TEST FAILURE
112---- 008- : SCSI INTERFACE TEST FAILURE
```

Figure 41. SCSI Error Codes with Q=0

D.1.4 Error Codes with "Q" = 1

```
QEE : 107 : ADAPTER HARDWARE FAILURE
      10C : COMMAND FAILED
      10E : COMMAND ERROR (INVALID COMMAND OR PARAMETER)
      10F : SEQUENCING ERROR
      180 : TIME OUT
      181 : ADAPTER BUSY ERROR
      182 : UNEXPECTED INTERRUPT PRESENTED BY ADAPTER
      183 : ADAPTER REGISTER TEST FAILURE
      184 : ADAPTER RESET (VIA BCR) FAILURE
      185 : ADAPTER BUFFER TEST FAILURE (CACHED
            ADAPTER ONLY)
      186 : ADAPTER RESET COUNT EXPIRED
      187 : ADAPTER REGISTERS NOT CLEARED ON RESET
            (POWER ON OR CHANNEL RESET)
      188 : CARD ID IN ADAPTER MICROCODE DID NOT MATCH
            ID IN POS REGISTERS
      190 : EXPECTED DEVICE DID NOT RESPOND (NOT POWERED
            ON AND SHOULD BE IF DEVICE NUMBER IS NOT 096
            OR 112)
      19X : DMA ARBITRATION LEVEL CONFLICT (IF DEVICE
            NUMBER IS 096 OR 112)
```

Figure 42. SCSI Error Codes with Q=1

D.1.5 Error Code with "Q" > 1

All error codes with "Q" > 1 are developed using information returned by either the adapter or a device. The "Q" value defines the origin of the "EE" code that is reported.

Error codes (EE) with "Q" = 4 or 5 may be reported that are not listed here or may actually have a different definition to those given. Those are dependent on the device.

The error codes defined here were obtained from the Common Command Set (Rev 4.B) of the ANSI SCSI-1 Specification. Error codes with "Q" = 2, 3, or 6 are defined in the *IBM SCSI Adapter Technical Reference*.

```
"Q" = 2 - Command Error field of Command Complete Status
          block returned by the adapter
    = 3 - SCSI Status field of the Command Complete
          Status  block or Command Error field values
          indicating software problems (less than 20H)
    = 4 - Sense Key value returned by a device
    = 5 - Additional Sense byte (byte 12) of Sense
          information from device
    = 6 - Device Error code field of Command Complete
          Status block
    = 7 - Device errors not normally considered an error
          but considered an error based on when the code
          was returned.
          (ie. Medium Corrupted error on device with non
          removable media)
```

Figure 43. SCSI Error Codes with Q>2

"Q" = 2

```
220 : ADAPTER HARDWARE ERROR
221 : GLOBAL TIMEOUT ON ADAPTER (DEVICE DID NOT RESPOND)
222 : ADAPTER DMA ERROR
223 : ADAPTER BUFFER DEFECTIVE
224 : COMMAND ABORTED BY ADAPTER
```

Figure 44. SCSI Error Codes with Q=2

"Q" = 3

```
301 : INVALID PARAMETER IN SCB
303 : COMMAND NOT SUPPORTED
304 : COMMAND ABORTED BY SYSTEM
305 : COMMAND REJECTED (BUFFER NOT DISABLED)
306 : COMMAND REJECTED (ADAPTER DIAGNOSTIC FAILURE)
307 : FORMAT REJECTED
308 : ASSIGN REJECTED (COMMAND IN PROGRESS)
309 : ASSIGN REJECTED (DEVICE ALREADY ASSIGNED)
30A : COMMAND REJECTED (DEVICE NOT ASSIGNED)
30B : COMMAND REJECTED (MAXIMUM LBA EXCEEDED)
30C : COMMAND REJECTED (16 BIT CARD SLOT ADDRESS EXCEEDED)
313 : INVALID DEVICE FOR COMMAND
3FF : STATUS NOT RETURNED BY ADAPTER (CCSB ALL 0)
```

Figure 45. SCSI Error Codes with Q=3

"Q" = 4

```
401 : RECOVERED ERROR (NOT CONSIDERED AN ERROR CONDITION)
402 : DEVICE NOT READY
403 : DEVICE MEDIUM ERROR
404 : DEVICE HARDWARE ERROR
405 : ILLEGAL REQUEST FOR DEVICE
406 : DEVICE UNIT ATTENTION WOULD NOT CLEAR
407 : DEVICE DATA PROTECT ERROR
409 : DEVICE VENDOR UNIQUE ERROR
40A : DEVICE COPY ABORTED
40B : DEVICE COMMAND ABORTED
40C : DEVICE SEARCH DATA COMMAND SATISFIED
40D : DEVICE VOLUME OVERFLOW (RESIDUAL DATA REMAINS IN
      BUFFER)
40E : DEVICE MISCOMPARE (SOURCE DATA DID NOT MATCH MEDIUM
      DATA)
```

Figure 46. SCSI Error Codes with Q=4

"Q" = 5

```
501 : NO INDEX OR SECTOR
502 : SEEK INCOMPLETE
503 : WRITE FAULT
504 : DRIVE NOT READY
505 : DRIVE NOT SELECTED
506 : NO TRACK ZERO FOUND
507 : MULTIPLE DRIVES SELECTED
508 : LOGICAL UNIT COMMUNICATION FAILURE
509 : HEAD POSITIONING ERROR (TRACK FOLLOWING ERROR)
510 : CRC OR ECC ERROR ON ID FIELD
511 : UNRECOVERABLE READ ERROR
512 : NO ADDRESS MARK (ID FIELD)
513 : NO ADDRESS MARK (DATA FIELD)
514 : RECORD NOT FOUND
515 : SEEK ERROR
516 : DATA SYNCHRONIZATION ERROR
517 : RECOVERABLE READ (WITHOUT ECC) ERROR
518 : ECC RECOVERED READ ERROR
519 : DEFECT LIST ERROR
51A : PARAMETER OVERRUN
51B : SYNCHRONOUS TRANSFER ERROR
51C : PRIMARY DEFECT LIST NOT FOUND
51D : COMPARE ERROR
520 : INVALID COMMAND
521 : ILLEGAL LOGICAL BLOCK ADDRESS (LBA)
522 : ILLEGAL FUNCTION FOR DEVICE TYPE
524 : ILLEGAL COMMAND BLOCK FIELD
525 : INVALID LUN
526 : ILLEGAL FIELD IN PARAMETER LIST
528 : MEDIA CHANGED
529 : POWER ON OR BUS DEVICE RESET OCCURRED (NOT AN
      ERROR)
52A : MODE SELECT PARAMETERS CHANGED (NOT AN ERROR)
531 : MEDIUM FORMAT CORRUPTED
532 : DEFECT SPARE LOCATION UNAVAILABLE
540 : DEVICE RAM FAILURE
541 : DATA PATH DIAGNOSTIC FAILURE
542 : POWER ON DIAGNOSTIC FAILURE
543 : MESSAGE REJECTED
544 : INTERNAL CONTROLLER ERROR
545 : DEVICE WAS UNABLE TO RE-CONNECT
547 : INTERFACE PARITY ERROR
548 : INITIATOR DETECTED ERROR
549 : ILLEGAL COMMAND OR COMMAND OUT OF SEQUENCE ERROR
5F0 : FORMAT IN PROGRESS (NOT AN ERROR)
5F1 : SPIN UP IN PROGRESS
```

Figure 47. SCSI Error Codes with Q=5

"Q" = 6

```
601 : SCSI BUS RESET OCCURRED
602 : SCSI INTERFACE FAULT
610 : SELECTION TIMEOUT ERROR (DEVICE NOT AVAILABLE)
611 : UNEXPECTED BUS FREE
612 : MANDATORY SCSI MESSAGE REJECTED
613 : INVALID SCSI PHASE SEQUENCE
620 : SHORT LENGTH RECORD ERROR
```

Figure 48. SCSI Error Codes with Q=6

"Q" = 7

```
702 : DEVICE NOT READY (REMOVABLE MEDIA DEVICES)
704 : DEVICE NOT READY (NON-REMOVABLE MEDIA DEVICES)
728 : MEDIA CHANGED ERROR WOULD NOT CLEAR
731 : MEDIUM FORMAT CORRUPTED
      (FORMAT UNIT INTERRUPTED - FORMAT MUST BE RE-ISSUED)
7F0 : FOMAT IN PROGRESS (PRIOR FORMAT UNIT ISSUED BEING
      COMPLETED)
7F1 : SPINUP IN PROGRESS
```

Figure 49. SCSI Error Codes with Q=7

D.1.6 Test State in Which Failure Occurred (T)

Please refer to the information below to see test state in which failure occurred.

```
0 : NOT APPLICABLE FOR ERROR CODE
A : ADAPTER INITIALIZATION
B : ADAPTER RESET
C : ADAPTER REGISTER TEST
D : ADAPTER BUFFER TEST PHASE 1 (CACHED ADAPTER ONLY)
E : ADAPTER BUFFER TEST PHASE 2 (CACHED ADAPTER ONLY)
F : ADAPTER BUFFER TEST PHASE 3 (CACHED ADAPTER ONLY)
G : ADAPTER BUFFER TEST PHASE 4 (CACHED ADAPTER ONLY)
H : ADAPTER INFORMATION TEST STATE
    (BUFFER ENABLE. BUFFER SIZE, RETRY ENABLE, ETC.)
I : DEVICE ASSIGNMENT SEQUENCE
J : DEVICE NOT READY (ALSO INITIAL UNIT ATTENTION
    CLEARING)
K : DEVICE RESET
L : DEVICE STARTING PHASE (APPROPRIATE DEVICES ONLY)
M : DEVICE IN PROCESS OF STARTING (WAIT FOR DEVICE TO
    BECOME READY)
N : DEVICE BLOCK SIZE DETERMINATION
O : DEVICE SELF TEST
P : DEVICE SINGLE BLOCK (LBA) READ
Q : DEVICE DOUBLE BLOCK (LBA) READ
S : ERROR OCCURRED AFTER DEVICE TESTING HAD COMPLETED
```

Figure 50. SCSI Test State in which Error Occurred (T)

A

all points addressable (APA). In computer graphics, pertaining to the ability to address and display or not display each picture element (pel) on a display surface.

alphanumeric (A/N). Pertaining to a character set that contains letters, digits, and usually other characters, such as punctuation marks.

American National Standards Institute (ANSI). An organization consisting of producers, consumers, and general interest groups, that establishes the procedures by which accredited organizations create and maintain voluntary industry standards in the United States.

Arithmetic and Logic Unit (ALU). A part of a computer that performs arithmetic operations, logic operations, and related operations.

arbitration. A method with which multiple devices attached to a single bus can bid to get control of that bus.

ASCII. American National Standard Code for Information Interchange. The standard code, using a coded character set consisting of 7-bit coded characters (8-bit including parity check), used for information interchange among data processing systems, data communication systems, and associated equipment. The ASCII set consists of control characters and graphic characters. IBM has defined an extension to ASCII code (characters 128-255).

asynchronous. A mode of data transfer across the SCSI bus where each byte of data transferred must be acknowledged as received by the target before the next byte can be sent. The maximum data transfer rate supported in asynchronous mode is 2 MBps.

AT Attachment. ATA defines a compatible register set and a 40-pin connector and its associated signals.

B

bitmap. A rectangular array of data that describes an image on a screen. Each array location carries information on screen attributes, for example color, intensity, pixel location etc. Many bitmaps carry more information than is actually displayed.

BIOS. Basic Input Output System. In an IBM personal computer, code that controls basic hardware operations such as interactions with diskette drives, fixed-disk drives, and the keyboard.

bit. Either of the binary digits: a 0 or 1.

blit. Block Pixel Transfer. The process of taking a rectangular array of pixels from a source location and transferring them to a destination location. This process often involves some manipulation of the pixels during the transfer. See PxBlt.

boot. To prepare a computer system for operation by loading an operating system.

buffer. (1) A routine or storage used to compensate for a difference in rate of flow of data, or time of occurrence of events, when transferring data from one to another. (2) A portion of storage used to hold input or output data temporarily.

bus. (1) In a processor, a physical facility on which data is transferred to all destinations, but from which only addressed destinations may read in accordance with appropriate conventions (2) One ore more signal conductors used for transmitting signals or power.

Bus Master. An intelligent device that, when attached to the Micro Channel bus, can bid for and gain control of the Micro Channel bus to perform its specific task.

byte. A string that consists of a particular number of bits, usually 8, that is treated as a unit, and that represents a character.

C

cache. A high-speed storage buffer that contains frequently accessed instructions and data; it is used to reduce access time.

cathode ray tube (CRT). A vacuum tube in which a beam of electrons can be moved to draw lines or to form characters or symbols on its luminescent screen.

CCS. The SCSI Common Command Set. A set of SCSI commands that is specified in the ANSI standard that all SCSI device must be able to use in order to be fully compatible with the ANSI standard.

CD-ROM. Compact Disk Read Only Media is a disc that you can only read data from. Data cannot be written to CD-ROM.

circuit. (1) A logic device. (2) One ore more conductors through which an electric current can flow.

coprocessor. A microprocessor on an expansion board or planar that extends the address range of the main processor or adds specialized instructions to handle a particular category of operations.

Cyclic Redundancy Check (CRC). A numeric value derived from the bits in a message that is used to check for any bit errors in transmission.

CSD. Corrective Service Diskette. A diskette provided by IBM to registered service coordinators

for resolving user-identified problems. This diskette includes program updates designed to resolve problems.

cylinder. (1) The fixed disk or diskette tracks that can be read or written without moving the disk or diskette drive read and write mechanism. (2) The number of tracks for space allocation.

D

direct access storage device (DASD). A device in which access time is effectively independent of the location of the data.

device. An input/output (I/O) unit such as a terminal, a display, or a printer.

device driver. A file that contains the code needed to attach and use a device.

Device Level Copying (DLC). When two devices attached to the SCSI bus perform data transfers between each other across the SCSI bus without using the attachment feature.

directory. A list of files that are stored on a disk or diskette. A directory also contains information about the files, such as size and date of last change.

DIP switch. In an IBM personal computer, a two-position switch on a circuit board that is preset to control certain functions; the user can change the position of a DIP switch to satisfy special requirements.

Direct Memory Access (DMA). A method used to transfer data directly from device to system memory without using the main system processor.

disconnect. When a device has received a command and disconnects from the SCSI bus,it enables other devices to use the SCSI bus while it processes its command.

dithering. Mixing patterns from one color with patterns from another color to create a third color.

DOS. Disk Operating System. A programm that controls the operation of an IBM Personal Computer, PS/1, PS/2, or PS/ValuePoint and the execution of application programs.

E

EPROM. Erasable programmable read-only memory. Programmable read-only memory that is read-only in normal use but can be erased by a special technique and then reprogrammed.

error checking and correction (ECC). In a processing unit, the detection and correction of all single-bit errors, plus the detection of double-bit and some multiple-bit errors.

F

Federal Communications Commission (FCC). A board of commissioners appointed by the President under the Communications Act of 1934, having the power to regulate all interstate and foreign communications by wire and radio originating in the United States.

first in/first out (FIFO). A queuing technique in which the next item to be retrieved is the item that has been in the queue for the longest time.

fixed disk. A flat, circular, nonremovable plate with a surface layer on which data can be stored by magnetic recording.

frequency. The rate of signal oscillation, expressed in hertz (cycle per second).

I

initial program load (IPL). (1) The initialization procedure that starts an operating system. (2) The process of loading programs and preparing a system to run jobs.

initiator. A device attached to the SCSI bus that sends a command to another device on the SCSI bus. The device that receives that command is a target.

instruction. A statement that specifies an operation to be performed by a system and that identifies data involved in the operation.

interface. A shared boundary between two or more entities. An interface may be a hardware component to link two devices or a portion of storage or registers accessed by two or more computer programs.

interlaced. An interlaced video system is a system in which the even scan lines are refreshed in one vertical cycle (field), and the odd scanlines are refreshed in another vertical field. The advantage is that the video bandwidth is roughly half that required for a non-interlaced system of the same resolution. This results in less costly hardware. The disadvantage of an interlaced system is flicker, especially when displaying objects that are only a few scanlines high.

International Organization for Standardization (ISO). An organization of national standards bodies from various countries established to promote the development of standards to facilitate international exchange of goods and services, and develop cooperation in intellectual, scientific, technological, and economic activity.

J

jumper. A connector between two pins on a circuit board that enables or disables an option, feature or parameter value.

K

kilobit (Kb). One thousand binary digits.

kilobyte (KB). 1024 bytes for processor and data storage (memory) size; otherwise, 1000 bytes.

L

Logical Block Address. This term defines the addressing mode of the drive as being by the linear mapping of sectors from 1 to n.

logical unit. A device attached to a SCSI device. An LU and is *not* directly attached to the SCSI bus.

logical unit number (LUN). A number given to a device that is attached to a SCSI device and not directly to the SCSI bus. The device is known as a Logical Unit.

M

megabit (Mb). 1 048 576 bits.

megabyte (MB). 1 048 576 bytes.

microchip. A small piece of semiconductive material, usually silicon, that contains miniaturized electronic circuits.

microprocessor. A microchip containing integrated circuits that executes instructions.

multitasking. A mode of operation that provides for concurrent performance, or interleaved execution of two or more tasks.

N

non-interlaced. A video system in which every pixel is refreshed during every vertical scan. A non-interlaced display is normally more expensive than an interlaced display of the same resolution, but has a more pleasing appearance to the human eye.

O

operating system. The software that controls the running of programs. An operating system may provide services such as resource allocation, scheduling, input/output (I/O) control, and data management.

P

pel. Picture Element. The minimum item that can be displayed on a video display. Also known as pixel.

pixel. Picture Element. The minimum item that can be displayed on a video display. Also known as pel.

Planar. Also known as the motherboard. The largest electronic board in a computer which connects the various subsystems together.

Power-on Self Test (POST). A series of diagnostic tests that are run automatically each time the computer's power is turned on.

processor. In a computer, a functional unit that interprets and executes instructions.

programmed input/output (PIO). A means of data transfer that requires the use of the host processor.

PROM. Programmable read-only memory. A field-programmable read-only storage that can have the data content of each storage cell altered only once.

physical unit number (PUN). Another term used to describe a device attached directly to the SCSI bus. Also known as a SCSI Device or SCSI ID.

PxBlt. Block Pixel Transfer. The process of taking a rectangular array of pixels from a source location and transferring them to a destination location. This process often involves some manipulation of the pixels during the transfer. See blit.

R

random access memory (RAM). A computer's or adapter's volatile storage area into which data may be entered or retrieved from in a non-sequential manner.

read-only memory (RAM). A computer's or adapter's storage area whose contents cannot be modified by the user except under special circumstances.

reconnect. When a device that has finished processing a command, it arbitrates for the SCSI bus in order to reconnect to it and perform its data transfer.

Reference Diskette. A diskette shipped with the IBM PS/2 computers. The diskette contains code and files used for configuration of options and for hardware diagnostic testing.

S

scan frequency. The number of times per second that a display refreshes the information on its screen. Often expressed in two parts, namely vertical and horizontal frequency.

SCSI Attachment Feature. The feature that attaches to the main system unit and the SCSI bus. It is the controlling feature of the SCSI subsystem.

SCSI bus. A term used to describe the 50-Conductor cable that attaches intelligent devices to the SCSI attachment feature.

SCSI device. An intelligent device that is directly attached to the SCSI bus. It conforms to the ANSI Standard X3.131-1986 for attached SCSI devices.

SCSI ID. A number configured on a SCSI device so that it can be addressed on the SCSI bus. Each SCSI device has a unique SCSI ID number. It is in the range from 0 to 7.

Small Computer System Interface (SCSI). SCSI defines the interface between an attachment feature and intelligent devices.

Sprite. A graphical pattern in memory that can be manipulated as a whole by software. Often used for animation. When enabled, it overlays the picture that is being displayed. It can be positioned anywhere on the display without affecting the contents of video memory. For example, this feature can be used for a mouse pointer.

subsystem. A secondary or subordinate system, or programming support, usually capable of operating independently of asychronously with a controlling system.

synchronous. A mode of data transfer across the SCSI bus where each byte of data transferred does not have to be acknowledged as received by the target device before the next byte can be sent. The maximum data transfer rate supported in synchronous mode is 5 MBps.

T

target. A device attached to the SCSI bus that receives and processes commands sent from another device on the SCSI bus. The device that sends the command is known as an initiator.

terminator. A piece of hardware that must be attached to both ends of the 50-Conductor SCSI attachment cable (commonly known as the SCSI bus).

V

very large-scale integration (VLSI). The process of integrating very large numbers of circuits on a single chip of semiconductor material.

List of Abbreviations

AIN	alphanumeric
ABIOS	Advanced Basic Input Output System
ALU	Arithmetic and Logic Unit
ANSI	American National Standards Institute
APA	All Points Addressable
AT-DBA	AT Direct Bus Attach
ATA	AT Attachment
ATC	Attribute Control
AVE	Auxiliary Video Extension
BASIC	Beginners All-Purpose Symbolic Instruction Code
BIOS	Basic Input Output System
BLT	Block Logical Transfer
BVE	Base Video Extension
CAMC	Common Access Method Committee
CAS	Column Access Strobe
CCS	Common Command Set
CD-ROM	Compact Disk - Read Only Media
CGA	Color Graphics Adapter
CHS	Cylinder Head Sector
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CRT	Cathode Ray Tube
CRTC	CRT Controller
CSD	Corrective Service Diskette
DAC	Digital to Analog Converter
DASD	Direct Access Storage Device
DCLK	Video Dot Clock
DES	Data Encryption Standard
DMA	Direct Memory Access
DMQS	Display Mode Query and Set
DoD	Department of Defense (USA)
DRAM	Dynamic Random Access Memory
EC	European Community
ECC	Error Checking and Correction
EGA	Enhanced Graphics Adapter
EEPROM	Electrically Erasable Programmable Read Only Memory
EMS	Expanded Memory Specification
EPROM	Erasable Programmable Read Only Memory
ESDI	Enhanced Small Device Interface
FCC	Federal Communication Commission (USA)
FIFO	First In/First Out
GDC	Graphic Display Controller
H-SYNCH	Horizontal Synchronization
IAS	Intelligent Address Sequencer
IDE	Integrated Drive Electronics
IPL	Initial Program Load
I/O	input/output
ISA	Industry Standard Architecture
ISO	International Organization for Standardization
ITSC	International Technical Support Center
Kb	kilobyte (1024 bytes)
Kbit	Kilobit (1000 bits)
kBps	kilobytes per second
kbps	kilobits per second
LBA	Logical Block Address
LCD	Liquid Crystal Display
LIM	Lotus Intel Microsoft
LRU	Least Recently Used
LUN	Logical Unit Number
MBps	Megabytes per second
Mbps	Megabits per second
Mb	Megabyte (1,048,576 bytes)
Mbit	Megabit (million bits)
MCA	Micro Channel Architecture
MCLK	Memory Clock
MCU	Memory Control Unit
MDA	Monochrome Display Adapter
MFI	Mainframe Interactive, same as NPT

MHz	mega hertz
MME	Matched Memory Extension
MMU	Memory Management Unit
NCSC	National Computer Security Centre
NPT	nonprogrammable terminal
OE	Output Enable
OEM	Other Equipment Manufacturer
PC	Personal Computer
PEL	Picture Element
PIO	Programmed Input/Output, Programmable Input/Output
POS	Programmable Option Select
POST	Power-On Self Test
PROM	Programmable Read Only Memory
PxBLT	Pixel Block Transfer
RAM	Random Access Memory
RAS	Row Address Strobe
ROM	Read Only Memory
RSA	Rivest-Shamir-Adelman algorithm (cryptography)
SCB	System Control Block
SCSI	Small Computer System Interface
SEK	Svenska Elektriska Kommissionen (Swedish counterpart to International Electrotechnical Commission)
SOD	Statement of Direction
SPC	System Priority Controller
SVGA	Super Video Graphics Adapter
TI	Timing Interface
TS	Timing Sequencer
TSR	Terminate and Stay Resident
V-SYNC	Vertical Synchronization
VCLK	Video Clock
VDT	Video Display Terminal
VESA	Video Electronic Standards Association
VGA	Video Graphics Adapter/Array
VLMF	Very Low Magnetic Field, below 20 milli-Teslar (SEK)
VLSI	Very Large Scale Integration
VPD	Vital Product Data
VRAM	Video Random Access Memory
VU	Vendor Unique
WE	Write Enable
XGA	Extended Graphics Adapter/Array

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