T-52-33-45

[redacted]

WD9500 (PWGA)

Enhanced 8514/A

Compatible Chip Set

[redacted]

WESTERN DIGITAL

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1.0 INTRODUCTION

Western Digital's WD9500-SET1 is comprised of two proprietary VLSI chips, the Pixel Address Manager (PAM) and the Pixel Data Manager (PDM). These chips serve as the primary components of intelligent, high-resolution graphics boards and motherboards for PC/AT, PS/2 Micro Channel and E.I.S.A. computer systems and compatibles. When the remaining board-level components and software are properly selected and integrated, the WD9500-SET1 provides full compatibility with the IBM 8514/A Display Adapter. The WD9500-SET1 provides superior performance plus functional enhancements (Western Digital Extensions). In order to take full advantage of all features, including the unique extensions, Western Digital supplies performance-enhanced software drivers for key software packages such as Microsoft Windows 286 and 386 and AutoCAD.

1.1 FEATURES

- Provides full functional compatibility with the IBM 8514/A Display Adapter, including hardware compatibility with the registers accessed by any application.
- Provides integrated bus interface for the PC/AT, PS/2 Micro Channel and E.I.S.A.
- Transparently runs software written for 8514/A interlaced monitors on non-interlaced monitors.
- Performance averages 30% to 100% faster than 8514/A on graphics operations.
- BITBLT performance 4.5 times that of IBM 8514/A in Turbo 4-bit mode. Turbo 4-bit BITBLT is two times faster than regular 4-bit or 8-bit BITBLT.
- Provides enhanced resolution: one page of 1280x1024 pixels 256 colors; two pages of 1024x768 pixels 256 colors; two pages of 640x480 pixels 256 colors.
- Provides enhanced graphics commands for high-speed hardware generation of textured lines and enhanced solid lines.
- Provides flicker-free video DAC programming.
- 60MHz Graphics Processor Clock Rate.
- All features, including most extensions, are supported by Western Digital Imaging Adapter Interface (A.I.) driver software.
- Provides performance enhanced software drivers for key software packages such as Windows 286/386 and AutoCAD.
- Supports 256Kx4 VRAM in different speed grades (120ns or faster) with programmable VRAM timing to minimize wait states.
- Provides independent Video and Data Clocks.
- Supports INMOS and Brooktree video DACs and compatibles with back-end integration to minimize external glue logic.
- Supports interlaced and non-interlaced monitors with a maximum vertical refresh rate of 70 MHz. Software written for 8514/A interlaced monitors needs no modification for non-interlaced monitors.
- Packaged in a 132-pin JEDEC Plastic Quad Fine Pitch Flat Pack.
- 1.25 Micron CMOS Technology.

1.2 DESCRIPTION

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Full compatibility with the IBM 8514/A provides intelligent graphics functions such as polyline drawing, pattern fill for rectangles, "areas" (polygons), and "scissoring" (clipping). In addition the WD9500-SET1 provides several functional enhancements and options which further improve performance.

One major enhancement is the support of higher screen resolution (1280x1024 pixels with 256 simultaneously displayable colors as opposed to the 1024x768 maximum for the IBM 8514/A). Alternatively, the WD9500-SET1 can support a second screen page at the highest 8514/A resolution.

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The WD9500-SET1 dramatically improves the speed of most graphics operations. In regular 4-bit mode, the WD9500-SET1 performs Bit Block Transfers (BITBLTs) twice as fast as the IBM 8514/A. In Turbo 4-bit mode, it is 4.5 times as fast. Enhanced performance is particularly obvious when moving large images on the screen (e.g. scrolling). Under turbo mode all horizontal data movement is twice as fast. This includes BITBLT, rectangle fill, horizontal line, and polygon search and fill.

Users also notice considerable performance improvement in all new line-drawing operations, because the WD9500-SET1 directly performs several functions that the IBM 8514/A must perform in the much slower CPU software. One such improvement is the direct generation of textured line; another is the automatic, high-speed calcula-

tion of line parameters by the WD9500-SET1, replacing the tedious CPU software procedures with simple specifications of only the beginning and ending points of any line.

Whereas the IBM Display Adapter 8514/A is designed only for PS/2 computer models that use the Micro Channel bus, the WD9500-SET1 provides an alternate interface to allow full 8514/A functionality (with extensions) for the Micro Channel, and more importantly, for all PC/AT computers and compatibles. The interface selection is made with a single device pin that is "strapped" at board design time.

Many graphics applications produce noticeable screen flickering when the software steals refresh cycles to modify the color palette in the video DAC. A unique, low-cost board design option will provide flicker-free display operation by allowing the WD9500-SET1 to buffer the new palette values and apply them during the monitor's horizontal retrace (flyback).

WD9500-SET1 based boards can accommodate both interlaced display monitors, such as the IBM 8514, and non-interlaced monitors. The WD9500-SET1 drives either type, automatically configuring itself at reset time based on the signals from the monitor interface cable (for IBM-compatible interlaced monitors) or on user selection through on-board switches or through a software utility. This gives the end user greater flexibility in balancing cost against performance, which is not possible with the IBM 8514/A board.

Software written directly to the 8514/A registers can program the video registers for an IBM 8514/A display with interlaced timing to achieve a 1024x768 resolution. To achieve maximum flexibility for driving different monitors, two sets of video registers are provided; one for 1024x768 resolution and one for 640x480 resolution. These registers can be programmed by the BIOS EPROM at power-up and their values locked in so that direct access by software does not affect the preset video timing.

The WD9500-SET1 offers the board designer several choices concerning cost, function, and performance. It saves design time, board space, and component costs by integrating much of the peripheral logic into its design. The designer can choose among several video memory (VRAM) architectures using 256Kx4 VRAM chips with back-end logic integrated into the WD9500-SET1. This allows for 8514/A emulation and extension to two pages of 1024x768x8 (1280x1024 extended resolution requires off-chip logic support). The designer may also exploit the use of different clock rates for the drawing process and the screen refresh process. The designer may bypass the design of video data multiplexing and serializing since these functions are integrated into the WD9500-SET1.

2.0 ARCHITECTURE

The WD9500-SET1 consists of two 132-pin chips: the PAM (Pixel Address Manager) and the PDM (Pixel Data Manager). Figure 2-1 illustrates the logical architecture of a board based upon the WD9500-SET1. Each of its functional elements are discussed below.

The VRAM block in Figure 2-1 represents the video memory subsystem which is used to store screen images generated in the WD9500-SET1 (as a result of CPU drawing instructions) or sent from the CPU (typically for the purpose of restoring previously drawn images that had been stored elsewhere in the system). The WD9500-SET1 then accesses these images for automatic refreshing of the display screen. Drawing operations take place within a pixel coordinate space of 2K by 2K. Remaining VRAM storage is available to the WD9500-SET1 and the CPU for "off-screen" use, including storage of fill patterns and scratchpad data. Section 3.2 describes VRAM operation and defines the detailed interface of the VRAM subsystem to the WD9500-SET1 chip set.

In the standard board configuration, the WD9500-SET1 is responsible for serializing and multiplexing data extracted from the VRAM for screen refresh, and then forwarding the data to the DAC via the video interface logic block. To achieve 1280 x 1024 pixel resolution, serializing and multiplexing is done within the VRAM block in VRAM architectures using external back-end support. The resultant screen refresh data bypasses the WD9500-SET1, as shown in Figure 2-1.

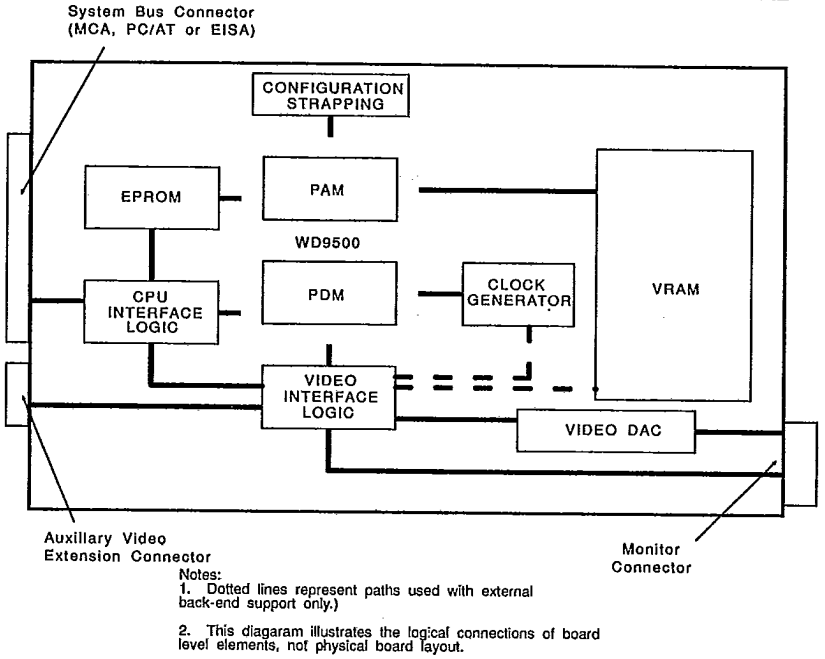

FIGURE 2-1. ARCHITECTURE

The primary function of the video DAC (Digital-to-Analog Converter) is to generate analog intensity signals for the red, green, and blue guns of the display monitor. These values are synchronized with the pixel coordinates as the guns sweep across the screen. The source of these values is the "pixel data" that the WD9500-SET1 reads out of VRAM in its screen refresh operation. With external back-end support, extra intelligence is required in the DAC to assist in the data formatting begun in the serializing and multiplexing logic within the VRAM block. The DAC contains the color palette, a small memory that maps a given pixel value into a specific combination of RGB intensities according to the contents of each of the cells in the palette memory. For example, in a 256-color arrangement, an eight-bit pixel value selects one of 256 palette memory cells. Each of the latter have been loaded with an 18-bit datum partitioned into three six-bit fields whose values are in turn converted into red, green, and blue signal intensities when that cell is selected. Palette values may be loaded directly from the CPU or indirectly through the WD9500-SET1 when using the Western Digital flicker-free option.

The video DAC and interface subsystem includes the auxiliary video extension (used to drive the monitor from an off-board source, normally the system VGA), the monitor interface, and other related logic and interfaces. Note that the small block in Figure 2-1 labeled "Video Interface Logic" represents only a modest amount of logic and, in fact, consists largely of pass-through routing of signals. The block is drawn chiefly for convenience in explanation.

The CPU Interface Logic block contains the bus transceivers and TTL logic necessary to interface the WD9500-SET1 chips to the system bus (either the IBM PS/2 Micro Channel of the IBM PC/AT bus, or compatible busses). This block also provides a data path to the DAC, which is used by the CPU to directly access palette values, and to the EPROM. The CPU interface logic is described in detail in Section 3.1.

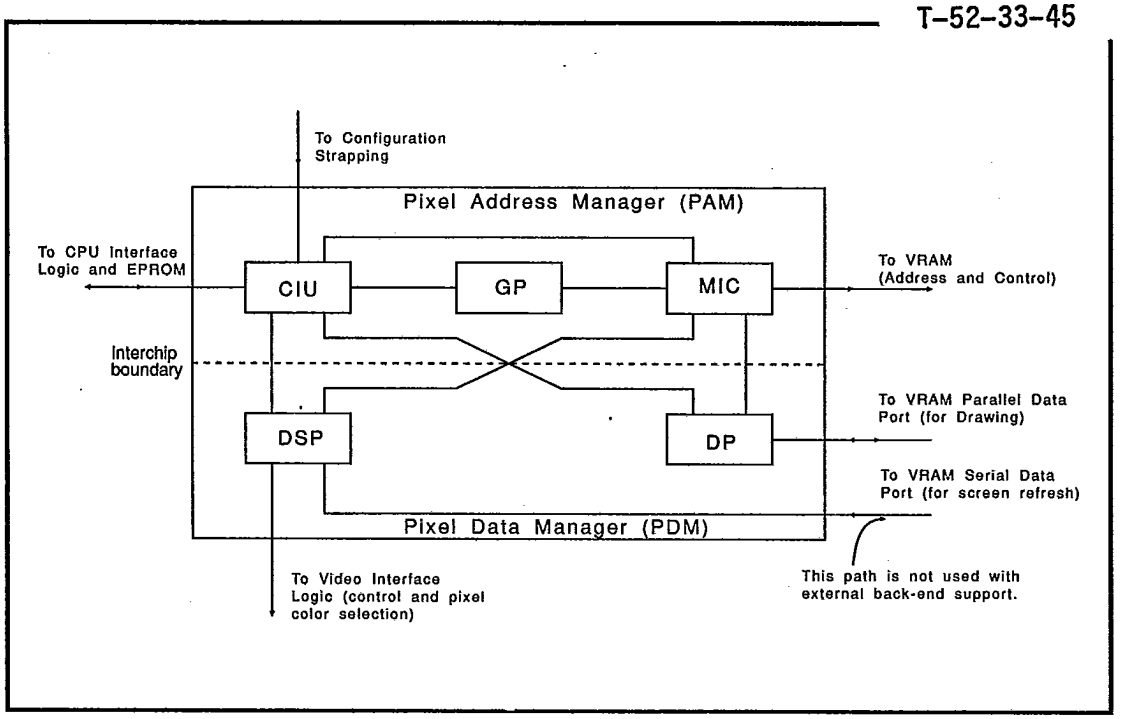

FIGURE 2-2. FUNCTIONAL ORGANIZATION

The remaining board elements are the EPROM (containing Western Digital-supplied BIOS extension firmware), the clock generators, and a group of minor components (pull-up/down logic and DIP switches) used by the WD9500-SET1 to sense its environmental configuration; whether Micro Channel or AT bus, VRAM organization, etc. These elements are described in Section 3.0, together with the inter-chip (PAM-PDM) connections.

Finally, the WD9500-SET1 contains a set of user-accessible internal registers that are compatible with those on the IBM 8514/A board, plus certain extra registers to support Western Digital extensions. From the user's point of view, these registers exist chiefly as destinations for software commands ("orders" in IBM terminology) and their parameters.

2.1 FUNCTIONAL ORGANIZATION

Figure 2-2 introduces the internal functional blocks of the PAM and PDM chips. Communication between the two chips is mediated by two Internal Bus Interface Units (IBIUs) that are transparent to user operations and not shown in the diagram.

In addition to the internal registers and the IBIUs, the functional modules within the WD9500-SET1 are as follows:

Within the **PAM**:

- **CIU:** CPU Interface Unit
- **GP:** Graphics Processor
- **MIC:** Memory Interface Controller

Within the **PDM**:

- **DP:** Data Processor
- **DSP:** Display Processor

The **CIU** controls communication with the system bus (via the CPU interface logic block external to the chip set), and passes data to and from all the other units on the chip set. It also performs certain miscellaneous functions, such as forwarding addresses from the system bus to the EPROM.

The **GP** performs the actual drawing computations. It supports all 8514/A graphics modes plus Western Digital extensions. The modes include line drawing, area fill area outline drawing (arbitrary polygons), rectangle drawing, image transfer from the CPU, BITBLT copying (Bit Block Transfer within VRAM), and scissoring. The GP receives its drawing instructions form the CIU and sends the resulting pixel coordinates to the MIC.

The **MIC** controls VRAM addressing and access. In a typical drawing operation, it converts the DP supplied pixel coordinates into VRAM addresses, causes the VRAM to send the addressed data (pixel color values) to the DP for modification, and then rewrites them back into VRAM. When not involved in a drawing or special-purpose access, the MIC manages the VRAM addressing portion of the constantly on-going screen refresh process. The MIC gives screen refresh the highest priority for VRAM access; next is timer-based VRAM chip refresh. DP-requested drawing access has the lowest priority.

The **DP** is responsible for updating VRAM in support of drawing and data transfer operations and altering pixel data (color values) according to masks and parameters, including "mix" specifications supplied in shared internal registers by the DP and GP. The DP receives pixel data on a bidirectional bus from the VRAM, modifies it, and then writes it back to the VRAM on the same bus.

The **DSP** manages the DAC and monitor, coordinating its role in the screen refresh process with the MIC. With an integrated back-end VRAM design, the DSP serializes and multiplexes pixel data ("pumped" out of VRAM by the MIC) to the DAC in synchronization with the timing of the monitor's sweep across the display screen. (With external back-end support, this DSP function is assumed by external logic within the VRAM block and the DAC).

2.2 BOARD OPERATION OVERVIEW

The functions of any WD9500-SET1 based board, as well as those of the IBM 8514/A, can be summarized as follows:

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Screen refresh: A key function is driving the display monitor. The board reads the data representation of the screen image from VRAM and then converts the data, pixel by pixel, into RGB signals for the display monitor which are synchronized with the sweeping of the monitor's RGB guns across its screen.

Drawing: The other major board function, less time-critical then screen refresh, is the generation of new lines and areas within VRAM in response to commands from the system CPU. In this context, "drawing" includes filling polygon shapes with patterns, establishing boundaries for "scissoring" (clipping), and similar operations. Drawing operations can involve complex algorithms, and they require correspondingly sophisticated processing by the WD9500-SET1.

Image transfer: In most graphics work, it is common to save board-drawn images (e.g. pop-up menus) elsewhere in the main system memory and/or on disk for later restoration to on-board video memory and hence to the display screen.

VGA input: The host CPU may request that the monitor be driven by the VGA (Video Graphics Array), a similar but less sophisticated graphics facility. In this case the WD9500-SET1 based board (or the 8514/A) essentially becomes a pass-through channel, taking video data and sync signals from the "auxiliary video extension" bus connector. Note that another monitor can be attached directly to the VGA. If the WD9500-SET1 based board (or 8514/A) is not in pass-through mode, then the two monitors can simultaneously display different images.

Palette loading: Pixel color interpretation is mediated by a small "palette" memory in the video DAC on the board. The CPU can very rapidly effect changes on the screen by changing the contents of this memory, as distinct from issuing drawing commands.

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
62-69, 71-82	A0-A19	I	CPU address bits 0 through 19
85	AUP	I	Decoding of upper CPU address bits 23-20, plus MADE24; all these should be 0 if the lower 20 bits of address are to be considered valid for the WD9500 based board.
57	M/$\overline{IO}$	I	Distinguishes memory access from I/O access
59	$\overline{S0}$	I	Status Bit 0
58	$\overline{S1}$	I	Status Bit 1
61	$\overline{ADL}$	I	Address Latch
60	$\overline{CMD}$	I	Command
56	$\overline{SBHE}$	I	System Byte High Enable
52	RESET	I	Channel Reset
86	$\overline{CDSETUP}$	I	Card Setup
90	CD CHRDY	O	Channel Ready
88	$\overline{IRQ}$	O	Interrupt Request; tied to Micro Channel IRQ 9
89	$\overline{CD\ SFFBK}$	O	Card Selected Feedback
55	$\overline{CD\ DS16}$	O	Card Data Size 16
91	$\overline{DBEN}$	O	Data Bus Enable
94-98, 100-110	D0-D15	I/O	CPU Data Bus Bits 0 through 16
92	DBDIR	O	Data Bus Direction (high for CPU read, low for CPU write)

TABLE 3-1. CPU INTERFACE PINS (PAM) FOR MICRO CHANNEL

EPROM access: The board includes a small EPROM containing a BIOS extension available to the CPU. The EPROM is mainly for initialization and diagnostic testing during power up. (Note that a portion of the EPROM contains certain board configuration information read by the WD9500-SET1 upon power up.)

Other: Finally, the board design must provide for customary CPU handshaking, interrupts, and miscellaneous bus interface signals.

3.0 WD9500 INTERFACES

3.1 CPU INTERFACE

The PAM provides interface pins to connect to either the IBM PS/2 Micro Channel or the AT bus via a small amount of external logic as illustrated in Figures 2-1 and 2-2. The CIO configures itself for one of the two different interfaces according to the value of the configuration strapping pin described later in this chapter (Table 3-12).

Because of the two possible external environments, most of these CPU interface pins have two alternate interpretations, as shown in the following tables. In both cases, however, the names and uses of most of these pins correspond precisely to the IBM specifications for the Micro Channel or AT bus and so do not need special explanation.

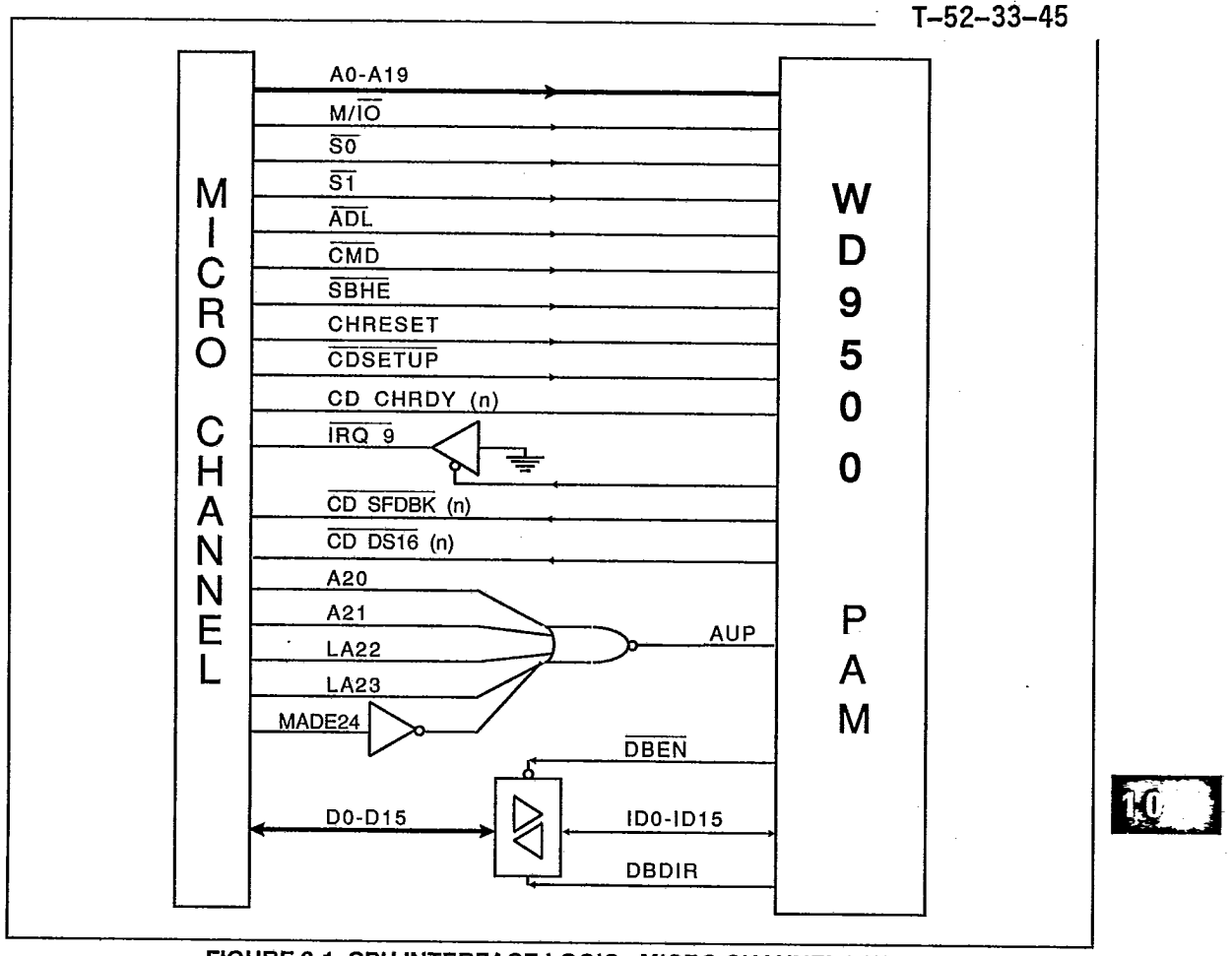

FIGURE 3-1. CPU INTERFACE LOGIC - MICRO CHANNEL BUS

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
62-69, 71-82	SA0-SA19	I	CPU address bits 0 through 19
85	AUP	I	Decoding of upper CPU address bits 23-20, plus MADE24; all these should be 0 if the lower 20 bits of address are to be considered valid for the WD9500 based board.
56	$\overline{\text{SBHE}}$	I	System Byte High Enable
57	$\overline{\text{MEMR}}$	I	Memory Read
59	$\overline{\text{MEMW}}$	I	Memory Write
58	$\overline{\text{IOR}}$	I	I/O Read
60	$\overline{\text{IOW}}$	I	I/O Write
61	BALE	I	Buffered Address Latch Enable
86	$\overline{\text{AEN}}$	I	Address Enable
52	RESET	I	System Reset
88	$\overline{\text{IRQ}}$	O	Interrupt Request; tied to any AT bus interrupt
55	$\overline{\text{CD CS16}}$	O	I/O 16-bit Chip Select
91	$\overline{\text{DBEN}}$	O	Data Bus Enable
94-98, 100-110	SD0-SD15	I/O	CPU Data Bus Bits 0 through 16
92	DBDIR	O	Data Bus Direction (high for CPU read, low for CPU write)
84	ATCLK	I	AT Bus Clock

TABLE 3-2. CPU INTERFACE PINS (PAM) FOR AT BUS

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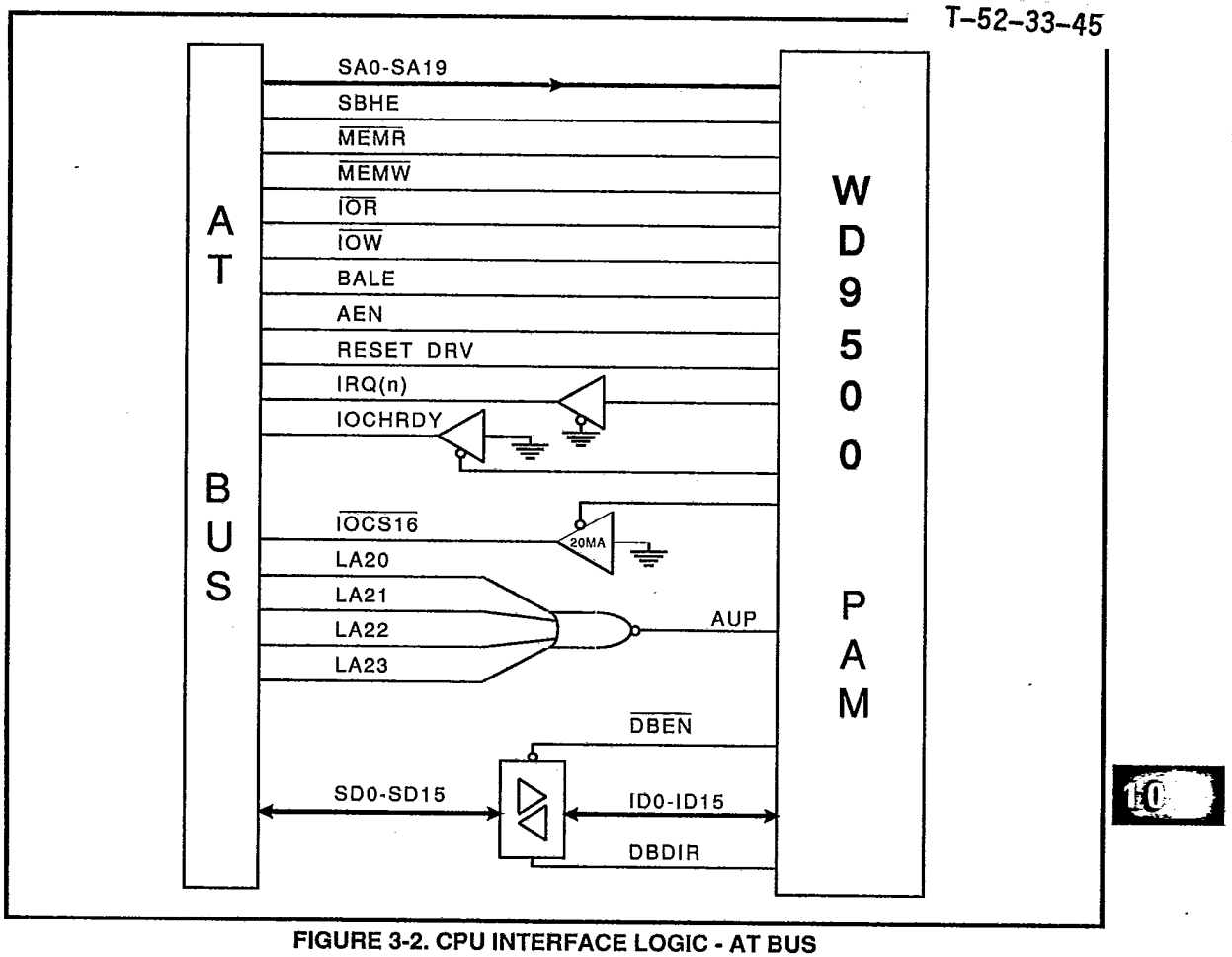

FIGURE 3-2. CPU INTERFACE LOGIC - AT BUS

I/E*	NUMBER OF CHIPS	PIXEL RESOLUTION	PIXEL DEPTH	NUMBER OF SCREEN PAGES	S/W**
I	4	1024x768	4	1	S
		640x480	4	2	S
	8	1024x768	8	1	S
		1024x768	4	2	W
		640x480	8	1	S
	16	1024x768	8	2	W
		1024x768	4	2	W
		640x480	8	2	W
E	8	1280X1024	4	1	W
		1024x768	8	1	S
		1024x768	4	2	W
		640x480	8	1	S
	16	1280x1024	8	1	W
		1024x768	8	2	W
		1024x768	4	2	W
		640x480	8	2	W

*I = Integrated Back-end Support

E = External Back-end Support

**S = Standard capability within 8514/A emulation

TABLE 3-3. VRAM PARAMETERS

3.2 VRAM DESIGN AND INTERFACE

The WD9500-SET1 supports two VRAM designs. Each of these in turn can be implemented with two or three levels of chip population for a total of five implementations. The design choice depends on the desired combination of the following criteria (with only certain combinations possible):

- Pixel resolution: 640x480, 1024x768, 1280x1024.
- Pixel depth: 4 or 8 bits per pixel.
- Number of screen pages: one or two.
- Number of VRAM chips (and hence board size).
- Field upgradeability.
- Type of design: with back-end (serializing and multiplexing of pixel data for screen refresh) integrated within the WD9500-SET1 or with external back-end support.
- External back-end support: includes the use of a more sophisticated DAC and is required to achieve a 1280x1024 resolution.

3.2.1 INTEGRATED BACK-END VRAM DESIGN

The capabilities of the various VRAM designs, with their several levels of chip population, are shown in Table 3-3. Note that, although not shown, each level of chip loading for a given design includes the capabilities of the smaller chip population(s).

If maximum IBM 8514/A resolution is desired, the design should be implemented to at least the 8-chip level; implementation at the 16-chip level provides for the extended capability of doubling the number of screen pages supported by the

PIN NUMBER	PIN SYMBOL	DESCRIPTION
19, 16-10	MA7-MA0	Low order address lines, into all quads.
34	LA13	Used as high-order address bit (MA8) for quads Q1, Q3, and their counterparts, in all designs.
35	LA24	Used as high-order address bit (MA8) for quads Q2, Q4, and their counterparts, in all designs.
22	$\overline{RAS0}$	Row Address Strobe 0 (Quads 1 & 2)
23	$\overline{RAS1}$	Row Address Strobe 1 (Quads 3 & 4)
20	$\overline{CAS12}$	Column Address Strobe 1 (Quads 1 & 2)
21	$\overline{CAS34}$	Column Address Strobe (Quads 3 & 4)
31-24	WE7-WE0	Pixel data Write Enable lines to enable writing into VRAM on the PD bus (bidirectional Parallel Data bus, between VRAM and DP; A given quad receives either WE0-3 or WE4-7.
32	$\overline{DT/OE}$	Transfer cycle control and serial data output enable, used by all quads.

TABLE 3-4. PAM PIN INTERFACE TO VRAM

8-chip version. See Appendix B for an illustration of the 16-chip version with indications of which chips should be left unpopulated if field upgradeable 4-chip and/or 16-chip versions are to be produced. The same diagram can also serve as the basis for an 8-chip design, with half of those chips omitted for future field upgrade if desired.

See Appendix B for a VRAM to PAM/PDM connection drawing. Tables 3-4 and 3-5 show the PAM and PDM pins used to form the VRAM interface. All the Pins in Table 3-4 drive control signals generated by the MIC.

The Data Processor module (DP) manages the PD Pixel Data bus. The Display Processor (DSP) manages all other pins listed in Table 3-5.

WE0-3 represent pixel positions 0-3, respectively. In turbo mode, WE4-7 represent positions 4-7. For x8 mode, WE4-7 are the same as WE0-3.

In the VRAM design diagrams (see Appendix B), the PD lines connect to the parallel data ports of the VRAM chips, while the SD lines connect to their serial data ports.

The different resolution modes require different memory addressing schemes to configure the display memory properly for screen pixel position.

3.2.2 EXTERNAL BACK-END VRAM DESIGN

See Appendix B (Figuare B-3) for an illustration of the 16-chip version with external back-end support. A Brooktree 8-bit video DAC BT458 is used.

3.3 VIDEO DAC AND INTERFACE SUB-SYSTEM

This section includes the following information for the board designer:

Routing of VRAM pixel data to the DAC. This involves two alternative designs, depending on whether back-end support is performed by the WD9500-SET1 or by external components.

Routing of control information from the WD9500-SET1 to the DAC and the monitor.

Signal routing in support of VGA modes. In the system VGA, the off-board control and data signals that drive the monitor are passed through to the monitor from the auxiliary extension connector.

Palette access. Palette access offers the option of implementing a "flicker-free mode", a Western Digital extension.

PIN NUMBER	PIN SYMBOL	DESCRIPTION
90-93, 95-98, 100-114, 117-125	PD31-PD0	Parallel Data bus connecting the DP module to the VRAM block; data is bidirectional. (This is the path through which the DP first reads, then rewrites pixels in support of drawing operations).
46-49, 52-67, 71-82	SD31-SD0	Serial Data bus, in VRAM designs with integrated back-end support, this is the path by which screen refresh data is extracted (by a transfer cycle) from the serial ports of the VRAM chips and then moved to the DSP module for serializing and multiplexing before being sent to the DAC. In VRAM designs with external back-end support, the serial data bus to the DSP is not used; instead, the DSP reconfigures itself to use some of these pins (SD0, SD1, SD4, SD5, SD6) as output drivers for additional control signals to the VRAM (see External Back-End VRAM Design).
87,85,86,84	SE12A, SE34A, SE12B, SE34B	Serial Data Output Enable T-52-33-45
88	SC13	Serial Data Clock 1
89	SC24	Serial Data Clock 2
The following pins are changed for external back-end support:		
82	SC3 (SD0)	Serial Data Clock 3
81	SC2(SD1)	Serial Data Clock 4
78	SEL0(SD4)	Mux Select 0
77	SEL1(SD5)	Mux Select 1

TABLE 3-5. PDM PIN INTERFACE TO VRAM

Note that a related topic, WD9500-SET1 recognition of monitor type, is grouped with other configuration strapping issues and is discussed later. (See section 3.4.3)

The PDM pins associated with the video interface subsystem are all outputs from the DSP, and are shown in Table 3-6.

Appendix C describes board implementation of the video DAC and interface subsystem with integrated and external back-end support. The flicker-free option applies to both and is discussed later. The WD9500-SET1 chip set supports INMOS IMS G171/176/178, Brooktree BT471/478 and compatible video DACs for 8514/A modes. It also supports Brooktree BT451/458 and compatible DACs for Western Digital enhanced 1280x1024 mode. The Brooktree BT471 DACs include a 256x18 palette, loaded with six-bit R, G, and B color intensity values. (The high two bits of the 8-bit data lines supplying these values are ignored.) The BT478 offers a 256x24 palette with all eight bits used for finer control of color. The DAC8 pin from the PAM can be used to select 6-bit or 8-bit palette fields. Note that the palette overlay capabilities are not used: the DAC's RS2 and OL0-OL3 pins should be tied down. Without the flicker-free option, CPU software writes data into the DAC's color palette on the low eight bits of the system CPU data bus. The WD9500-SET1 intercepts CPU addressing and controls DAC access using the low two bits of its EPROM address bus, BIOSA1 and BIOSA0. When the flicker-free option is incorporated into the board design, as

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
30-27, 24-21	VDATA0-7	O	With integrated back-end support, these pins output the video data for the DAC. With external back-end support, they are not used for this purpose, since the DAC receives its data from the external logic within the VRAM block. In both cases, however, these same pins are the source of palette-loading data in flicker-free mode. (tri-state output)
132	SELVD	O	With the flicker-free design option, this pin selects the source of palette-loading data to be either the low eight bits of the PC data bus (normal mode) or VDATA0-7 (flicker-free mode). SELVD is also the tri-state control signal for $\overline{\text{DACRD}}$ and $\overline{\text{DACWR}}$ from the PAM. When high, PAM $\overline{\text{DACRD}}$ and $\overline{\text{DACWR}}$ signals are disabled.
25	VCLK	O	Video clock for the DAC (tri-state output)
20	BLANK	O	Video blank signal for the DAC (tri-state output)
31	$\overline{\text{DACRD}}$	O	DAC palette read. Note that data read from the palette is always routed to the PC data bus in the CPU interface logic.
32	$\overline{\text{DACWR}}$	O	DAC palette write (see SELVD above)
33	HSYNC	O	Horizontal sync to the monitor (tri-state output).
34	VSYNC	O	Vertical sync to the monitor (tri-state output)
42	$\overline{\text{ENVGA}}$	O	VGA pass-through mode: This signal selects the source of video data to the DAC (either VDATA0-7 from the PDM or P0-7 from the auxiliary video extension). It also selects the control signals to the DAC (either VCLK and BLANK from the PDM, or HSYNC and VSYNC from the PDM, or HSYNC and VSYNC from the auxiliary video extension).
76	LDCLK	O	External back-end support: This output signal drives the LD (load) input of the BT458/451 DAC, where it synchronizes the serialization of the 32 bits of pixel data from the VRAM into four 8-bit pixel color selections. With integrated back-end support this pin is SD6 of the serial data bus from VRAM.

TABLE 3-6. PDM PIN INTERFACE TO VIDEO SUBSYSTEM

PIN NUMBER	PIN SYMBOL	I/O	DESCRIPTION
54, 53, 49-37	BSA0-BSA14	O	EPROM BIOS address lines
36	$\overline{\text{BSOE}}$	O	$\overline{\text{EPROM BIOS}}$ output enable

TABLE 3-7. EPROM INTERFACE PINS

	MICRO CHANNEL	AT BUS	
		IAD5 = 0*	IAD5 = 1*
2K (Fixed)	C6800-C6FFF	C8800-C8FFF	D8800-D8FFF
4K (Bank Selectable)	C7000-C7FFF	C9000-C9FFF	D9000-D9FFF
2K (Fixed)	CA000-CA7FFF	N/A	N/A

TABLE 3-8. BIOS EPROM ADDRESS MAPPING

shown in Appendix C, the CPU software can invoke the flicker-free mode. In this mode, palette data is buffered by the WD9500-SET1 and released to the DAC over the VDATA0-7 lines, with the SELD control signal activated to select the VDATA lines in preference to the system data bus. Routing of the latter lines to the DAC via the SELD multiplexer is still required, both to allow for a non flicker-free mode (8514/A emulation) and for palette reads.

Appendix C shows the implementation of 1280x1024 resolution with external back-end support and two DACs. The fast DAC BT451/458 is used for 1280x1024 and 1024x768 resolutions. The slower DAC BT471/478 is used for VGA pass-through. The flicker-free capabilities do not apply to DAC BT471/478.

3.4 OTHER BOARD DESIGN ELEMENTS

3.4.1 EPROM

A 27256 32K UV EPROM is used on the Micro Channel board to store the Western Digital BIOS extension plus two configuration parameters that the WD9500-SET1 loads into internal registers upon board reset. These configuration parameters are the POS ID (for PS/2 Micro Channel system integration) chosen by the customer, and a VRAM wait-state control parameter. The VRAM wait-state control parameter is dependant upon characteristics of the VRAM chips chosen for the board and the manner in which the configuration parameter pins are strapped (four configuration choices are possible). See Appendix D.

The EPROM is remapped for the AT bus board because of VGA conflict and widespread use of Shadow RAM in 80386 machines. BIOS EPROM Address mapping for WD9500-SET1 chip set is as presented in Table 3-7.

For PC/AT and compatibles, two sets of addresses minimize memory conflict with other products (C8800-C9FFF or D8800-D9FFF). Either address can be selected by a jumper in a board design.

The EPROM is accessed through the CIU on the PAM, which generates addressing for the EPROM and activates an output enable line. Data from the EPROM ties to both the CIU and the system data bus through an 8-bit connection to the internal data bus. (See Figures 2-1 and 2-2). The PAM pins involved are shown in Table 3-8.

3.4.2 PAM-PDM INTERFACE

The PAM and PDM are connected to each other through a 22-pin interface. Both chips include an internal bus interface unit (IBIU) which controls inter-chip communication. One of its functions is to buffer data transfers larger than eight bits, since the general purpose inter-chip bus is eight-bits wide due to pin count constraints. Inter-chip communication is transparent to the user. See Table 3-9.

PAM PIN NUMBER	SIGNAL DIRECTION	PDM PIN NUMBER	PIN SYMBOL
PAM 125-132	↔	PDM 9-2	IAD0-7
PAM 124	→	PDM 10	IADSTAT
PAM 8	→	PDM 126	RWCAS
PAM 123	→	PDM 11	RD/WR
PAM 122	→	PDM 12	AS
PAM 121	→	PDM 13	DS
PAM 114	←	PDM 19	RMWE
PAM 2	←	PDM 132	SELVD
PAM 119	←	PDM 15	SLC
PAM 118	←	PDM 16	SLD
PAM 6	→	PDM 128	WROE
PAM 3	→	PDM 131	MDT0
PAM 4	→	PDM 130	MDT1
PAM 5	→	PDM 129	MDT2

TABLE 3-9. INTERCHIP INTERFACE PINS

3.4.3 CONFIGURATION STRAPPING

The WD9500-SET1 configures itself to its board design environment by latching the values of certain strapped input pins on the rising edge of the CPU's RESET signal. (It also reads two parameters from the EPROM, as mentioned earlier). One of these pins, which distinguishes between the Micro Channel and PC/AT bus CPU interfaces, is dedicated to this purpose. Three other dedicated pins receive monitor type information. The remaining pins, which all deal with VRAM configuration information, are actually part of the inter-chip communication interface; the strapped values are driven to the inter-chip lines through tri-state buffers. See Tables 3-10 through 3-13.

Note: If a field-upgradeable VRAM design is selected (with the VRAM chips partially populated), the appropriate strappings should be implemented with jumpers, switches or some other method that allows the user to change the strapped values in the course of field upgrade.

3.4.4 CLOCK CONSIDERATIONS

A major design element of the WD9500-SET1 is the provision for two separate and independent clock rates; one for drawing operations, the other for screen refresh. In particular, faster monitors can be used without changing the clock rate of the drawing facilities within the WD9500-SET1, and conversely, use of slower monitors will not degrade drawing speed.

The system clock signal, provided by an external 60MHz oscillator, drives the drawing process within the WD9500-SET1, and is used to generate VRAM timing. The pixel clock, used to drive the screen refresh process, is selected from among eight oscillator outputs to accommodate different types of monitors. Three PDM output signals, CLKSEL2, CLKSEL1, and CLKSEL0, are provided to make the selection.

In the United States, non-interlaced video monitors use a vertical refresh frequency of 60Hz; in Europe, the standard is 70Hz. Table 3-14 shows the "Pixel Frequency" as the frequency of the oscillator selected by CLKSEL2, CLKSEL1, and CLKSEL0 which is the input to the PDM's PCLK pin. Table 3-14 also includes the interlaced IBM 8514 monitor (vertical frequency 43.48Hz).

The typical WD9500-SET1 board is therefore configured with oscillators at 25.28, 44.90 and 64.37 MHz for use with U.S. standard monitors, or with oscillators at 31.40, 44.90, and 74.16 MHz for use

PAM PIN NUMBER	PDM PIN NUMBER	PIN SYMBOL	DESCRIPTION
120		MC/$\overline{AT}$	High if Micro Channel; low if PC/AT bus.
	36-38	MID2-MID0	Monitor ID Bits 2-0.
130	3	IAD5	EPROM location for AT bus design (not used in Micro Channel); low for EPROM memory address at C8800H-C9FFFH, high for address at D8800H-D9FFFH.
131	3	IAD6	Test Mode. Low for test mode; high for normal operation.
132	2	IAD7	DAC Type. Low for 6-bit DAC; high for 8-bit DAC.
129	5	IAD4	VRAM Chip Speed. Low for -8 spec; high for -10 spec.
128	6	IAD3	External Back-End. This pin specifies the maximum resolution allowed by VRAM design: low for 1280 x 1024 resolution (external back-end required), high for 1024 x 768 (internal back-end)
125	9	IAD0	VRAM Chip Type. Must be tied high.
126	8	IAD1	Chip Count 0. Low order bit of 2-bit VRAM chip count field (see below)
127	7	IAD2	Chip Count 1. High order bit of 2-bit VRAM chip count field (see below).
122	12	$\overline{AS}$	Monitor Type 0 (see below)
123	11	RD/WR	Monitor Type 1 (see below)

TABLE 3-10. CONFIGURATION STRAPPING PINS

	Chip Count 1	Chip Count 0
4 Chips	0	0
8 Chips	0	1
16 Chips	1	0
Reserved	1	1

TABLE 3-11. CHIP COUNT STRAPPING

Type of Monitor	Monitor Type 0	Monitor Type 1
8514 Display	0	0
60 Hz monitor	0	1
Reserved	1	0
70 Hz monitor	1	1

TABLE 3-12. MONITOR SELECTION

with European standard monitors. A more ambitious design might include all seven clock frequencies, with the MID2-MID0 inputs (as per "Configuration Strapping" earlier in this chapter) aiding in the selection.

The WD9500-SET1 pins involved in clock signal generation and use are summarized in Table 3-14.

MID2	MID1	MID0	MONITOR TYPE
0	0	0	Not Defined
0	0	1	Not Defined
0	1	0	IBM 8514 (color monitor, 1024 x 768 interlaced)
0	1	1	Not defined
1	0	0	Not defined
1	0	1	IBM 8503 (monochrome, 640 x 480, non-interlaced)
1	1	0	IBM 8513 (color, 640 x 480, non-interlaced & 8514
1	1	1	Other display*

Note: MID2-0 have internal pull-up resistors. During reset, MID2-0 can also be used to test PDM internal counters. For in-circuit board test, MID2-0 should be high when REST is asserted.

TABLE 3-13. MONITOR ID INTERPRETATION

CLKSEL			RESOLUTION*	VERTICAL FREQUENCY	HORIZONTAL FREQUENCY	PIXEL FREQUENCY
2	1	0				
0	0	0	640 X 480N	60 Hz	31.47 KHz	25.18 MHz
1	0	0	640 X 480N	70 Hz	37.28 KHz	31.32 MHz
0	0	1	1024 X 768I	43.48 Hz	35.52 KHz	44.90 MHz
1	0	1	1280 X 1024N	60 Hz	63.78 KHz	109.64 MHz**
0	1	0	1280 X 1024N	70 Hz	74.83 KHz	136.71 MHz**
0	1	1	1024 X 768N	60 Hz	49.06 KHz	63.98 MHz
1	1	1	1024 X 768N	70 Hz	56.17 KHz	74.16 MHz

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*N = Non-interlaced

I = Interlaced

** In these cases the oscillator frequency must be halved (to 54.82 MHz or 68.36 MHz) before being connected to the PCLK input pin of the PDM. Since this resolution requires external back-end support, however, the original frequency, as shown, must remain intact to drive the BT451/458 DAC clock.

TABLE 3-14. PIXEL CLOCK FREQUENCY DERIVATION

NAME	PAM/PDM PIN#	I/O	DESCRIPTION
SCLK	PAM 113/PDM 39	I	System clock input; requires 60 MHz
CLKSEL2	PDM 43	O	Selects from seven frequencies for PCLK (see Table 3-14)
CLKSEL1	PDM 44	O	See Table 3-14
CLKSEL0	PDM 45	O	See Table 3-14
PCLK	PDM 68	I	Pixel clock input
VCLK	PDM 25	O	DAC clock source
LDCLK (SD6)	PDM 76	O	LD signal for BT451/458 DAC for external back-end support

TABLE 3-15. CLOCK PIN SUMMARY

4.0 ABSOLUTE MAXIMUM RATINGS AND DC CHARACTERISTICS

PAM ELECTRICAL SPECIFICATIONS			
PAM AC Specifications			
CLK period: 16 ns minimum, 16.7 ns typical.			
CLK rise and fall time (0.4 v to 2.4 v): 2.5 ns maximum			
All outputs rise and fall time (10% to 90%): t.b.d.			
Input capacitance: 10 pF maximum			
PAM DC SPECIFICATIONS			
Absolute maximum ratings:			
Voltages on all inputs and outputs with respect to GND		-0.3 V to 7.0 V	
Operating ambient temperature		$0^{\circ}C \leq TA \leq 65^{\circ} C$	
Storage temperature		$-65^{\circ}C$ to $150^{\circ}C$	
DC Characteristics:			
	Minimum	Maximum	**Unit**
Supply voltage (VCC)	4.75	5.25	Volts
Input low voltage (VIL)	-0.3	0.8	Volts
Input high voltage (VIH)	2.0	VCC	Volts
Output low voltage (VOL)		0.4	Volts
Output high voltagae (VOH)	2.4		
Input leakage current (ILI)		± 10	µA*
Tri-state output leakage current (IOL)		± 10	µA**
Power supply current (ICC)		t.b.d.	mA

*VIN = 0 to VCC
**VOUT = 0.4V to VCC

Note: All inputs have static charge and latch up protection circuits. All inputs, including bi-directional pads, have 20K ohm pull-up resistors.

TABLE 4-1. PAM ELECTRICAL SPECIFICATIONS

SIGNAL NAME	I/O	IOL (Min) @0.4V	IOH (Min) @ 2.4V	Capacitive Loading
D15-0	I/O	1.0 mA	200 µA	75 pF
$\overline{\text{CDDS16}}$	O	2.0 mA	200 µA	250 pF
$\overline{\text{IRQ}}$	O	2.0 mA	200 µA	250 pF
CHRDY	O	2.0 mA	200 µA	250 pF
SFDBK	O	2.0 mA	200 µA	250 pF
$\overline{\text{BIOSOE}}$	O	1.0 mA	200 µA	50 pF
BIOSA14-0	O	1.0 mA	200 µA	50 pF
$\overline{\text{DBEN}}$	O	1.0 mA	200 µA	50 pF
DBDIR	O	1.0 mA	200 µA	50 pF
WROE	O	1.0 mA	200 µA	50 pF
$\overline{\text{DACWR}}$	O	1.0 mA	200 µA	100 pF
$\overline{\text{DACRD}}$	O	1.0 mA	200 µA	100 pF
DAC8	O	0.5 mA	200 µA	50 pF
$\overline{\text{RWCAS}}$	O	1.0 mA	200 µA	50 pF
IADSTAT	O	1.0 mA	200 µA	50 pF
IAD7-0	I/O	1.0 mA	200 µA	50 pF
RD/$\overline{\text{WR}}$	O	1.0 mA	200 µA	50 pF
$\overline{\text{AS}}$	O	1.0 mA	200 µA	50 pF
$\overline{\text{DS}}$	O	1.0 mA	200 µA	50 pF
SWAP	O	1.0 mA	200 µA	50 pF
MDT2-0	O	1.0 mA	200 µA	50 pF
MA7-0	O	1.0 mA	200 µA	130 pF
LA13	O	1.0 mA	200 µA	80 pF
LA24	O	1.0 mA	200 µA	80 pF
LA24	O	1.0 mA	200 µA	100 pF
$\overline{\text{RAS1}}$	O	1.0 mA	200 µA	100 pF
$\overline{\text{RAS0}}$	O	1.0 mA	200 µA	100 pF
$\overline{\text{CAS12}}$	O	1.0 mA	200 µA	100 pF
$\overline{\text{CAS34}}$	O	1.0 mA	200 µA	100 pF
WE7-0	O	1.0 mA	200 µA	50 pF
$\overline{\text{DTOE}}$	O	1.0 mA	200 µA	160 pF

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TABLE 4-2. PAM OUTPUT SPECIFICATIONS

PDM ELECTRICAL SPECIFICATIONS

PAM AC Specifications

SCLK period: 16 ns minimum, 16.7 ns typical.

PCLK PERIOD: 13.5 ns minimum; 15.4 or 22.2 ns typical.

All outputs rise and fall time (10% to 90%): t.b.d.

Input capacitance: 10 pF maximum

PDM DC SPECIFICATIONS

Absolute maximum ratings:

Voltages on all inputs and outputs with respect to GND	-0.3 V to 7.0 V
Operating ambient temperature	$0^{\circ}C \leq TA \leq 65^{\circ}$ C
Storage temperature	$-65^{\circ}C$ to $150^{\circ}C$

DC Characteristics

	Minimum	Maximum	**Unit**
Supply voltage (VCC)	4.75	5.25	Volts
Input low voltage (VIL)	-0.3	0.8	Volts
Input high voltage (VIH)	2.0	VCC	Volts
Output low voltage (VOL)		0.4	Volts
Output high voltagae (VOH)	2.4		
Input leakage current (ILI)		± 10	µA*
Tri-state output leakage current (IOL)		± 10	µA**
Power supply current (ICC)		t.b.d.	mA

*VIN = 0 to VCC
**VOUT = 0.4V to VCC

Note: All inputs have static charge and latch up protection circuits. All inputs, including bi-directional pads, have 20K ohm pull-up resistors.

TABLE 4-3. PDM ELECTRICAL SPECIFICATIONS

SIGNAL NAME	I/O	IOL (Min) @0.4V	IOH (Min) @ 2.4V	Capacitive Loading
IAD7-IAD0	I/O	4.20 mA	200 µA	50
RMWE	O	1.00 mA	200 µA	50
SLC	O	4.20 mA	200 µA	50
SLD/TOUT	O	4.20 mA	200 µA	50
PD31-PD0	I/O	4.20 mA	200 µA	50
VCLK	O	4.20 mA	200 µA	30
HSYNC	O	4.20 mA	200 µA	50
VSYNC	O	4.20 mA	200 µA	70
BLANK	O	4.20 mA	200 µA	70
VDATA7-VDATA0	O	4.20 mA	200 µA	30
$\overline{\text{DACWR}}$ ($\overline{\text{DACWE}}$)	O	4.20 mA	200 µA	30
$\overline{\text{DACRD}}$ $\overline{\text{DACRD}}$)	O	4.20 mA	200 µA	50
SELVD	O	4.20 mA	200 µA	50
CLKSEL2-CLKSEL0	O	0.80	200 µA	50
$\overline{\text{ENVGA}}$	O	4.80 mA	200 µA	100
SE12A, SE34A, SE12B, SE34B	O	4.20 mA	200 µA	70
SC13, SC24	O	4.20 mA	200 µA	70
SD6, SD5	I/O	4.20 mA	200 µA	100

TABLE 4-4. PDM OUTPUT SPECIFICATIONS

5.0 AC TIMING CHARACTERISTICS

T-52-33-45

5.1 RESET INITIALIZATION TIMING

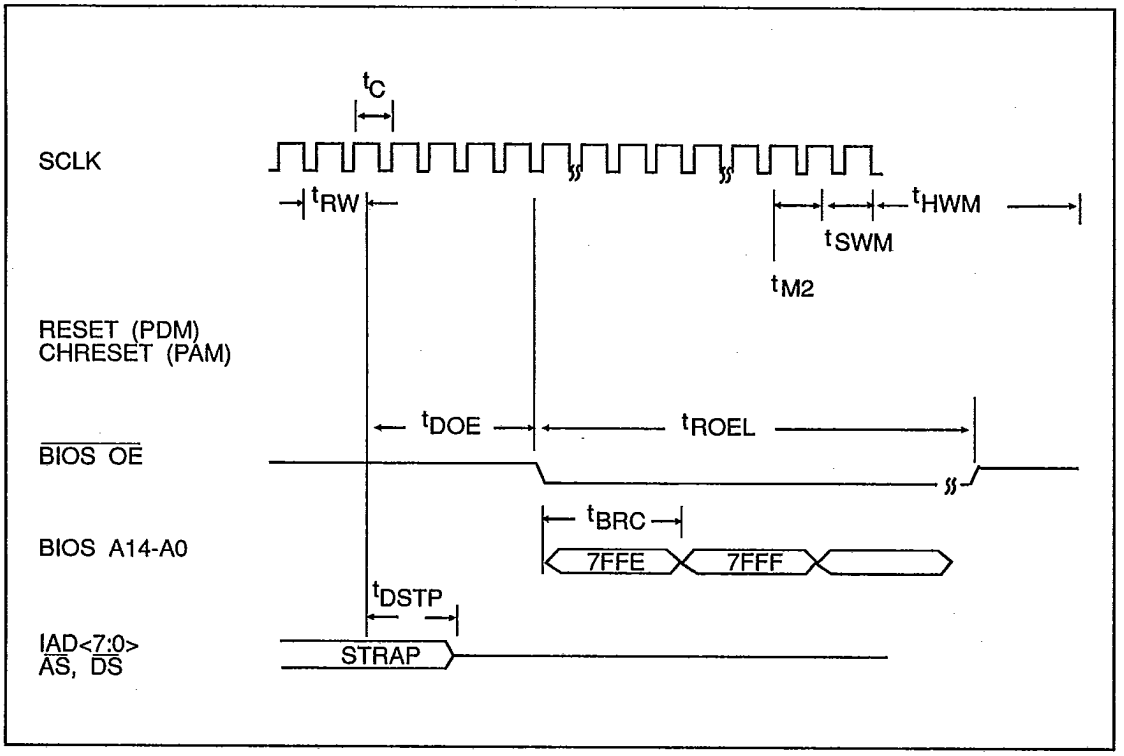

FIGURE 5-1. RESET INITIALIZATION TIMING

SYMBOL	TIMING PARAMETER	MINIMUM	MAXIMUM
t_{RW} *	Reset high period	$20t_c$	
t_{DOC} †	BIOS OE delay from falling edge of RESET	$40t_c$	
t_{DSTP} *	STRAP DATA valid after falling edge of RESET (hold time)	$4t_c$	
t_{ROEL} †	Initial BIOS OE low period after RESET	$115t_c$	
t_{BRC} †	Read cycle time after RESET	$25t_c$	

* Applies to both PAM and PDM
† Applies to PAM only

TABLE 5-1. RESET INITIALIZATION TIMING

5.2 MICRO CHANNEL INTERFACE TIMING

This section provides the critical timing parameters for the Micro Channel interface. Timing parameters related to PAM are listed separately.

5.2.1 SETUP CYCLE

T-52-33-45

The setup cycle occurs during system configuration following reset. CD SETUP is pulled low by writing to I/O port 96H. Then the Adapter ID is read from I/O registers 100H and 101H using default cycles. Finally, an asynchronous extended I/O write cycle is performed to 102H.

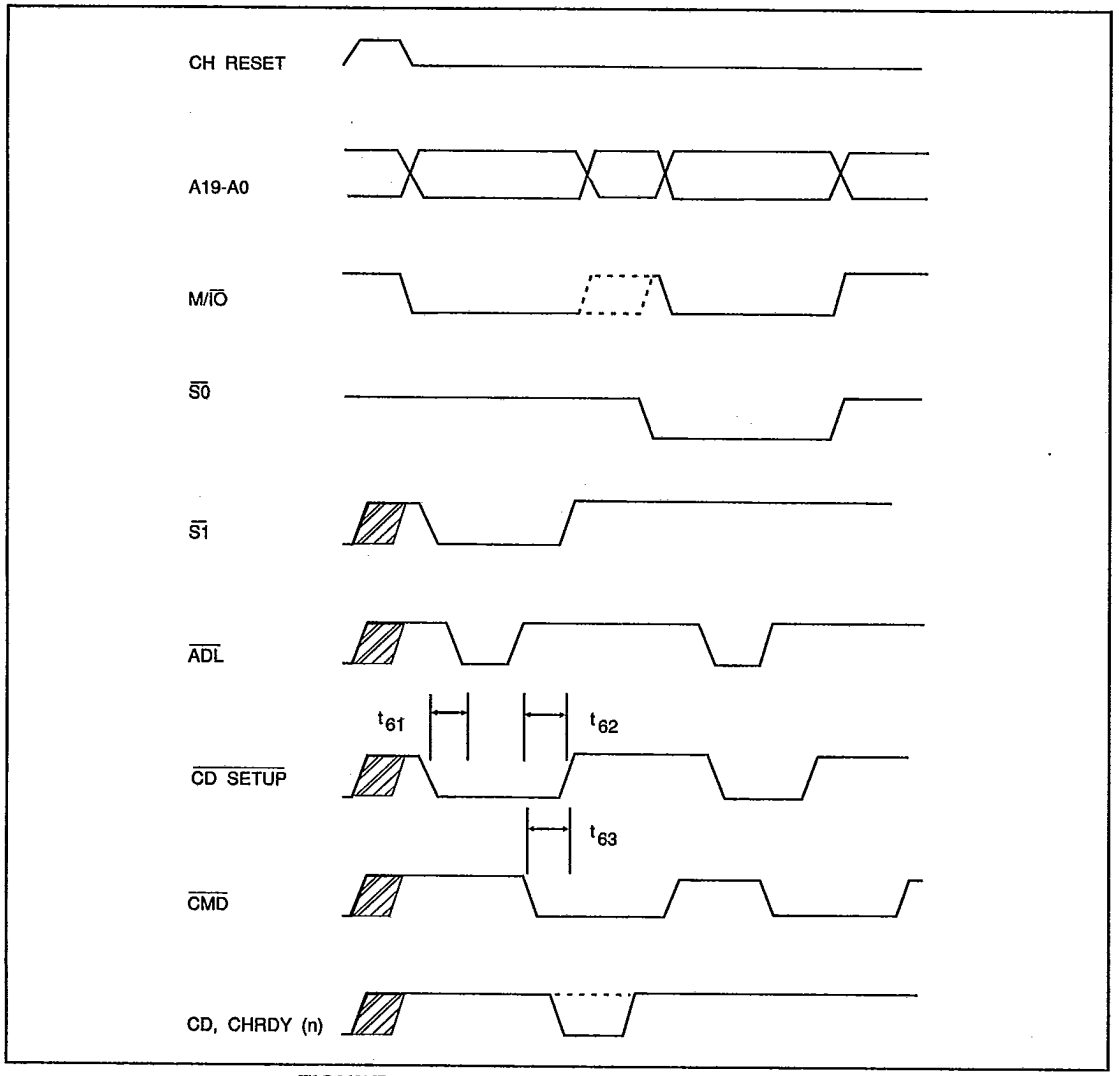

FIGURE 5-2. SETUP CYCLE TIMING DIAGRAM

TIMING PARAMETER	MINIMUM/MAXIMUM
t_{61} $\overline{\text{CD SETUP}}$ (n) active low to $\overline{\text{ADL}}$ active low	15/ nanoseconds
t_{62} $\overline{\text{CD SETUP}}$ (n) hold from $\overline{\text{ADL}}$ inactive high	25/ nanoseconds
t_{63} $\overline{\text{CD SETUP}}$ (n) hold from $\overline{\text{CMD}}$ active low	30/ nanoseconds

TABLE 5-2. SETUP CYCLE TIMING

5.2.2 DEFAULT CYCLE

T-52-33-45

Reading of POS registers and reading/writing of DAC registers are accomplished using this cycle.

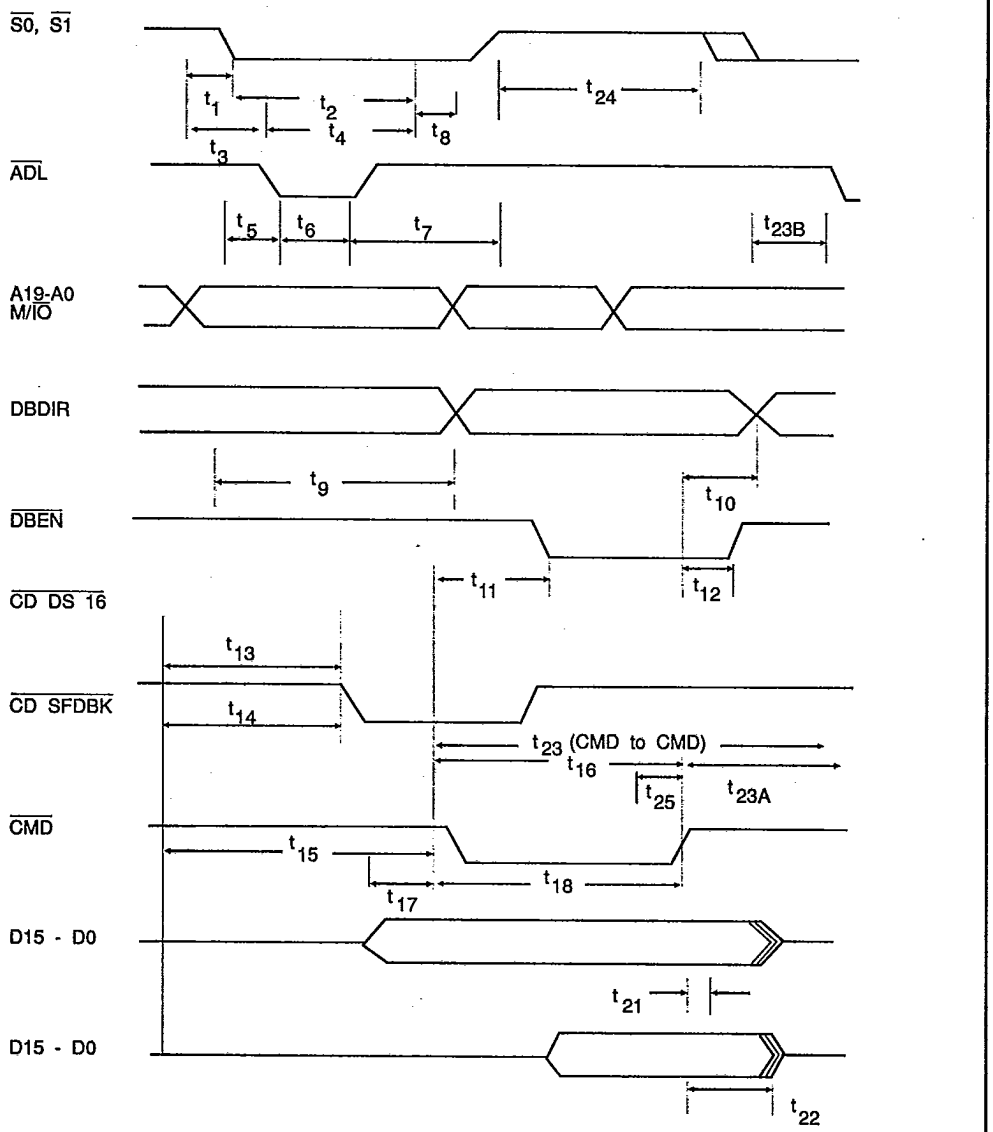

FIGURE 5-3. I/O DEFAULT CHANNEL TIMING

SYMBOL	TIMING PARAMETERS	MIN/MAX	PAM
t_1	Status active (low) from ADDRESS, M/$\overline{IO}$, valid	10/ -ns	
t_2	$\overline{CMD}$ active (low) from Status active (low)	55/ -ns	
t_3	$\overline{ADL}$ active (low) from ADDRESS, M/IO, valid	45/ -ns	
t_4	$\overline{ADL}$ active (low) to $\overline{CMD}$ active (low)	40/ -ns	
t_5	$\overline{ADL}$ active (low) from Status active (low)	12/ -ns	
t_6	$\overline{ADL}$ pulse width	40/ -ns	
t_7	Status hold from $\overline{ADL}$ inactive (high)	25/ -ns	
t_8	ADDRESS, M/$\overline{IO}$, hold from $\overline{ADL}$ inactive	15/ -ns	
t_9	DBDIR change from status active (low)	-/-	-/45 ns
t_{10}	DBDIR change from $\overline{CMD}$ high	-/-	-/40 ns
t_{11}	$\overline{DBEN}$ change from CMD (low)	-/-	-/35 ns
t_{12}	$\overline{DBEN}$ change from $\overline{CMD}$ high	-/-	-/30 ns
t_{13}	$\overline{CD\ DS\ 16}$ active (n) (low) from ADDRESS, M/$\overline{IO}$ valid	-/55 ns	
t_{14}	$\overline{CD\ SFDBK}$ active (low) from ADDRESS, M/$\overline{IO}$ valid	-/60 ns	
t_{15}	$\overline{CMD}$ active (low) from ADDRESS, valid	85/ -ns	
t_{16}	$\overline{CMD}$ pulse width	90/ -ns	
t_{17}	Write data setup to $\overline{CMD}$ active (low)	0/ -ns	
t_{18}	Write data hold from $\overline{CMD}$ inactive (high)	30/ -ns	
t_{21}	Read data hold from $\overline{CMD}$ inactive (high)	0/ -ns	
t_{22}	Read data bus tri-state from $\overline{CMD}$ inactive (high)	-/ 40 ns	
t_{23}	$\overline{CMD}$ active to next $\overline{CMD}$ active	190/ -ns	
t_{23A}	$\overline{CMD}$ inactive to next $\overline{CMD}$ active	80/ -ns	
t_{23B}	$\overline{CMD}$ inactive to next $\overline{ADL}$ active	40/ -ns	
t_{24}	Next Status active (low) from Status inactive	30/ -ns	
t_{25}	Next Status active (low) to $\overline{CMD}$ inactive	-/ 20 ns	

TABLE 5-3. I/O AND MEMORY DEFAULT CYCLE (200 NS MINIMUM)

5.2.3 ASYNCHRONOUS EXTENDED CYCLE (GENERAL CASE)

Access to all registers in the WD9500-SET1 or the BIOS EPROM use this cycle. An asynchronous extended cycle occurs when the chip set releases CD CHRDY asynchronously. The chip set provides the read data within the specified time for CD CHRDY release. The timing sequence is illustrated by Figure 5-4 which only shows the additional parameters to the default cycle. All other parameters are the same as the default cycle.

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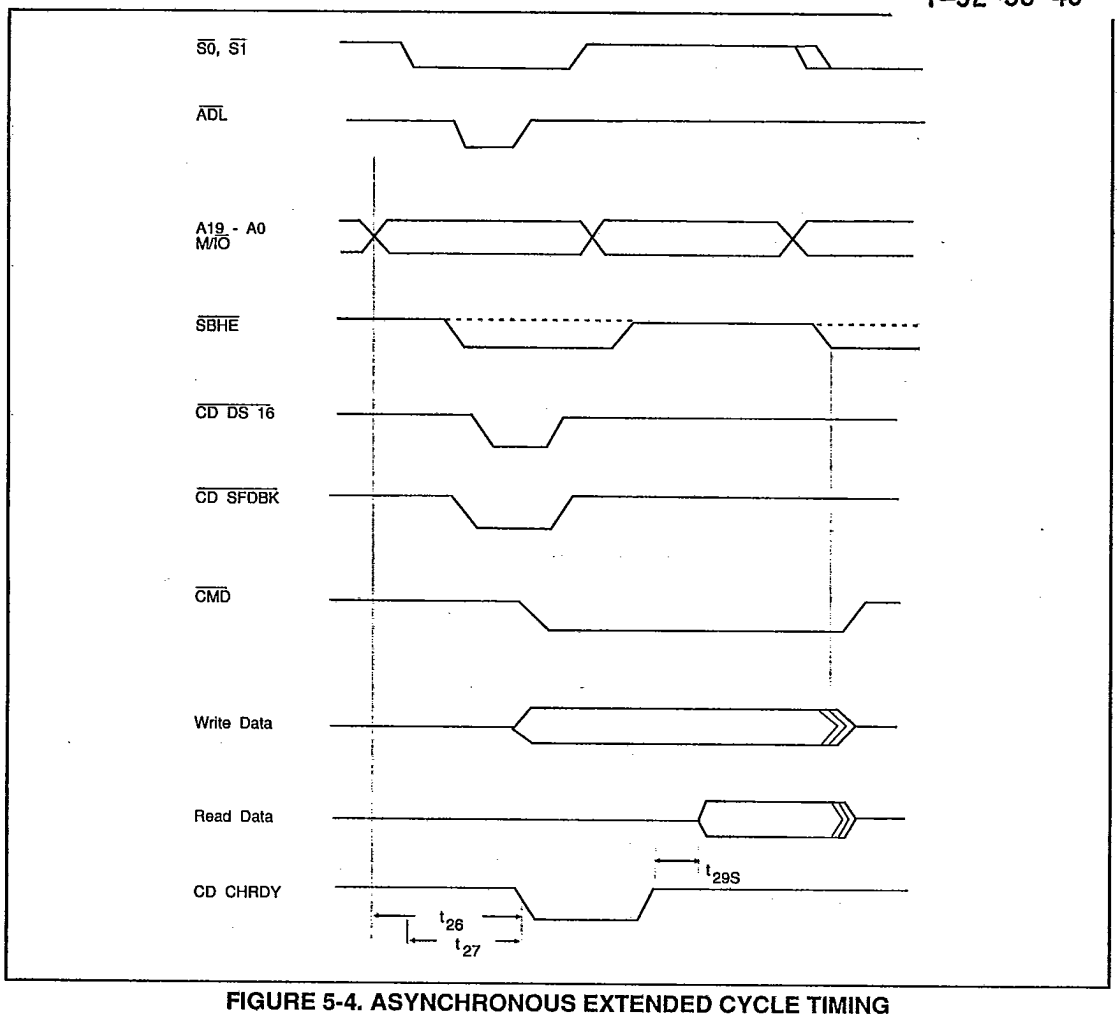


FIGURE 5-4. ASYNCHRONOUS EXTENDED CYCLE TIMING

SYMBOL	TIMING PARAMETERS	MIN/MAX
t_{26}	CD CHRDY (n) inactive (low) from ADDRESS valid	-/60 ns
t_{27}	CD CHRDY (n) inactive (low) from Status active	0/30 ns
t_{29S}	Read data valid from CD CHRDY (n) active (high)	-/60 ns

TABLE 5-4. ASYNCHRONOUS EXTENDED CYCLE TIMING

5.3 AT BUS INTERFACE TIMING (16-BIT)

5.3.1 I/O MEMORY EXTENDED READ CYCLE

T-52-33-45

This cycle is used when reading any WD9500-SET1 register.

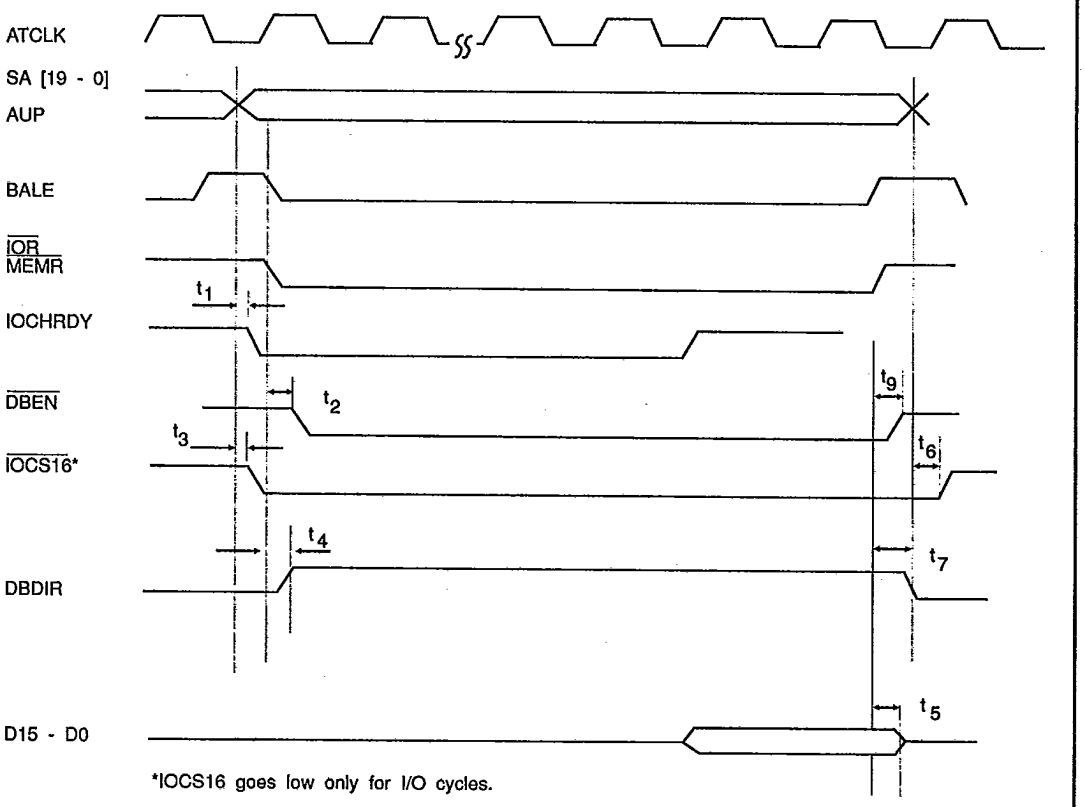
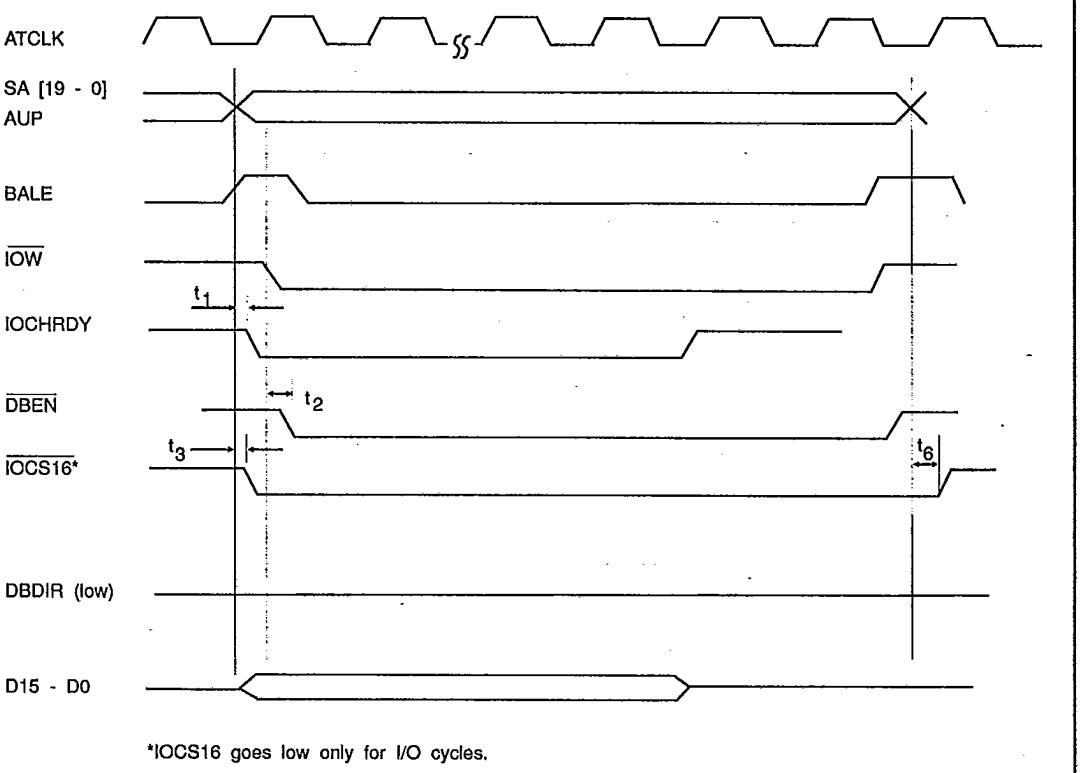


FIGURE 5-5. AT BUS I/O MEMORY TIMING

5.3.2 I/O EXTENDED WRITE CYCLE

This cycle is used when writing to any WD9500-SET1 register.



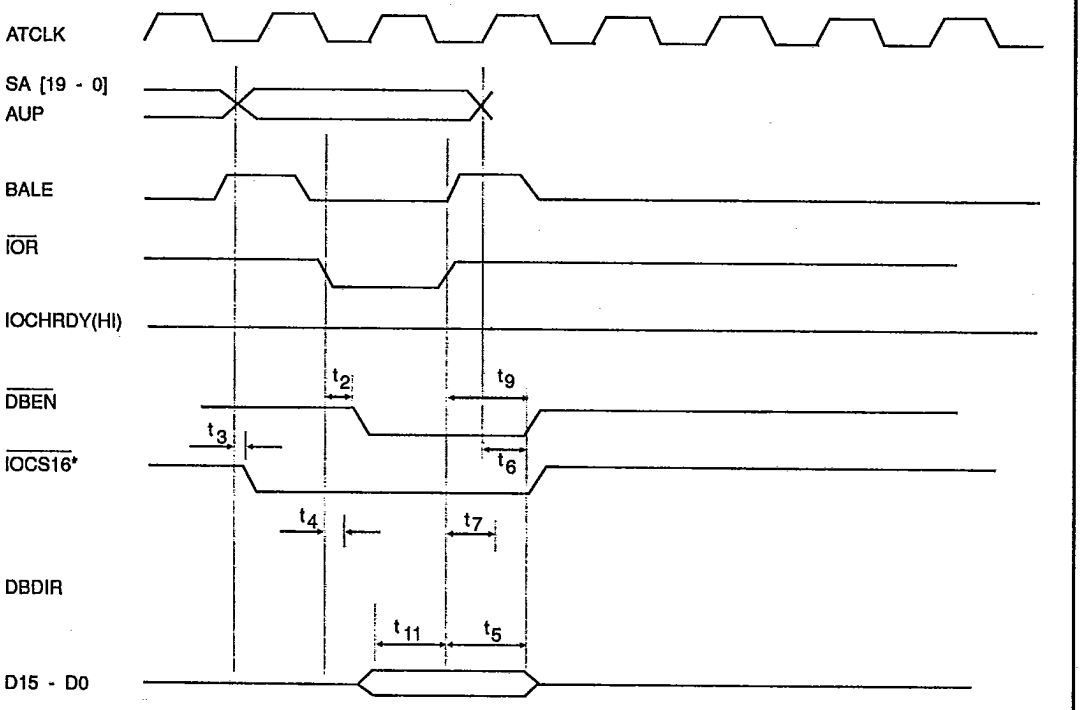
*IOCS16 goes low only for I/O cycles.

FIGURE 5-6. AT BUS I/O WRITE CYCLE (>1 WAIT STATE) TIMING

5.3.3 I/O READ CYCLE

This cycle is used only for DAC access.

T-52-33-45



*IOCS16 goes low only for I/O cycles.

FIGURE 5-7. AT BUS - I/O READ (1 WAIT STATE) TIMING

5.3.4 I/O WRITE CYCLE

This cycle is used only for DAC access (flicker-free mode is disabled).

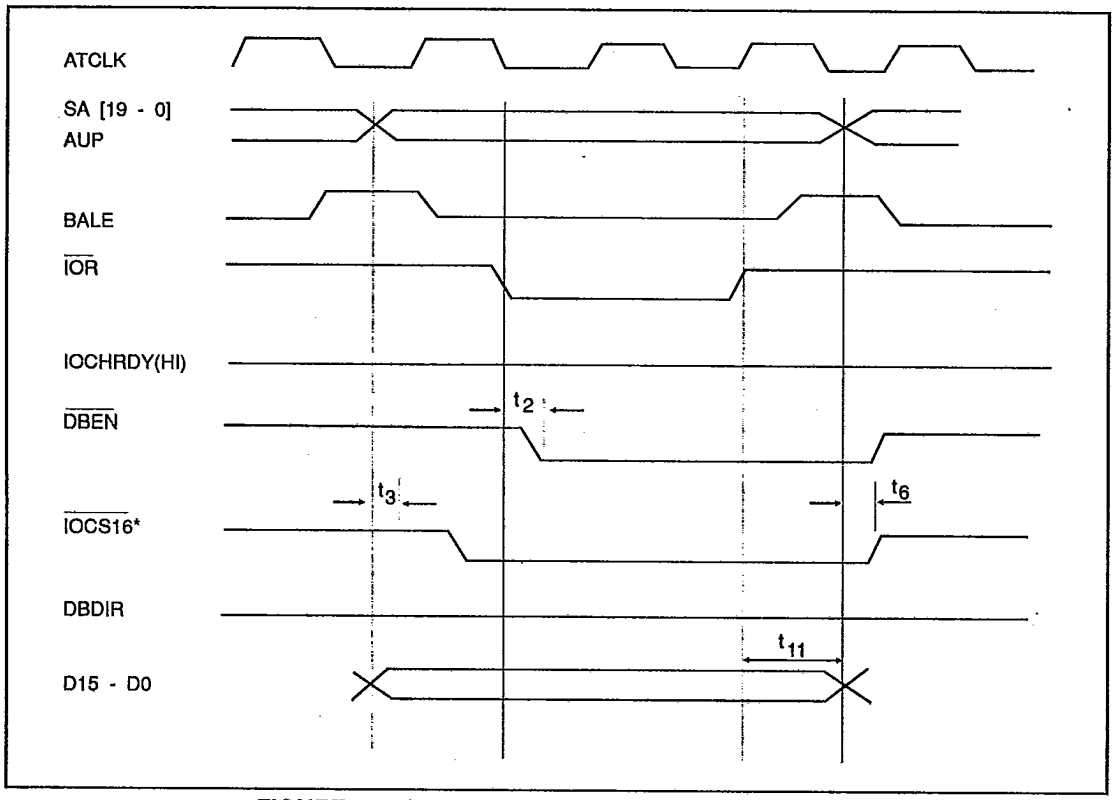


FIGURE 5-8. AT BUS - WRITE (1 WAIT STATE) TIMING

SYMBOL	TIMING PARAMETER	MINIMUM	MAXIMUM
t_1	SA[19-0] valid to IOCHRDY (BALE is high)		65*
t_2	IOR, MEMR, IOW valid to DBEN low	35	
t_3	SA[19-0] valid to IOCS16		55
t_4	DBDIR delay from IOR, MEMR		40
t_5	IOR invalid to data valid	40	
t_6	SA[19-0] invalid to IOCS16		55
t_7	IOR high to DBDIR low		40
t_9	IOW, MEMR, IOR high to DBEN high		30
t_{11}	Read data setup to IOR high	40	

*If no command (MEMR, IOR, IOW) becomes active IOCHRDY times out and goes high after four ATCLK cycles.

TABLE 5-5. AT RESPONSE TIME

5.4 VRAM MEMORY INTERFACE TIMING

5.4.1 VRAM READ CYCLE

Page mode cycle follows the standard entry cycle if the row address of a subsequent access is the same. Page mode terminates if: (1) operations are completed; (2) a memory refresh request is pending; (3) a different row address is given in next access; or (4) RAS low width = 50.

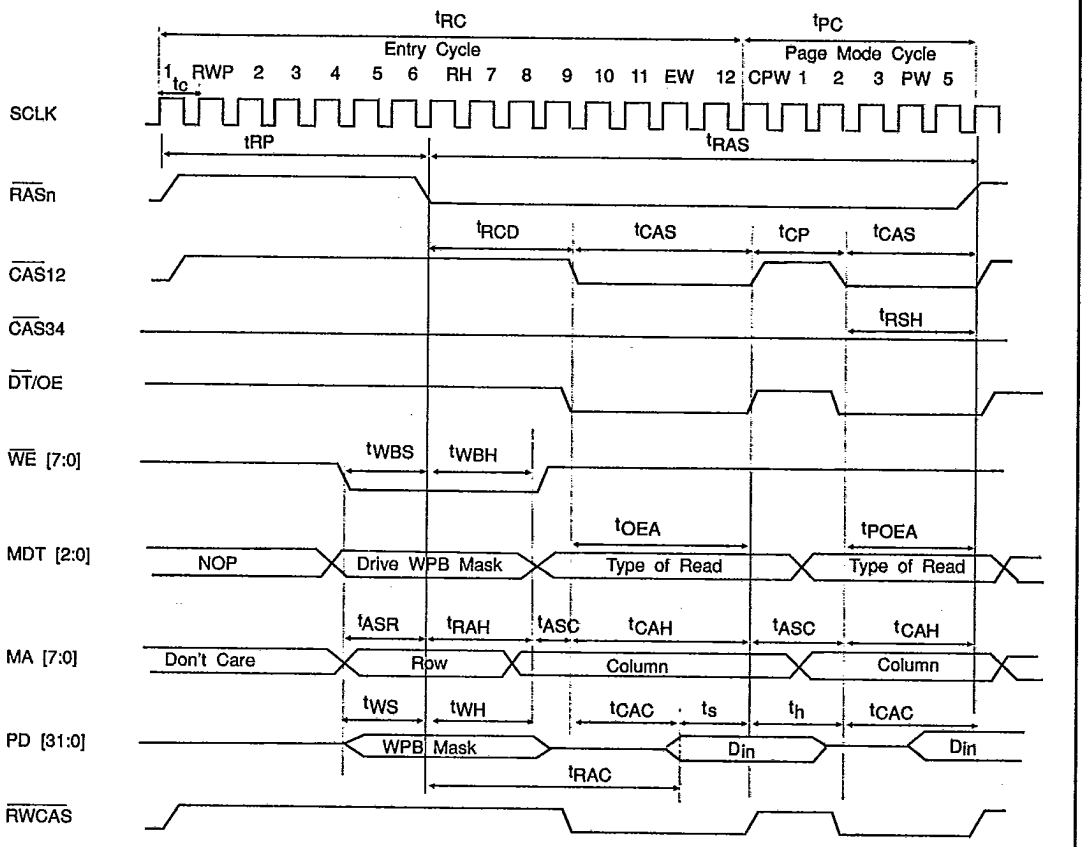


FIGURE 5-9. VRAM READ CYCLE TIMING

SYMBOL	TIMING PARAMETER	MINIMUM	MAXIMUM
t_{RC}	Random read/write cycle time	(12 + RPW + EW + RH) t_C	
t_{PC}	Page mode cycle time	(5 + CPW + PW) t_C	
t_{RP}	$\overline{RAS}$ precharge time	(5 + RPW) t_C	
t_{CP}	$\overline{CAS}$ precharge time	(2 + CPW) t_C	
t_{RAS}	$\overline{RAS}$ pulse width	(7 + EW + RH) t_C	500t_C
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay	(4 + RH) t_C	
t_{CAS}	$\overline{CAS}$ pulse width	(3 + EW) t_C*	
t_{ASR}	Row address setup	2t_C	
t_{RAH}	Row address hold	(2 + RH) t_C	
t_{ASC}	Column address setup	2t_C	
t_{CAH}	Column address hold	(3 + EW) t_C*	
t_{CRP}	$\overline{CAS}$ high to $\overline{RAS}$ precharge time	(5 + RPW) t_C	
t_{OEA}	$\overline{OE}$ low to read data valid		(2 + EW) t_C
t_{POEA}	$\overline{OE}$ low to read data valid for page mode		(3 + PW) t_C
t_{RAC}	Access time from $\overline{RAS}$	(6 + RH + EW) t_C	
t_{CAC}	Access time from $\overline{CAS}$	(2 + EW) t_C	
t_s	Read data setup time	32	
t_h	Read data hold time	0	

* Under page mode cycle, EW = PW

RPW, EW, CPW, PW and RH are all memory wait control parameters.
The parameters listed in this table only indicate the period of each timing parameter when there is zero delay. CLK is given for reference.

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TABLE 5-6. VRAM READ CYCLE

5.4.2 VRAM WRITE CYCLE

Page mode cycle follows the standard entry cycle if the row address of a subsequent access is the same. Page mode terminates if: (1) operations are complete; (2) a memory refresh request is pending; (3) a different row address is given in the next access; or (4) RAS low width = 50.

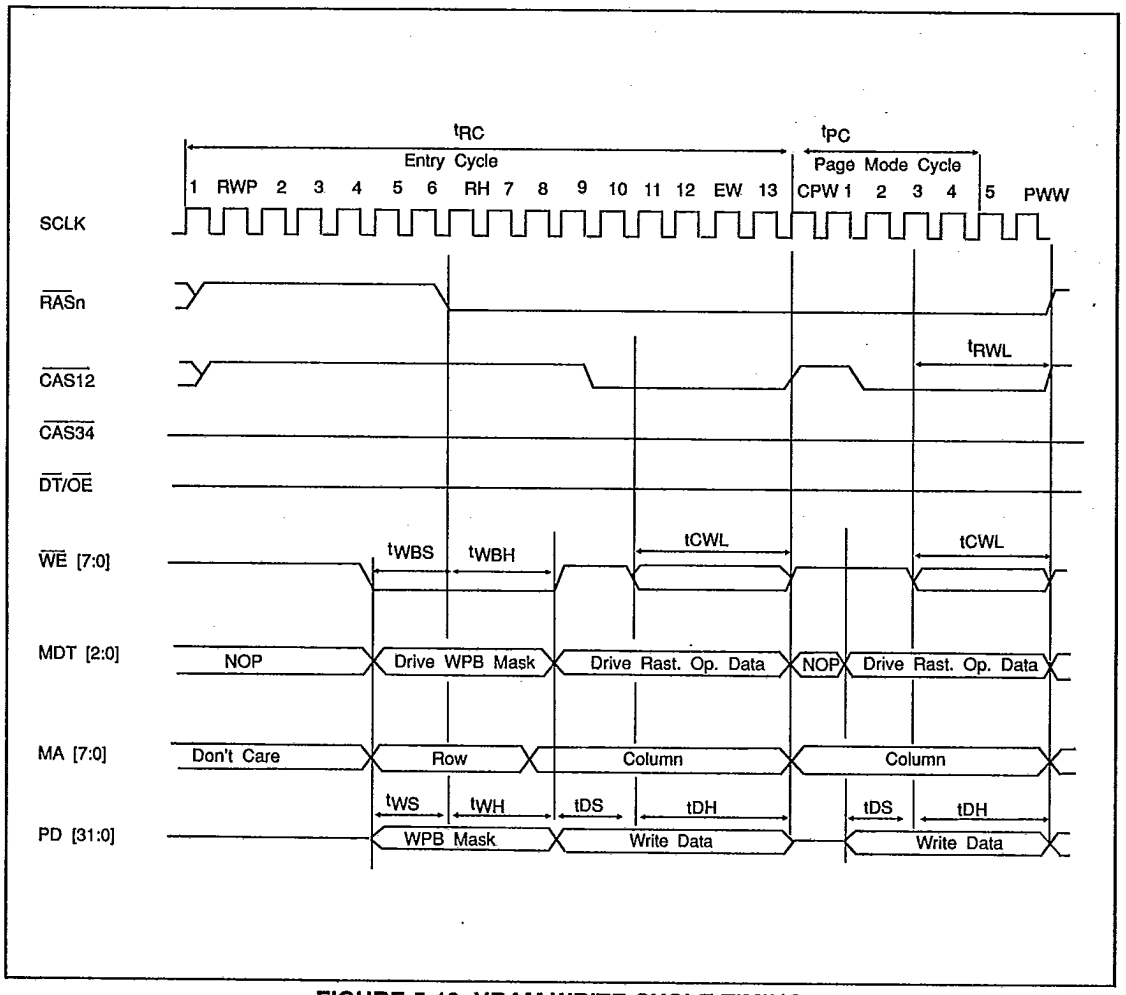

FIGURE 5-10. VRAM WRITE CYCLE TIMING

SYMBOL	TIMING PARAMETER	MINIMUM	MAXIMUM
t_{RWL}	Write command to $\overline{RAS}$ lead time	(3 + EW) t_C*	
t_{CWL}	Write command to $\overline{CAS}$ lead time	(3 + EW) t_C*	
t_{RCS}	Setup time	t_C	
t_{WP}	Write command pulse width	(3 + EW) t_C*	
t_{DS}	Data in setup time	0	
t_{DH}	Data in hold time	2t_C	
t_{WBS}	Write-per-bit setup time	2t_C	
t_{WBH}	Write-per-bit hold time	(3 + RH) t_C	
t_{WS}	Write bit selection setup time	2t_C	
t_{WH}	Write bit selection hold time	(2 + RH) t_C	

* Under page mode cycle, EW = PW

$\overline{RAS}$, $\overline{CAS12}$, $\overline{CAS34}$, $\overline{DT/OE}$, $\overline{WE}$[7:0], MDT[7:0], and MA[7:0] all have a SCLK synchronization flip-flop before the output buffer. The worst case delay of all signals from SCLK is 28 nanoseconds with the exception of MA[7:0] which has a worst case delay of 30 nanoseconds. All of these signals use the same output buffer. Under identical load conditions, the skew between these signals is less than one nanosecond.

TABLE 5-7. VRAM WRITE CYCLE

5.4.3 VRAM TRANSFER READ CYCLE TIMING

This cycle occurs during retrace time when the VRAM serial port is in standby mode.

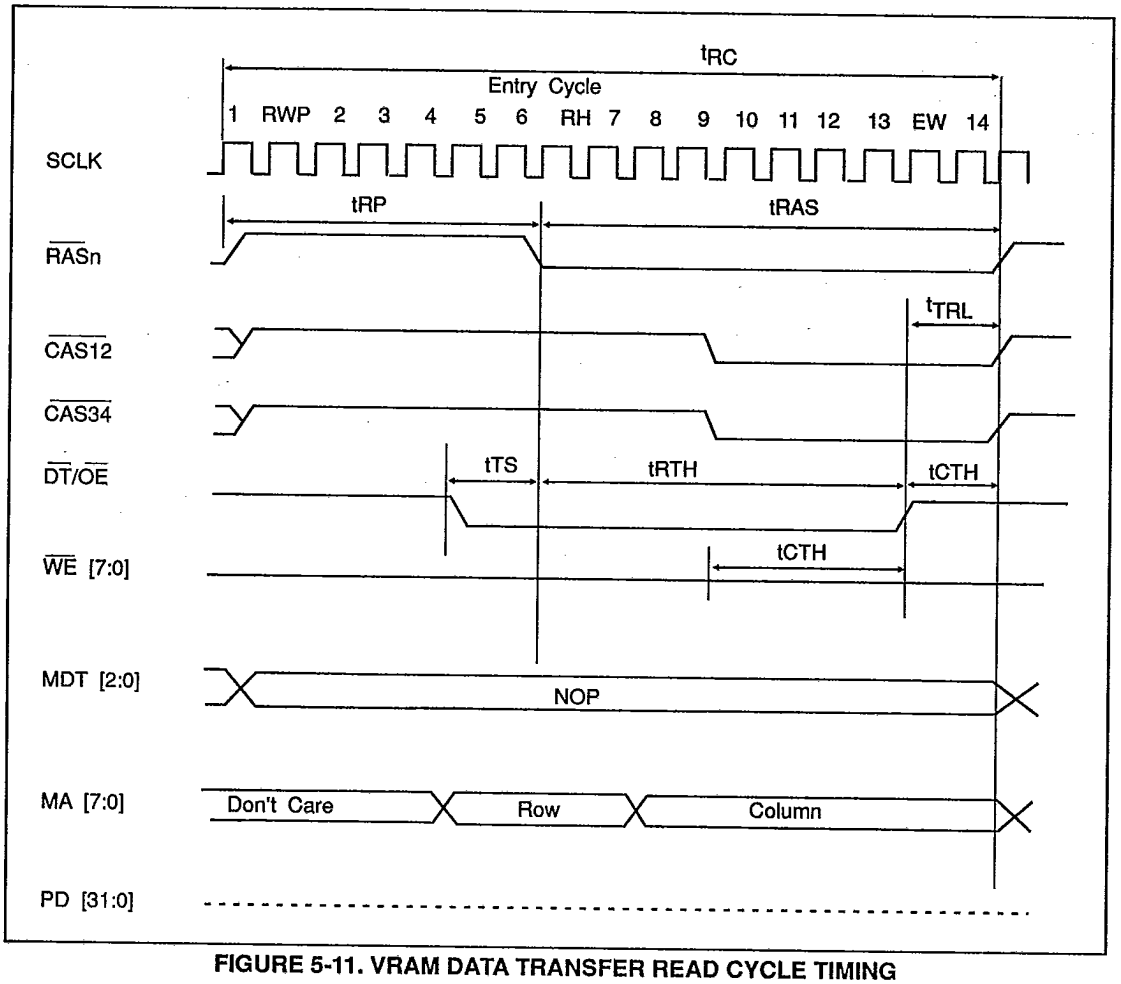

FIGURE 5-11. VRAM DATA TRANSFER READ CYCLE TIMING

SYMBOL	TIMING PARAMETER	MINIMUM	MAXIMUM
t_{TS}	$\overline{DT}$ low setup time	2tc	
t_{RTH}	$\overline{DT}$ low hold time after $\overline{RAS}$ low	(8 + RH) tc	
t_{CTH}	$\overline{DT}$ low hold time after CAS low	4tc	
t_{TRL}	$\overline{DT}$ high to $\overline{RAS}$ high delay	(1 + EWS) tc	
t_{CTH}	$\overline{DT}$ high to $\overline{CAS}$ high delay	(1 + EW) tc	

TABLE 5-8. VRAM DATA TRANSFER READ CYCLE

5.4.4 VRAM REFRESH TIMING

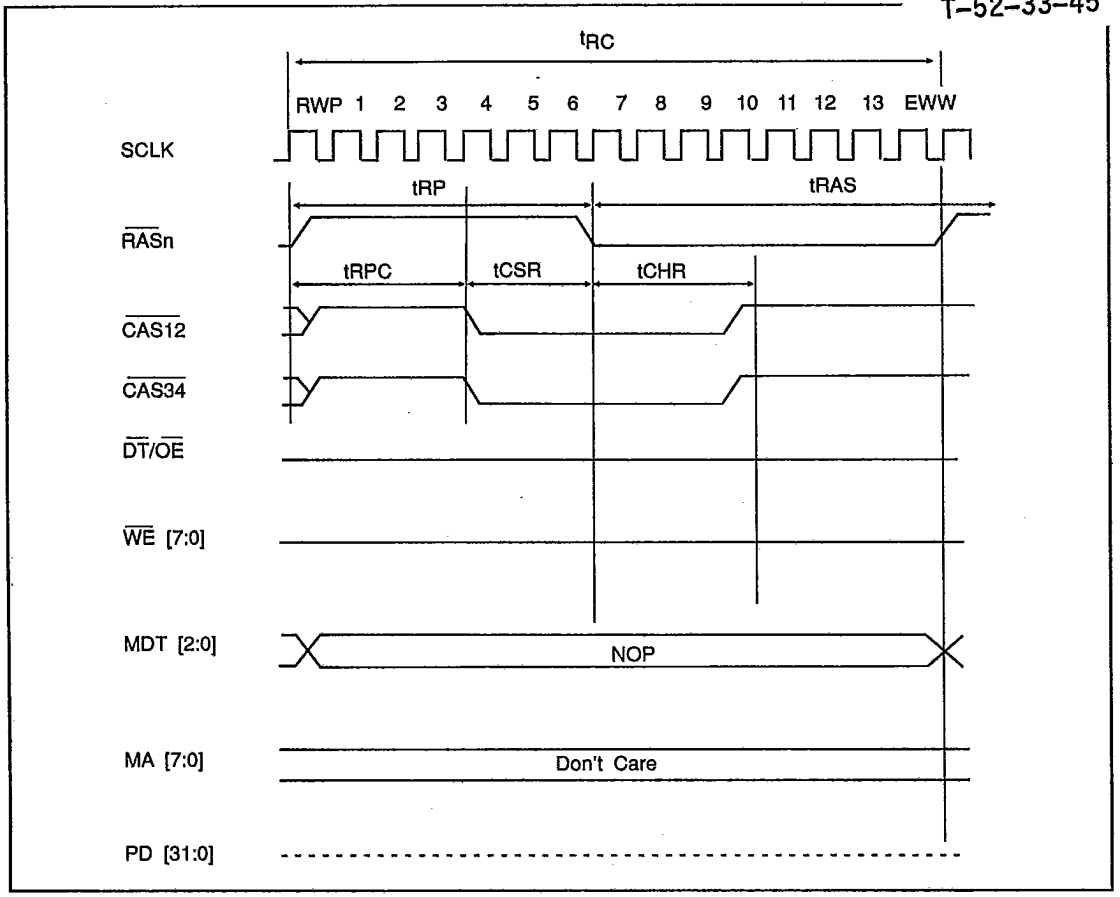

FIGURE 5-12. VRAM REFRESH TIMING

SYMBOL	TIMING PARAMETER	MINIMUM	RANGE tC = 16.667 ns
t_{CSR}	$\overline{CAS}$ before $\overline{RAS}$ setup time	$3t_C$	50
t_{CHR}	$\overline{CAS}$ before $\overline{RAS}$ hold time	$(4 = RH)t_C$	66-83
t_{RPC}	$\overline{RAS}$ rising to $\overline{CAS}$ falling	$(2 + RPW)t_C$	33-83

TABLE 5-9. VRAM CAS BEFORE RAS REFRESH TIMING

5.4.5 SERIAL READ CYCLE TIMING

Serial output from VRAM is read into PDM for all integrated back-end support designs.

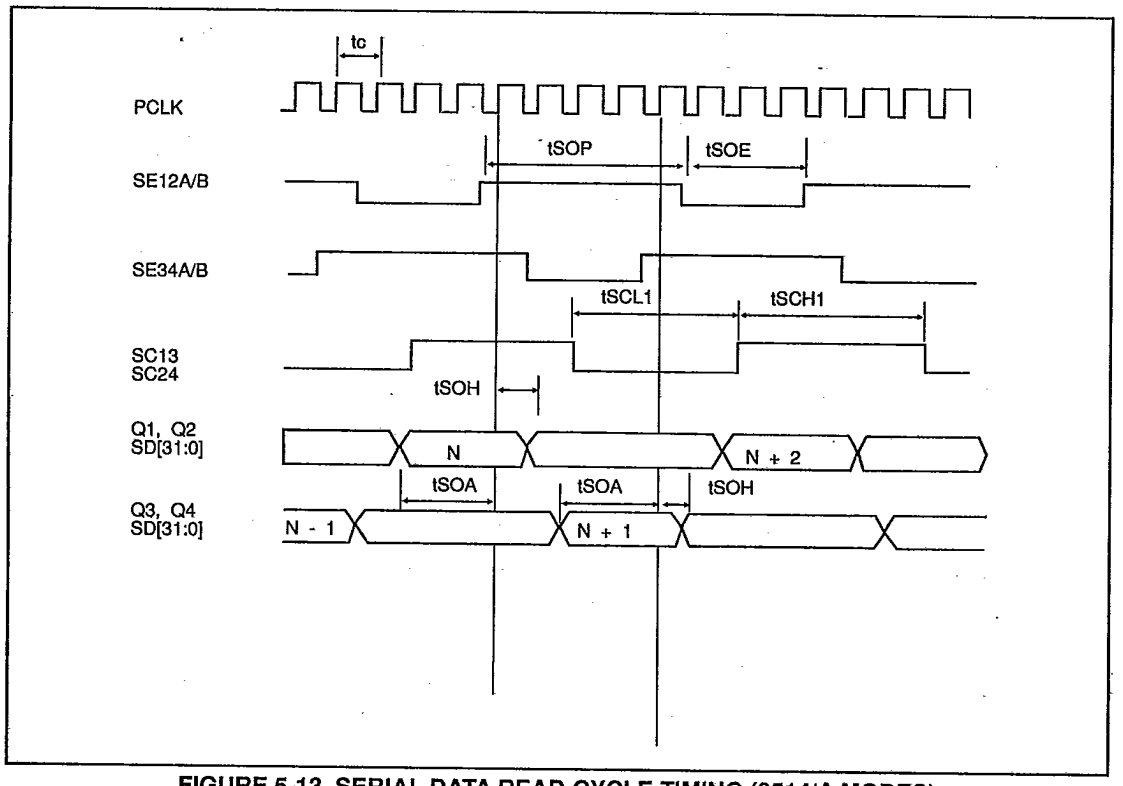

FIGURE 5-13. SERIAL DATA READ CYCLE TIMING (8514/A MODES)

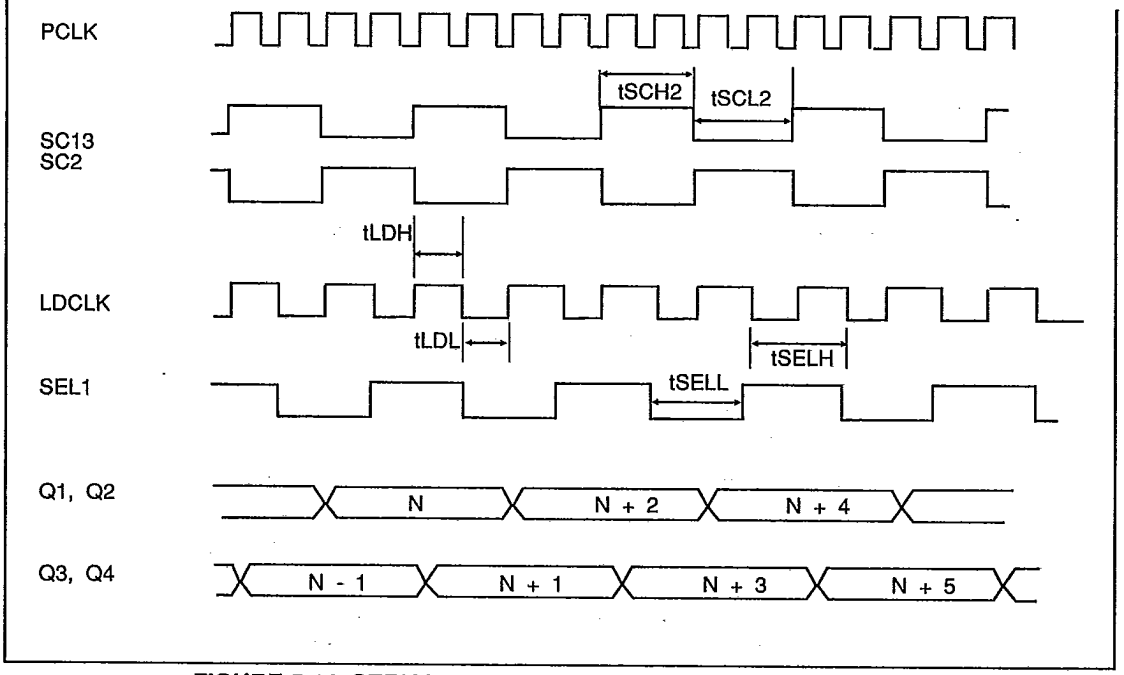

FIGURE 5-14. SERIAL DATA READ CYCLE TIMING (1280x1024x4)

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SYMBOL	TIMING PARAMETERS	MINIMUM	MAXIMUM
t_{SOE}	SE† pulse width	3tc	
t_{SOP}	SE† precharge time	5tc	
t_{SCL1}	SC* pulse width	4tc	
t_{SCH1}	SC* precharge time	4tc	
t_{SOH}	Serial input hold	tc-4	
t_{SOA}	Serial input setup	t4	
t_{SCL2}	SC* pulse width	2tc	
t_{SCH2}	SC* precharge time	2tc	
t_{LDH}	LDCLK high time	tc	
t_{LDL}	LDCLK low time	tc	
t_{SELH}	SEL1 high time	2tc	
t_{SELL}	SEL1 low time	2tc	

† SE12A, SE12B, SE34A, SE34B, SE only toggles during active display period in 640x480 mode using 64Kx4. It stays high or low for all other modes.
* SC13, SC24

TABLE 5-10. SERIAL DATA READ CYCLE

5.5 BACK-END VIDEO TIMING

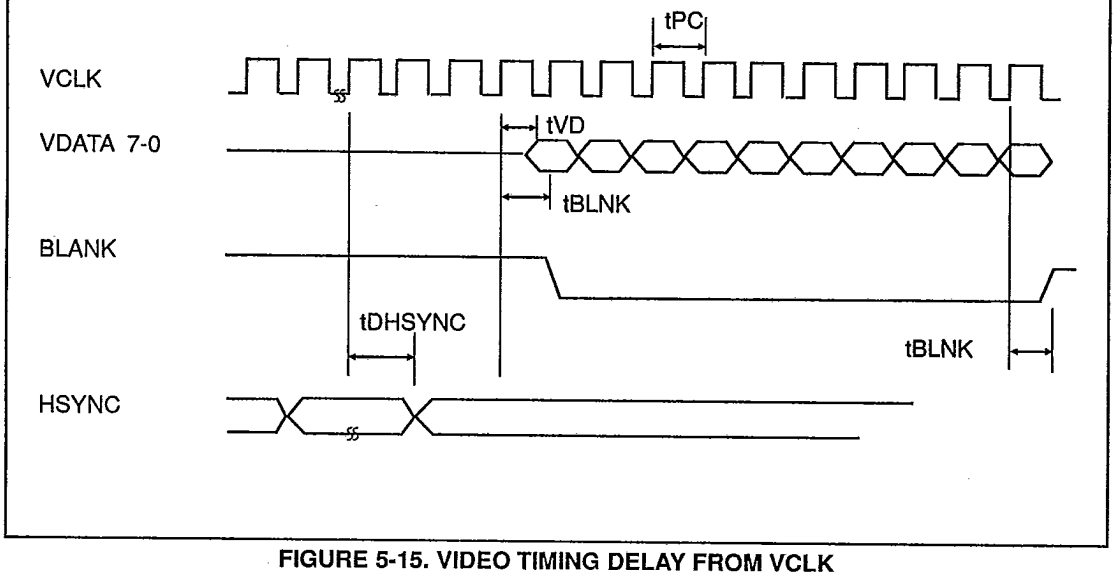

FIGURE 5-15. VIDEO TIMING DELAY FROM VCLK

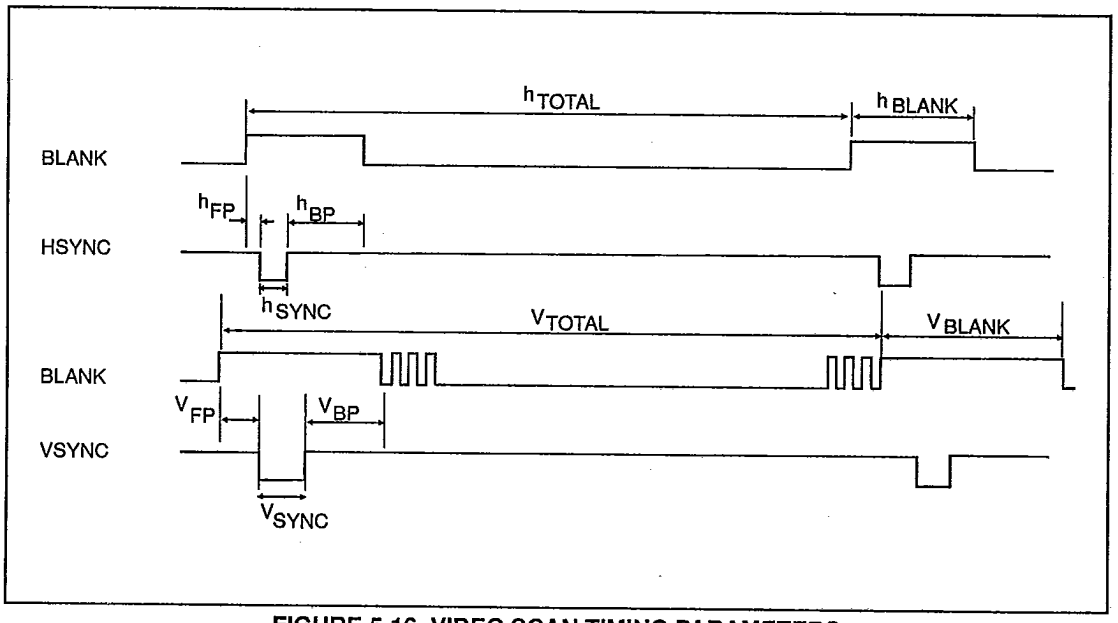

FIGURE 5-16. VIDEO SCAN TIMING PARAMETERS

SYMBOL	TIMING PARAMETER	MINIMUM	MAXIMUM
t_{BLNK}	Delay of BLANK from the rising edge of VCLK	3	t_{PC} -3
t_{VD}	Delay of VDATA from the rising edge of VCLK	3	t_{PC} -3
t_{DHSYNC}	Delay of HSYNC from the rising edge of VCLK	3	t_{PC} -3
t_{PC}	PCLK period	13	

TABLE 5-11. VIDEO DELAY TIMING PARAMETERS

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SYMBOL	VIDEO REGISTER PROGRAMMING EQUATION	UNITS
H_{total}	[(02E8)* + 1] x8	Pixels
H_{disp}	[(06E8) + 1] x8	Pixels
H_{sync}	(Bits 4-0; 0EE8)** x8	Pixels
H_{fp}	[(0EA8) x8]-H_{disp}	Pixels
H_{bp}	H_{total} -H_{syncw} -(0AE8) x8	Pixels
V_{total} †	[(12E8)] + 1	Lines
V_{disp} †	[(16E8)] +1	Lines
V_{sync}	(Bits 4-0: 1EE8) /2	Lines
V_{fp} †	[(1AE8)]-[(16E8)]	Lines
V_{bp} †	V_{total} -V_{syncw} -(1AE8)	Lines

* (02E8) - content of register 02E8H
** (Bits 4-0; 0EE8) - value of bits 4-0 for register 0EE8H
† The true value of these parameters are controlled by bit 2 and bit 1 of 22E8 register as shown below.

TABLE 5-12. VIDEO TIMING RELATIONSHIP TO VIDEO REGISTERS

Register 22E8		Function
Bit 2	Bit 1	
0	0	Skip Y2 & Y1
0	1	Skip Y2
1	0	Skip Y1
1	1	No skip

5.6 INTERCHIP TIMING

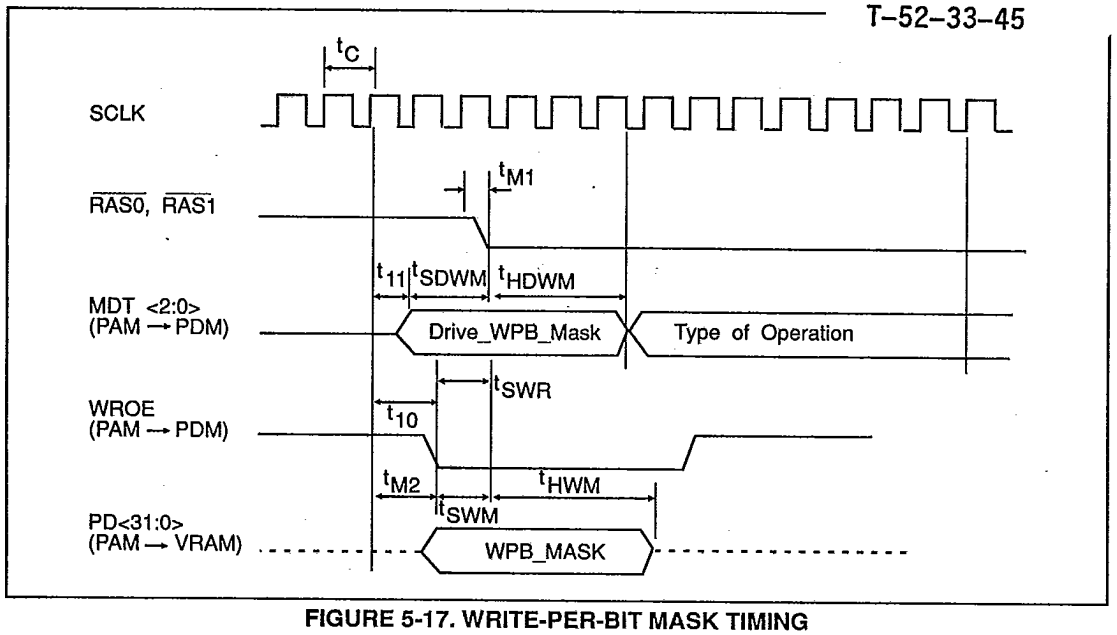
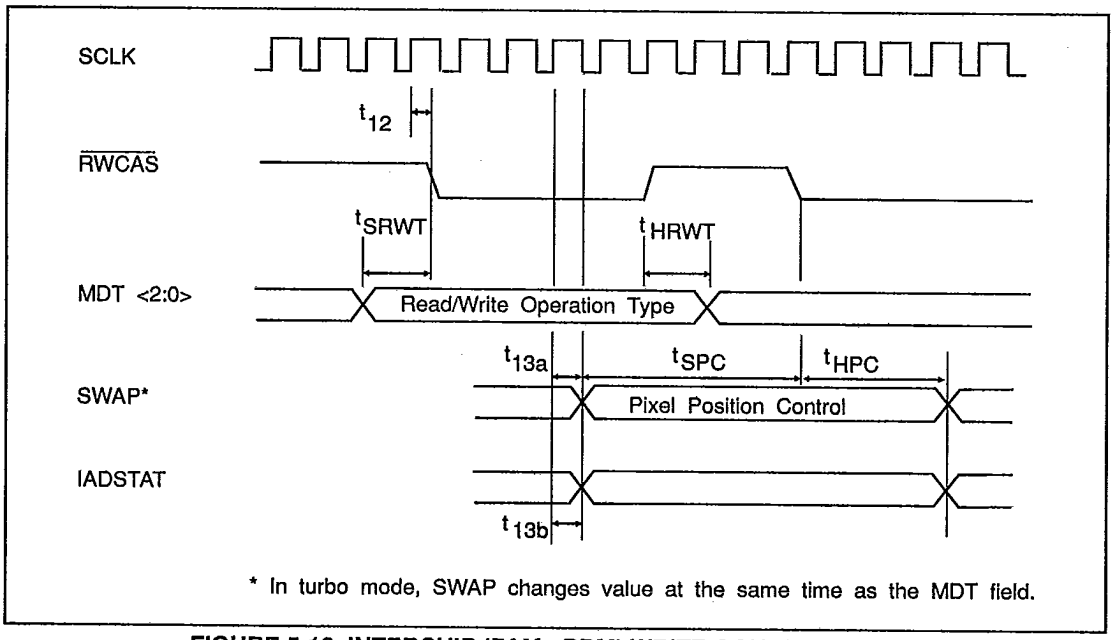


FIGURE 5-17. WRITE-PER-BIT MASK TIMING



* In turbo mode, SWAP changes value at the same time as the MDT field.

FIGURE 5-18. INTERCHIP (PAM - PDM) WRITE CONTROL TIMING (IADSTAT = LOW)

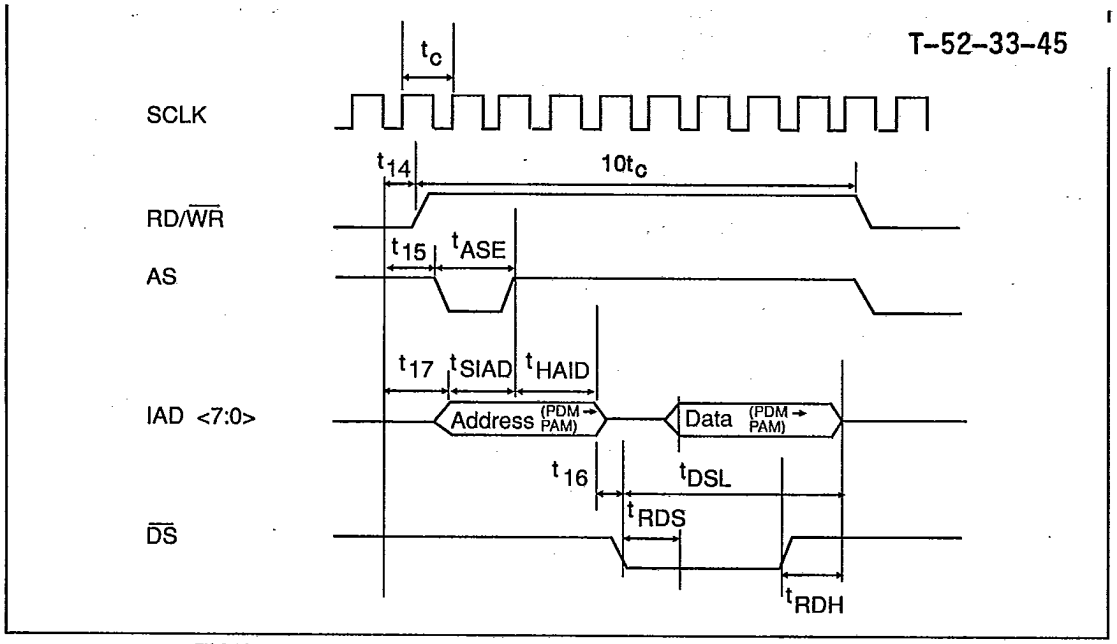


FIGURE 5-19. INTERCHIP DATA READ TIMING (IADSTAT = HIGH)

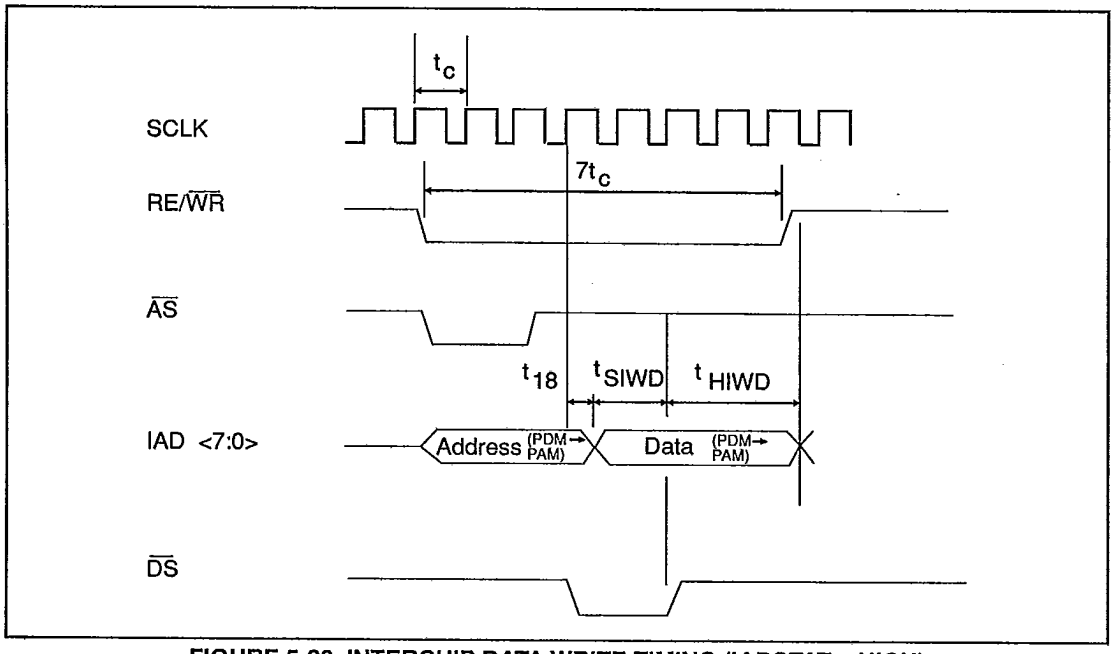


FIGURE 5-20. INTERCHIP DATA WRITE TIMING (IADSTAT = HIGH)

SYMBOL	TIMING PARAMETER	OUTPUT	MAXIMUM
t_{10}	WROE active from rising edge of SCLK	PAM	28 ns
t_{11}	MDT valid from rising edge of SCLK	PAM	28 ns
t_{12}	$\overline{RWCAS}$ change from rising edge of SCLK	PAM	30 ns
t_{13a}	SWAP valid from rising edge of SCLK	PAM	28 ns
t_{13b}	IADSTAD valid from rising edge of SCLK	PAM	35 ns
t_{14}	RE/$\overline{WR}$ valid from rising edge of SCLK	PAM	35 ns
t_{15}	$\overline{AS}$ change from rising edge of SCLK	PAM	35 ns
t_{16}	$\overline{DS}$ change from rising edge of SCLK	PAM	33 ns
t_{17}	Address valid from rising edge of SCLK	PAM	38 ns
t_{18}	Write Data valid from rising edge of SCLK	PAM	38 ns
t_{m1}	$\overline{RAS}$ low from rising edge of SCLK	PAM	28 ns
t_{m2}	PD bus WPWGA1_Mask valid from rising edge of SCLK	PDM	31 ns

TABLE 5-13. DELAY FROM SCLK FOR INTERCHIP TIMING

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SYMBOL	TIMING PARAMETER	PAM	PDM
t_{SWR}	Setup time for WROE to falling edge of $\overline{RAS}$	$(2t_C + t_{m1} - t_{10}$	T-52-33-45
t_{SDWM}	Setup time for MDT to falling edge of $\overline{RAS}$	$(2t_C + t_{m1} - t_{11})$	
t_{HDWM}	Hold time for MDT from falling edge of $\overline{RAS}$	$(3t_C - t_{m1} + t_{11})$	
t_{SWM}	Setup time for PD Write_mask to falling edge of $\overline{RAS}$	$(2t_C + t_{m1} - t_{m2})$	
t_{HWM}	Hold time for PD Write_mask from falling edge of $\overline{RAS}$	$(3t_C - t_{m1} + t_{m2})$	
t_{SRWT}	Setup time for MDT to falling edge of $\overline{RWCAS}$	$(2t_C + t_{12} - t_{11})$	
t_{HRWT}	Hold time for MDT from rising edge of $\overline{RWCAS}$	$(t_C - t_{12} + t_{11})$	
t_{SPC}	Setup time for IAD control to falling edge of $\overline{RWCAS}$	$(4t_C - t_{13} + t_{12})$	
t_{HPC}	Hold time for IAD control from falling edge of $\overline{RWCAS}$	$(2t_C + t_{13} - t_{12})$	
t_{ASL}	$\overline{AS}$ low time	$(2t_C)$	
t_{DSL}	$\overline{DS}$ low time	$(2t_C)$ for write, $(3t_C)$ for read	
t_{SIAD}	Setup time for IAD address to rising edge of $\overline{AS}$	$(2t_C + t_{15} - t_{17})$	
t_{HIAD}	Hold time for IAD address from rising edge of $\overline{AS}$	$(t_C - t_{15} + t_{17})$	
t_{SIRD}	Setup time for IAD read data to rising edge of $\overline{DS}$	$2t_C - t_{18} + t_{16})$	
t_{HIRD}	Hold time for IAD read data from rising edge of $\overline{DS}$	$(t_C + t_{18} - t_{16})$	
t_{SIWD}	Setup time for IAD write data to rising edge of $\overline{DS}$	$(2t_C - t_{19} + t_{16})$	
t_{HIWD}	Hold time for IAD write data from rising edge of $\overline{DS}$	$(2t_C + t_{19} - t_{16})$	
t_{RDS}	IAD read data access time		38 ns max.

TABLE 5-14. INTERCHIP RELATIVE TIMING PARAMETERS

5.7 RAMDAC INTERFACE TIMING

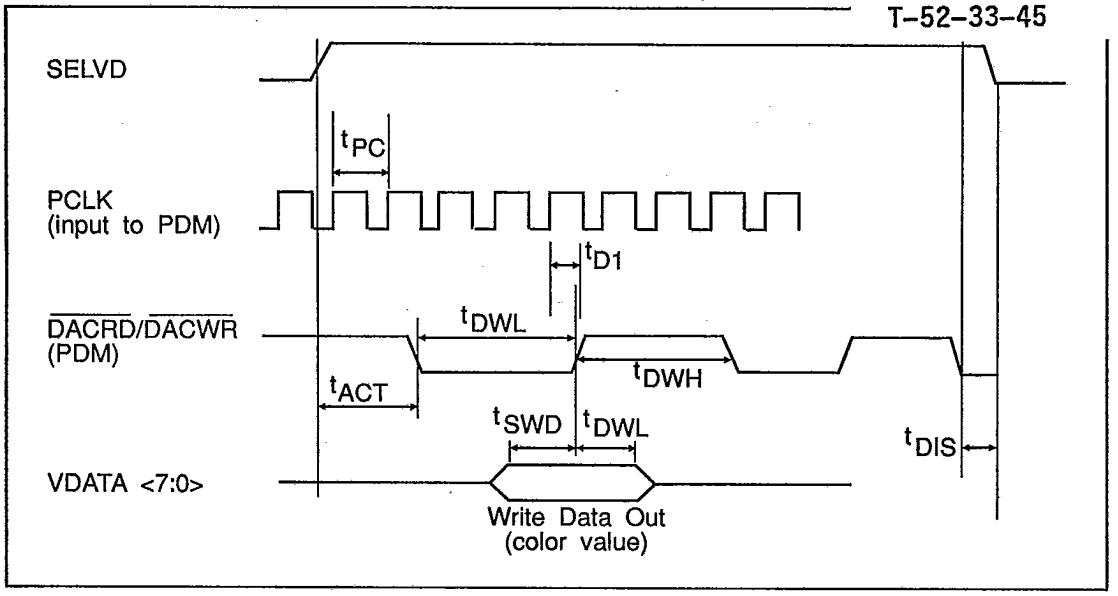

FIGURE 5-21. DAC WRITE TIMING (FLICKER-FREE MODE)

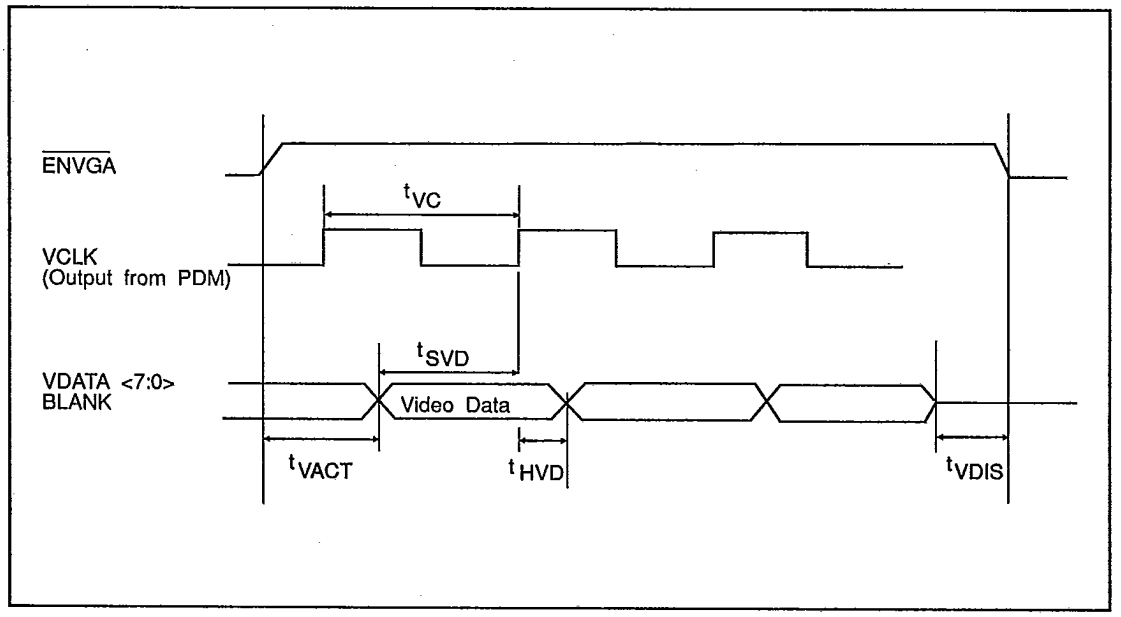

FIGURE 5-22. PIXEL VIDEO CLOCK AND DATA TIMING

SYMBOL	TIMING PARAMETER	MINIMUM	MAXIMUM
t_{DWL}	$\overline{DACWR}$ low time (PDM)	$5t_{PC}$	
t_{DWH}	$\overline{DACWR}$ high time (PDM)	$5t_{PC}$	
t_{SWD}	Setup time for Write Data to $\overline{DACWR}$	$4t_{PC}$	
t_{HWD}	Hold time for Write Data from $\overline{DACWR}$	$2t_{PC}$	
t_{D1}	Delay of $\overline{DACWR}$ (PDM) from rising edge of PCLK		30
t_{D2}	Delay of VDATA <7:0> from rising edge of PCLK		30
t_{VC}	Output video pixel clock period	t_{PC}	$2t_{PC}$
t_{SVD}	Setup time for video data to rising edge of VCLK	3	
t_{HVD}	Hold time for video data from rising edge of VCLK	3	
t_{ACT}	SELVD high to $\overline{DACWR}$/$\overline{DACRD}$ actively driven low	$2t_{PC}$	
t_{DIS}	$\overline{DACRD}$/$\overline{DACWR}$ inactive to SELVD low	t_{PC}	
t_{VACT}	$\overline{ENVGA}$ high to VDATA, BLANK, HSYNC and VSYNC active	t_C	

TABLE 5-15. DAC INTERFACE TIMING PARAMETERS

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6.0 WD9500 REGISTERS

Although a WD9500 based board is significantly more capable than the IBM 8514/A, especially when configured with sufficient VRAM, the base mode of the board's operations is that of exact 8514/A emulation, including exact compatibility with the 8514/A's user-accessible registers.

The WD9500 internal registers that are compatible with the IBM 8514/A are defined in this section. A summary of 8514/A compatible registers is shown in Table 6-6 and Table 6-7 respectively.

All WD9500 registers, except DAC interface registers, are addressed by 16-bit words. The unused bits are either not shown or marked with the letter U in the description of the register definitions below. The reserved bits are marked with the letter R. Both unused and reserved bits default to 0.

6.1 DAC INTERFACE REGISTERS

The eight-bit registers in Table 6-2 are used to program the external video DAC. It is possible to write and read the DAC. Once the read/write index is written, multiple read/write operations can be performed without having to set the index for each entry.

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POS Register Interface (Micro Channel only)		
The POS registers are used to identify the WD9500 to IBM's setup program. They operate only when the CDSETUP pin goes low. Returns POS ID LSByte from EPROM.		
SETUP MODE IDENTIFICATION	**SETUP_ID1**	**BYTE ACCESSIBLE**
Read only		Setup address 100
Returns POS ID LSByte from EPROM		
SETUP MODE IDENTIFICATION	**SETUP_ID2**	**BYTE ACCESSIBLE**
Returns POS ID MSByte from EPROM		
SETUP MODE IDENTIFICATION	**SETUP_OPT**	**BYTE ACCESSIBLE**
Bit 0 of the Setup Mode Option Select register can be used by the host PC to disable the WD9500 in case of an address conflict. Bit 0 = 1 Enable WD9500 registers Bit 0 = 0 Disable WD9500 registers		

TABLE 6-1. POS REGISTER INTERFACE (MICRO CHANNEL ONLY)

COLOR PROGRAMMING			8514/A	VGA
DAC Mask	R/W	DAC_MASK	02EA	03C6
DAC Read Index	R/W	DAC_R_INDEX	02EB	03C7
DAC Write Index	R/W	DAC_W_INDEX	02EC	03C8
DAC Data	R/W	DAC_DATA	02ED	03C9
The 851114/A DAC can be written but not read at the VGA addresses when in VGA pass-through mode (4AE8 bit 0 = 0).				

TABLE 6-2. DAC COLOR PROGRAMMING REGISTERS

Procedure to write to the DAC: (1) Set start write color index at 02ECH; (2) Write three bytes [RGB values] at 02EDH [The index auto increments the next write entry]; (3) Repeat step 2 until the desired number of entries have been programmed.

Procedure to read from the DAC: (1) Set start read color index at 02EBH. (2) Write three bytes [R. G. B. values] at 02EDH [The index auto increments to the next read entry]. (3) Repeat step 2 until the desired number of entries have been read.

6.2 ADVANCED FUNCTION CONTROL REGISTER (WRITE ONLY - 4AE8H)

Graphics mode is selected by writing to the Advanced Function Control (ADVFUNC_CTL). This register is used by all modules within the WD9500-SET1.

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BIT	FUNCTION
0	Set to 0 for VGA pass-through mode Set to 1 for 8514/A graphics mode
1	Mode extension - set to 1
2	Screen Resolution Set to 0 for 640 x 480 (25.18 MHz) Set to 1 for 1024 x 768 (44.9 MHz)
3	Reserved for Mode Extension Default = 0
4-15	Unused - Default = 0

MNEMONIC	NAME	ADDRESSS
H_TOTAL	Horizontal Total Register	02E8
H_DISP	Horizontal Displayed Register	06E8
H_SYNC_START	Horizontal Sync Start Register	0AE8
H_SYNC_WID	Horizontal Sync Width Register	0EE8
V_TOTAL	Vertical Total Register	12E8
V_DISP	Vertical Displayed Register	16E8
V_SYNC_START	Vertical Sync Start Register	1AE8
V_SYNC_WID	Vertical Sync Width Register	1EE8

TABLE 6-3. VIDEO TIMING SETUP REGISTERS T-52-33-45

6.3 VIDEO TIMING SETUP REGISTERS

There are nine registers for setting up video timing: four for horizontal, four for vertical, and one for control. Two sets of these registers (Table 6-3) are provided by WD9500 to allow video timing parameters to be pre-programmed and locked in for 640x480 and 1024x768 resolutions by Western Digital's BIOS. This extended feature is designed for interfacing with different monitors requiring different timing parameters. Once the timing parameters are locked in, application software that writes directly to the video registers need not be changed for different monitors, e.g. interlaced vs. non-interlaced. These registers affect the DSP module of the WD9500. The horizontal and vertical registers are set by the selected resolution. For example, 1024x768 is the graphics mode selected by the ADVFUNC_CNTL Register, then the horizontal and vertical registers are set accordingly. The following tables show the format for the horizontal and vertical registers. Vertical timing is programmed in line resolution. Horizontal timing is programmed in eight-pixel resolution.

6.3.1 HORIZONTAL TOTAL REGISTER (WRITE ONLY - ADDRESS 02E8H)

7	6	5	4	3	2	1	0

Set number of pixels per line, including blanking. Eight pixel blocks.

6.3.2 HORIZONTAL DISPLAYED (WRITE ONLY - ADDRESS 06E8H)

7	6	5	4	3	2	1	0
0							

Set number of pixels per line, including blanking. Eight pixel blocks.

6.3.3 HORIZONTAL SYNC START REGISTER (WRITE ONLY - ADDRESS 0AE8H)

7	6	5	4	3	2	1	0

Set Horizontal Sync Start. Eight pixel increments.

6.3.4 HORIZONTAL SYNC WIDTH REGISTER (WRITE ONLY - ADDRESS 0EE8H)

7	6	5	4	3	2	1	0
0	0						

Bit 5 = Polarity (1 = negative; 0 = positive)
Bits 0-4 = Set Horizontal Sync Width. Eight pixel increments.

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6.3.5 VERTICAL TOTAL REGISTER (WRITE ONLY - ADDRESS 12E8H)

11	10	9	8	7	6	5	4	3	2	1	0
Set number of lines per frame.											

6.3.6 VERTICAL DISPLAYED REGISTER (WRITE ONLY - ADDRESS 16E8H)

11	10	9	8	7	6	5	4	3	2	1	0
Set number of lines displayed.											

6.3.7 VERTICAL SYNC START REGISTER (WRITE ONLY - ADDRESS 1AE8H)

11	10	9	8	7	6	5	4	3	2	1	0
Set vertical sync start.											

6.3.8 VERTICAL SYNC WIDTH POLARITY REGISTER (WRITE ONLY - ADDRESS 1EE8H)

7	6	5	4	3	2	1	0
0	0						
Bit 5 = Polarity (1 = negative; 0 = positive) Bits 0-4 = Set Vertical Sync Width.							

6.3.9 DISPLAY CONTROL REGISTER (WRITE ONLY - ADDRESS 22E8H)

The Display Control DISP_CNTL Register sets various control features for the display functions.

BIT	POSITION
1 & 2	**Specify resolution.** These bits should match bits 2 and 3 of BEE8-5.
3	**Scan.** A "1" specifies a double scan; "0" specifies a single scan.
4	**Interlace.** A "1" specifies interlaced mode; "0" specifies non-interlaced mode.
5 & 6	**Enable Display.** Together these bits enable/reset the display. The display is enabled when bits 5 and 6 are set to "01"; and reset when set to "10". These bits are not affected by the locked-in extended feature.

		1024 x 768			640 x 480 (4 or 8)	
Frame Rate		43 Hz I	60 Hz NI	70 Hz NI	60 Hz NI	70 Hz NI
pclk		44.90MHz 22.27ns	63.98MHz 15.63ns	74.16MHz 13.46ns	25.18MHz 39.92ns	31.32MHz 31.93ns
02EH	Htotal	9d	a2	a4	63	68
06E8	Hdisplay	7f	7f	7f	4f	4f
0AE8	Hsync position	81	83	83	52	54
0EE8	Hsync & polarity	16	16	16	2c	2c
12E8	Vtotal	660	660	642	830(4) 418 (8)	848 (4) 426 (8)
16E8	Vdisplay	5fb	5fb	5fb	779(4) 3bb(8)	779 (4) 3bb (8)
1AE8	Vsync position	600	600	600	7a8 (4) 3d2 (8)	7b8 (4) 3de (8)
1EE8	Vsync & polarity	8	8	8	22	22
22E8	Control	33	23	23	21 (4) 23 (8)	21 (4) 23 (8)
Htotal	µ	28.25	20.38	17.80	31.78	26.82
Hdisp.	µ	22.89	16.00	13.81	25.42	20.44
Hblank	µ	5.37	4.376	3.99	6.355	6.39
Hsync	µ	3.93	2.751	2.373	3.813	3.07
Hfporch	µ	0.178	0.375	0.323	0.636	1.02
Hbporch	µ	1.25	1.250	1.294	1.906	2.30
Vtotal	ms	23.08	16.65	14.29	16.68	14.24
Vdisp.	ms	21.70	15.65	13.67	15.25	12.87
Vblank	ms	0.706 (even) 0.678 (odd)	0.999	0.623	1.430	1.368
Vsync	ms	0.113	0.082	0.071	0.079	0.067
Vfporch	ms	0.0141 (even) 0 (odd)	0.020	0.018	0.350	0.402
Vbporch	ms	0.579 (even) 0.565 (odd)	0.897	0.534	1.00	0.898
HS polarity	ms	+	+	+	-	-
VS polarity	ms	+	+	+	-	-

TABLE 6-4. CRT CONTROL REGISTER PARAMETERS AND TIMING

6.4 ROM PAGE SELECT REGISTER (WRITE ONLY - ADDRESS 46E8 MC/36E8 AT)

The ROM Page Select (ROM_PAGE_SEL) Register is used by the CIU to enable ROM bank selection and select a bank of ROM. The register format for bank selection is shown below. This register is remapped to 36E8h for AT Bus because VGA used the 46E8h register.

7	6	5	4	3	2	1	0
U	U	U	U	U			
Bits 0-2 select the ROM bank							

2 1 0	Select Bank
0 0 0	0
0 0 1	1
0 1 0	2
1 1 1	3
1 0 0	4
1 0 1	5
1 1 0	6
1 1 1	7

6.5 SUBSYSTEM CONTROL REGISTER (WRITE ONLY - ADDRESS 42E8H)

The Subsystem Control (SYBSYS_CNTL) Register is used for interrupt and reset control of the WD9500 FIFO and other CPU interface functions. This register affects Bits 3-0 of the Subsystem status (SUBSYS_CNTL) Register (see "Subsystem Status Register", Section 6.7.1).

BIT	POSITION
0	Puts a zero in the vertical sync status bit of the IS Register that can be read at address 42E8h. (1 = clear; 0 = no change)
1	Puts a zero in the GE window hit bit of the IS Register; readable at address 42E8h. (1 = clear; 0 = no change)
2	Puts a zero in the FIFO overflow status bit of the IS Register; readable at address 42E8h. This bit is cleared at the end of every line during a read across the plane. (1 = clear; 0 = no change)
3	Puts a zero in the GE Idle status bit of the IS Register; readable at address 42E8h. (1 = clear; 0 = no change)
8	Enables/disables the vertical sync interrupt. (1 = enable; 0 = disable)
9	Enables/disables the GE busy interrupt. (1 = enable; 0 = disable)
10	Enables/disables the FIFO overflow interrupt. (1 = enable; 0 = disable)
11	Enables/disables the FIFO empty interrupt. (1 = enable; 0 = disable)
12 & 13	Selects normal mode or test mode.
14 & 15	Graphic Engine Reset - Used to switch between normal mode and reset.

Bit 13	Bit 12	
0	0	No Change
0	1	Normal
1	0	Test

Bit 15	Bit 14	
0	1	Normal
1	0	Reset
0	0	No Change

10

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6.6 DRAWING CONTROL REGISTERS

There are sixteen registers involved in drawing control. These registers affect the operation of the GP, DP, MIC and CIU Current Y Position Register.

6.6.1 CURRENT Y POSITION REGISTER (READ/WRITE - ADDRESS 82E8H)

The 16-bit CUR_Y Register at address 82E8h uses Bits 10-0 to define the current position of Y for the pixel being drawn. The value is 11 bits unsigned. Bit 11 is reserved for higher resolution. WD9500's enhanced resolution (1280x1024) mode does not use this bit.

BIT	POSITION
0-10	Current Y of drawing point value
11	Reserved
12-15	Unused

6.6.2 CURRENT X REGISTER (READ/WRITE - ADDRESS 86E8H)

The CUR_X Register at address 82E8h uses Bits 10-0 to define the current position of X for the pixel being drawn. The value is 11 bits unsigned. Note that Bit 11 is reserved for higher resolution. WD9500's enhanced resolution (1280x1024) mode does not use this bit. The status of this register can be read.

BIT	POSITION
0-10	Current X of drawing point value
11	Reserved
12-15	Unused

6.6.3 DESTINATION Y POSITION/AXIAL STEP CONSTANT REGISTER (WRITE ONLY - ADDRESS 8AE8H)

The Command (CMD) Register specifies the command to be performed. The value is 12 unsigned bits when line drawing is specified. The minterm for the line drawing is: (Increment 1 = 2*(min(|dx|,dy|)).

BIT	POSITION
Line Drawing Mode: Increment line parameter 1.	
0-11	Defines increment 1 value
12-15	Unused
BITBLT Copying Mode: Copy Y Destination	
0-10	Defines Y destination
11	Reserved
12-15	Unused

6.6.4 DESTINATION X POSITION/DIAGONAL STEP CONSTANT REGISTER (WRITE ONLY - ADDRESS 8EE8H)

The Command (CMD) Register specifies the command to be performed. The value is 12 unsigned bits when line drawing is specified. The minterm for the line drawing is: (Increment 2 = 2*(min(|dx|,dy|)-max(|dx|,dy|)).

BIT	POSITION
Line Drawing Mode: Increment line parameter 2.	
0-11	Defines increment 2 value
12-15	Unused
BITBLT Copying Mode: Copy X Destination	
0-10	Defines X destination
11	Reserved
12-15	Unused

6.6.5 ERROR TERM REGISTER (READ/WRITE - 92E8H)

The minterm for the line drawing is: 2*[min(dx|,|dy)]-max(|dx,dy|)-1 if starting x ending x, and 2*[min(|dx,|dy|)] - max(|dk|,|dy|) if starting x = ending x. The status of this register, when read after line drawing, is sign extended to 16 bits.

BIT	POSITION
0-12	Defines the delta for the current line drawing. Value is 13 bits signed 2's complement.
13-15	Sign extension.

6.6.6 MAJOR AXIS PIXEL COUNT REGISTER (WRITE ONLY - ADDRESS 96E8H)

This parameter is used for line drawing, BITBLT, or rectangle commands. The value is 11 bits unsigned. When line drawing is specified, the minterm for the line drawing is: Line Parameter = max(|dx|,|dy|). For BITBLT or rectangle commands, Rectangle Width Value = Rectangle Width -1.

BIT	POSITION
0-10	Defines either the width for a rectangle in BITBLT or rectangle mode or defines the length of a line in a line draw.
11-15	Unused

6.6.7 COMMAND REGISTER (WRITE ONLY - ADDRESS 9AE8H)

The CMD Register at Address 9AE8h provides commands for drawing. All parameters have to be set before this command is sent to activate the drawing.

BIT	POSITION
0	R/W: 1 = Write; 0 = Read.
1	Pixel mode: 1 = multi; 0 = single.
2	Last pixel: 1 = off; 0 = on.
3	DIR type: 1 = deg; 0 = XY
4	Draw: 1 = yes; 0 = no.
5-7	Drawing Direction
8	Wait: 1 = yes; 0 = no.
9	Bus select: 1 = 16; 0 = 8.
10	Don't care
11	Reserved
12	Swap MSB/LSB: 1 = yes; 0 = no.
13-15	Drawing function command

BITS 765	DRAWING DIRECTION Bit 3 = 1	Bit 3 = 0
000	0 degrees	Y neg, X major, X neg
001	45 degrees	Y neg, X major, X pos
010	90 degrees	Y neg, Y major, X neg
011	135 degrees	Y neg, Y major, X pos
100	180 degrees	Y pos, X major, X neg
101	225 degrees	Y pos, X major, X pos
110	270 degrees	Y pos, Y major, X neg
111	315 degrees	Y pos, Y major, X pos

BITS 15-13	DRAWING FUNCTION COMMAND
000	No operation
001	Draw line
010	Fill rectangle (Hor. 1st by 4 hor. pixels); Search & fill (see BEE8-A)
011	Fill rectangle (Vert. 1st by 2 vert. pixels - see BEE8-A)
100	Fill rectangle (Vert. 1st by 4 hor. pixels)
101	Draw line (polygon boundary)
110	BITBLT
111	Not defined

10

6.6.8 COMMAND REGISTER (WRITE ONLY - ADDRESS 9AE8H)

BIT	FUNCTION
0	**R/W:** specifies a read operation when set to "0" or a write operation when set to "1".
1	**Pixel Mode:** specifies single pixel mode when set to "0" or a multi-pixel mode when set to "1".
2	**Last pixel Off:** specifies the last pixel drawn when set to "0"; turned off when set to "1".
3	**Dir Type:** specifies the type of line drawing direction as either radial.
4	**Draw:** Specifies draw when set to "1" and updates the drawing point only when set to "0".
5-7	**Drawing Direction:** Specifies the direction of the draw using the direction type indicated by Bit 3.

				4	3	2	1	0	
				Plane 3	Plane 2	Plane 1	Plane 0		**4-bit Bit Plane**
BITBLT	7	6	5	4					
	Plane 6	Plane 5	Plane 4	Plane 3	Plane 2	Plane 1	Plane 0	Plane 7	**8-bit Bit Plane**
	7	6	5	4	3	2	1	0	
	Plane 7	Plane 6	Plane 5	Plane 4	Plane 3	Plane 2	Plane 1	Plane 0	

* = Plane number corresponds to bit number for search and fill

For each plane: 1 = use source; 0 = do not use source

FIGURE 6-1. BIT PLANE READ MASK REGISTER

BIT	FUNCTION (CONT'D)
8	**Wait:** Provides a wait state when set to "1" to allow waiting for CPU data during functions such as image transfer and texture line drawing.
9	**Bus Select:** Specifies that the 16-bit data bus is selected when set to "1"; the 8-bit data bus is selected when set to "0".
10	**Future:** Allows the PAM to interface with two PDM chips. This capability is not currently supported.
12	**Swap MSB/LSB:** When set to "1", specifies that the most significant byte (MSB) be swapped with the least significant byte (LSB) when the 16-bit data bus is selected. Bit 12 is normally set to "0"; the MSB is drawn first, then the LSB.
13-15	**Command type:** Specify the commands for drawing.

6.6.9 SHORT STROKE VECTOR TRANSFER REGISTER (WRITE ONLY - ADDRESS 9EE8H)

Provides two types of data. Each byte specifies the length, direction, and move draw control for a short vector.

BITS	FUNCTION
0-3, 8-11	**Pixel line length**
4, 12	**Move/Draw:** Indicates a draw function when set to "1"; indicates a move function when set to "0".
5-7, 13-15	**Drawing direction:** Specifies the direction of the draw when using the direction type, either radial-based or coordinate-based, as specified by Bit 3 of the CMD register.

BITS	DRAWING DIRECTION	
15 14 13 7 6 5	**Command Register: Bit 3 = 1**	**Bit 3 = 0**
0 0 0	0 degrees	X major, X neg (Left)
0 0 1	45 degrees	X major, X pos (Right)
0 1 0	90 degrees	Y major, Y neg (Up)
0 1 1	135 degrees	Y major, Y neg (Up)
1 0 0	180 degrees	X major, X neg (Left)
1 0 1	225 degrees	X major, X pos (Right)
1 1 0	270 degrees	Y major, Y pos(Down)
1 1 1	315 degrees	Y major, Y pos(Down)

6.6.10 BACKGROUND COLOR REGISTER (WRITE ONLY - ADDRESS A2E8H)

The BKGD_COLOR Register specifies the background color. The MSB in this 8-bit word is not used.

6.6.11 FOREGROUND COLOR REGISTER (WRITE ONLY - ADDRESS A6E8H)

The FRGD_COLOR Register specifies the foreground color. The MSB in this 8-bit word is not used.

6.6.12 WRITE MASK REGISTER (WRITE ONLY - ADDRESS AAE8H)

This register specifies the bit-plane selected for a graphics or text update. The MSB in this word is not used.

BIT	FUNCTION
0-7	Planes 0-7

6.6.13 READ MASK REGISTER (WRITE ONLY - ADDRESS AEE8H)

This register specifies the read source mask for image read or fill operations. The value is the true mask rotated left one bit. Bit 0 is the mask for plane 7 and bits 1-7 are the mask bits for planes 0-6, respectively. However, for polygon fill, bits 2, 3, and 4 are for planes 2, 3, and 4, respectively. The MSB in this word is not used. See Figure 6-1.

6.6.14 COLOR COMPARE REGISTER (WRITE ONLY - ADDRESS B2E8H)

This register specifies the comparison color. The MSB in this 8-bit word is not used.

6.6.15 BACKGROUND MIX REGISTER (WRITE ONLY - ADDRESS B6E8H)

This register specifies the background mix. The MSB in this word is not used.

BIT	FUNCTION
0-4	Background mix command
5,6	Color select

BITS 6 5	BACKGROUND SOURCE SELECT
0 0	BGC
0 1	FGC
1 0	CPU data
1 1	Display memory

6.6.16 FOREGROUND MIX REGISTER (WRITE ONLY - ADDRESS BAE8H)

This register specifies the foreground mix. The MSB in this 16-bit word is not used.

BIT	FUNCTION
0-4	Foreground mix command
5,6	Color select
7-15	Unused

BITS 6 5	FOREGROUND SOURCE SELECT
0 0	BGC
0 1	FGC
1 0	CPU data
1 1	Display memory

BITS 4-0	FOREGROUND MIX COMMAND
00	Not screen
01	Zero
02	One
03	Leave alone
04	Not new
05	XOR
06	Not screen XOR new
07	Overpaint
08	Not screen or not new
09	Screen or not new
0A	Not screen or new
0B	Screen or new
0C	Screen and new
0D	Not screen and new
0E	Screen and not new
0F	Not screen and not new
10	Minimum
11	(Screen-new) without saturate
12	(New-screen) without saturate

BITS 4-0	FOREGROUND MIX COMMAND
13	(New+screen) without saturate
14	Maximum
15	(Screen-new)/2 without saturate
16	(New-screen)/2 without saturate*
17	Average = (new + screen)/2 w/o saturate
18	(Screen-new) with saturate
19	(Screen-new) with saturate
1A	(New-screen) with saturate
1B	(New+screen) with saturate
1C	(Screen-new)/2 with saturate
1D	(Screen-new)/2 with saturate
1E	(New-screen)/2 with saturate**
1F	(Screen + new)/2 with saturate
*Borrow included in shifting	
**Set to 0 in borrow = 1	

6.6.17 MULTIFUNCTION CONTROL REGISTER (WRITE ONLY - ADDRESS BEE8-0,1,2,3,4)

This register specifies several drawing control parameters. Bits 15-12 control the use of this register. When these bits are changed, the register changes function.

BIT	FUNCTION
0-10	Rectangle/clipping parameter value
11	Reserved (don't care for BEE8-0)
12-15	Drawing select

15 14 13 12	ADDR	PARAMETER
0 0 0 0	BEE8-0	Minor Axis Pixel Count Index
0 0 0 1	BEE8-1	Top Scissors Index
0 0 1 0	BEE8-2	Left Scissors Index
0 0 1 1	BEE8-3	Bottom Scissors Index
0 1 0 0	BEE8-4	Right Scissors Index

Minor Axis Pixel Count Index (MIN_AXIS_PCNT) - When bits 15-12 are set to 0, the value of bits 10-0 specifies the rectangle height. Value = rectangle height - 1

Top Scissors Index (SCISSORS_T) - When bits 15-12 are set to 1, the value of bits 10-0 specifies the clipping window top limit.

Left Scissors Index (SCISSORS_L) - When bits 15-12 are set to 3, the value in bits 10-0 specifies the clipping window left limit.

Bottom Scissors Index (SCISSORS_B) - When bits 15-12 are set to 3, the value of bits 10-0 specifies the clipping window bottom limit.

Right Scissors Index (SCISSORS_R) - When bits 15-12 are set to 4, the value in bits 10-0 specifies the clipping window right limit.

Note: Reading display memory outside of the clipping window returns the content of that memory location.

6.6.18 MEMORY CONTROL INDEX REGISTER (WRITE ONLY - ADDRESS BEE8-5)

BIT	FUNCTION
0,1	X coordinate control: Reserved, Bit 0 should be set to "0". Bit 1 should be set to "1".
2,3	Y coordinate control: Specifies resolution.
4	Specifies planes for drawing: "0" specifies lower 4 planes; "1" specifies upper 4 planes.
5-7	Reserved
8-11	Unused
15-12	Selects memory configuration when set to "0101".

Y Coordinate Control	3 2	Resolution
Skip Z & YI	0 0	640x480x4 (Bit 1 of 22E8H must be 0)
Skip Y2	0 1	1024x768 or 640x480x8
Not used	1 0	Not defined
Not used	1 1	Not defined

6.6.19 FIXED PATTERN LOW INDEX REGISTER FIXED PATTERN HIGH INDEX REGISTER (WRITE ONLY - ADDRESS BEE8-8, BEE8-9)

BIT	POSITION
0	Bit 0 = 0
5-11	Unused
Fixed Pattern Low Index Register (PATTERN_L):	
4-1	Specifies pixel position mix control for pixels 0-3. A "0" selects the background color source; "1" selects the foreground color source (if enabled by bits 6,7 of the Pixel Control Index Register).
15-12	When set to 8, Fixed Pattern Low is selected.
Fixed Pattern High Index Register (PATTERN_H):	
4-1	Specifies pixel position mix control for pixels 4-7. A "0" selects the background color source; "1" selects the foreground color source (if enabled by bits 6,7 of the Pixel Control Index Register.
15-12	When set to 9, Fixed Pattern High is selected.

6.6.20 PIXEL CONTROL INDEX REGISTER (WRITE ONLY - ADDRESS BEE8-A)

BIT	POSITION
0	Bit 0 = 0
1	Mask select poly-fill operations. Read mask = 0; write mask = 1.
2	Packed Data/Search Enable
3-5	Data compare
6-7	These bits define the source of the bit pattern used to select color and the mix operation to be used.
11-8	"0000"
15-12	"1010"

Bit 2	Packed Data		Use
1	Enabled	Read	Read packed data
		Write	Search and fill mode
0	No	Read/Write	Normal

BITS 3-5	COMPARISON TYPE
0	False (always draw)
1	True (never draw)
2	Plane data > = comparison
3	Plane data < comparison
4	Plane data <> comparison
5	Plane data = comparison
6	Plane data <= comparison
7	Plane data > comparison

7 6	**Data Extension** Bit pattern from the following source	**Use** Depending on the color source and mix
0 0	Bit pattern always = 1; BGRD_MIX not used.	BAE8h bits 6,5 = "01" → regular solid BAE8h bits 6,5 = "10" → regular image write BAE8h bits 6,5 = "11" → regular BIT BLT
01	Pixel position mix control (BEE8-8,9)	BAE8h bits 6,5 = "01" → horizontal text line B6E8h bits 6,5 = "00" → horizontal text line
1 0	CPU pixel data	FMX → CPU 10-bit pattern image BMX → transfer to display memory BAE8h bits 6,5 = "01"; B6E8h = "00": image write across the plane or from 1 bit plane to FGC and BGC

10

Bits 7 6	Data Extension Bit pattern from the following source	Use Depending on the color source and mix
10	Display memory used to display packed data* bit pattern	BAE8h bits 6,5 = "01"; B6E8h bits 6,5 = "00": BITBLT across the plane or from 1 bit plane to FGC and BGC BAE8h bits 6,5 = "10"; B6E8h bits 6,5 = "00": Special multicolor marker mode**

* Packed data - During a read operation, packed data is computed from the source. Packed Data is defined as "the screen data ORed with the complement of the bit plane read mask". If the result is all 1's, then "1" is extracted, otherwise a "0" is extracted per pixel. When a write operation is selected, WD9500 goes into a special search and fill mode. The screen data is read and, if the packed data extracted is "0", the write operation is suspended. When a paced data "1" is encountered, the write operation is enabled until the next "1". This mode is used to detect the boundary of a polygon for fill operation.

** Marker - special BITBLT mode used for multi-color marker. A "10" pattern is stored in display memory. During BITBLT, if display memory data = 1, CPU data is used.

6.6.21 PIXEL DATA TRANSFER REGISTER (READ/WRITE - ADDRESS E2E8H)

The Pixel Data Transfer (PIX_TRANS) Register specifies the read/write port for image transfer. For an across-the-plane image transfer, read/write data is determined by the nibble boundary on the screen. The starting point falls on the first nibble group for word mode. Two nibbles of data can be transferred for each read/write. For through-the-plane image transfer, two pixels can be transferred for each read/write operation in work mode.

BIT	FUNCTION
	Across The Plane
0, 6-8, 13-15	Unused T-52-33-45
4-1	Pixel read/write value: Pixels 4-7
12-9	Pixel read/write value: Pixels 0-3
	Through the Plane
0-7	Pixel 2: bp0-bp7
8-15	Pixel 1 if 16-bit mode selected: bp0-bp7

Note: For Image Read operation, all data (including the last pixel) must be read from the CPU before issuing a new command to the Graphics Processor.

6.7 STATUS REGISTERS

There are three status registers that can be read to acquire information: the Subsystem Status (SUBSYS_STAT) register at address 42E8h, the Graphics Processor Status (GP_STAT) register at address 9AE8h, and the Display Status (DISP_STAT) register at address 02E8h.

6.7.1 SUBSYSTEM STATUS REGISTER (READ ONLY - ADDRESS 42E8H)

Subsystem Status Register (SUBSYS_STAT) Register provides interrupt status, monitor ID, and plane size.

BIT	FUNCTION
0	**Vsync:** when set to "1", it indicates a vertical sync interrupt.
1	**Window Hit:** When set to "1", indicates
2	**FIFO Overflow:** When set to "1", indicates FIFO overflow.
3	**GE Idle:** When set to "1", indicates
4-6	**Monitor ID:** Indicates the monitor type being driven by the WD9500 or 8514/A.
7	**Plane size:** Indicates a 4-bit plane when set to "0" or an 8-bit plane when set to "1".
8-15	Reserved for hardware test.

Address Decoding Table for Read				
Bits 15-12 / 11-0	**2e8**	**6e8**	**ae8**	**ee8h**
0	2e8	2e8	2e8	2e8
1	2e8	2e8	2e8	2e8
2	2e8	2e8	2e8	2e8
3	2e8	2e8	2e8	2e8
4	42e8	42e8	42e8	42e8
5	42e8	42e8	42e8	42e8
6	42e8	42e8	42e8	42e8
7	42e8	42e8	42e8	42e8
8	82e8	86e8	0*	0*
9	92e8	0*	9ae8	0*
a	e2e8	e2e8	0*	0*
b	0*	0*	0*	0*
c	82e8	86e8	0*	0*
d	92e8	0*	9ae8	0*
e	e2e8	e2e8	0*	0*
f	0*	0*	0*	0*

* A value of zero will be read.

Address Decoding Table for Write				
Bits 15-12 / 11-0	**2e8**	**6e8**	**ae8**	**ee8h**
0	2e8	6e8	ae8	ee8
1	12e8	16e8	1ae8	1ee8
2	22e8	X	X	X
3	X	X	X	X
4	42e8	46e8	4ae8	X
5	42e8	46e8	4ae8	X
6	42e8	46e8	4ae8	X
7	42e8	46e8	4ae8	X
8	82e8	86e8	8ae8	8ee8
9	92e8	96e8	9ae8	9ee8
a	a2e8	a6e8	aae8	aee8
b	b2e8	b6e8	bae8	bee8
c	82e8	86e8	8ae8	8ee8
d	92e8	96e8	9ae8	9ee8
e	a2e8	a6e8	aae8	aee8
f	b2e8	b6e8	bae8	bee8

TABLE 6-5. ADDRESS DECODING TABLES FOR 8514/A REGISTERS

6 5 4	Monitor ID
0 1 0	8514/A color 16"
1 0 1	VGA 8503 mono 12"
1 1 0	VGA 8513 color 12"
1 1 0	VGA 8512 color 14"
1 1 1	No monitor or other monitor

6.7.2 GRAPHICS PROCESSOR STATUS REGISTER (READ ONLY - ADDRESS 9AE8H)

Provides FIFO status information. PC read data status, and hardware busy status.

BIT	FUNCTION
7-0	FIFO Entries 7-0: Indicates data status of the FIFO (i.e., a "1" indicates that an input entry is occupied by data.
8	Data Available: Indicates that PC read data is available when set to "1"; not available when set to "0".
9	Hardware Busy: Indicates that the hardware is busy when set to "1"; not busy when set to "0".
15-10	Not used.

6.7.3 DISPLAY STATUS REGISTER (READ ONLY - ADDRESS 02E8H)

Provides video status information.

BIT	FUNCTION
0	Analog RGB signal test: 0 = R, G, or B greater than 0.30 volts; 1 = R, G, and B all less than 0.30 volts
1	Vertical Sync
2	Line Count
3	0
4-15	Unused

Table 6-5 illustrates how the addresses are decoded for 8514/A compatible registers. The leftmost column gives the hexadecimal value of address bits 15-12, and the top row shows the value of the rest of the twelve address bits. For example, the read address A2E8 (hex) is decoded as "E2E8" column at the a-th row. This also means an I/O read from A2E8 is the same as if reading from address E2E8, the IRW register. Address decoding for a read operation is different from that for a write operation.

6.8 SOFTWARE INTERFACE EXTENSIONS T-52-33-45

Suitable CPU Adapter interface software (AI), such as the Western Digital Adapter Interface (WDAI), can make use of the WD9500's advanced capabilities by invoking "Western Digital Enhanced Mode" on a short-term basis as explained later. There are two advantages to using this software interface design. First, a WD9500-based board can be inserted into a system with no change in software, and it will function as a faster 8514/A. Second, it provides for performance enhancement for custom software. In order to minimize future register conflict, all functions for Western Digital Enhanced Mode are implemented using register address, 96E8h (BEE9 can also be usedh). A dummy I/O read at address 28E9h must precede any access to 96E8h for the Western Digital Enhanced Mode. Under 8514/A emulation mode. Location 96E8h is a write only register for rectangle width.

To identify the WD9500 chip set, see Figure 6-2. To escape to Western Digital Enhanced Mode, the AI should execute a byte read of I/O address 28E9h. (The purpose of the byte read is to perform the escape; the WD9500 does not return any data). This operation is a no-op for the IBM 8514/A since it involves a write-only register, which furthermore does not respond to any access to an odd-numbered byte address. This operation tags the next register access through a special bit in the FIFO. FIFO is fully functional in Western Digital Enhanced Mode. After escaping to Western Digital Enhanced Mode, the WD9500 automatically resets itself back to 8514/A emulation mode in one of these four circumstances:

1. If, at its next board access immediately after the escape, the AI reads the Western Digital Status Register (I/O address 96E8h).
2. If, at its next board access immediately after escape, the AI writes to one of the six Western Digital Control Registers or to the

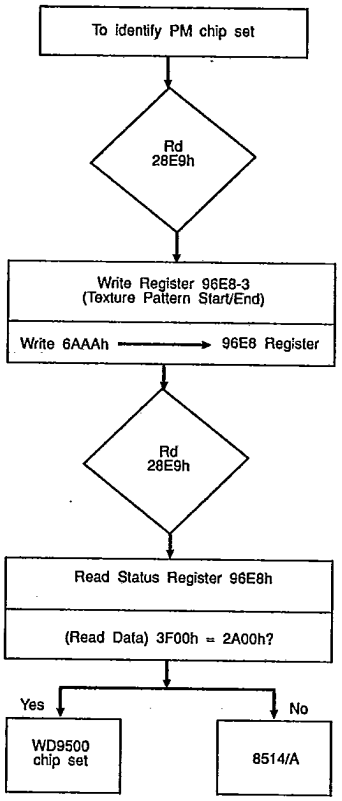


FIGURE 6-2. METHOD OF IDENTIFYING WD9500 CHIP SET

Rectangle Width Register (I/O address 96E8h).

3. If, at its next board access immediately after an escape, the AI writes to either I/O address 82E8 (register name in 8514/A Emulation Mode: Copy Y Destination/Incr 1 Register). Figure 6-2.

The purpose of the second two, however, deserves explanation. Western Digital enhancements simplify and speed line drawing commands in two ways: first, line drawing parameters are simpler, in that the AI needs to specify only the pixel coordinates of the line's end point, rather than the tediously calculated parameters used by the 8514/A. Therefore, the WD9500-SET1 needs to be in Western Digital Enhanced Mode to "know" that the write into register 8AE8 contains the Y ending point parameter, in preparation for line-drawing command (case 4). Second, in 640x480 resolution, the WD9500-SET1 can, through Western Digital Enhanced Mode, make use of a much simpler Y-coordinate format than is required by the 8514/A. In the Western Digital Enhanced Mode the WD9500-SET1 is notified that this simpler format is being written to one of the Y-coordinate registers (82E8 or 8AE8, case 3 above). The parameters are defined in Section 6.9, "Enhanced Solid Line Drawing".

The same system I/O address (96E8) is used to access the Western Digital Status Register, and all six of the Western Digital Control Registers.

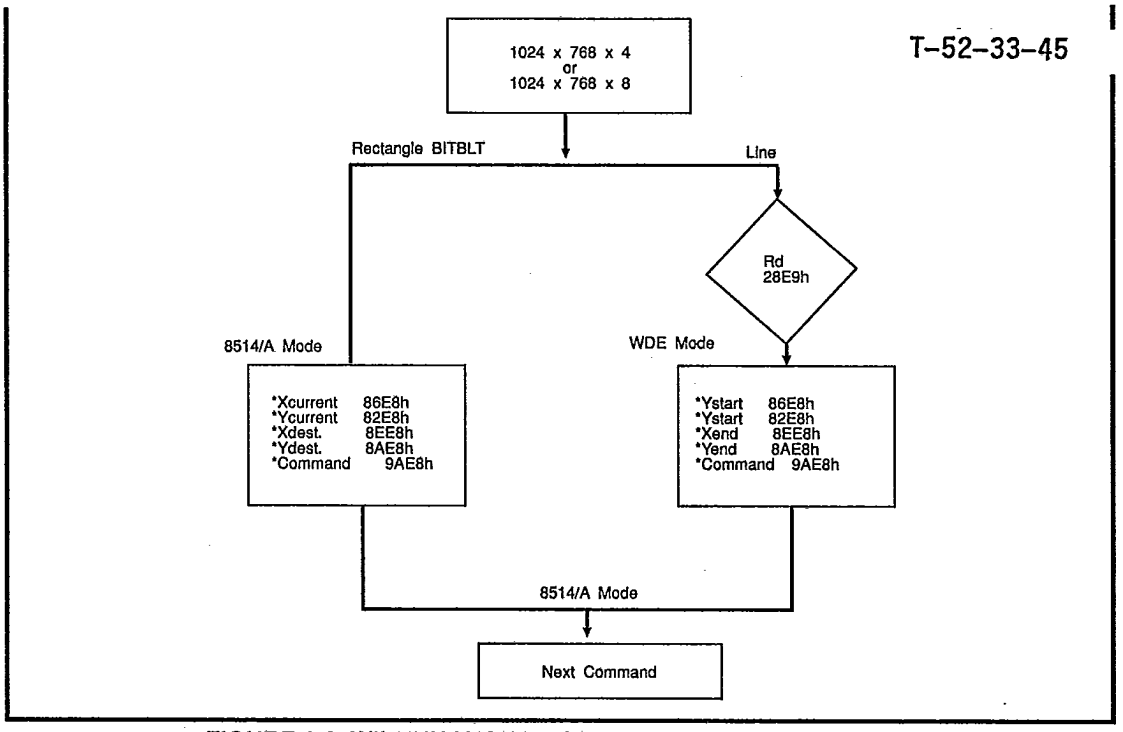


FIGURE 6-3. WD ENHANCED MODE / 1024 X 768 RESOLUTION

In 8514/A Emulation Mode, this address is that of the Rectangle Width Register.

6.8.1 WESTERN DIGITAL ESCAPE REGISTER (READ ONLY - ADDRESS 28E9)

A read of the Western Digital Escape Register allows access to WD enhancements. The data returned is not significant.

6.8.2 WESTERN DIGITAL STATUS REGISTER (READ ONLY - 96E8H)

BIT	FUNCTION
0	VRAM type: 1 = 256k; 0 = 64k
1,2	Number of VRAM chips
3	Resolution: indicates the maximum resolution permitted by the VRAM design. When set to "0", it indicates 1024x768; when set to "1", it indicates 1280x1204.
4	Pal Write: indicates whether a palette write is pending. When set to "0", a palette write is not pending; when set to "1", a palette write is pending.
5	DAC Type: Indicates whether the DAC used is 6-bit only or a switchable 6-bit/8-bit. The 6-bit/8-bit DAC allows compatibility at 6-bit color to 8514/A and a large 8-bit color palette that requires special programming. 1 = 6/8 bit color; 0 = 6-bit color only.
7, 6	Monitor Selection
13-8	Current texture pattern position
15, 14	Chip set revision number

A byte read at 28E9 followed by a 16-bit read of this address, 96E8, yields the contents of the

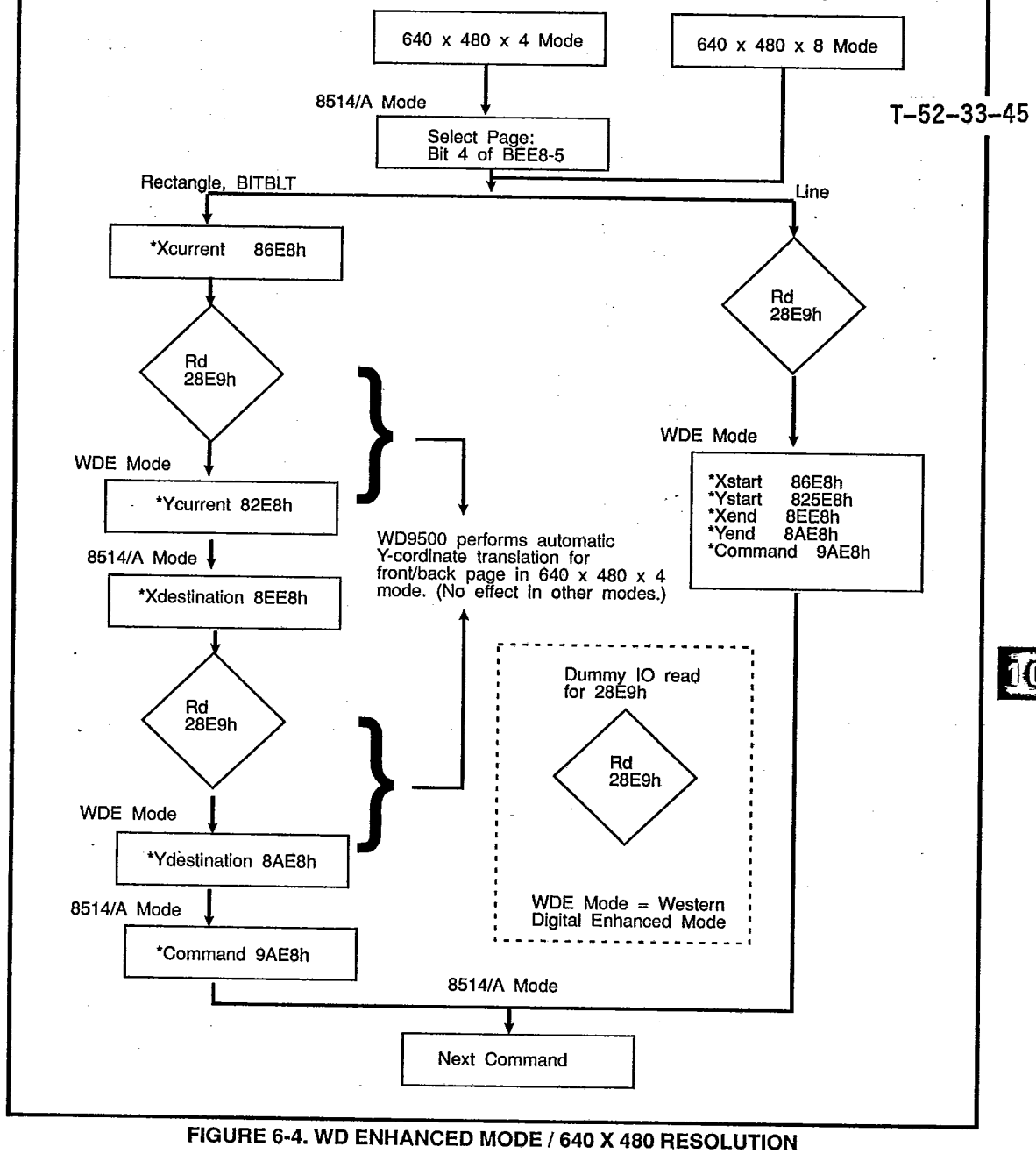


FIGURE 6-4. WD ENHANCED MODE / 640 X 480 RESOLUTION

Western Digital Status Register. Note that in 8514/A Emulation Mode, 96E8 is a write-only register.

6.8.3 WESTERN DIGITAL CONTROL REGISTER (WRITE ONLY - ADDRESS 96E8)

In Western Digital Enhanced Mode, when a 16-bit write is made to address 96E8, the WD9500-SET1 interprets the highest three bits as a selection of one of six Western Digital Control Register destinations for the lower 13 bits of data. In this sense, address 96E8 can be thought of as a "gateway" for writes to the six Western Digital Control Registers, and the notations 96E8-1,96E8-2,...., 96E8-7 are used to refer to those registers. Note also that this design provides "double insurance" against accidental 8514/A-mode access to these registers. First, they can be accessed only after escaping to Western Digital Enhanced Mode. Secondly, the rectangle width parameter should never be so large as to involve 1-bits in the three highest bit positions of the 16-bit data field (and in fact, "96E8-1" leads to the "real" rectangle width register). When Bits 15-13 are set to "011", bits 12-6 specify the texture pattern ending position. Bits 5-0 specify the texture pattern starting position within the 48 bits available in the four texture pattern registers (see "Textured Line Drawing", section 6.10). Bit 12 is unused. The following table defines the Western Digital Enhanced Mode Register (ie., bits 12-0 of 96E8 when bits 15-13 = 001). All the control fields in this register are one-bit mode control. They select between two alternate modes, and the selected mode remains in effect through all future operations until the AI changes it by inverting the associated control bit.

BIT	FUNCTION
0	**Pixel Depth:** Specifies the number of bit planes to be used in all operations. Four-bit planes are specified when set to "0"; 8-bit planes are specified when set to "1".
1	**Page Select Draw:** In modes other than 640x480x4, bit 1 specifies screen page selection for drawing (if the VRAM supports two screen pages at the current resolution). Page 1 is selected when set to "0" and page 2 is selected when set to "1". Note that the page select controls provide a simple mechanism for drawing in the background so that the user can instantly replace one screen image with another.
2	**Page Select View:** In modes other than 640x480x4, bit 2 specifies screen page selection for viewing (source of screen refresh). Page 1 is selected when set to "0" and page 2 is selected when set to "1". Note that the page select controls provide a simple mechanism for drawing in the background so that the user can instantly replace one screen image with another.
3	**Mode Extension:** In conjunction with Bit 2 of register 4AE8 this bit is used to select different resolutions. Bit 3 = 0 is the default for 8514/A resolution modes (i.e., 1024x768 and 640x480).
4	**Flicker-free mode:** Setting this bit to "1" enables the flicker-free palette loading mode. A "0" clears the mode.
5	**Texture Mode:** Setting this bit to "1" enables the textured line mode and a "0" clears the mode.

MODE EXT.	8513/A MODE	MONITOR TYPE (BIT 8)	VERTICAL REFRESH FREQUENCY (BIT 7)	CLKSEL 2-0 T-52-33-45
0	0	X	0	**000**, 640x480, 60 Hz
0	0	X	1	**100**, 640x480, 70 Hz
0	1	0	0	**001**, 1024x768, 43 Hz
0	1	1	0	**011**, 1024x768, 60 Hz
0	1	X	1	**111**, 1024x768, 70 Hz

TABLE 6-5. MONITOR TYPE AND VERTICAL REFRESH FREQUENCY

BIT	FUNCTION
6	**DAC Palette:** Used only if the board has a 8/6 bit/color switchable DAC. (See Selection, Western Digital Status Register.) Bit 6 = 1 selects 6-bit/color mode (default); Bit 6 = 1 = 8-bit DAC.
8-7	**Monitor Type and Vertical Refresh Frequency:** Combined with the mode extension bit and 8514/A bit (Bit 2 of 4AE8), these bits set the CLKSEL values that select the pixel clock frequency. Bit 2 of 4AE8 automatically selects a proper frequency after the control bits are programmed by the BIOS. When Bit 7 is set to "0", it selects a vertical refresh frequency of 60 Hz or 43 Hz; when set to "1", it selects 70 Hz. When bit 8 is set to "0", it selects a 43 Hz monitor type; when set to "1", it selects 60 Hz/70 Hz. (See Table 6-5.)
9	**Standard Video Registers Enable:** Controls the programming of the standard video registers. The default "0" setting disables loading.
10	**Standard Video Registers Ena ble:** Controls the programming of the alternate video registers (WD9500 extended feature). The default "0" setting disables loading.

BIT	FUNCTION
11	When set, this bit causes a wait on I/O read or write cycles (when address Bit 14 is set). When Bit 11 is "0", wait is disabled.
12	This bit specifies the length of wait for I/O access when address bit 14 is set. A "0" specifies 4.8 µseconds; " 1" specifies ? µseconds.
15-13	Western Digital Control Register Select (see below)

BITS 15 14 13	Western Digital Control Registers
0 0 0	Rectangle Width Register (96E8-0) (Same as regular 8514A register)
0 0 1	Western Digital Enhanced Mode Register (96E8-1)*
0 1 0	Reserved (96E8-2)
0 1 1	Texture Pattern Start/End (96E8-3)*
1 0 0	Texture Pattern 11-0 (96E8-4)*
1 0 1	Texture Pattern 23-12 (96E8-5)*
1 1 0	Texture Pattern 35-24 (96E8-6)*
1 1 1	Texture Pattern 47-36 (96E8-7)*

* Accessed only after a dummy read operation at address 28E9h.

6.8.4 TEXTURE PATTERN START/END REGISTER (WRITE ONLY - ADDRESS 96E8-3)

BIT	FUNCTION
5-0	Starting Bit Position
11-6	Ending Bit Position
12	Reserved
15-13	0 1 1

BITS 10 9	DESCRIPTION
0 1	Load standard video timing registers (default)
1 0	Load alternate video timing registers
1 1	Load both register sets
0 0	Activate automatic switching between register sets and locks registers 4AE8h Bit 2 = 0 (640x480) selects Standard Register Set; bit 2 = 1 (1024x768) selects Alternate Register Set

BIT 3	4AE8 BIT 2	RESOLUTION
0	0	640x480
0	1	1024x768
1	0	800x600
1	1	1280x1024

6.9 ENHANCED SOLID LINE DRAWING

The following procedure should be used to draw a solid line in Western Digital Enhanced Mode:

1. Escape to Western Digital Enhanced Mode by doing a byte read of I/O address 28E9.
2. Write the X pixel coordinate of the beginning point of the new line to I/O address 86E8 (Current X Drawing Point Register). If this value has not changed since the last drawing operation (i.e. the new line will start with the X-coordinate of the current drawing point), then the X pixel coordinate of the ending point of the new line should be written to I/O address 8EE8 (Ending X Register in Western Digital Enhanced Mode), even if that X coordinate has not changed. At least one of the two X-coordinate registers must be loaded prior to loading a Y-coordinate register in order to avoid leaving Western Digital Enhanced Mode prematurely. T-52-33-45
3. Write the Y pixel coordinate of the beginning point of the new line to I/O address 82E8 (Current Y Drawing Point Register). If the value has not changed since the last drawing operation (i.e., the new line will start with the Y-coordinate ending point of the last line), this step may be skipped.
4. Unless already completed in step 2, write the X pixel coordinate of the ending point of the new line to I/O address 8EE8 (Ending X Register in Western Digital Enhanced Mode). If this value has not changed since the last drawing operation, this step may be skipped.
5. Write the Y pixel coordinate of the ending point of the new line to I/O address 8AE8 (Ending Y Register in Western Digital Enhanced Mode). This step has to be performed in order to start the line parameter calculation.
6. Conclude by writing the standard line drawing command to the Command Register at I/O address 9AE8.

Western Digital Enhanced Mode simplifies the calculation of Y coordinates when using two pages, including the case of 640x480 resolution. In contrast to the 8514/A Emulation Mode. Western Digital Enhanced Mode requires no transformations; the desired page-oriented Y coordinate can be written directly into the Y-coordinate register. The coordinates apply to the page selected by the 640x480x4 drawing page selection bit in the MEM_CNTL register. In both 8514/A Emulation Mode and Western Digital Enhanced Mode, however, the user must be aware of pixel coordinate usage with regard to boundaries.

First, under all circumstances, X and Y coordinates wrap around at the 2K boundary; in other words, pixel coordinates are processed as 11-bit values and hence manipulated modulo 2048.

Second, under all circumstances, Y coordinates between 1K and 2K are "lost" (i.e., drawn objects or parts of drawn objects whose Y coordinates are between 1K and 2K are not recorded in VRAM.)

Third, where only one page is available (except for the 1280x1024 case), X coordinates between 1K and 2K are similarly "lost".

Fourth, where two pages are available, first-page X coordinates between 1K and 2K will "intrude" into the second page (modulo 1024), and second page X coordinates between 1K and 2K will intrude into the first page (modulo 1024). When two pages are provided, the 1Kx1K pages are arranged "side by side" in physical memory with the logical (page-oriented) X coordinate internally processed as a physical X coordinate between 0 and 2K. The intrusion can be avoided by establishing clipping boundaries at the 1K page limit (or less).

Finally, images drawn within a (1K by 1K) page but beyond the screen viewing boundary (1Kx768 or 640x480) are not "lost", and can be copied from their "off-screen" location into the viewing area by a BITBLT operation. In the (single page) case of 1280x1024 resolution, "off-screen" storage is provided for coordinates between 1280 and 2K.

6.10 TEXTURED-LINE DRAWING

In Western Digital Enhanced Mode, textured lines can be drawn directly. After the "texture pattern" and its pointers have been set up, the AI needs only to turn on the textured-line mode by setting control bits 7 and 6 (BEE8-A) to "01", setting bits 6 and 5 (BAE8) to "01", and then using the same procedure as for solid-line drawing (see "Enhanced Solid-Line Drawing" in Section 6.9). The texture pattern is a string of bits whose 0/1 values are consulted in sequence as the WD9500 draws the line, applying the current mix to the combination of current texture-pattern bit and current pixel. (For example, a "1" bit in the texture pattern might be interpreted as an overpaint instruction). The pattern may be up to 48 bits long. Four Western Digital Control Registers 96E8-4, 96E8-5, 96E8-6, and 96E8-7 are provided for its storage. (Bit 12 of each of these registers is reserved.) The pattern must be defined beginning at Bit 47, but need not continue to Bit 0; the 6-bit "ending position" field in Western Digital Control Register 96E8-3 is provided to specify the number of its last bit. The related 6-bit "starting position" field, however, is used differently. It specifies where (between Bit 47 and the ending-position bit) the texture-pattern pointer should be placed. This pointer marks the beginning of a textured line-drawing process from the start position toward the defined ending position (i.e., from high-order to low-order bits within the texture pattern). After the WD9500-SET1 uses the texture-pattern bit at the ending position, it circulates the pointer back, not to the specified starting position but to Bit 47, and then repeats the process. After the line is complete, the WD9500-SET1 places the current position of the texture-pattern pointer into the appropriate field within the Western Digital Status Register, where it may be read by the AI. If the user does not store a new value into the starting position field, then in its next textured-line-drawing operation, the WD9500 uses the current pointer from the status register. The chief purpose of this feature is the convenience of allowing the user to automatically continue a texture pattern from one line to the next without needing to do an explicit read and write of the pointer position. For example, a dashed line will properly turn a corner without user concern for the texture pattern pointer. Note that after board reset, all texture controls, including current position, are undefined, and must be initialized by the AI. T-52-33-45

6.11 FLICKER-FREE PALETTE LOADING

When using the IBM 8514/A, the CPU must wait for vertical screen refresh before reloading its color palette. In a high resolution design, however, especially with a non-interlaced monitor, the vertical retrace time (typically less than 600 microseconds) may not be long enough to program all 256 color entries. When the Western Digital flicker-free option is incorporated into the design of a WD9500-based board ("Video DAC and Interface Subsystem" in Section 3.3), the WD9500-SET1 can accept palette writes from the CPU at any time, but buffers them in the DSP until horizontal retrace time. During horizontal flyback, it writes them to the DAC's palette, avoiding flicker. Note that in VGA pass-through mode, any VGA palette-loading operation also loads the DAC on the 8514/A (and hence will do the same on a WD9500-based board). Flicker-free programming

I/O ADDRESS	READ/WRITE	FUNCTION
O2EA/03C6	R/W	DAC Mask
O2EB/03C7	W	DAC Read Index
O2EB/03C7	R	DAC State
O2EC/03C8	R/W	DAC Write Index
O2ED/03C9	R/W	DAC Data
02E8	R	Display Status
02E8	W	Horizontal Total
06E8	W	Horizontal Displayed
0AE8	W	Horizontal Sync Start
0EE8	W	Horizontal Sync Width
12E8	W	Vertical Total
16E8	W	Vertical Displayed
1AE8	W	Vertical Sync Start
1EE8	W	Vertical Sync Width
22E8	W	Display Control
42E8	W	Subsystem Status
42E8	W	Subsystem Control
46E8	W	ROM Page Select (MC)
4AE8	W	Advanced Function Control
82E8	R/W	Current Y Position
86E8	R/W	Current X Position
8AE8	W	Destination Y Position/Axial Step Constant
8EE8	W	Destination X Position/Diagonal Step Constant
92E8	R/W	Error Term
96E8	W	Major Axis Pixel Count
9AE8	R	Graphics Processor Status
9AE8	W	Command
9EE8	W	Short Stroke Transfer
A2E8	W	Background Color
A6E8	W	Foreground Color
AAE8	W	Write Mask
AEE8	W	Read Mask

TABLE 6-6. IBM 8514/A COMPATIBLE REGISTERS

does not apply in VGA pass-through mode. Flicker-free mode is enabled by setting Bit 4 of the Western Digital Enhanced Mode Control Register. When sending color data to the board, however, the AI must monitor Bit 4 of the Western Digital Status Register. If set, this bit indicates that a palette write is pending, and no further palette color data should be sent until the WD9500 clears

I/O ADDRESS	READ/WRITE	FUNCTION
B2E8	W	Color Compare
B6E8	W	Background Mix
BAE8	W	Foreground Mix
BEE8		Multifunction Control
BEE8(0)	W	Minor Axis Pixel Count
BEE8(1)	W	Top Scissors
BEE8(2)	W	Left Scissors
BEE8(3)	W	Bottom Scissors
BEE8(4)	W	Right Scissors
BEE8(5)	W	Memory Control
BEE8(8)	W	Fixed Pattern - Low
BEE8(9)	W	Fixed Pattern - High
BEE8(A)	W	Pixel Control

TABLE 6-6. IBM 8514/A COMPATIBLE REGISTERS (CONT'D)

I/O ADDRESS	READ/WRITE	FUNCTION
28E9	R	Dummy Read/Enable for 96E8
36E8	W	EPROM Select--AT Bus Only
8AE8	W	Ending X Point for Line
8EE8	W	Ending Y Point for Line
96E8	R	Western Digital Status
96E8(1)	W	Western Digital Enhanced Mode
96E8(3)	W	Texture Pattern Start End
96E8(4)	W	Texture Pattern 11-0
96E8(5)	W	Texture Pattern 23-12
96E8(6)	W	Texture Pattern 35-24
96E8(7)	W	Texture Pattern 47-36

TABLE 6-7. WD9500 ENHANCED REGISTERS

the bit. When clear, the AI can then send three bytes, representing the contents of one of the 256 entries in the palette. Other AI accesses of the DAC, including reading color values, are independent of the flicker-free design, and should emulate 8514/A operations.

A.0 APPENDIX A - PIN DIAGRAMS

A.1 WD9500 (PAM)

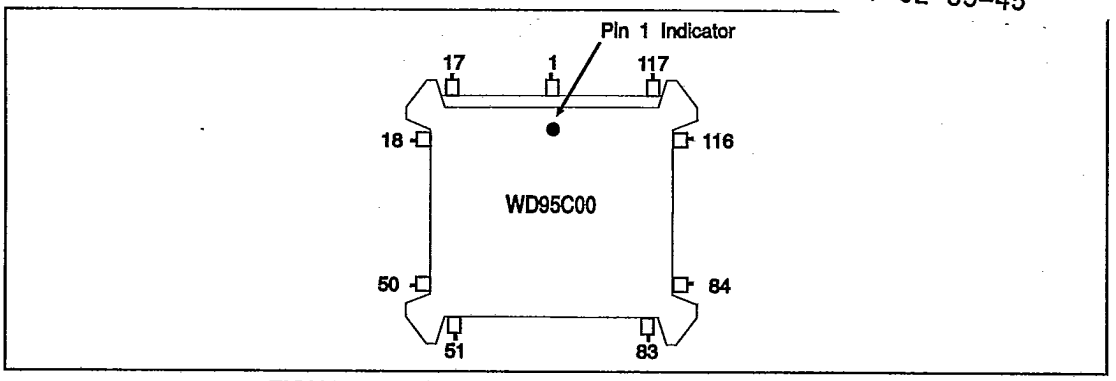


FIGURE A-1. WD95C00 132-PIN JEDEC FLAT PACK

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	VSS	24	$\overline{WE0}$ (O)	47	BSA10 (O)	70	VDD
2	SELVD (i)	25	$\overline{WE1}$ (O)	48	BSA11 (O)	71	A8(I)
3	MDT0 (O)	26	$\overline{WE2}$ (O)	49	BSA12 (O)	72	A9(I)
4	MDT1 (O)	27	$\overline{WE3}$ (O)	50	VDD	73	A10(I)
5	MDT2 (O)	28	$\overline{WE4}$ (O)	51	VSS	74	A11(I)
6	WROE (O)	29	$\overline{WE5}$ (O)	52	RESET (I)	75	A12(I)
7	SWAP (O)	30	$\overline{WE6}$ (O)	53	BSA13 (O)	76	A13(I)
8	$\overline{RWCAS}$ (O)	31	$\overline{WE7}$ (O)	54	BSA14 (O)	77	A14(I)
9	VSS	32	$\overline{DT/OE}$ (O)	55	$\overline{DS/IO16}$ (O)	78	A15(I)
10	MAO(O)	33	VSS	56	$\overline{SBHE}$ (I)	79	A16(I)
11	MA1 (O)	34	LA13 (O)	57	MIO/$\overline{MEMR}$ (I)	80	A17(I)
12	MA2 (O)	35	LA24 (O)	58	$\overline{S1/IOR}$ (I)	81	A18(I)
13	MA3 (O)	36	$\overline{BIOS\ OE}$ (O)	59	$\overline{S0/MEMW}$ (I)	82	A19(I)
14	MA4 (O)	37	BSA0 (O)	60	$\overline{CMD/IOW}$ (I)	83	VSS
15	MA5 (O)	38	BSA1 (O)	61	$\overline{ADL/BALE}$ (I)	84	ATCLK(I)
16	MA6 (O)	39	BSA2 (O)	62	A0(I)	85	AUP(I)
17	VDD	40	BSA3 (O)	63	A1(I)	86	$\overline{SETUP}$/ AEN(I)
18	VSS	41	BSA4 (O)	64	A2(I)	87	VSS
19	MA7 (O)	42	BSA5 (O)	65	A3(I)	88	$\overline{IRQ}$ (O)
20	$\overline{CAS12}$ (O)	43	BSA6 (O)	66	A4(I)	89	$\overline{CDSFDBK}$ (O)
21	$\overline{CAS34}$ (O)	44	BSA7 (O)	67	A5(I)	90	CHRDY (O)
22	$\overline{RAS0}$ (O)	45	BSA8 (O)	68	A6(I)	91	$\overline{DBEN}$ (O)
23	$\overline{RAS1}$ (O)	46	BSA9 (O)	69	A7(I)	92	DBIR (O)

TABLE A-1. WD95C00 132-PIN JEDEC FLAT PACK

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
93	VDD	103	D8/SD8 (I/O)	113	SCLK (I)	123	RD/$\overline{WR}$ (O)
94	D0SD0 (I/O)	104	D9/SD9 (I/O)	114	DAC8 (O)	124	IADSTAT (O)
95	D1/SD1 (I/O)	105	D10/SD10 (I/O)	115	VDD	125	IAD0 (I/O)
96	D2/SD2 (I/O)	106	D11/SD11 (I/O)	116	VSS	126	IAD1 (I/O)
97	D3/SD3 (I/O)	107	D12/SD12 (I/O)	117	RMWE s(I)	127	IAD2 (I/O)
98	D4/SD4 (I/O)	108	D13/SD13 (I/O)	118	SLD (I)	128	IAD3 (I/O)
99	VSS	109	D14/SD14 (I/O)	119	SLC (I)	129	IAD4 (I/O)
100	D5/SD5 (I/O)	110	D15/SD15 (I/O)	120	MC/AT (I)	130	IAD5 (I/O)
101	D6/SD6 (I/O)	111	$\overline{DACRD}$ (O)	121	$\overline{DS}$ (O)	131	IAD6 (I/O)
102	D7/SD7 (I/O)	112	$\overline{DACWR}$ (O)	122	$\overline{AS}$ (O)	132	IAD7 (I/O)

TABLE A-1. WD95C00 132-PIN JEDEC FLAT PACK (CONT'D)

10

A.2 WD95C01 (PDM)

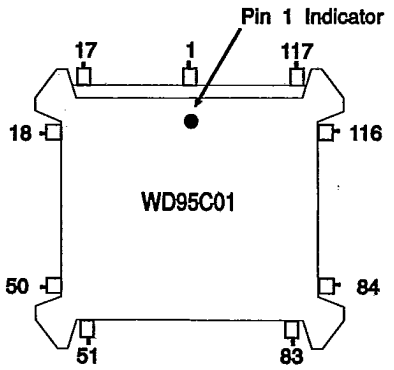


FIGURE A-2. WD95C01 132-PIN JEDEC FLAT PACK

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	VSS	26	VSS	51	SD26 (I)	76	SD6 (I)
2	IAD7	27	VDATA3 (O)	52	SD27 (I)	77	SD5 (I)
3	IAD6	28	VDATA2 (O)	53	SD26 (I)	78	SD4 (I)
4	IAD5	29	VDATA1 (O)	54	SD25 (I)	79	SD3 (I)
5	IAD4	30	VDATA0 (O)	55	SD24 (I)	80	SD2 (I)
6	IAD3	31	DACRD (O)	56	SD23 (I)	81	SD1 (I)
7	IAD2	32	DACWR (O)	57	SD22 (I)	82	SD0 (I)
8	IAD1	33	HSYNC (O)	58	SD21 (I)	83	VSS
9	IAD0	34	VSYNC (O)	59	SD20 (I)	84	SE34B (O)
10	IADSTAT	35	DACV (I)	60	SD19 (I)	85	SE34A (O)
11	RD/WR	36	MID2 (I)	61	SD18 (I)	86	SE12B (O)
12	AS	37	MID0 (I)	62	SD17 (I)	87	SE12A (O)
13	DS	38	MID0 (O)	63	SD16 (I)	88	SC13 (O)
14	VSS	39	SCLK	64	SD15 (I)	89	SC24 (O)
15	SLC (O)	40	RESET (I)	65	SD14 (I)	90	PD31 (I/O)
16	SLD (O)	41	VSS	66	SD13 (I)	91	PD30 (I/O)
17	VDD	42	ENVGA (O)	67	SD12 (I)	92	PD29 (I/O)
18	VSS	43	CLKSEL2 (O)	68	PCLK (I)	93	PD28 (I/O)
19	RMWE(O)	44	CLKSEL1 (O)	69	VSS	94	VDD
20	BLANK (O)	45	CLKSEL0 (O)	70	VDD	95	PD27 (I/O)
21	VDATA7 (O)	46	SD31 (I)	71	SD11 (I)	96	PD26 (I/O)
22	VDATA6 (O)	47	SD30 (I)	72	SD10 (I)	97	PD25 (I/O)
23	VDATA (O)	48	SD29 (I)	73	SD9 (I)	98	PD24 (I/O)
24	VDATA4 (O)	49	SD28 (I)	74	SD8 (I)	99	VSS
25	VCLK (O)	50	VDD	75	SD7 (I)	100	PD23 (I/O)

TABLE A-2. WD95C01 132-PIN JEDEC FLAT PACK

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
101	PD22 (I/O)	109	PD14 (I/O)	117	PD8 (I/O)	125	PD0 (I/O)
102	PD21 (I/O)	110	PD13 (I/O)	118	PD7 (I/O)	126	RWCAS s(I)
103	PE20 (I/O)	111	PD12 (I/O)	119	PD6 (I/O)	127	SWAP (I)
104	PD19 (I/O)	112	PD11 (I/O)	120	PD5 (I/O)	128	WROE (I)
105	PD18 (I/O)	113	PD10 (I/O)	121	PD4 (I/O)	129	MDT2 (I)
106	PD17 (I/O)	114	PD9 (I/O)	122	PD3 (I/O)	130	MDT1 (I)
107	PD16 (I/O)	115	VSS	123	PD2 (I/O)	131	MDT0 (I)
108	PD15 (I/O)	116	VDD	124	PD1 (I/O)	132	SELVD (O)

TABLE A-2. WD95C01 132-PIN JEDEC FLAT PACK (CONT'D)

A.3 SOCKET DIAGRAM

T-52-33-45

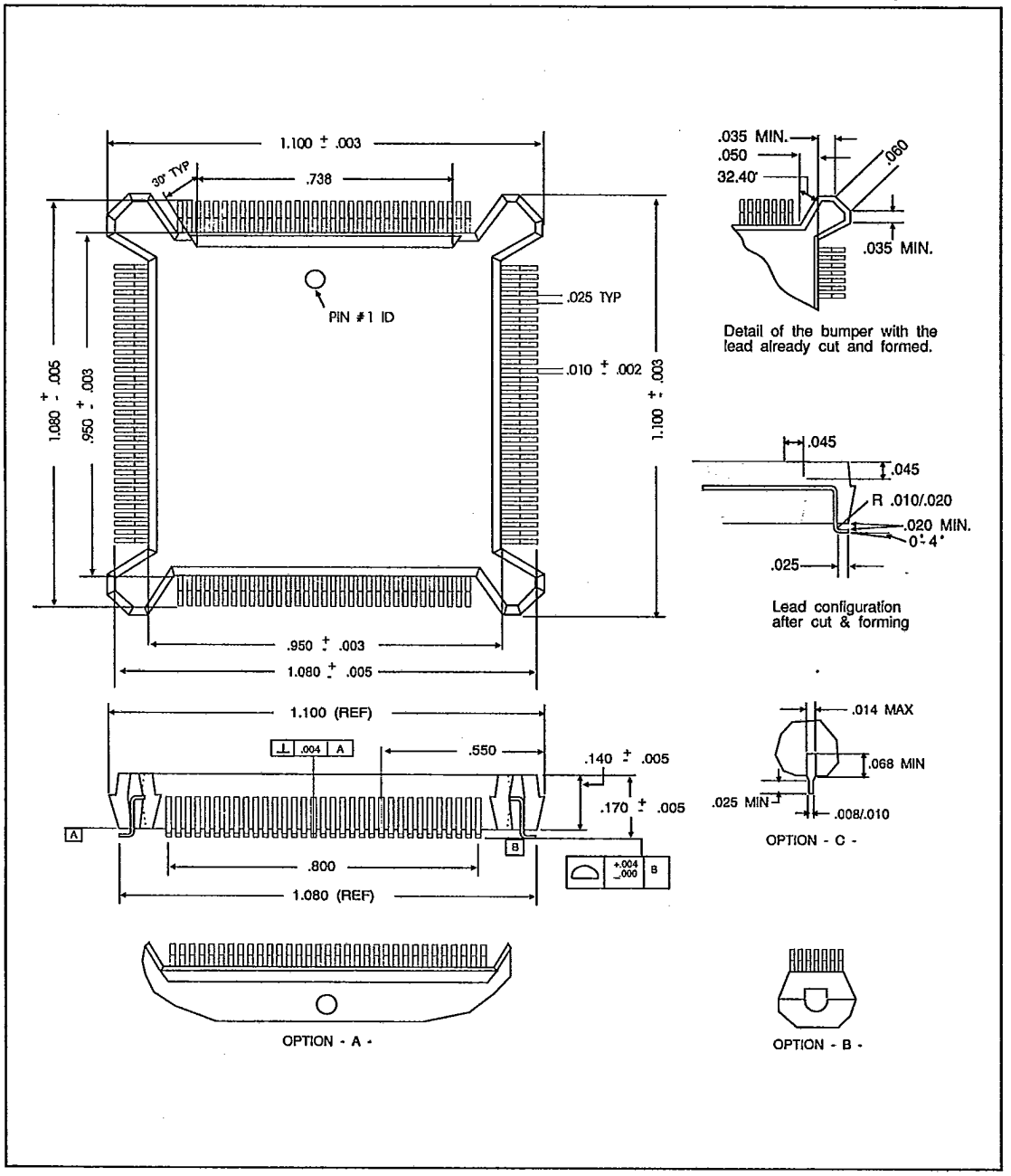
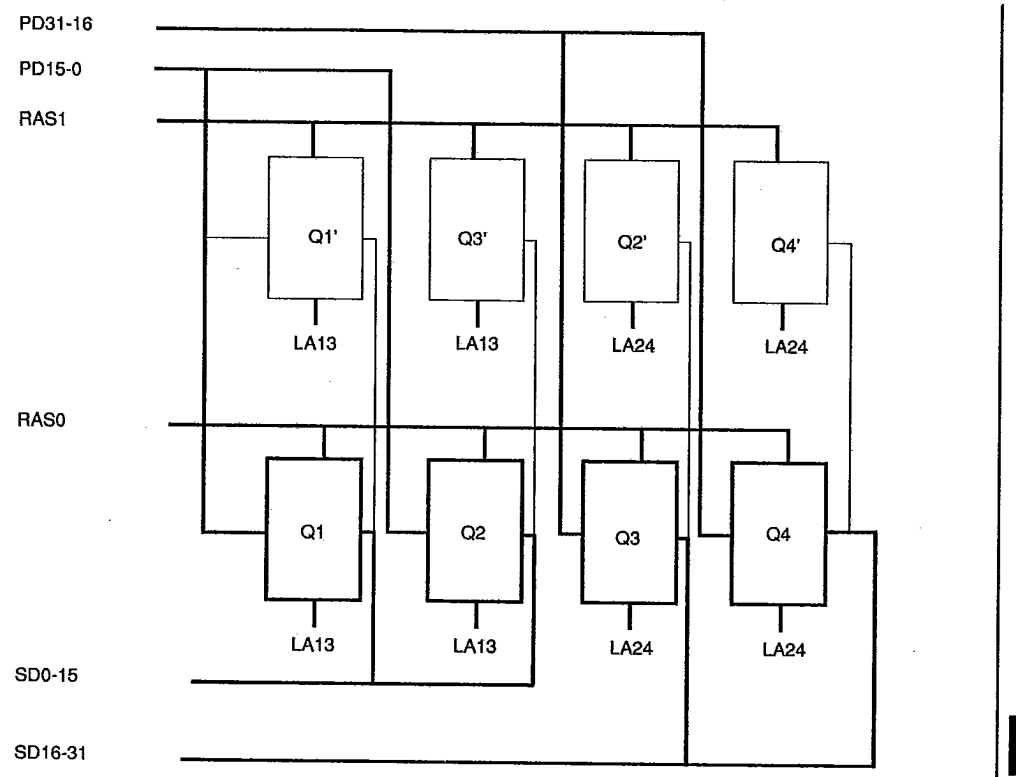


FIGURE A-3. SOCKET DIAGRAM

B.0 VRAM DESIGN

T-52-33-45



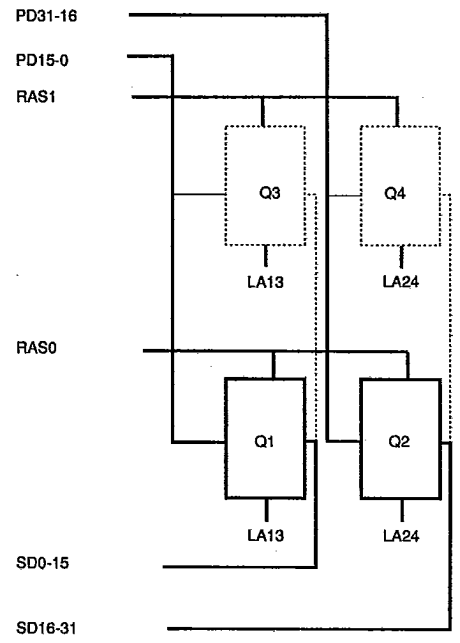
Note: Heavy lines represent the minimum chip population (16 chips).
Heavy lines plus light lines represent the standard chip population (32 chips).

FIGURE B-1. VRAM DESIGN WITH 64K X 4 CHIPS AND INTEGRATED BACK-END SUPPORT

QUAD	SE	SC	RAS	CAS	WE	DISPLAY MEMORY CONFIGURATION
Q1	SE12A	SC13	RAS0	CAS12	WE0-3	1024x1024x4 1024x1024x8 2048x1024x4
Q2	SE12A	SC24	RAS0	CAS12	WE4-7	
Q3	SE34A	SC13	RAS0	CAS34	WE0-3	
Q4	SE34A	SC24	RAS0	CAS34	WE4-7	
Q1'	SE12B	SC13	RAS1	CAS12	WE0-3	1024x1024x8 2048x1024x4
Q2'	SE12B	SC24	RAS1	CAS12	WE4-7	
Q3'	SE34B	SC13	RAS1	CAS34	WE0-3	
Q4'	SE34B	SC24	RAS1	CAS34	WE4-7	

TABLE B-1. CONTROL SIGNAL ASSIGNMENTS FOR FIGURE B-1

T-52-33-45



Note: Heavy lines represent the minimum chip population (4 chips).
Heavy lines plus light lines represent the standard chip population (8 chips).
Heavy lines plus light lines and dotted lines represent an extended chip population (16 chips).

FIGURE B-2. VRAM DESIGN WITH 256K X 4 CHIPS AND BACK-END SUPPORT

QUAD	SE	SC	RAS	CAS	WE	DISPLAY MEMORY CONFIGURATION
Q1	SE12A	SC13	RAS0	CAS12	WE0-3	1024X1024X4 1024X1024X8 2048X1024X4 2048X1024X8 2048X2048X4
Q2	SE12A	SC24	RAS0	CAS12	WE4-7	1024X1024X8 2048X1024X8 2048X1024X8 2048X2048X4
Q3	SE34A	SC13	RAS1	CAS34	WE0-3	2048X1024X8
Q4	SE34A	SC24	RAS1	CAS34	WE4-7	2048X2048X4

TABLE B-2. CONTROL SIGNAL ASSIGNMENTS FOR FIGURE B-2

T-52-33-45

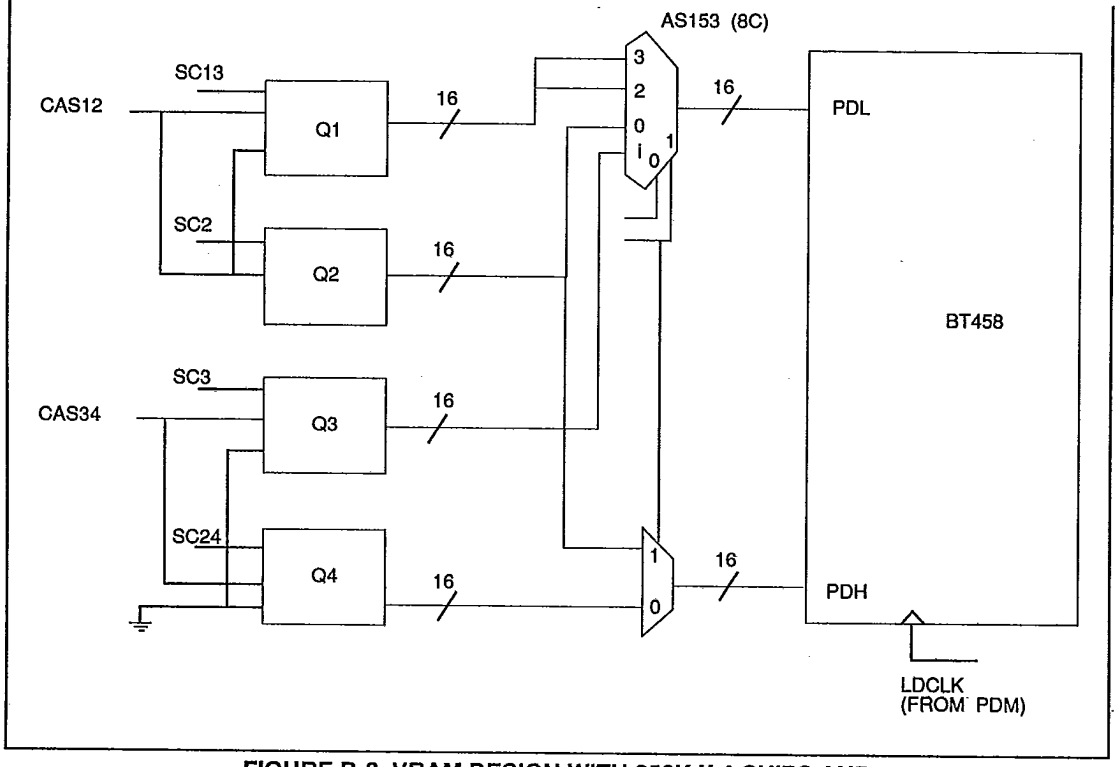


FIGURE B-3. VRAM DESIGN WITH 256K X 4 CHIPS AND EXTERNAL BACK-END SUPPORT

QUAD	SE	SC	RAS	CAS	WE
Q1	GND	SC13	RAS0	CAS12	WE0-3
Q2	GND	SC2	RAS0	CAS12	WE4-7
Q3	GND	SC3	RAS1	CAS34	WE0-3
Q4	GND	SC24	RAS1	CAS34	WE4-7

TABLE B-3. CONTROL SIGNAL ASSIGMENTS FOR FIGURE B-3

T-52-33-45

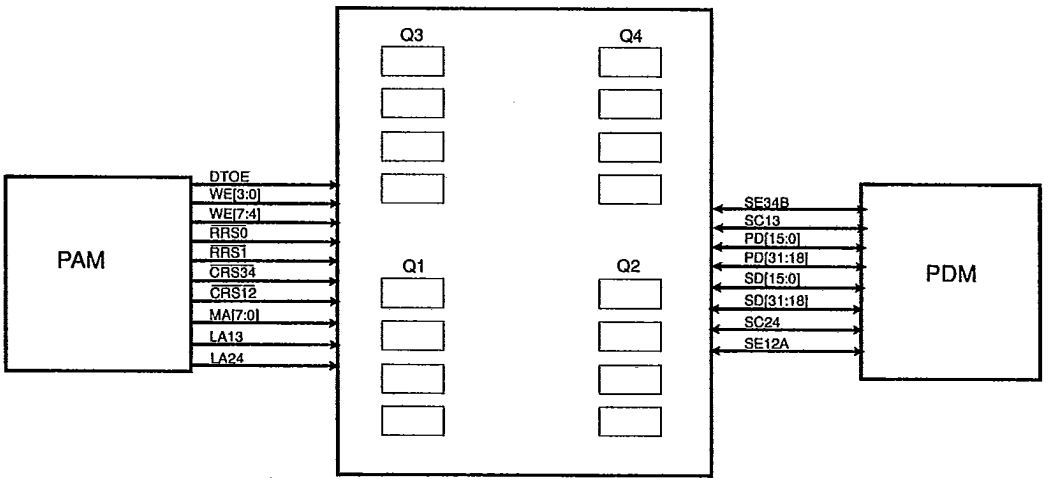


FIGURE B-4. VRAM CONNECTIONS TO PAM AND PDM FOR ALL 256K X 4 VRAM MEMORY CONFIGURATIONS

C.0 VIDEO DAC DESIGN

Figures C-1 and C-2 describe board implementation of the video DAC and interface subsystem with integrated and external back-end support, respectively. The flicker-free design option applies to both. The WD9500-SET1 supports INMOS IMS G171/176/178, Brooktree BT471/478 and compatible video DACs for 8514/a modes. It also supports Brooktree BT451/458 and compatible video DACs for Western Digital's enhanced 1280 x 1024 mode.

The Brooktree BT471 DACs include a 256 x 18 palette loaded with six-bit R, G, and B color intensity values. (The two highest bits of the eight-bit data lines supplying these values are ignored.) The BT478 offers a 256 x 24 palette with all eight bits used to define color. The DAC8 pin from PAM can be used to select six-bit or eight-bit palette fields. Note that the palette overlay capabilities are not used. The DAC's RS2 and OL0-OL3 pins should be tied down.

Without the flicker-free option, CPU software writes data into the DAC's color palette on the lower eight bits of the system data bus. The WD9500-SET1 intercepts CPU addressing and controls DAC access using the lower two bits of its EPROM address bus, BIOSA1 and BIOSA0. When the flicker-free option is incorporated into the board design, the CPU software can invoke flicker-free mode. In this mode palette data is buffered by the WD9500-SET1 and released to the DAC over the VDATA0-7 lines with the SELD control signal activated to select the VDATA lines in preference to the system data bus. Routing of the latter lines to the DAC via the SELD multiplexor is required to allow for non flicker-free mode (8514/A emulation) and for palette reads.

Figure C-2 shows the implementation of 1280 x 1024 resolution with external back-end support and two DACs. The fast DAC Bt451/Bt458 is used for 1280 x 1024 and 1024 x 768 resolutions The slow DAC is used for VGA video signal. The flicker-free capabilities do not apply to that DAC.

T-52-33-45

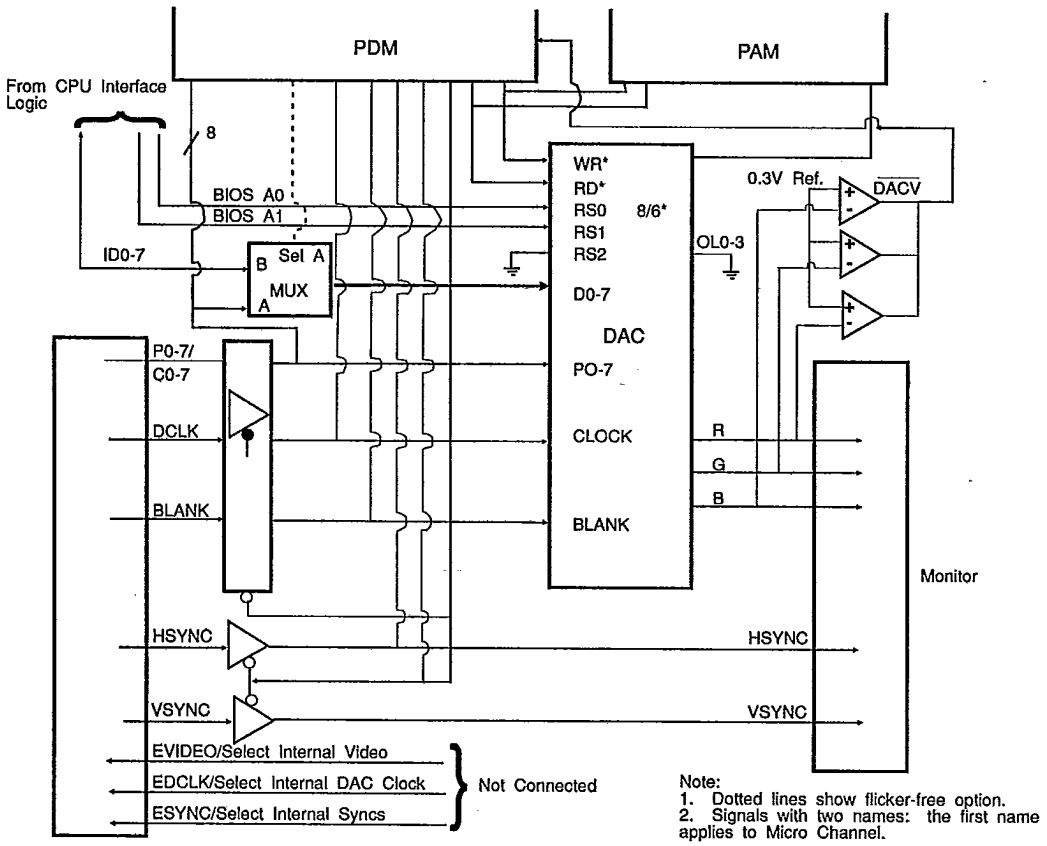


FIGURE C-1. VIDEO DAC AND INTERFACE SUBSYSTEM WITH INTEGRATED BACK-END SUPPORT

T-52-33-45

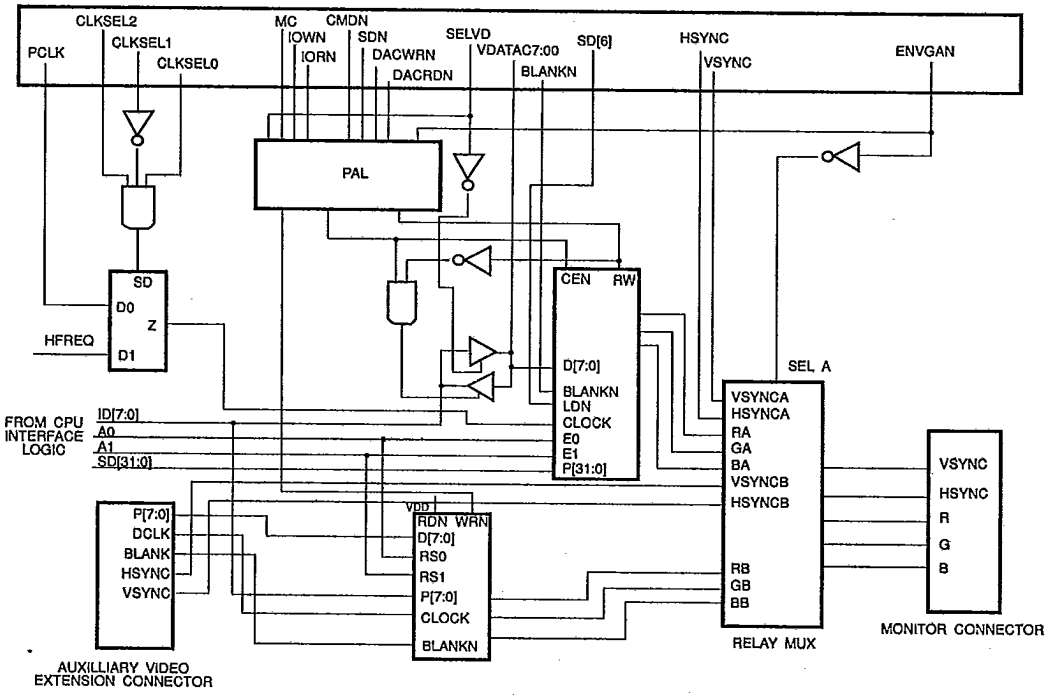


FIGURE C-2. 1280 X 1024 RESOLUTION IMPLEMENTATION WITH TWO DACS

T-52-33-45

D.0 ADDITIONAL BOARD DESIGN ELEMENTS

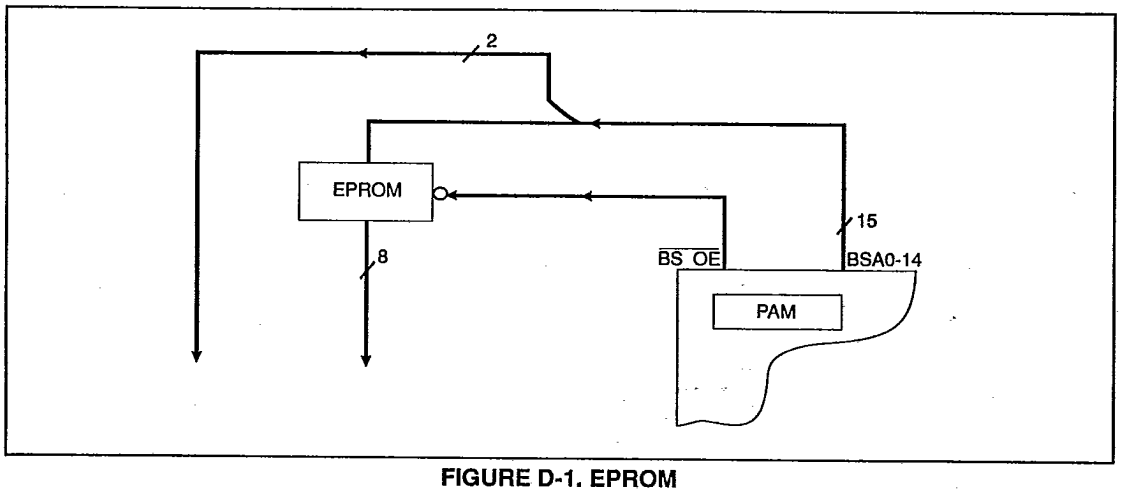


FIGURE D-1. EPROM

VRAM CHIP SPEED*	VRAM CHIP TYPE*	EPROM CONTENTS (BYTES)		EPROM BYTE ADDRESS
1	1		POS ID (MSByte)	7FFF
1	0		POS ID (LSByte)	7FFE
0	1	RESERVED		7FFD
0	0	VWSCP3**	(MSB)	7FF8
		VWSCP3	(LSB)	7FF7
		VWSCP2	(MSB)	7FF6
		VWSCP2	(LSB)	7FF5
		VWSCP1	(MSB)	7FF4
		VWSCP1	(LSB)	7FF3
		VWSCP0	(MSB)	7FF2
		VWSCP0	(LSB)	7FF1

VRAM Chip Speed: "0", if -8 spec.; "1", if -10 spec., IAD4 pin
VRAM Chip Type: "0", if 64K x 4; "1" if 256k x 4, IAD0 pin

TABLE D-1. EPROM BYTE ADDRESS

EPROM		MC	AT	BANK
7FFF 7800 77FF	2K	C6800-C6FFF	C8800-C8FFF	7 (4K)
7000 6FFF	2K	CA000-CA7FF	C9000-C97FF	6
6000 5FFF	4K	C7000-C7FFF	C9000-C9FFF	5
5000 4FFF	4K	C7000-C7FFF	C9000-C9FFF	4
4000 3FFF	4K	C7000-C7FFF	C9000-C9FFF	3
3000 2FFF	4K	C7000-C7FFF	C9000-C9FFF	2
2000 1FFF	4K	C7000-C7FFF	C9000-C9FFF	1
1000 0FFF 0000	4K	C7000-C7FFF	C9000-C9FFF	0

TABLE D-2. EPROM CONFIGURATION PARAMETERS

15	14	13	12	11-9	8	7-6	5-4	3-2	1-0
0	TM	DPL	DPM	ROW	RH	PW	EW	CPW	RPW

RPW<1:0> RAS Precharge Wait is used to select the minimum RAS precharge time. Encoding of the field is as follows:

RPW<1:0>	Minimum RAS Precharge Clocks
0 0	5
0 1	6
1 0	7
1 1	8

CPW<1:0> CAS Precharge Wait is used to select the minimum CAS precharge time, the minimum time CAS is high between page mode cycles. Encoding of this field is as follows:

CPW<1:0>	Minimum CAS Precharge Clocks
0 0	2
0 1	3
1 0	4
1 1	5

EW<1:0> Entry Wait is used to select CAS low time for entry cycles. Encoding of this field is as follows:

EW<1:0>	CAS low for *n* clocks during entry
0 0	3
0 1	4
1 0	5
1 1	6

PW<1:0> Page Wait is used to select CAS low time for page mode cycles. Encoding of this field is as follows:

EW<1:0>	CAS low for *n* clocks during page mode
0 0	3
0 1	4
1 0	5
1 1	6

RH RAS Hold. If set, RAS address hold time is extended from two clocks to three clocks.

ROW<2:0> Raster Operation Wait. The binary value in this field (0-7), gives the minimum number of clocks between the read and write of a destination RMW.

DPM Disable Page Mode. If this bit is set, no memory cycles will be performed in page mode, regardless of their addresses.

DPL Delay Pixel Location. If this bit is set, the earliest possible change in pixel location information (on the IAD bus and on the swap pin) is one clock period before the rising edge of CAS (or two clock periods, if cleared).

TM Test Mode. If this bit is cleared, the MIC operates normally. If set, the MIC goes into test mode and DRAM refresh cycles are requested every 135 clocks. In page mode the RAS low timer times out after 20 clocks of RAS low.

TABLE D-3. VRAM WAIT STATE CONTROL PARAMETERS

T-52-33-45

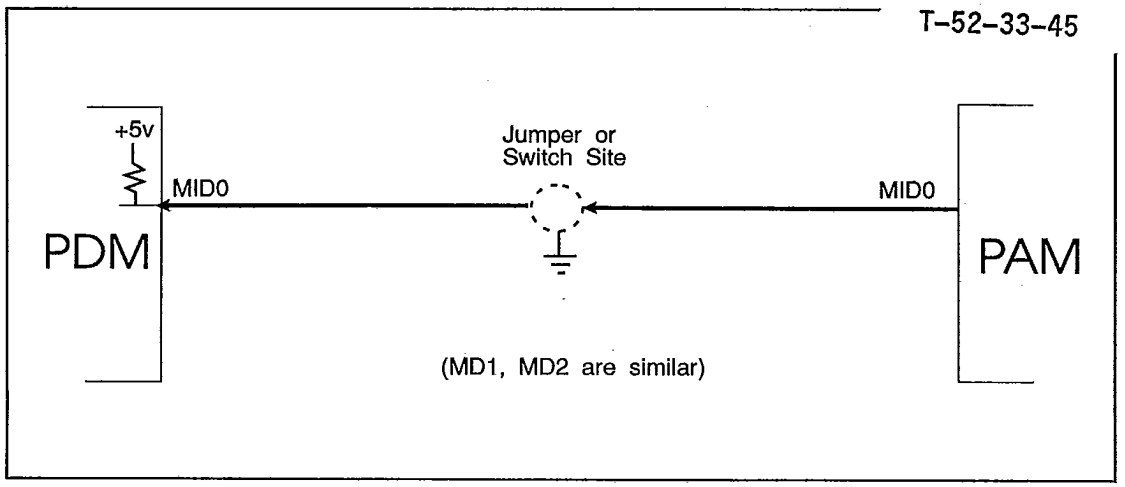


FIGURE D-2. MONITOR ID STRAPPING

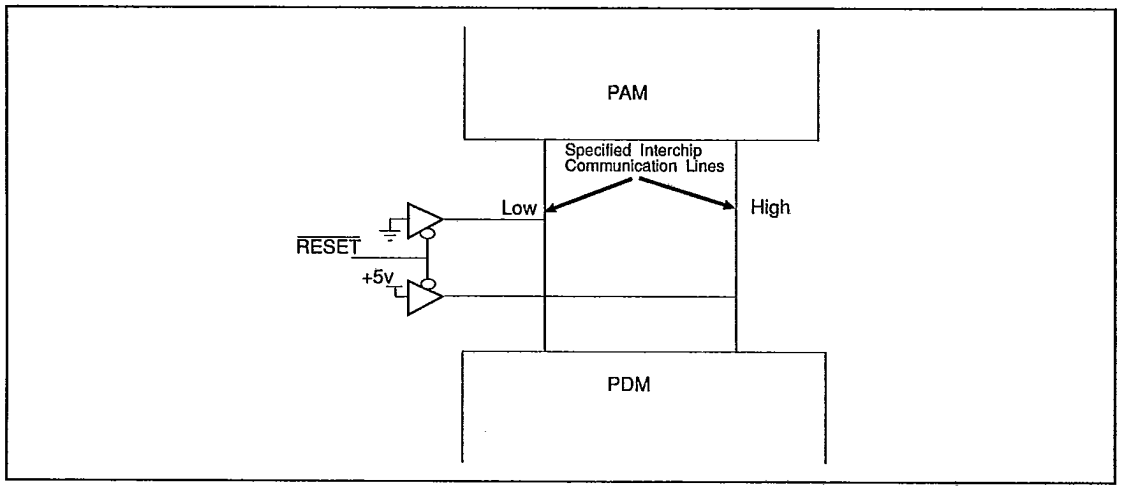


FIGURE D-3. VRAM CONFIGURATION STRAPPING