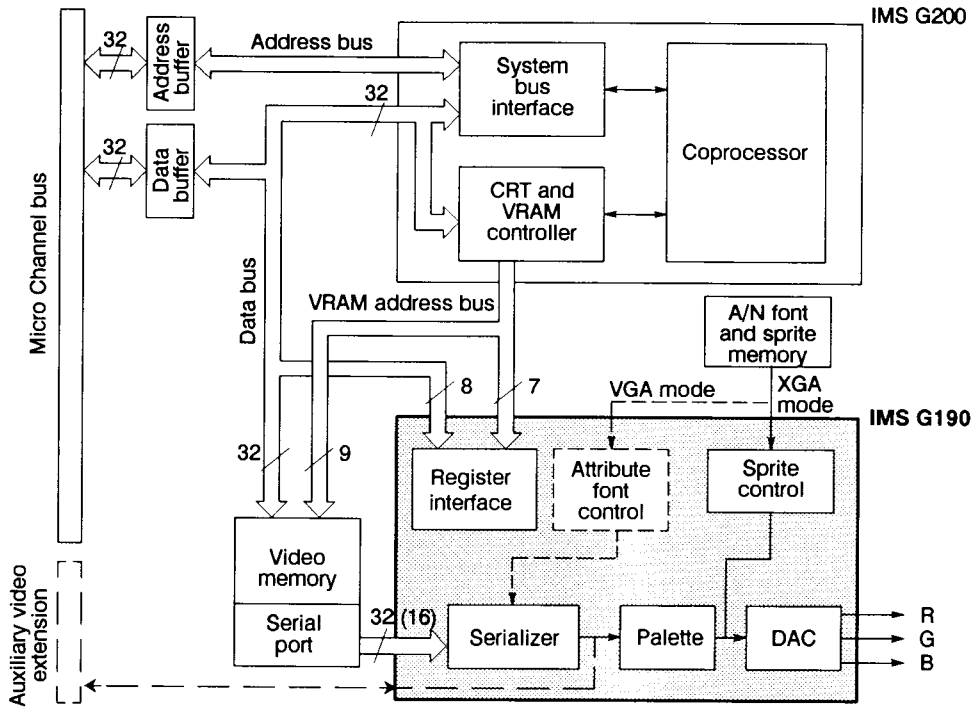
IMS G190
XGA serializer palette DAC

Preliminary information
The information in this datasheet is subject to change



FEATURES

VGA and XGA standard register set
32 bit pixel port
High speed pixel serializer
Hardware sprite input
VGA font and attribute controller
256×18 color palette
Triple 6-bit DAC
State save/restore
Monitor identification

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1 Introduction

The IMS G190 serializer palette DAC is one of two major components of the eXtended Graphics Array (XGA) subsystem. The other one is the IMS G200 display controller. These two components coupled with dual port VRAMs form the basis of a high performance graphics subsystem suitable for use with Graphical User Interface (GUI) windowing environments common in many personal computers and workstations. A more detailed description of the XGA subsystem is given in the *XGA Software Programmer's Guide*, INMOS document number 72 OEK 258 00. For information on the IBM PS/2 Micro Channel interface refer to the *IBM PS/2 Hardware Interface Technical Reference*, IBM document number '84F9809'.

1.1 XGA subsystem features

The following features summarize the capabilities of the XGA subsystem.

VGA compatible mode

When in VGA mode, the XGA subsystem is VGA register compatible as defined in the *VGA Function* chapter of the *Video Subsystem* section in the *IBM PS/2 Hardware Interface Technical Reference - Common Interfaces* IBM document number '84F9809'.

132 column text

In this mode, text is displayed in132 vertical columns using a number of scan lines, typically selected by a BIOS display mode. Each character is 8 pixels wide.

Extended graphics

The extended graphics mode provides the following support:

High resolution support
High resolution screen modes allow more windows to be displayed on the screen at any one time and give greater text clarity. Depending on the display attached and the amount of memory installed, the image on a screen can be defined using 1024 pixels and 768 scan lines with 256 colors.

16 bit true color mode
XGA introduces a new 16-bit-per-pixel mode allowing 65,536 colors to be displayed simultaneously on a 640 by 480 screen. True color mode does not use a color look-up table (palette) in the conventional way. Instead, the bits in each pixel are assigned Red, Green or Blue. Of the 16 bits in each pixel, 5 are assigned to Red, 6 to Green, and 5 to Blue. This allows images from many sources (e.g. photographs, computer-generated materials) to be displayed with almost photo-realistic quality.

Packed pixel format
In the packed-format, reads and writes to the video memory can access all of the data that defines a pixel (or pixels) in a single operation.

Hardware sprite
A hardware sprite allows a steady graphics cursor to be displayed without affecting the contents of video memory. This avoids the need for software collision detection. The sprite is a 64 by 64 pixel image. When enabled, it overlays the picture that is being displayed.

Display identification
Signals driven by the display identify characteristics of the attached monitor. Applications can use the monitor IDs to determine the maximum resolution and whether the display is color or monochrome.

Coprocessor
A coprocessor provides hardware drawing-assist functions throughout real or virtual memory.

When in extended graphics mode, the amount of video memory installed determines the screen resolutions and number of colors that are supported. The following table summarizes this relationship:

Video memory required	Resolution	Maximum colors
512 Kbytes	640×480	256
	1024×768	16
1 Mbyte	640×480	65, 536
	1024×768	256

Table 1.1 Screen resolution and number of colors supported for different VRAM sizes

1.2 XGA subsystem description

The following major components (shown in the figure on the front cover) provide the extended graphics function:

- System bus interface (IMS G200)
  The *system bus interface* and the *CRT and memory controller* manage the XGA subsystem and the screen display. They provide the system processor with direct access to the video memory. All video memory is accessible by the system processor through one of three apertures: one for real mode, one for protect mode on a 16-bit processor or operating system, and one for protect mode on a 32-bit processor with a 32-bit operating system.

- CRT and memory controller (IMS G200)

- Drawing coprocessor (IMS G200)
  The *drawing coprocessor* provides a range of hardware drawing functions that operate on pixels in memory.

- Video memory (External VRAM)
  Dual-port VRAM stores pixel data. VRAM offers better performance than DRAM, since one port updates the displayed information while the other refreshes the screen.

- Serializer (IMS G190)
  The *serializer* takes pixel data from the serial port of the video memory, and passes it pixel-by-pixel to address the 256-entry palette. The color values from the palette are passed to the three 6 bit DACs (red, green and blue), which produce the analog video signals for the monitor. In 16 bit true color mode, the pixel data essentially bypasses the palette and is transferred to the DACs.

- Palette (IMS G190)

- Digital-to-Analog Converters (G190)

- Sprite controller (IMS G190)
  The *sprite controller* interfaces to the *sprite buffer* to display the 64×64 pixel sprite image on the screen.

- Sprite buffer (External SRAM)
  The sprite buffer stores the alphanumeric fonts and sprite data.

XGA is controlled using a combination of I/O-mapped and memory-mapped registers. I/O-mapped registers are those that appear in the I/O address space of an 80X86 processor, and are accessed using IN, OUT, or other I/O instructions. Memory-mapped registers appear in the memory address space of an 80X86 processor, and are accessed using standard memory operations with all the available combinations of registers and addressing modes. In addition, many I/O-mapped registers are indexed (that is, the register is selected using an index in one I/O port, and the data for all indexed registers is written through a second I/O port). This technique, used also by the VGA, reduces the I/O address space required.

Memory-mapped registers are generally used to control the drawing coprocessor, where frequent access requires good performance. I/O-mapped registers (indexed and direct) are used for the remainder (mainly setup registers, where performance is less important).

Multiple XGA adapters (multiple instances) can be used in a system. Each instance has an instance number and has its registers mapped at different addresses. The memory-mapped registers are located at some point within the address range C0000 and DFFFF. The precise location is set by a system dependent configuration process, such as the PS/2 Micro Channel auto-configuration. Figures 1.1 and 1.2 illustrate how the I/O and memory-mapped registers are located. When multiple XGA subsystems are installed in a system, the memory-mapped registers for all instances can be mapped within the same 8 Kbyte block of address space. The allocation of addresses is the responsibility of the system configuration process, which ensures that there is no conflict between installed adapters (XGA or others).

Base address of the sixteen I/O registers of an XGA is 21x0, where x is the instance number. Figure 1.1 shows instance 6.

Base address of the memory-mapped registers of an XGA is (ROM Base address) + 7K + (128 x instance number). Figure 1.2 shows instance 6.

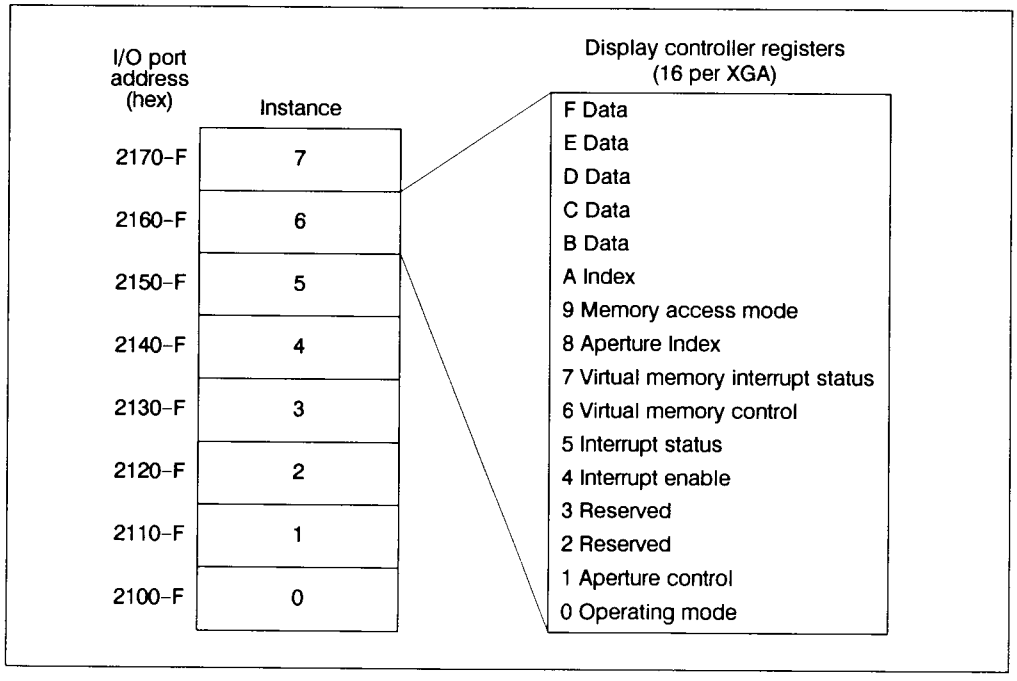


Figure 1.1 I/O port addressing of XGA registers

I/O port address	Register	Read/ Write	Description
21x0	Operating mode	R/W	Defines display mode (VGA, 132 or XGA)
21x1	Aperture control	R/W	Controls a 64K aperture through which the XGA memory can be accessed in the system address space. This window gives real mode applications and operating systems a means of accessing the XGA video memory.
21x2			Reserved
21x3			Reserved
21x4	Interrupt enable	R/W	Contains bits to enable/disable the interrupt conditions that can be generated by the subsystem.
21x5	Interrupt status	R/W	Indicates the interrupt status bits that can be generated by the subsystem and used to reset the corresponding interrupts.
21x6	Virtual memory control	R/W	This register is directly mapped to the I/O address space.
21x7	Virtual memory interrupt status	R/W	This register is directly mapped to the I/O address space.
21x8	Aperture index	R/W	Used to provide address bits to the video memory when the aperture in system address space being used is smaller than the amount of video memory installed.
21x9	Memory access mode	R/W	Controls pixel ordering when the video memory is being accessed by the system (not the coprocessor). Intel or Motorola order can be selected. This register also controls the number of bits per pixel.
21xA	Index	R/W	Selects which indexed Extended Graphics Mode register is accessed when any address (base + B) to (base + F) is read or written.
21xB 21xC 21xD 21xE 21xF	Data	R/W	These registers are used when reading and writing to the register indexed by the Index register (21xA). The read/write operation can be of byte, word, or double-word size using these data registers.

Table 1.2 XGA direct access I/O registers

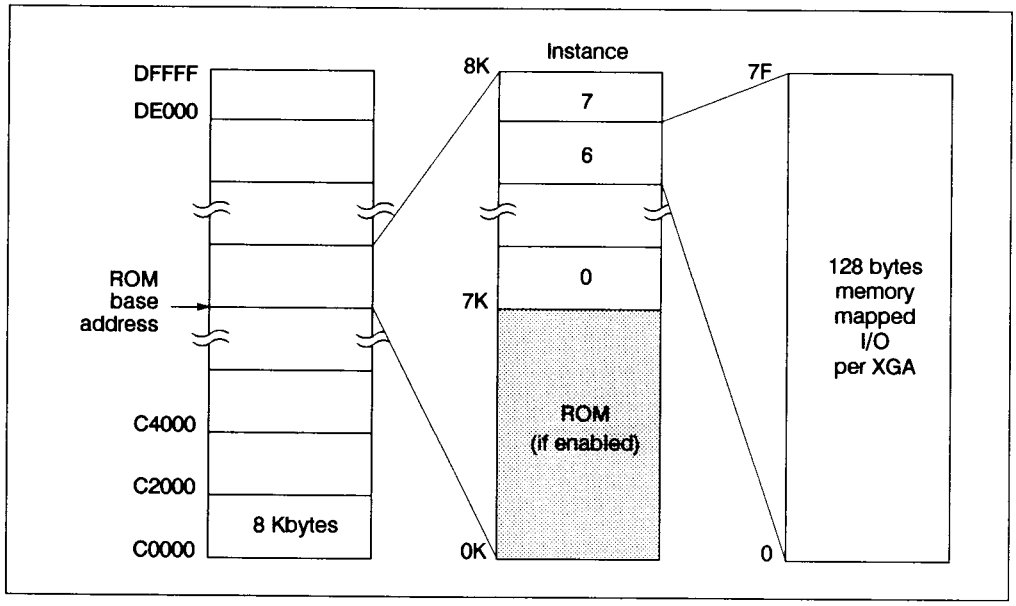


Figure 1.2 Memory mapped addressing of XGA registers

Traditionally, display adapters such as the VGA and the 8514/A have been controlled through registers mapped into the 80X86 I/O address space. Memory-mapped registers have been introduced in the XGA for controlling the drawing coprocessor, where accesses are frequent and good performance is essential.

The I/O address space in the 80X86 is limited to 64 Kbytes, so individual adapters can only use a restricted number of addresses (to avoid possible conflicts between adapters). When the adapter contains many registers (typical of a display controller), indexed register addressing schemes are often used, as noted above. Memory address space is much larger (1 Mbyte minimum in real mode), so adapters with memory-mapped registers can avoid using indexing, thus allowing direct access to all registers, and reducing code space and execution time.

When the 80386 is running in protect mode, the processor normally checks I/O accesses by applications to ensure they are allowed. It reads the I/O Permission Bitmap, a process that adds twenty cycles to each individual I/O access. Memory-mapped registers avoid this overhead, reducing to one-tenth the time taken to start many graphics operations.

Another advantage relates to multiple display adapters. Each instance of the XGA has a different set of register addresses, as shown earlier. Software must be able to run with any possible set. The 80X86 allows base-plus-offset addressing for memory accesses, using a segment register and an immediate or register-based offset. The software would typically set the segment register to point to the first address of the memory-mapped registers, and then have immediate pointers to specific registers. I/O addresses, on the other hand, are always contained in the DX register of an 80X86 processor; no form of base-plus-offset addressing is possible. For I/O-mapped registers, DX must be calculated correctly before each access, taking time and code space.

2 Detailed IMS G190 block diagram

Figure 2.1 shows the main functional units of the IMS G190 with all pin connections. The following sections of this document include pin details, a description of each of the functional units which make up the IMS G190, and package details.

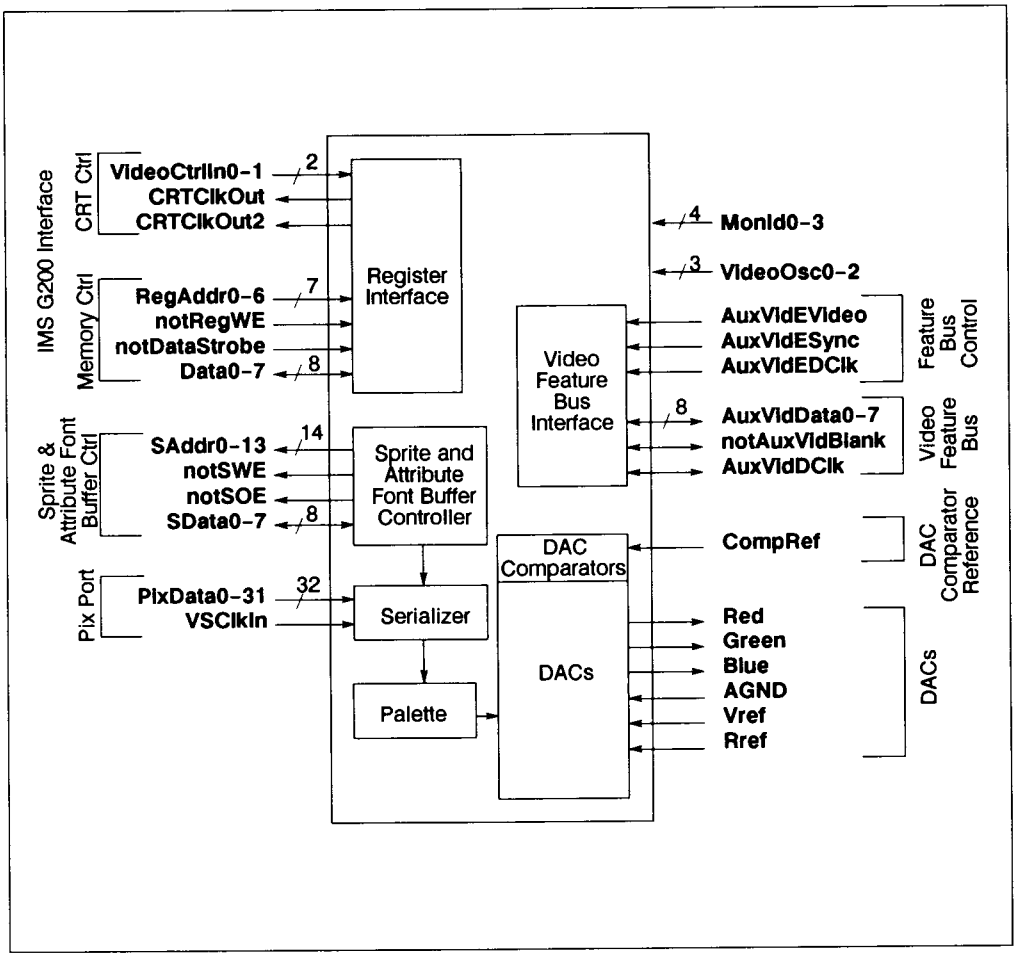


Figure 2.1 IMS G190 block diagram

3 Pin function reference guide

Signal names are prefixed by **not** if they are active low, otherwise they are active high.

3.1 IMS G200 interface

Signal	I/O	Description
RegAddr0-6	I	These pins provide the address of parameter registers in the IMS G190. They are driven by bits 0:6 of the VRAM address bus generated by the IMS G200.
notRegWE	I	A low level on this pin indicates that the addressed parameter register is being written to, a high level indicates that it is being read. It is driven by bit 8 of the VRAM address bus generated by the IMS G200.
notDataStrobe	I	A low level on this pin indicates that the IMS G190 should perform the action defined by the **RegAddr** and **notRegWE** inputs. This is a signal unique to the IMS G190 generated by the IMS G200.
VideoCtrlIn0-1	I	The levels on these pins, driven by the IMS G200, are encoded to indicate events on a horizontal scan line. **VideoCtrlIn**(1:0) = 00 Blanking 01 Border 10 Picture 11 Picture and start of cursor
Data0-7	I/O	The data from a parameter register being read is put onto these pins by the IMS G190; the data on these pins is used by the IMS G190 when its parameter registers are being written. This data is received/driven by the IMS G200 on the low order eight bits of the data bus which goes to the VRAMs and (via buffers) to the Micro Channel bus.
CRTClkOut **CRTClkOut2**	O	The selected video oscillator appears on these pins, divided by appropriate amounts. They drive inputs on the IMS G200, and are used to generate the clocks for its CRT controller (CRTC).

3.2 Auxiliary Video Extension

Signal	I/O	Description
AuxVidEVideo	I	A high level on this pin means that the IMS G190 will drive the **AuxVidData** pins. A low level will make the IMS G190 receive data on the **AuxVidData** pins. **AuxVidEVideo** is pulled to a high level by a 5 Kohm 20% resistor internal to the IMS G190.
AuxVidESync	I	A high level on this pin means that the IMS G190 will drive the **notAuxVidBlank** pin. A low level will make the IMS G190 receive data on the **notAuxVidBlank** pin. **AuxVidESync** is pulled to a high level by a 5 Kohm 20% resistor internal to the IMS G190.
AuxVidEDClk	I	A high level on this pin means that the IMS G190 will drive the **AuxVidDClk** pin. A low level will make the IMS G190 receive a clock on the **AuxVidDClk** pin. **AuxVidEDClk** is pulled to a high level by a 5 Kohm 20% resistor internal to the IMS G190.
AuxVidData0-7 **notAuxVidBlank** **AuxVidDClk**	I/O	These pins are part of the video feature interface. Their function is as defined by Micro Channel architecture.

3.3 Pixel port

Signal	I/O	Description
PixData0-31	I	The IMS G190 receives video data from the VRAMs on these pins. They are driven by the serial outputs of the VRAMs.
VSClkIn	I	A low level on the **VSClkIn** input pin strobes the VRAM serial data into the IMS G190. The rising edge of this input also clocks the serial clock counter in the IMS G190. The **VSClkIn** is generated by the IMS G200. It may then be buffered to drive the serial clock inputs of the VRAMs, but the IMS G190 must be driven by the unbuffered version because of timing constraints.

3.4 Sprite and attribute font buffer controller

Signal	I/O	Description
SData0-7	I/O	These pins are used to transfer data to and from the static RAM which holds the character fonts in VGA mode and the sprite definition in extended mode. They are received/driven by the sprite buffer data pins.
SAddr0-13	O	Address bus driven by the IMS G190 to the SRAM.
notSOE	O	Sprite buffer output enable
notSWE	O	Sprite buffer write enable

3.5 Monitor detection and video oscillators

Signal	I/O	Description
MonId0-3	I	The levels on these pins may be read via one of the parameter registers. These pins are pulled to high levels by 5 Kohm 20% resistors internal to the IMS G190.
VideoOsc0-2	I	For VGA compatibility, **VideoOsc0** should be driven by a 25.175MHz oscillator and **VideoOsc1** by a 28.321MHz oscillator. **VideoOsc2** is only used in extended mode, and is typically driven by a 44.9MHz oscillator to support 1024×768 mode. A 41.539MHz clock is also multiplexed onto **VideoOsc0** to support 132 column text mode frequencies.

3.6 Video signals

Signal	I/O	Description
Red **Green** **Blue**	O O O	These pins output currents proportional to the intensity value being presented to the 6-bit DACs. Each output is intended to drive 50 ohms, provided by a 150 ohm termination resistor at the IMS G190 in parallel with a 75 ohm termination resistor in the monitor.
AGND	O	The DACs generate variable output currents by switching current sources either to their output pin or to the **AGND** pin. The **AGND** pin should be connected to analog ground.
Vref **Rref**	I I	These pins are used to define the full-scale DAC output current. **Vref** should be connected to a voltage reference device generating 2.5 volts above analog ground. **Rref** should be connected to analog ground via a 1.87 Kohm resistor. Both these pins should be decoupled to analog ground via 10 nF ceramic capacitors. With these values of **Vref** and **Rref** the full scale output will be 0.7 volt into 50 ohms.
CompRef	I	This pin provides the DAC comparator reference voltage of 0.36 volts. Three analog comparators compare the voltage on the three video outputs with the voltage on this pin. The state of the comparators may be read via a parameter register.

3.7 Supplies

Signal	Description
VDD	Digital VDD
GND	Digital GND
AVDD	A specially decoupled analog + 5V supply should be provided. This should be fed from the regular + 5V plane via a 1μH choke, and decoupled to the analog ground plane by bulk decoupling and ceramic high-frequency decoupling capacitors.
AGND	A separate analog ground plane should be provided, joined to the regular ground plane at only one point. Only those components associated with the analog circuitry should be placed over and connected to the analog ground plane.

4 Device description

The IMS G200 and IMS G190 together support the full XGA and VGA register set. All VGA modes and the 132 column text mode are supported, regardless of the amount of video memory installed. They also support the Extended Graphics Mode (extended mode) for a screen resolution of 1024×768 with 256 colors, depending on the amount of video memory.

4.1 The serializer, palette and DAC

The serializer takes data from the serial port of video memory in 16 or 32 bit widths (depending on the amount of video memory installed) and converts it to a serial stream of Pixel data. The Pixel data is used to address a palette location, which contains the color value. The color value is then passed to the DAC, which converts the digital information into analog red, green, and blue signals to the display.

4.2 Palette

The palette has 256 locations. Each location contains 3 fields, one each for red, green and blue. It is used to translate the pixel value to a displayed color.

Before the pixel value is used to address the palette, it is masked by the palette mask register, thus all bits in the pixel corresponding to zeros in the palette mask register are forced to zero before reaching the palette.

4.3 Attribute controller

The attribute controller works together with the font and sprite memory and CRT controller (CRTC) to control the color selection and character generation in the 132-column text mode and VGA text modes.

4.4 Sprite controller

This component is used to display and control the position and image of the sprite, which is used as the cursor. The sprite is not available in 132-column text mode or VGA modes.

The sprite is a 64×64 pixel image stored in the XGA Sprite buffer. When active, it overlays the picture that is being displayed. Each 2 bit pixel can take on one of four values, setting the pixel appearance to be one of two preprogrammed colors, transparent or the one's complement of the underlying pixel color. These pixel values can be used to enable the sprite to achieve the effect of a colored marker of arbitrary shape.

4.5 Video DACs

The IMS G190 incorporates a triple 6-bit video DAC. The output level is set by an external voltage reference input.

5 Hardware interfaces

The IMS G190 serializer palette DAC interfaces to several other components in an XGA subsystem. These include the IMS G200 display controller, VRAM, SRAM, video feature bus interface.

5.1 IMS G200 display controller interface

Figure 5.1 shows the signals used to connect the IMS G190 to the IMS G200 display controller.

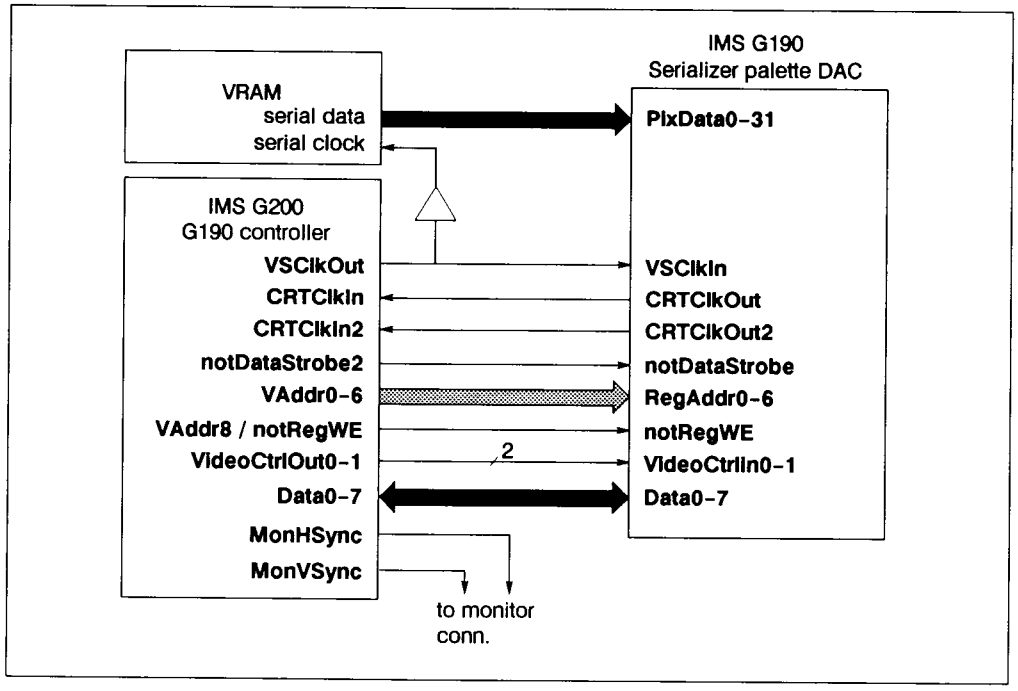


Figure 5.1 IMS G190 interface to the IMS G200

Derivation of addresses on IMS G200/IMS G190 interface

This section provides a correlation between the addresses on the IMS G200/IMS G190 interface and the addresses on the Micro Channel interface. All addresses and indexes are in hexadecimal.

All the Micro Channel addresses given are I/O addresses as opposed to memory addresses.

The majority of registers within the IMS G190 and IMS G200 are indexed. All register accesses are decoded by the IMS G200. To access a register in the IMS G190, first write to the index register (I/O address 21xA) followed by a number of writes/reads to the data registers (I/O address 21xB-21xF). The IMS G200 then generates a corresponding IMS G190 address (**RegAddr0-6**) and an address strobe (**notDataStrobe**) to update the IMS G190.

Extended mode addresses

The functions of these registers are described in Section 6. Note that the IMS G200 indexes are read only.

Micro Channel Address	IMS G200 Index	IMS G190 Address (RegAddr0-6)	Writeable Bits in the IMS G190	Readable Bits in the IMS G190	Register name
N/A	N/A	00	N/A	N/A	Power on reset
21x0	N/A	02	2	-	Operating mode register
21xB-F	00	01	0,1	-	Memory config register
21xB-F	30	03	0-2	0-2	Sprite horizontal start lo
21xB-F	32	04	0-5	0-5	Sprite horizontal preset
21xB-F	36	05	0	0	Sprite control
21xB-F	38	38	2-7	2-7	Sprite color 0 red
21xB-F	39	39	2-7	2-7	Sprite color 0 green
21xB-F	3A	3A	2-7	2-7	Sprite color 0 blue
21xB-F	3B	3B	2-7	2-7	Sprite color 1 red
21xB-F	3C	3C	2-7	2-7	Sprite color 1 green
21xB-F	3D	3D	2-7	2-7	Sprite color 1 blue
21xB-F	50	06	0,1,4	-	Display control 1
21xB-F	51	07	0-2,4-5	-	Display control 2
21xB-F	52	08	-	0-7	Display Id and comparator
21xB-F	53	09	-	-	RESERVED
21xB-F	54	0A	0,2-3	0,2-3	Clock frequency select
21xB-F	55	0B	0-7	0-7	Border color
21xB-F	56	0C	-	-	RESERVED
21xB-F	57	0D	-	-	RESERVED
21xB-F	58	0E	-	-	RESERVED
21xB-F	59	0F	-	-	RESERVED
21xB-F	5A	1C	-	-	RESERVED
21xB-F	5B	1D	-	-	RESERVED
21xB-F	60	10	0-7	0-7	Sprite/palette index lo
21xB-F	61	11	0-5	0-5	Sprite index hi
21xB-F	62	12	0-7	0-7	Sprite/palette index lo with prefetch
21xB-F	63	13	0-5	0-5	Sprite index hi with prefetch
21xB-F	64	14	0-7	0-7	Palette mask
21xB-F	65	15	2-7	2-7	Palette data
21xB-F	66	16	0-2	0-2	Palette sequence
21xB-F	67	17	2-7	2-7	Palette red prefetch
21xB-F	68	18	2-7	2-7	Palette green prefetch
21xB-F	69	19	2-7	2-7	Palette blue prefetch
21xB-F	6A	1A	0-7	0-7	Sprite data
21xB-F	6B	1B	0-7	0-7	Sprite prefetch reg
21xB-F	6C	1E	-	-	RESERVED
21xB-F	6D	1F	-	-	RESERVED
21xB-F	6E	3E	-	-	RESERVED
21xB-F	6F	3F	-	-	RESERVED

VGA mode addresses

In the addresses shown as 3*4 and 3*5, the * has the value B in mono mode and D in color mode.

VGA Address		IMS G200 Index	IMS G190 Address (RegAddr0-6)	Writeable Bits in the IMS G190	Readable Bits in the IMS G190	Register name
Rd @	Wr @					
3C0	3C0	N/A	28	All bits	5 only	Attribute address
3C1	3C0	3C0=0-0F	29	All bits	All bits	Internal palette
3C1	3C0	3C0=10	2A	All bits	All bits	Attribute mode control
3C1	3C0	3C0=11	2B	All bits	All bits	Attribute overscan color
3C1	3C0	3C0=12	2C	All bits	All bits	Attribute color plane enable
3C1	3C0	3C0=13	2D	All bits	All bits	Attribute horiz pixel pan
3C1	3C0	3C0=14	2E	All bits	All bits	Attribute color select
3C2	N/A	N/A	21	None	4 only	Input status zero
3C5	3C5	3C4=00	22	All bits	None	Sequencer reset
3C5	3C5	3C4=01	23	All bits	All bits	Sequencer clocking mode
3C5	3C5	3C4=04	24	3 only	None	Sequencer memory mode
3C6	3C6	N/A	34	All bits	All bits	Palette mask
3C7	3C7	N/A	32	All bits	0,1 only	Palette pixel address (rd)
3C8	3C8	N/A	30	All bits	All bits	Palette pixel address (wr)
3C9	3C9	N/A	35	All bits	All bits	Palette data
3CC	3C2	N/A	20	2,3 only	2,3 only	Miscellaneous output
3CF	3CF	3CE=05	27	5,6 only	5,6 only	Graphics mode
3*5	3*5	3*4=14	25	6 only	None	CRTC underline location
3*5	3*5	3*4=17	26	6 only	None	CRTC mode control

Note: 'All bits' refers to all bits defined in the *IBM PS/2 Hardware Interface Technical Reference*

These registers are fully VGA register compatible and a description of their function can be found in the 'Video subsystem' section in the *IBM PS/2 Hardware Interface Technical Reference,* document number 84F9809.

In the attribute section the same address (3C0) is used to write to the index register (called the 'address' register in VGA documentation) and to the register pointed to by this index register. A flip-flop which toggles on each write to 3C0 determines which register is written.

Accesses between IMS G200 and IMS G190

Parameter register accesses are timed by the IMS G200 update clock (**Clk**), which results in a clock period of 50ns (with a 40MHz oscillator). A parameter register access occurs whenever **notDataStrobe** is active.

There are two basic types of accesses between the IMS G200 and IMS G190, fast accesses and slow accesses. Fast accesses are used for parameter register updates to the IMS G190 and slow accesses are used for sprite/palette accesses since extra time is needed to allow these RAMs to be accessed.

Control codes from the IMS G200 to the IMS G190

The address bits on the IMS G200/IMS G190 interface are used at certain times to carry control data from the IMS G200 to the IMS G190. This data is not transferred as a result of Micro Channel activity, but during

each VRAM transfer cycle, in particular during the transfer cycle at the start of each line. This data mainly consists of information about the line that is about to be displayed. The data is not transferred on the data bus, but on the low-order six bits of the address.

These bits are encoded as follows:

RegAddr0-6						
6	5	4	3	2	1	0
0	@	@	@	@	@	@
1	0	N	A	S	U	C
1	1	R	R	R	R	R

normal IMS G190 address for register updates

@-@ are address bits used to address the data registers within the IMS G190.

N is the 'new font pair' bit. When this goes to a one it causes a reset of the sprite buffer address register used during alphanumeric font loading.

A is the 'active line' bit. This bit is a one for picture lines, and a zero for border (overscan) lines and for blank (flyback) lines.

S is the 'scrollable/border line' bit. When it is1 during an active line it indicates that the line is scrollable. When it is 1 during a non-active line it indicates that the line is a border line.

U is the 'underline/panning sync/sprite line' bit. In VGA mode during active lines a 1 indicates that this is an underline scan line. During non-active lines a 1 causes updates to the pixel panning register to be sampled for display. In extended mode a 1 indicates that the sprite should be displayed on the line.

C is bit 5 of the character row number.

R-R in VGA mode are character row bits 4-0. In extended mode these bits indicate the sprite prefetch row number.

Video control

The video control signals (**VideoCtrlOut0-1**) are generated by the IMS G200 from the IMS G190 CRTC clocks and fed back into the IMS G190 via the **VideoCtrlIn0-1** pins. The video control signals are encoded to indicate events on a horizontal scan line. The encoding is given below.

VideoCtrlOut0-1		Video data function
Bit 1	Bit 0	
0	0	Blanking
0	1	Border
1	0	Picture
1	1	Picture and start of cursor

Table 5.1 **VideoCtrlOut0-1** decoding

5.2 VRAM interface

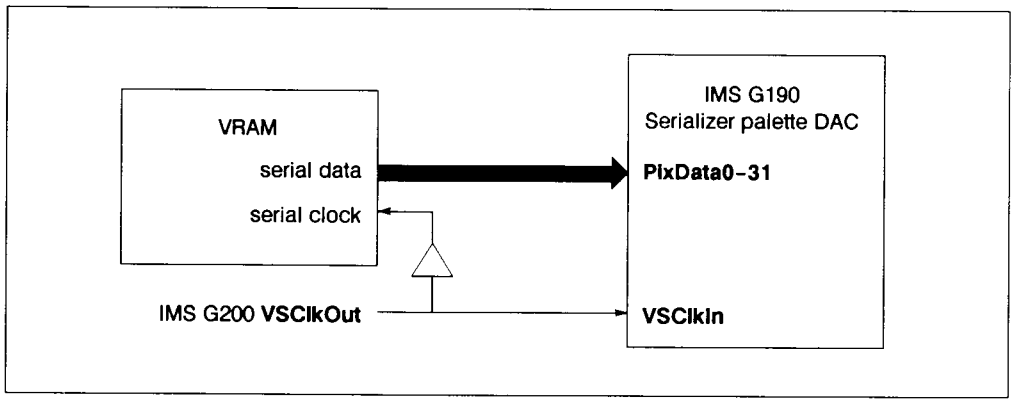


Figure 5.2 IMS G190 VRAM interconnection

The IMS G190 receives video data from the VRAM's on the **PixData0-31** pins. The pins are driven by the serial outputs of the VRAM's.

The **VSClkIn** signal is generated by the IMS G200 from the IMS G190 CRTC clocks, and fed back into the IMS G190. A rising edge on **VSClkIn** strobes the VRAM serial data into the IMS G190.

5.3 Video feature bus interface

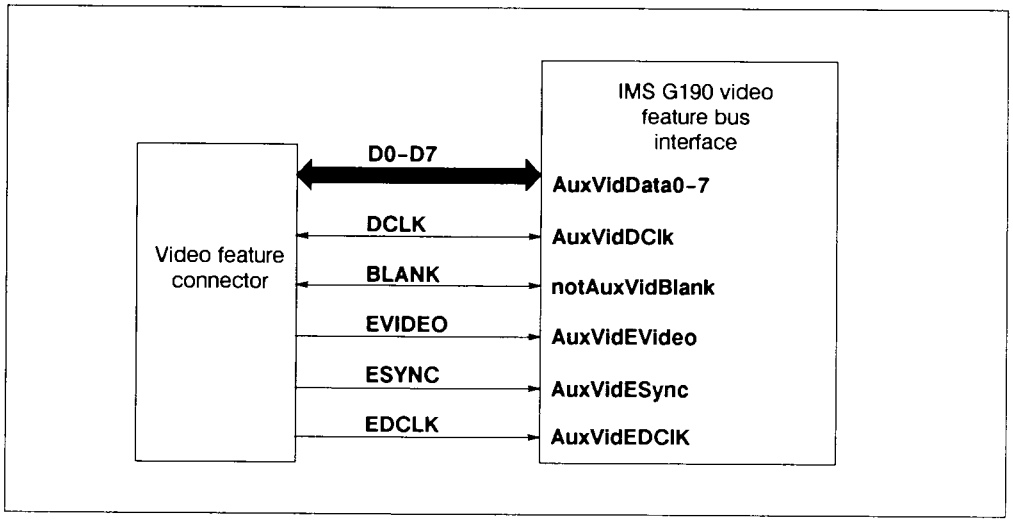


Figure 5.3 IMS G190 interconnection diagram to video feature connector

The **AuxVidData0-7** is the VGA palette address bus. The **AuxVidDClk** is the pixel clock used by the IMS G190 to latch the digital video signals **AuxVidData0-7**. The signals are latched into the IMS G190 on the rising edge of **AuxVidDClk**. When an adapter provides the clock, the adapter must also provide the video information on **AuxVidData0-7** to the IMS G190.

The **notAuxVidBlank** signal connects to the IMS G190 DAC and when active low forces all DAC outputs to zero.

For a full description of these Micro Channel signals refer to the *IBM PS/2 Hardware Interface Technical Reference,* document number 84F9809.

5.4 SRAM (sprite and attribute font buffer) interface

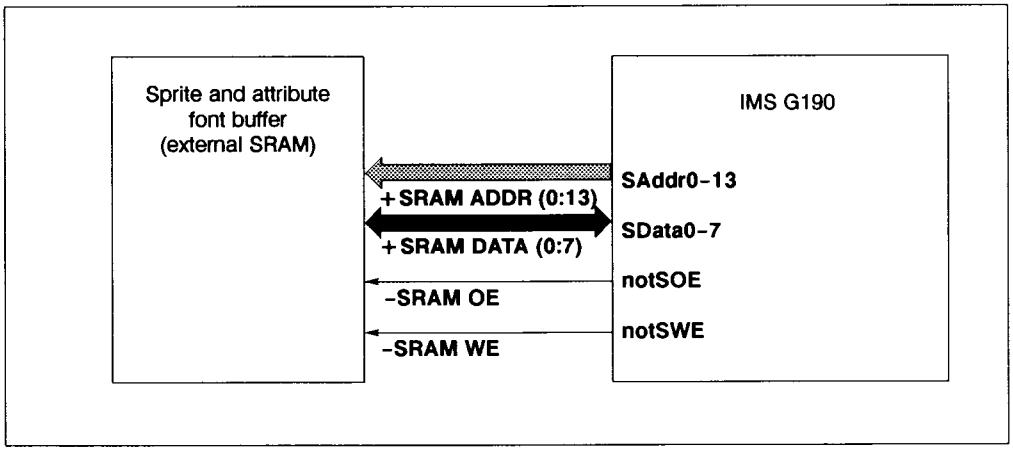


Figure 5.4 IMS G190 SRAM interconnection

This section describes the sprite and attribute font buffer interface. External memory is used as a VGA font buffer in VGA modes and as a hardware sprite buffer in extended mode. The IMS G190 initiates accesses to this external memory when necessary. These accesses are synchronously timed to the CRTC clocks.

In VGA mode two fonts are held in this external memory. These fonts are continuously updated during the active line time of vertical retrace.

The **SData0-7** pins transfer data to and from the SRAM. The **SAddr0-13**, **notSWE** and **notSOE** provide the address, write enable and output enable signals required by the SRAM.

5.5 Analog interfaces

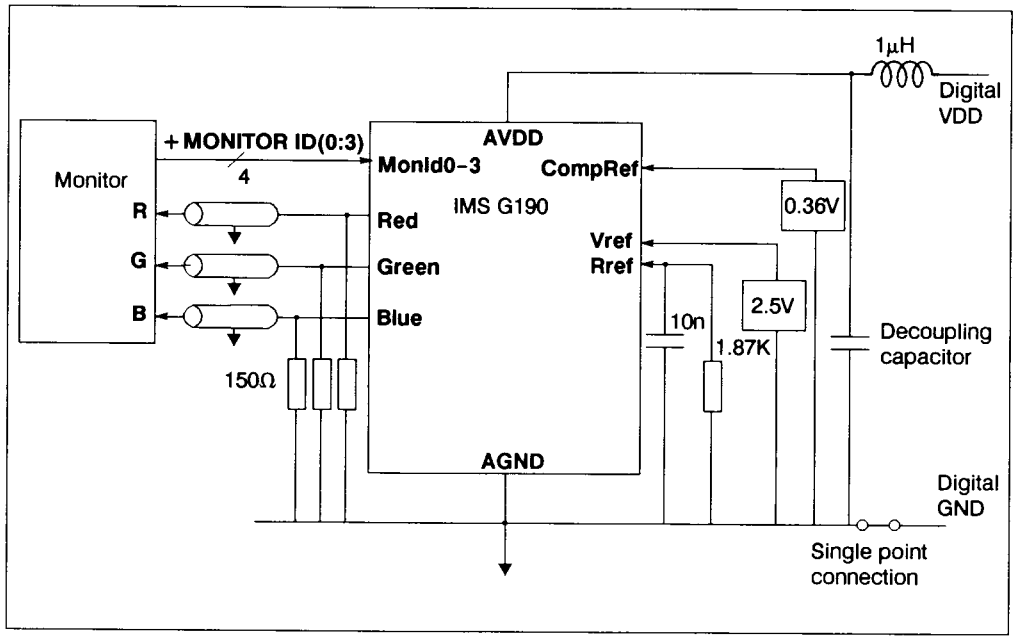


Figure 5.5 IMS G190 analog connections

The IMS G190 interfaces directly to a color or monochrome monitor. The three video signals **Red**, **Green** and **Blue** are designed to drive a 50 ohm load made up from a 75 ohm monitor load in parallel with a 150 ohm resistor at the IMS G190.

The current out of the DAC's should be set to 14mA, by applying a 2.5V voltage reference to the **Vref** pin and connecting a 1870 ohm resistor between **Rref** and **GND**. The 14mA full-scale current from the DAC, across a 50 ohm load will then give a 0.7V full scale voltage.

The IMS G190 receives four monitor ID bits (**MonId0-3**) back from the monitor which enable the XGA subsystem to determine the type of monitor which is connected. These monitor ID bits can be read from the display ID and comparator register.

The IMS G190 takes in a further voltage reference (**CompRef**). This should be set to 0.36V. The IMS G190 contains internal comparators which compare this voltage with each of the DAC outputs. The results of these comparisons can be read back from the display ID and comparator register.

The comparator polarity is a high output when the DAC output voltage is less than the 0.36V reference.

6 Internal Registers

This section gives brief descriptions of all the extended mode parameter register bits which physically reside in the IMS G190 (Note: some of the registers defined in the XGA architecture are physically split between the IMS G200 and the IMS G190). For a description of the VGA mode register bits refer to VGA documentation.

6.1 Memory configuration (0:1)

These two bits indicate the width (16 or 32 bits) of the serial data of the VRAMS.

6.2 Operating mode(2)

This bit indicates whether the system is in VGA or extended mode.

Both VGA and extended addresses are always valid regardless of which mode the system is in. Note, however, that some parameter latches are shared between the two modes and may have widely different meanings in the two modes. Therefore writing to a VGA address in extended mode may change an unexpected extended parameter, and vice versa.

6.3 Sprite horizontal start lo (0:2)

These are the low-order 3 bits of the horizontal sprite start position. The IMS G200 uses the higher order bits to control when the video controls go to the cursor state with a granularity of 8 pixels. The IMS G190 uses the 3 low-order bits to position the sprite horizontally to the exact pixel.

6.4 Sprite horizontal preset (0:5)

These bits define horizontally which is the first sprite pixel to be displayed at the indicated position. A value of 0 means that the whole of the sprite line is displayed. A value of 63 means that only the right-most pixel of the sprite is displayed.

6.5 Sprite control (0)

This bit controls whether the sprite is displayed. Reading or writing the sprite buffer is not allowed when this bit is in the state which allows the sprite to be displayed. Apart from causing unwanted changes to the appearance of the sprite, attempts to read the sprite buffer while displaying the sprite will return undefined values, and attempts to write the sprite buffer while displaying the sprite may cause the contents of the sprite buffer to be corrupted.

6.6 Display control 1 (0,1,4)

Bit 4 controls the enabling of the video feature interface. It is reset by power on reset to '0', the disabling state. When this bit is a 0 the video feature data, blanking and pixel clock output drivers are disabled, and IMS G190 will ignore the three video feature enable signals so that no data will be received either. When this bit is a 1 the video feature signals can be driven or received as normal under the control of the three enable signals.

The video feature interface is not designed to work with a pixel clock frequency higher than 30MHz, and bit 4 allows it to be disabled by software whenever clock frequencies higher than this are being used.

Bit 1, when 0, forces blanking on.

Bit 0, when 0, causes a CRTC reset. This initialises various CRTC related functions in the IMS G190.

6.7 Display control 2 (0:2, 4:5)

Bits 4:5 indicate which horizontal scale factor (1, 2 or 4) to use. This function is sometimes referred to as horizontal replication, a horizontal scale factor of 2 or 4 causes the same pixel to be replicated and displayed as 2 or 4 consecutive identical pixels.

Border pixels and sprite pixels are not replicated.

Bits 0:2 indicate how many (1, 2, 4, 8 or 16) bits there are for each pixel. For 1, 2, 4 and 8 bits per pixel the palette is used; higher order bits of the palette address are automatically forced to 0. 16 bits per pixel is the direct color mode which does not use look-up table indirection.

6.8 Display Id and comparator (0:7)

This is a read-only register.

Bits 5:7 indicate the state of the blue, green and red analogue comparators.

Bits 0:4 indicate the state of 5 inputs to IMS G190, four of which are intended to be used for the monitor ID. The fifth bit is not used by the IMS G190.

6.9 Clock frequency select (0, 2:3)

Bits 2:3 control which oscillator is selected to be the source of the pixel clock.

Bit 0 indicates whether to use clock scale factor 1 or 2. The IMS G190 does not support a clock scale factor of 4. The clock scale factor ensures that **CRTClkOut** and **CRTClkOut2** are always within the correct range of frequencies for use by the IMS G200 CRT controller.

6.10 Border color (0:7)

This register is the palette index for the border color which resides in the palette. Bit 7 is also used to force the direct color expansion table to be in the opposite half of the palette to the border.

The border color is output on the video feature interface during blanking (as well as during the borders). This retains compatibility with VGA.

6.11 Sprite/palette index lo (0:7) (used for write & save/restore)

This register provides the 8-bit palette address and also the low-order 8 bits of the external memory (sprite) address used when accessing these RAMs. Accessing this register does not cause the palette or external memory to be accessed, unlike the sprite/palette index registers for read (prefetch). This is why this register is used to save and restore the sprite/palette index lo.

Writing to this register causes the palette sequence count to be reset to the red state.

6.12 Sprite index hi (0:5) (used for write & save/restore)

This register provides the high-order 6 bits of the external memory (sprite) address used when accessing the sprite buffer. These high-order 6 bits are not used when accessing the palette; in particular they do not have to be 0. Accessing this register does not cause any other action to occur, unlike the sprite/palette index registers for read (prefetch). This is why this register is used to save and restore the sprite/palette index hi.

Although the sprite only occupies 1 Kbyte of the sprite buffer, access to the entire 16 Kbytes is provided for diagnostic purposes. Reading data back from outside the 1 Kbyte range will return undefined data.

6.13 Sprite/palette index lo with prefetch (0:7)

Accessing this register accesses physically the same register as the 'sprite/palette index lo' register. However, writing to it causes both the palette and the sprite buffer to be read and the data saved in their respective data registers. Also, the sprite/palette index lo register is incremented by one after this read of the two RAMs. This incrementing wraps from 255 to 0. Reading this register does not cause any additional activity.

Writing to this register causes the palette sequence count to be reset to the red state.

6.14 Sprite index hi with prefetch (0:5)

Accessing this register accesses physically the same register as the 'sprite index hi' register. However, writing to it causes the sprite buffer to be read and the data saved in the sprite buffer data register. Reading this register does not cause any additional activity. This register will increment after data has been written to it.

When preparing to read the sprite buffer the hi and lo indexes can be provided in either order, but it is important to use the 'index for read' only for the second of the two parts of the address. The first part of the address must be provided by using the 'index for write'. This is to prevent any possible alteration of the address caused by the auto-incrementing that occurs after the 'index for read' is written.

6.15 Palette mask (0:7)

The pixel data is ANDed with this register before being used to address the palette. This register must be set to 'FF' hex in direct color mode. The addresses used by software to access the palette are not ANDed with the palette mask.

6.16 Palette data (2:7)

This register is used to access the palette data register one primary color at a time. The primary color currently being accessed is controlled by the palette sequence register. After accessing the palette data register, the palette sequence count is incremented.

When the palette sequence count changes either from blue to red or from green to 'X' (depending on the order selected by palette sequence register bit 2), as a result of writing the palette data register, the palette is written with the three primary colors that have been accumulated in the palette data register, and the sprite/palette index lo register is incremented.

When the palette sequence count changes either from blue to red or from green to 'X' as a result of reading the palette data register the sprite/palette index lo register is incremented and the palette is read into the palette data register from the new address.

In either case the sprite/palette index hi is NOT incremented when the sprite/palette index lo register wraps from 255 to 0, because it is known that it is the palette that is being accessed and not the sprite buffer.

The entire palette can be written or read simply by successively writing or reading this register.

6.17 Palette sequence (0:2)

Bit 2 controls the order in which the the primary colors are handled.

Bits 0:1 indicate which primary color is currently being handled. For instance, if they indicate 'blue', the next byte written to the palette data register must contain blue data, and the next byte read from the palette data register will be blue data.

6.18 Palette red, green, blue prefetch (2:7)

Because accessing the palette data register causes other things to happen, these three registers are provided for save and restore purposes. Accessing them will not change the palette sequence register, nor will any palette access occur.

6.19 Sprite data (0:7)

This register is used to access the addressed sprite buffer (sprite) location.

After writing this register the sprite buffer is written and the sprite/palette index lo register is incremented.

After reading this register the sprite/palette index lo register is incremented and the sprite buffer is read from the new address and the data put into the sprite data register.

The sprite/palette index hi is also incremented in either case when the sprite/palette index lo register wraps from 255 to 0.

The entire sprite buffer can be written or read simply by successively writing or reading this register.

6.20 Sprite prefetch register (0:7)

Because accessing the sprite data register causes other things to happen, the sprite save/restore register is provided for save and restore purposes. Accessing it will not change the palette/sprite index register, nor will any sprite buffer access occur.

6.21 Sprite color 0 red, green, blue (2:7)

These three registers define sprite color 0.

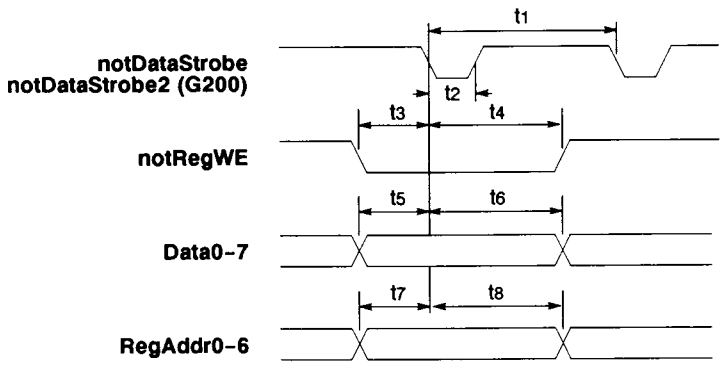
6.22 Sprite color 1 red, green, blue (2:7)

These three registers define sprite color 1.

7 Timing reference guide

7.1 IMS G200 display controller interface timings

Write to G190 register timings



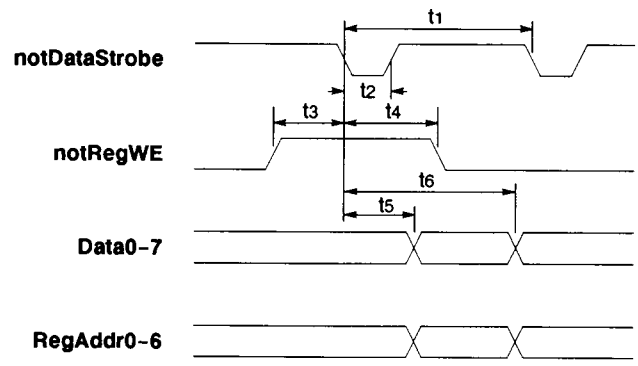
Note: These cycles are synchronous to the IMS G200 processor clock

Figure 7.1 Write to IMS G190 register

Symbol	Parameter	Min	Max	Units	Notes
t1	**notDataStrobe** period - fast access	250.0		ns	
	notDataStrobe period - slow access	500.0		ns	
	notDataStrobe period - control codes	40.0		ns	
t2	**notDataStrobe** width - fast access	100.0		ns	
	notDataStrobe width - slow access	150.0		ns	
	notDataStrobe width - control codes	20.0		ns	
t3	**notRegWE** set up to **notDataStrobe**	50.0		ns	
t4	**notRegWE** hold after **notDataStrobe**	100.0		ns	
t5	**Data0-7** set up to **notDataStrobe**	40.0		ns	
t6	**Data0-7** hold after **notDataStrobe**	40.0		ns	
t7	**RegAddr0-6** set up to **notDataStrobe**	40.0		ns	
t8	**RegAddr0-6** hold after **notDataStrobe**	100.0		ns	

Table 7.1 Write to IMS G190 register timings

Read from G190 register timings



Note: These cycles are synchronous to the IMS G200 processor clock

Figure 7.2 Read from IMS G190 register

Symbol	Parameter	Min	Max	Units	Notes
t1	**notDataStrobe** period - fast access	250.0		ns	
	notDataStrobe period - slow access	500.0		ns	
	notDataStrobe period - control codes	40.0		ns	
t2	**notDataStrobe** width - fast access	100.0		ns	
	notDataStrobe width - slow access	150.0		ns	
	notDataStrobe width - control codes	20.0		ns	
t3	**notRegWE** set up to **notDataStrobe**	50.0		ns	
t4	**notRegWE** hold after **notDataStrobe**	100.0		ns	
t5	**Data0-7** read access	60.0		ns	
t6	**Data0-7** hold after **notDataStrobe**	100.0		ns	

Table 7.2 Read from IMS G190 register timings

7.2 CRTC controller timings

CRTC clock timings

The CRTC clocks are generated by the IMS G190. They provide synchronization of signals between the IMS G200, VRAM and the IMS G190. Their frequency is set by bit 0 of the clock frequency select register (see Section 6.9).

The interface timing requirements of the clocks are given below. **CRTClkOut2** is always half the frequency of **CRTClkOut**.

Video control timings

The video control signals (**VideoCtrlOut0-1**) are generated by the IMS G200 from the CRTC clocks and fed back into the IMS G190 via the **VideoCtrlIn0-1** pins.

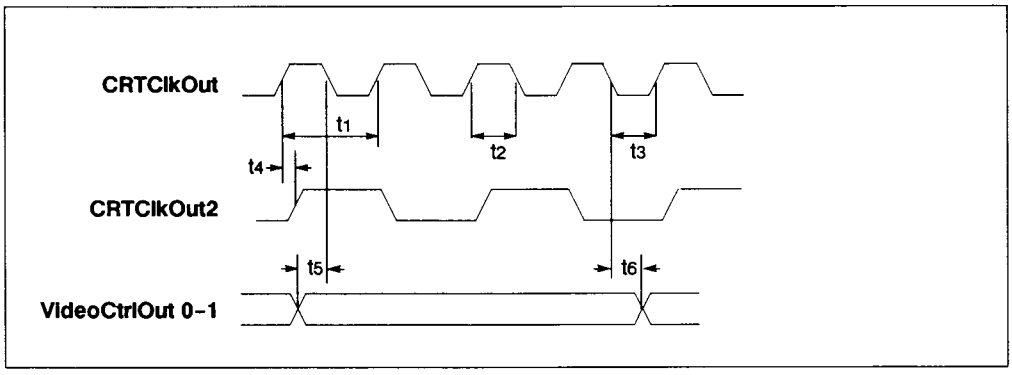


Figure 7.3 CRTC clock and video control timings

Symbol	Parameter	Min	Max	Units	Notes
t1	IMS G190 **CRTClkOut** period	25.0	50.0	ns	
t2	IMS G190 **CRTClkOut** pulse width high	12.5	25.0	ns	
t3	IMS G190 **CRTClkOut** pulse width low	12.5	25.0	ns	
t4	IMS G190 **CRTClkOut** to **CRTClkOut2** delay	-5.0	5.0	ns	
t5	**VideoCtrlOut0-1** setup time	5.0	-	ns	
t6	**VideoCtrlOut0-1** hold time	12.5	-	ns	

Table 7.3 CRTC clock timings

7.3 Video feature bus timings

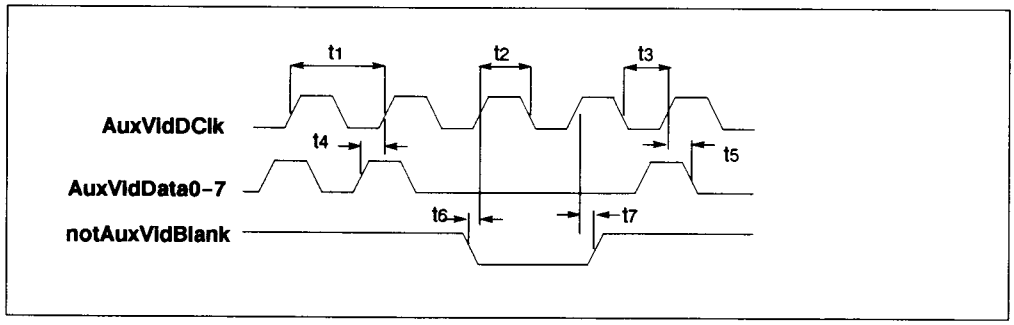


Figure 7.4 Video feature bus timings diagram

Symbol	Parameter	Min	Max	Units	Notes
t1	**AuxVidDClk** period	33.3	10,000	ns	
t2	**AuxVidDClk** pulse width high	7.0	10,000	ns	
t3	**AuxVidDClk** pulse width low	9.0	10,000	ns	
t4	**AuxVidData0-7** set up time	4.0	-		
t5	**AuxVidData0-7** hold time	4.0	-		
t6	**notAuxVidBlank** set up time	4.0	-		
t7	**notAuxVidBlank** hold time	4.0	-		

Table 7.4 Video feature bus timings

7.4 VRAM interface timings

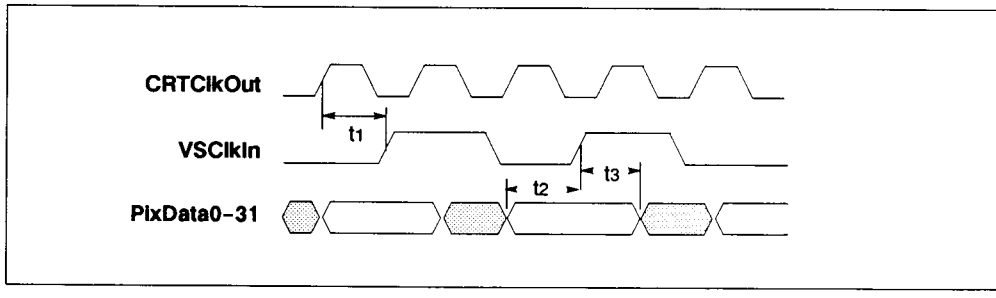
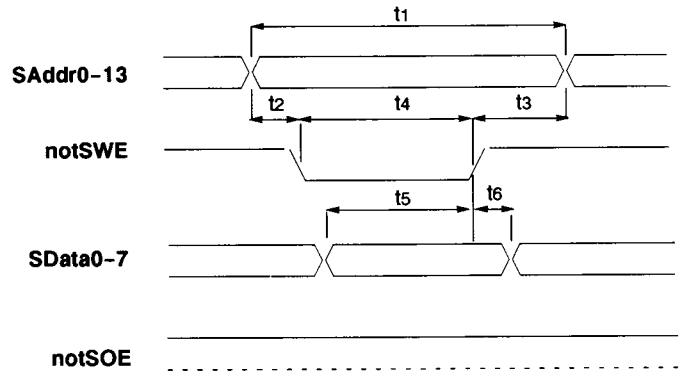


Figure 7.5 VRAM interface timings diagram

Symbol	Parameter	Min	Max	Units	Notes
t1	**CRTClkOut** high **VSClkIn** high		20.0	ns	
t2	**PixData0-31** setup time	5	-	ns	
t3	**PixData0-31** hold time	15	-	ns	

Table 7.5 VRAM interface timings

7.5 SRAM (sprite buffer) timings



Note: **notSOE** is always high during a write cycle

Figure 7.6 SRAM write cycle timings diagram

Symbol	Parameter	Min	Max	Units	Notes
t1	Write cycle time	177.6		ns	
t2	**SAddr0-13** set up time	22.2		ns	
t3	**SAddr0-13** hold time	44.4		ns	
t4	**notSWE** pulse width low	111.0	250.0	ns	
t5	**SData0-7** set up time	88.8		ns	
t6	**SData0-7** hold time	22.2		ns	

Note: Minimum times assume a maximum operating frequency of 44.9 MHz.

Table 7.6 SRAM write cycle timings

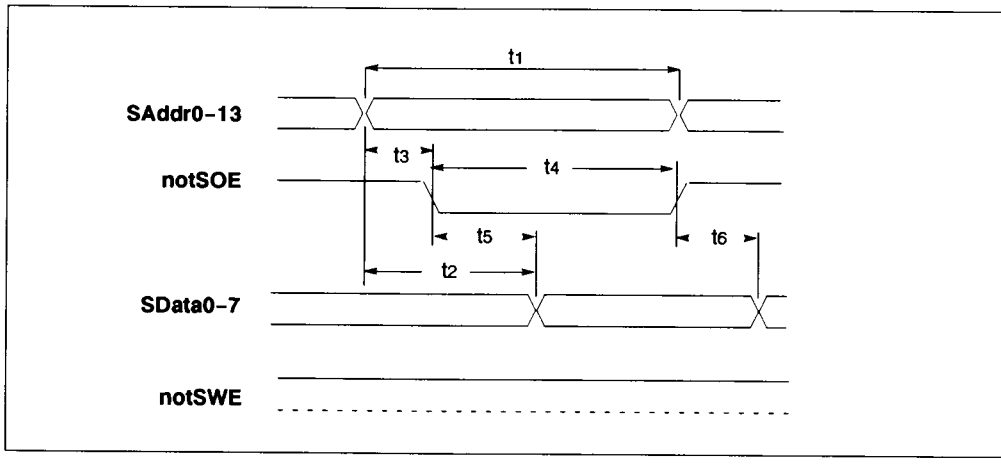


Figure 7.7 SRAM read cycle timings diagram

Symbol	Parameter	Min	Max	Units	Notes
t1	Read cycle time	177.6		ns	
t2	**SAddr0-13** access time		150.0	ns	
t3	**SAddr0-13** to **notSOE** set up time	44.4		ns	
t4	**notSOE** pulse width low	133.2	300.0	ns	
t5	**notSOE** to data valid		80.0	ns	
t6	**SData0-7** hold from **SAddr0-13** change	0.0		ns	

Note: Minimum times assume a maximum operating frequency of 44.9 MHz.

Table 7.7 SRAM read cycle timings

8 Electrical specifications

8.1 DC operating conditions

Symbol	Parameter	Typical	Units	Notes
PDmax	Power dissipation	0.72 0.78	W W	44.9MHz 50MHz

Symbol	Parameter	Min	Max	Units
VIH	Input logic '1' voltage	2.0	VCC+0.5	Volts
VIL	Input logic '0' voltage	-0.5	0.8	Volts
VOH	Output logic '1' voltage	2.4	VDD	Volts
VOL	Output logic '0' voltage	0	0.4	Volts
IIN	Digital input current	-10	+10	µA
IO	Digital output current	-5	+5	mA

Note: Some of the inputs have a 5K pull-up resistor connected to +5V. These are **MonId0-3**, **AuxVidEVideo**, **AuxVidESync**, **AuxVidEDClk**.

8.2 Video oscillator input clock specification

The following specification applies to the video oscillator input clock signals **VideoOsc0-2**.

Parameter		Units
Mark/Space ratio (minimum)	45:55	
Edge transition time	<1.5	ns

8.3 DAC characteristics

Symbol	Parameter	Min	Max	Units	Notes
	Resolution		6	bits	
VO(max)	Output voltage		1.5	Volts	IO < 10mA
IO(max)	Output current		21	mA	VO < 1V
	Integral linearity error		0.5	LSB	
	Full scale error		±5	%	
	DAC to DAC matching, full scale O/P		1	%	
	Rise/Fall time, 10-90%		8	ns	

8.4 Pin output loading characteristics

Pin name	C_L (pF)	V_{OH} (Volts)		V_{OL} (Volts)		I_{OH} (mA)	I_{OL} (mA)	Rs (Ω)		Islew
	Max	Min	Max	Min	Max	Max	Max	Min	Max	Min
AuxVidData0-7 **AuxVidDClk** **notAuxVidBlank**	50	2.4	4.5	0.0	0.4	-0.7	8.0	20	30	Medium
SAddr0-13 **SData0-7** **notSWE** **notSOE** **CRTClkOut** **CRTClkOut2**	25	2.4	4.5	0.0	0.4	-1.5	4.0	40	50	Fast
Data0-7	100	2.4	4.5	0.0	0.4	-0.7	8.0	40	50	Slow

Where,

C_L is the maximum load capacitance
V_{OH} is the high level output voltage
V_{OL} is the low level output voltage
I_{OH} is the high level output current
I_{OL} is the low level output current
Rs is the termination impedance
Islew is the current slew rate

9 Package specifications

The IMS G190 is constructed in a 144 pin ceramic quad flat pack (CQFP) package.

9.1 144 pin ceramic quad flatpack dimensions

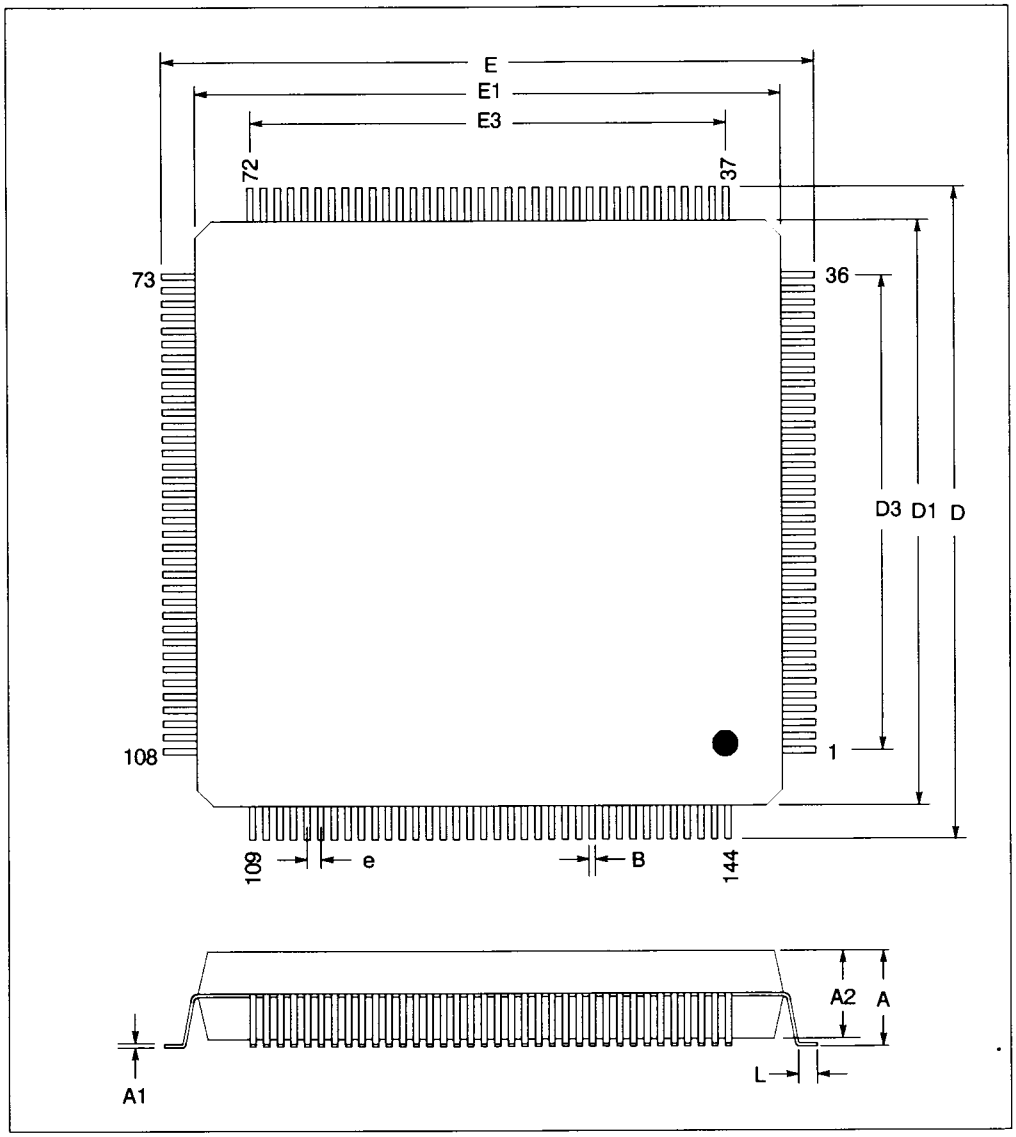


Figure 9.1 144 pin ceramic quad flat pack package dimensions

Dim	Millimetres			Inches			Notes
	Min	Nom	Max	Min	Nom	Max	
A			4.50			0.177	
A1	0.10	0.15	0.20	0.004	0.006	0.008	
A2		4.20			0.165		Ref.
D	31.60	31.80	32.00	1.244	1.252	1.260	
D1	27.80	28.00	28.20	1.094	1.102	1.110	
D3		22.75			0.896		Ref.
E	31.60	31.80	32.00	1.244	1.252	1.260	
E1	27.80	28.00	28.20	1.094	1.102	1.110	
E3		22.75			0.896		Ref.
L	0.65	0.80	0.95	0.026	0.032	0.038	
e		0.65			0.0256		BSC
B	0.25	0.30	0.35	0.010	0.012	0.014	

Table 9.1 144 pin ceramic quad flat pack package dimensions

9.2 IMS G190 package pinout

Tables 9.2 and 9.3 detail the IMS G190 package pinout by pin number and by signal name respectively.

A summary of the pin functions is given in Section 3.

Pin	Signal name	Pin	Signal name	Pin	Signal name	Pin	Signal name
1	PixData5	37	Data0	73	RegAddr3	109	GND
2	PixData4	38	Data1	74	RegAddr4	110	GND
3	PixData3	39	Data2	75	RegAddr5	111	GND
4	PixData2	40	Data3	76	RegAddr6	112	GND
5	PixData1	41	VDD	77	GND	113	VDD
6	PixData0	42	VDD	78	VDD	114	VDD
7	GND	43	Data4	79	notRegWE	115	VDD
8	notAuxVidBlank	44	Data5	80	VSClkIn	116	VDD
9	AuxVidData0	45	Data6	81	VideoCtrlIn1	117	PixData31
10	AuxVidData1	46	Data7	82	VideoCtrlIn0	118	PixData30
11	AuxVidData2	47	VDD	83	AuxVidEVideo	119	PixData29
12	AuxVidData3	48	SAddr0	84	AuxVidESync	120	PixData28
13	VDD	49	SAddr1	85	AuxVidEDClk	121	PixData27
14	VDD	50	SAddr2	86	MonId3	122	PixData26
15	AuxVidData4	51	SAddr3	87	MonId2	123	PixData25
16	AuxVidData5	52	SAddr4	88	MonId1	124	PixData24
17	AuxVidData6	53	SAddr5	89	MonId0	125	PixData23
18	AuxVidData7	54	SAddr6	90	Blue	126	PixData22
19	AuxVidDClk	55	GND	91	Green	127	PixData21
20	GND	56	GND	92	Red	128	PixData20
21	SData0	57	VDD	93	AGND	129	PixData19
22	SData1	58	SAddr7	94	AGND	130	PixData18
23	SData2	59	SAddr8	95	AGND	131	PixData17
24	SData3	60	SAddr9	96	AVDD	132	PixData16
25	VDD	61	SAddr10	97	AVDD	133	VDD
26	GND	62	SAddr11	98	AGND	134	GND
27	GND	63	SAddr12	99	Rref	135	PixData15
28	SData4	64	SAddr13	100	Vref	136	PixData14
29	SData5	65	GND	101	VideoOsc2	137	PixData13
30	SData6	66	GND	102	VideoOsc1	138	PixData12
31	SData7	67	notSOE	103	VideoOsc0	139	PixData11
32	VDD	68	notSWE	104	GND	140	PixData10
33	CRTClkOut	69	VDD	105	VDD	141	PixData9
34	CRTClkOut2	70	RegAddr0	106	notDataStrobe	142	PixData8
35	GND	71	RegAddr1	107	HoldToGND	143	PixData7
36	GND	72	RegAddr2	108	CompRef	144	PixData6

Table 9.2 IMS G190 144 pin QFP package pinout by pin number

Signal name	Pin	Signal name	Pin	Signal name	Pin	Signal name	Pin
AGND	93	GND	47	PixData13	137	SAddr8	59
AGND	94	GND	55	PixData14	136	SAddr9	60
AGND	95	GND	56	PixData15	135	SAddr10	61
AGND	98	GND	65	PixData16	132	SAddr11	62
AuxVidData0	9	GND	66	PixData17	131	SAddr12	63
AuxVidData1	10	GND	77	PixData18	130	SAddr13	64
AuxVidData2	11	GND	104	PixData19	129	SData0	21
AuxVidData3	12	GND	109	PixData20	128	SData1	22
AuxVidData4	15	GND	110	PixData21	127	SData2	23
AuxVidData5	16	GND	111	PixData22	126	SData3	24
AuxVidData6	17	GND	112	PixData23	125	SData4	28
AuxVidData7	18	GND	134	PixData24	124	SData5	29
AuxVidEDClk	85	Green	91	PixData25	123	SData6	30
AuxVidEVideo	83	HoldToGnd	107	PixData26	122	SData7	31
AuxVidESync	84	MonId0	89	PixData27	121	VDD	13
AuxVidDClk	19	MonId1	88	PixData28	120	VDD	14
AVDD	96	MonId2	87	PixData29	119	VDD	25
AVDD	97	MonId3	86	PixData30	118	VDD	32
Blue	90	notDataStrobe	106	PixData31	117	VDD	41
CompRef	108	notAuxVidBlank	8	Red	92	VDD	42
CRTClkOut	33	notRegWE	79	RegAddr0	70	VDD	57
CRTClkOut2	34	notSOE	67	RegAddr1	71	VDD	69
Data0	37	notSWE	68	RegAddr2	72	VDD	78
Data1	38	PixData0	6	RegAddr3	73	VDD	105
Data2	39	PixData1	5	RegAddr4	74	VDD	113
Data3	40	PixData2	4	RegAddr5	75	VDD	114
Data4	43	PixData3	3	RegAddr6	76	VDD	115
Data5	44	PixData4	2	Rref	99	VDD	116
Data6	45	PixData5	1	SAddr0	48	VDD	133
Data7	46	PixData6	144	SAddr1	49	VideoCtrlIn0	82
GND	7	PixData7	143	SAddr2	50	VideoCtrlIn1	81
GND	20	PixData8	142	SAddr3	51	VideoOsc0	103
GND	26	PixData9	141	SAddr4	52	VideoOsc1	102
GND	27	PixData10	140	SAddr5	53	VideoOsc2	101
GND	35	PixData11	139	SAddr6	54	Vref	100
GND	36	PixData12	138	SAddr7	58	VSClkIn	80

Table 9.3 IMS G190 144 pin QFP package pinout by signal name

10 Ordering information

Device	Clock rate	Package	Part number
IMS G190	50MHz	144 pin ceramic quad flat pack	IMS G190F-50S

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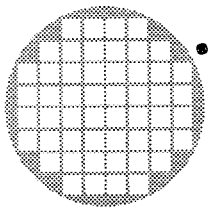

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