21256
256K (262,144 x 1) DYNAMIC RAM WITH FAST PAGE MODE

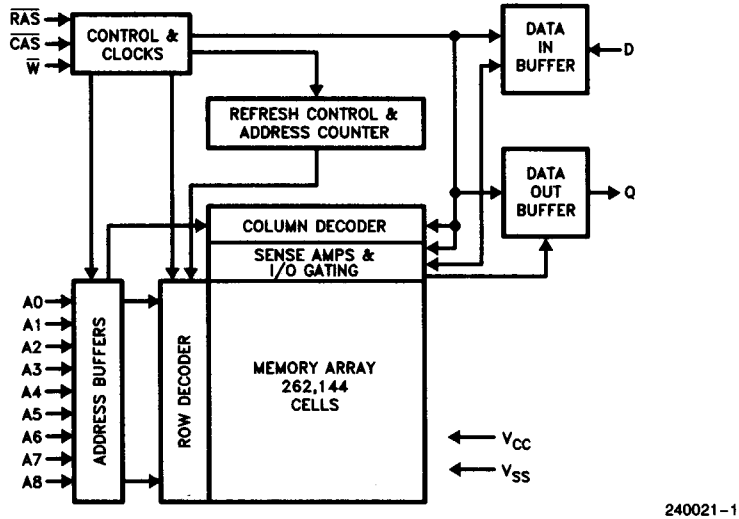
Symbol	Parameter	21256-08	Units
t_{RAC}	Access Time from $\overline{RAS}$	80	ns
t_{CAC}	Access Time from $\overline{CAS}$	20	ns
t_{RC}	Read Cycle Time	150	ns

- **Page Mode Capability**
- **$\overline{CAS}$-before-$\overline{RAS}$ Refresh Capability**
- **$\overline{RAS}$-Only and Hidden Refresh Capability**
- **TTL Compatible Inputs and Output**
- **Common I/O Using Early Write**
- **Single +5V ±10% Power Supply**
- **256 Cycle/4 ms Refresh**
- **JEDEC Standard Pinout in PDIP (P)**

Intel's 21256 is a fully decoded dynamic random access memory organized as 262,144 one-bit words. The design is optimized for high speed, high performance applications such as computer memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

The 21256 features page mode which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. Multiplexed row and column address inputs permit the 21256 to be housed in a JEDEC standard 16-pin DIP.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.



240021-1

Figure 1. Functional Block Diagram

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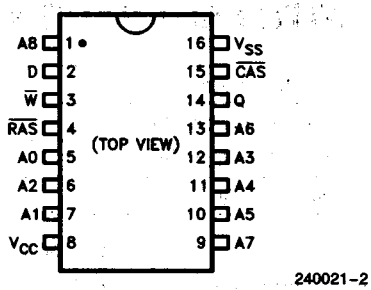
May 1991
Order Number: 240021-005

PDIP (P)



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Pin Names

A_0–A_8	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin
Relative to V_{SS} ..... V_{OUT} −1.0V to +7.0V
Voltage on V_{CC} Supply
Relative to V_{SS} ..... −1.0V to +7.0V
Storage Temperature ..... −55°C to +125°C
Power Dissipation 1.0W
Short Circuit Output Current ..... 50 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS Voltages referenced to V_{SS}, T_A = 0 to 70°C

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.4		V_{CC}+1	V
V_{IL}	Input Low Voltage	−1		0.8	V

DC AND OPERATING CHARACTERISTICS

Recommended operating conditions unless otherwise noted.

Symbol	Parameter		Min	Max	Units	Test Condition
I_{CC1}	Operating Current*	21256-08		60	mA	($\overline{RAS}$ and $\overline{CAS}$ cycling @ t_{RC} = min.)
I_{CC2}	Standby Current	21256-08		2.0	mA	($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})
I_{CC3}	$\overline{RAS}$-Only Refresh Current*	21256-08		60	mA	($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling @ t_{RC} = min.)
I_{CC4}	Page Mode Current*	21256-08		40	mA	($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)
I_{CC5}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current*	21256-08		55	mA	($\overline{RAS}$ cycling @ t_{RC} = min.)
I_{CC6}	Standby Current			1.0	mA	($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)
I_{IL}	Input Leakage Current		−10	10	µA	(Any input 0 ≤ V_{IN} ≤ 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, All other pins not under test = 0.)
I_{OL}	Output Leakage Current		−10	10	µA	(Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V, V_{CC} = 5.5V, V_{SS} = 0V)

***NOTE:**
I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as average current.

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DC AND OPERATING CHARACTERISTICS

Recommended operating conditions unless otherwise noted. (Continued)

Symbol	Parameter		Min	Max	Units	Test Condition
V_{OH}	Output High Voltage Level		2.4		V	(I_{OH} = 5 mA)
V_{OL}	Output Low Voltage Level			0.4	V	(I_{OL} = 4.2 mA)

CAPACITANCE T_A = 25°C

Symbol	Parameter	Min	Max	Units
C_{IN1}	Input Capacitance (A_0–A_8, D)		5	pF
C_{IN2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)		8	pF
C_{OUT}	Output Capacitance (Q)		7	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{CC} = 5.0V ±10%. See Notes 1, 2)

Symbol	Parameter	21256-08		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	150		ns	
t_{RWC}	Read-Modify-Write Cycle Time	175		ns	
t_{RAC}	Access Time from $\overline{RAS}$		80	ns	3,4,11
t_{CAC}	Access Time from $\overline{CAS}$		30	ns	3,4,5
t_{AA}	Column Address Access Time		40	ns	3,10
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5		ns	3
t_{OFF}	Output Buffer Turn-Off Delay	0	25	ns	7
t_T	Transition Time (Rise and Fall)	3	50	ns	2
t_{RP}	$\overline{RAS}$ Precharge Time	75		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	30		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time (All Cycles except Page Mode)	15		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	30	10,000	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	ns	4
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	ns	11
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time ($\overline{RAS}$ Only Refresh)	15		ns	
t_{ASR}	Row Address Setup Time	0		ns	

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$. See Notes 1, 2) (Continued)

Symbol	Parameter	21256-08		Units	Notes
		Min	Max		
t_{RAH}	Row Address Hold Time	15		ns	
t_{ASC}	Column Address Setup Time	0		ns	
t_{CAH}	Column Address Hold Time	20		ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	65		ns	6
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40		ns	
t_{RCS}	Read Command Setup Time	0		ns	
t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	5		ns	9
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5		ns	9
t_{WCS}	Write Command Setup Time	0		ns	8
t_{WCH}	Write Command Hold Time	15		ns	
t_{WP}	Write Command Pulse Width	15		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	30		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	30		ns	
t_{DS}	Data-In Setup Time	0		ns	10
t_{DH}	Data-In Hold Time	15		ns	10
t_{CWD}	$\overline{CAS}$ to Write Enable Delay	25		ns	8
t_{RWD}	$\overline{RAS}$ to Write Enable Delay	80		ns	8
t_{AWD}	Column Address to $\overline{W}$ Delay Time	40		ns	8
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	60		ns	6
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	60		ns	6
t_{REF}	Refresh Period (256 Cycles)		4	ms	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH					
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh)	10		ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh)	25		ns	
t_{CPT}	Refresh Counter Test $\overline{CAS}$ Precharge Time	50		ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	10		ns	
PAGE MODE					
t_{PC}	Page Mode Cycle Time	55		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Page Mode Only)	15		ns	

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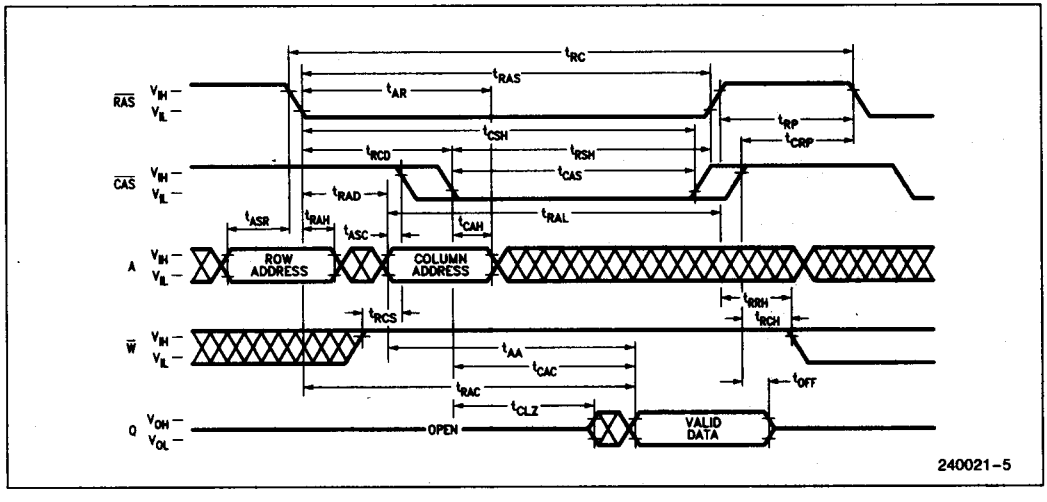
AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$. See Notes 1, 2) (Continued)

Symbol	Parameter	21256-08		Units	Notes
		Min	Max		
PAGE MODE (Continued)					
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		50	ns	3
t_{PRWC}	Fast Page Mode Read-Modify-Write	85		ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	10,000	ns	

NOTES:
1. An initial pause of 200 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5 ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100 pF.
4. Operation within the T_{RCD}(max) limit ensures that T_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \ge t_{RCD}$(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non-restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \ge t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \ge t_{CWD(min)}$, $t_{RWD} \ge t_{RWD(min)}$ and $t_{AWD} \ge t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.

TIMING DIAGRAMS

READ CYCLE



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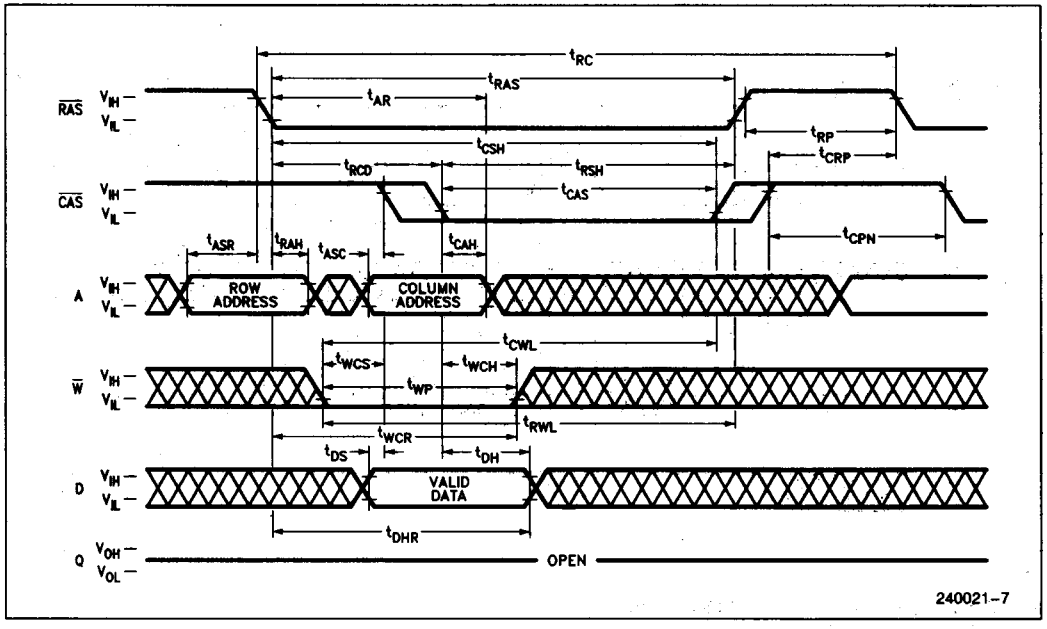
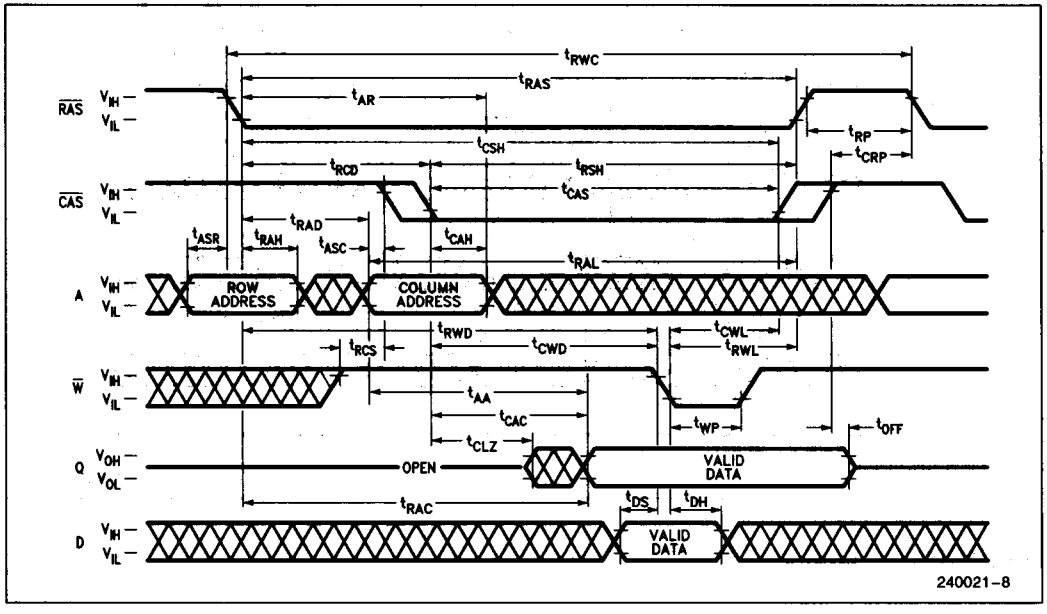
TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



READ-WRITE/READ-MODIFY-WRITE CYCLE



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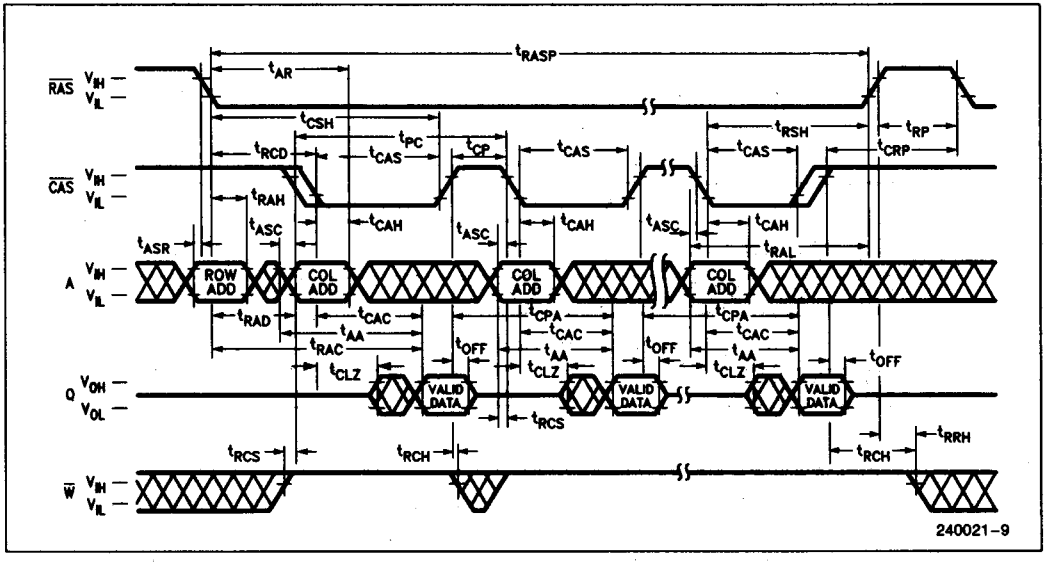
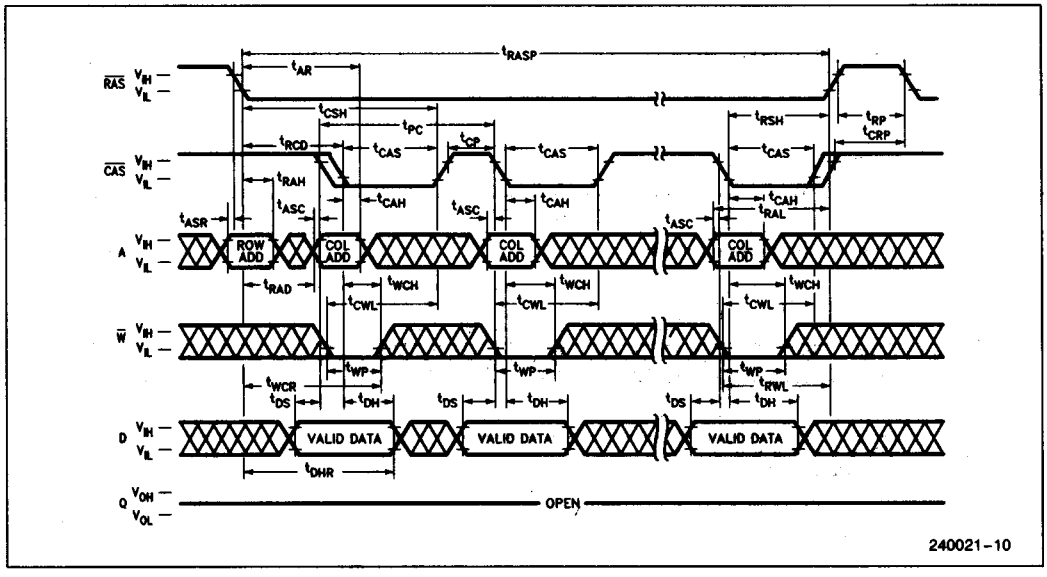
TIMING DIAGRAMS (Continued)

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE (EARLY WRITE)



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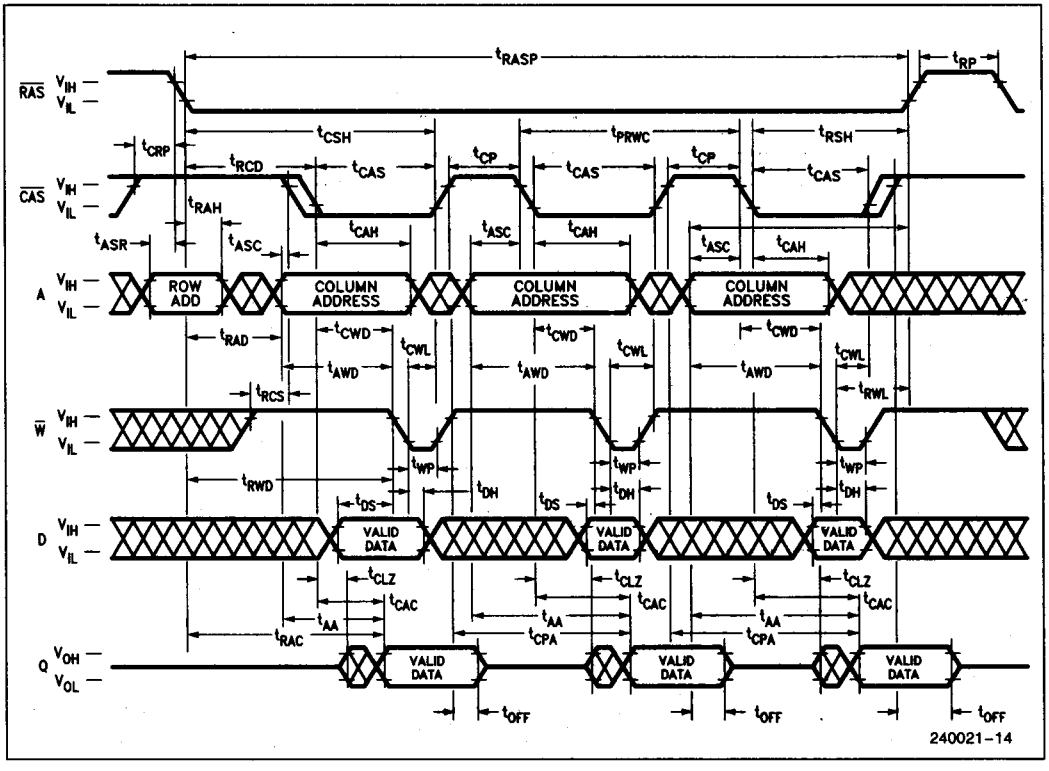
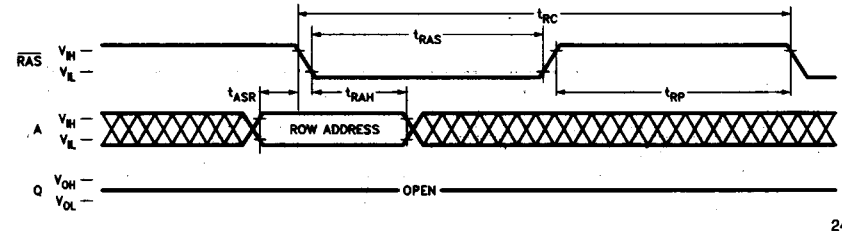
TIMING DIAGRAMS (Continued)

PAGE MODE READ-WRITE CYCLE



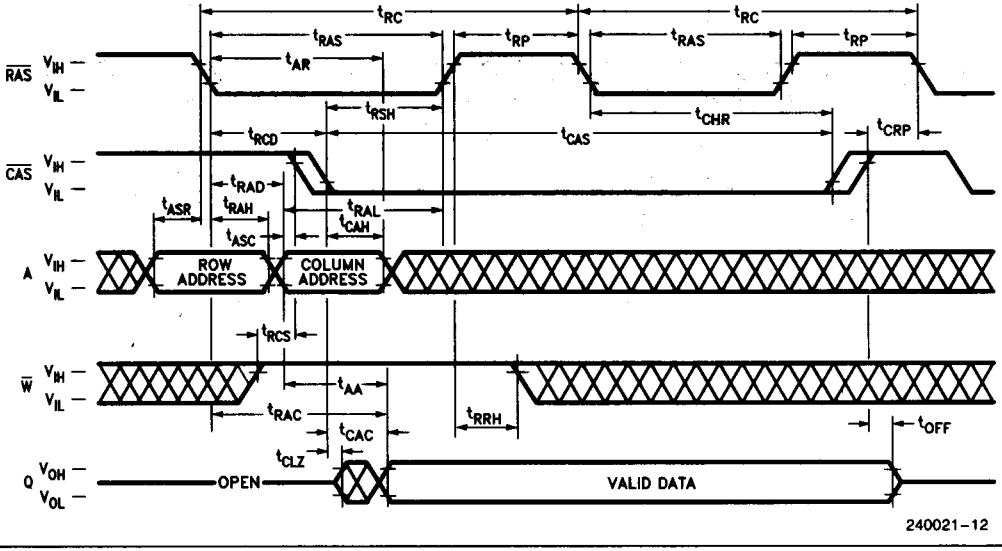
TIMING DIAGRAMS (Continued)

$\overline{RAS}$-ONLY REFRESH CYCLE



NOTE:
$\overline{CAS}$ = V_{IH}; $\overline{W}$, D = Don't Care

HIDDEN REFRESH CYCLE



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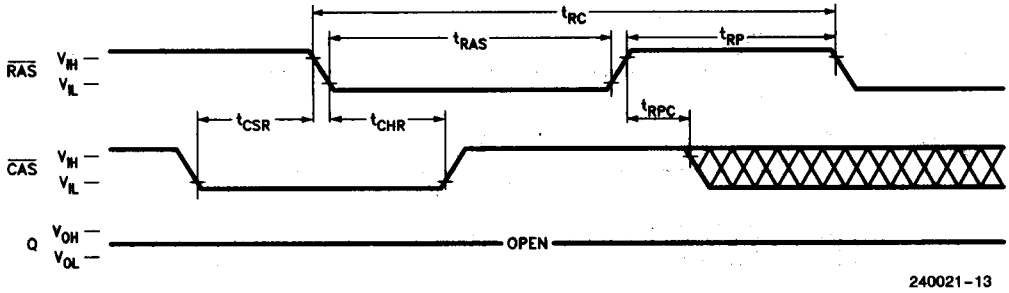
TIMING DIAGRAMS (Continued)

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



NOTE:
Address, $\overline{W}$, D = Don't Care

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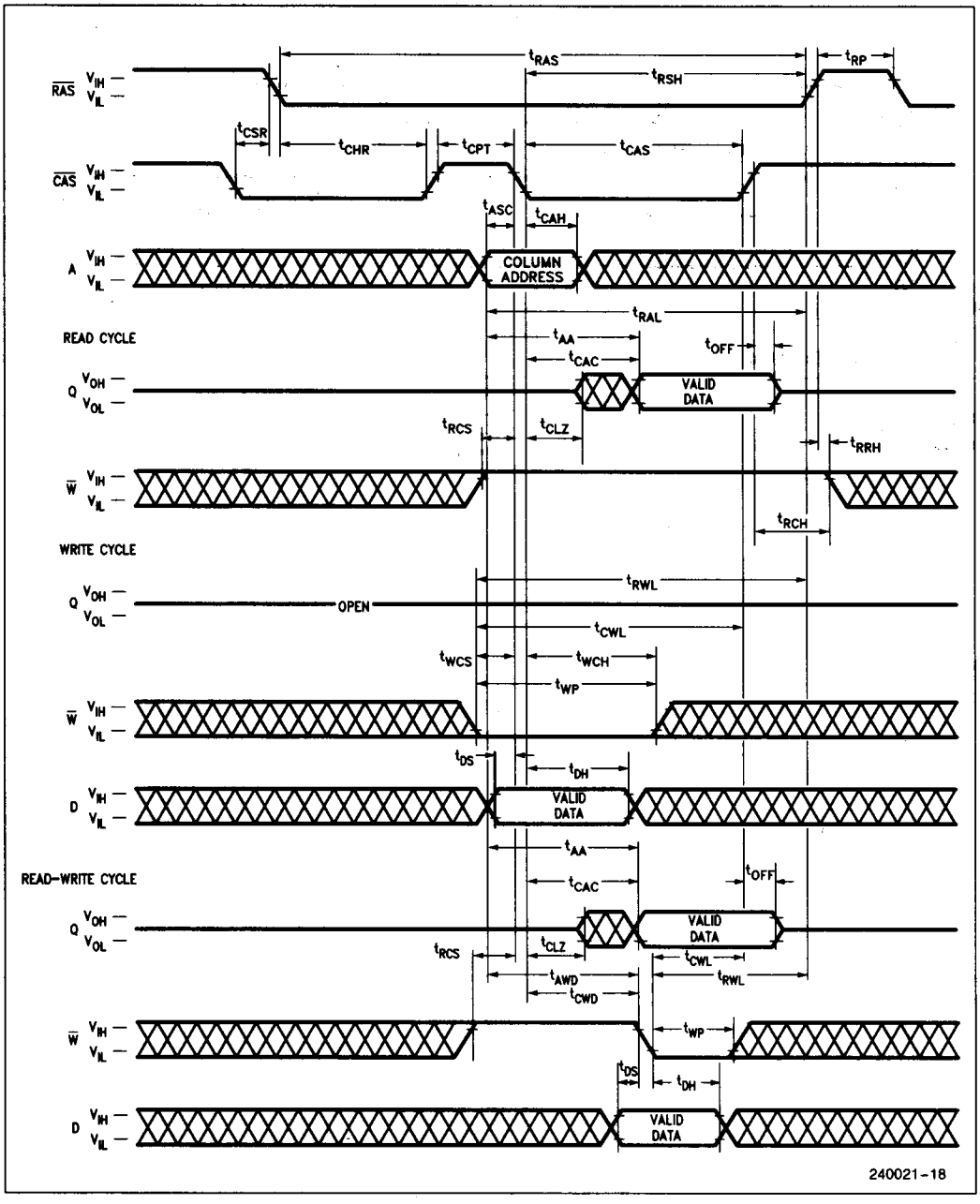
TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



Don't Care

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DEVICE OPERATION

The 21256 contains 262,144 memory locations. Eighteen address bits are required to address a particular memory location. Since the 21256 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the 21256 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any 21256 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the 21256 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The output of the 21256 remains in the Hi-Z state until valid data appears at the output. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The 21256 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing W low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD} and t_{CWD}, are not necessarily met. The state of data-out is indeterminate since the output could be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The 21256 has a tri-state output buffer which is controlled by $\overline{CAS}$ (and $\overline{W}$ for early write). Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output first remains in the Hi-Z state until the data is valid and then the valid data appears at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the 21256 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Page Mode Read, Page Mode Read-Modify-Write.

HI-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the 21256 is stored on a tiny capacitor within each memory cell. Due to leakage, the data will leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 4 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The 21256 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified setup time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs and the on-chip refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The 21256 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required in hidden refresh cycles by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Other Refresh Methods: It is also possible to refresh the 21256 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Page Mode

The 21256 has page mode capability. Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In page mode, it is possible to perform read, write or read-modify-cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A page mode cycle begins with a normal cycle. While $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 9 row address bits and 9 column address bits defined as follows:

Row Address—Bits A0 through A7 are supplied by the on-chip refresh counter. The A8 bit is set high internally.

Column Address—Bits A0 through A8 are strobed-in by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 256 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 256 times so that highs are written into the 256 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-Up

If $\overline{RAS}$ = V_{SS} during power-up, the 21256 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 100 μs is required after power-up followed by 8 initialization cycles before proper device operation is assured. 8 initialization cycles are also required after any 4 ms period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the 21256 inputs act like unterminated transmission lines resulting in significant positive and negative overshoots at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the 21256 input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20Ω to 40Ω.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMs. The impedance is minimized if all the power supply traces to all DRAMs run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMs these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMs.

Decoupling

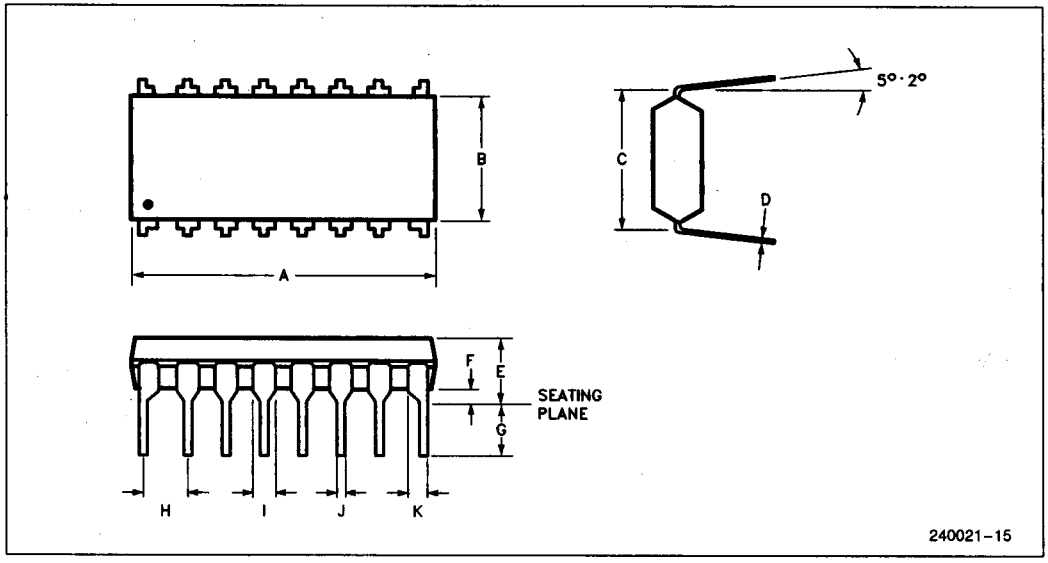
The importance of proper decoupling cannot be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). The total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500 mV.

A high frequency 0.3 μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each 21256 using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the 21256 and they supply much of the current used by the 21256 during cycling.

In addition, a large tantalum capacitor with a value of 47 μF to 100 μF should be used for bulk decoupling to recharge the 0.3 μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor throughout the memory array.

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL-IN-LINE PACKAGE (P)



Item	Millimeters	Inches
A	19.43 ±0.05	0.765 ±0.002
B	6.86 ±0.05	0.270 ±0.002
C	7.62	0.300
D	0.25 ±0.025	0.010 ±0.001
E	3.56 ±0.05	0.140 ±0.002
F	0.506 ±0.1	0.020 ±0.004
G	3.3 ±0.1	0.130 ±0.004
H	2.54	0.100
I	1.52	0.060
J	0.457 ±0.05	0.018 ±0.002
K	0.1 ±0.05	0.040 ±0.002

REVISION SUMMARY

The following list represents the key differences between version -004 and -005 of the 21256 Data Sheet.

1. Deleted 21256-06, 21256-07, and 21256-10 products and specifications.
2. Deleted ZIP (Z) and PLCC (N) packages.
3. Deleted Sales Office mailing lists.