MOTOROLA

MCM6664A

Advance Information

MOS
(N-CHANNEL, SILICON-GATE)

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

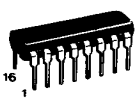
64K-BIT DYNAMIC RAM

The MCM6664A is a 65,536 bit, high-speed, dynamic Random-Access Memory. Organized as 65,536 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology, this new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM6664A requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{CAS}$ allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6664A incorporates a one-transistor cell design and dynamic storage techniques. In addition to the $\overline{RAS}$-only refresh mode, the refresh control function available on pin 1 provides two additional modes of refresh, automatic and self refresh.

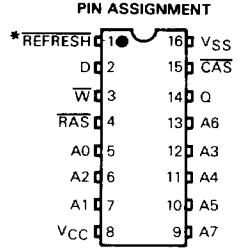
- Organized as 65,536 Words of 1 Bit
- Single 5 Volt Operation (±10%)
- Maximum Access Time: MCM6664A-12 = 120 ns
  MCM6664A-15 = 150 ns
  MCM6664A-20 = 200 ns
- Low Power Dissipation
  302.5 mW Maximum (Active) (MCM6664A-15)
  22 mW Maximum (Standby)
- Three-State Data Output
- Early-Write Common I/O Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- Control on Pin 1 for Automatic or Self Refresh
- $\overline{RAS}$-only Refresh Mode
- $\overline{CAS}$ Controlled Output
- Fast Page Mode Cycle Time
- Low Soft Error Rate <0.1% per 1000 Hours (See Soft Error Testing)



P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 690

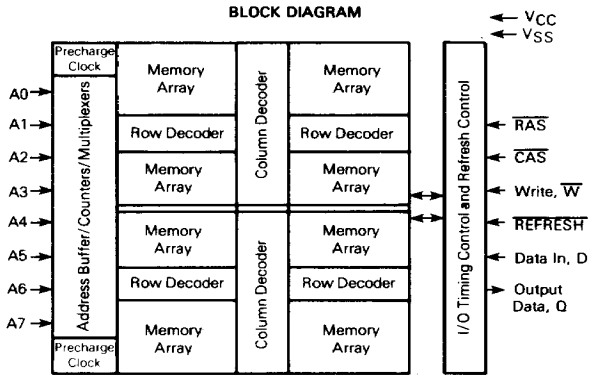
PIN ASSIGNMENT



*If pin is not used, it should be connected to V_{CC} through a 10 k resistor.

PIN NAMES	
$\overline{REFRESH}$	Refresh
A0-A7	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

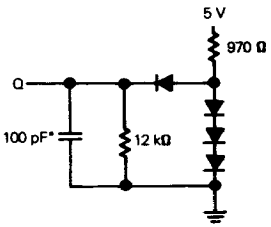
ADI-875R1/3-82

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS} (except V_{CC})	V_{in}, V_{out}	−2 to +7	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current (Short Circuit)	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 1 — OUTPUT LOAD



*Includes Jig Capacitance

DRAM

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	MCM6664A-12, -15, -20	V_{CC}	4.5	5.0	5.5	V	1
		V_{SS}	0	0	0	V	1
Logic 1 Voltage, All Inputs		V_{IH}	2.4	–	V_{CC}+1	V	1
Logic 0 Voltage, All Inputs		V_{IL}	−1.0	–	0.8	V	1, 19

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Units	Notes
V_{CC} Power Supply Current (Standby)	I_{CC2}	–	4.0	mA	5
V_{CC} Power Supply Current					
6664A-12, t_{RC} = 250 ns	I_{CC1}	–	60	mA	4
6664A-15, t_{RC} = 270 ns		–	55		
6664A-20, t_{RC} = 330 ns		–	45		
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles					
6664A-12, t_{RC} = 250 ns	I_{CC3}	–	50	mA	4
6664A-15, t_{RC} = 270 ns		–	45		
6664A-20, t_{RC} = 330 ns		–	35		
V_{CC} Power Supply Current During Page Mode Cycle for t_{RAS} = 10 μsec					
6664A-12, $t_{PC} = t_{RP}$ = 120 ns	I_{CC4}	–	45	mA	4
6664A-15, $t_{PC} = t_{RP}$ = 145 ns		–	40		
6664A-20, $t_{PC} = t_{RP}$ = 200 ns		–	35		
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$) (Any Input Except $\overline{REFRESH}$)	$I_{I(L)}$	–	10	μA	–
$\overline{REFRESH}$ Input Current ($V_{SS} \le V_{in} \le V_{CC}$)	I_F	–	20	μA	–
Output Leakage Current ($\overline{CAS}$ at logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{O(L)}$	–	10	μA	–
Output Logic 1 Voltage @ I_{out} = −4 mA	V_{OH}	2.4	–	V	–
Output Logic 0 Voltage @ I_{out} = 4 mA	V_{OL}	–	0.4	V	–

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit	Notes
Input Capacitance (A0-A7), D	C_{I1}	3	5	pF	7
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{REFRESH}$	C_{I2}	6	8	pF	7
Output Capacitance (Q), ($\overline{CAS}$ = V_{IH} to disable output)	C_O	5	7	pF	7

NOTES:

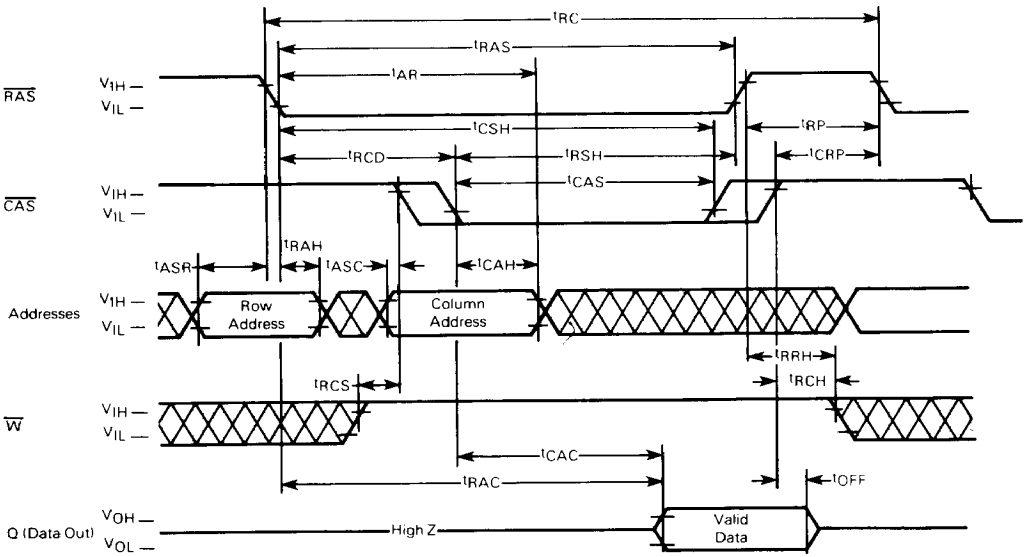
1. All voltages referenced to V_{SS}.
2. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
3. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation guaranteed.
4. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
5. Output is disabled (open-circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
6. The transition time specification applies for all inputs signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$
8. The specifications for t_{RC} (min), and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
9. AC measurements t_T = 5.0 ns.
10. Assumes that $t_{RCD} \le t_{RCD}$ (Max).
11. Assumes that $t_{RCD} \ge t_{RCD}$ (Max)
12. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

AC OPERATING CONDITIONS AND CHARACTERISTICS (Read, Write, and Read-Modify-Write Cycles)
(Full Operating Voltage and Temperature Range Unless Otherwise Noted. See Notes 2, 3, 6, and Figure 1)

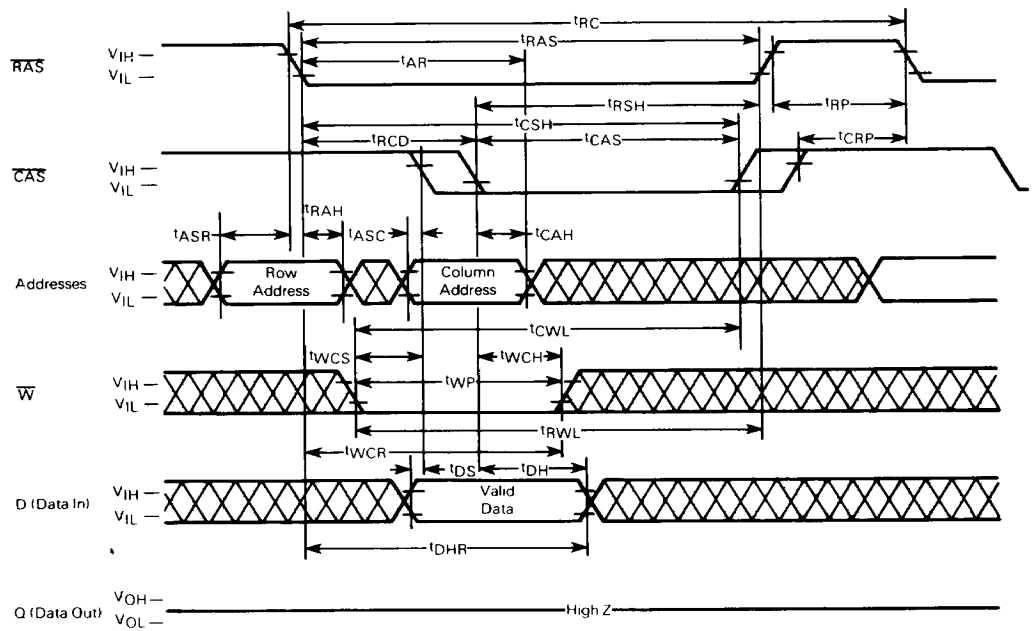
Parameter	Symbol	6664A-12		6664A-15		6664A-20		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	250	–	270	–	330	–	ns	8, 9
Read Write Cycle Time	t_{RWC}	255	–	280	–	345	–	ns	8, 9
Access Time from Row Address Strobe	t_{RAC}	–	120	–	150	–	200	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	60	–	75	–	100	ns	11, 12
Output Buffer and Turn-Off Delay	t_{OFF}	0	30	0	30	0	40	ns	18
Row Address Strobe Precharge Time	t_{RP}	100	–	100	–	120	–	ns	–
Row Address Strobe Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	–
Column Address Strobe Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	–
Row to Column Strobe Lead Time	t_{RCD}	20	60	25	75	30	100	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	ns	–
Row Address Hold Time	t_{RAH}	15	–	20	–	25	–	ns	–
Column Address Setup Time	t_{ASC}	0	–	0	–	0	–	ns	–
Column Address Hold Time	t_{CAH}	25	–	35	–	45	–	ns	–
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	85	–	95	–	120	–	ns	17
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns	–
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	ns	14
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	14
Write Command Hold Time	t_{WCH}	25	–	35	–	45	–	ns	–
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	85	–	95	–	120	–	ns	17
Write Command Pulse Width	t_{WP}	25	–	35	–	45	–	ns	–
Write Command to Row Strobe Lead Time	t_{RWL}	40	–	45	–	55	–	ns	–
Write Command to Column Strobe Lead Time	t_{CWL}	40	–	45	–	55	–	ns	–
Data in Setup Time	t_{DS}	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{DH}	25	–	35	–	45	–	ns	15
Data in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	85	–	95	–	120	–	ns	17
Column to Row Strobe Precharge Time	t_{CRP}	−10	–	−10	–	−10	–	ns	–
$\overline{RAS}$ Hold Time	t_{RSH}	60	–	75	–	100	–	ns	–
Refresh Period	t_{RFSH}	–	2.0	–	2.0	–	2.0	ms	–
$\overline{WRITE}$ Command Setup Time	t_{WCS}	−10	–	−10	–	−10	–	ns	16
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	40	–	45	–	55	–	ns	16
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	100	–	120	–	155	–	ns	16
$\overline{CAS}$ Hold Time	t_{CSH}	120	–	150	–	200	–	ns	–
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CP}	50	–	60	–	80	–	ns	–
Page Mode Cycle Time	t_{PC}	120	–	145	–	200	–	ns	–
$\overline{RAS}$ to $\overline{REFRESH}$ Delay	t_{RFD}	−10	–	−10	–	−10	–	ns	–
$\overline{REFRESH}$ Period (Battery Backup Mode)	t_{FBP}	2000	–	2000	–	2000	–	ns	–
$\overline{REFRESH}$ to $\overline{RAS}$ Precharge Time (Battery Backup Mode)	t_{FBR}	290	–	320	–	400	–	ns	–
$\overline{REFRESH}$ Cycle Time (Auto Pulse Mode)	t_{FC}	250	–	270	–	330	–	ns	–
$\overline{REFRESH}$ Pulse Period (Auto Period Mode)	t_{FP}	60	2000	60	2000	60	2000	ns	–
$\overline{REFRESH}$ to $\overline{RAS}$ Setup Time (Auto Pulse Mode)	t_{FSR}	−30	–	−30	–	−30	–	ns	–
$\overline{REFRESH}$ to $\overline{RAS}$ Delay Time (Auto Pulse Mode)	t_{FRD}	290	–	320	–	400	–	ns	–
$\overline{REFRESH}$ Inactive Time	t_{FI}	60	–	60	–	60	–	ns	–
$\overline{RAS}$ to $\overline{REFRESH}$ Lead Time	t_{FRL}	350	–	370	–	450	–	ns	–
$\overline{RAS}$ Inactive Time During $\overline{REFRESH}$	t_{FRI}	350	–	370	–	450	–	ns	–

14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. Addresses, data-in and WRITE are don't care. Data-out depends on the state of CAS. If CAS remains low, the previous output will remain valid. CAS is allowed to make an active to inactive transition during the pin #1 refresh cycle. When CAS is brought high, the output will assume a high-impedance state.
18. t_{off} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
19. The device will withstand undershoots to the −2 volt level with a maximum pulse width of 20 ns at the −1.5 volt level. This is periodically sampled rather than 100% tested.

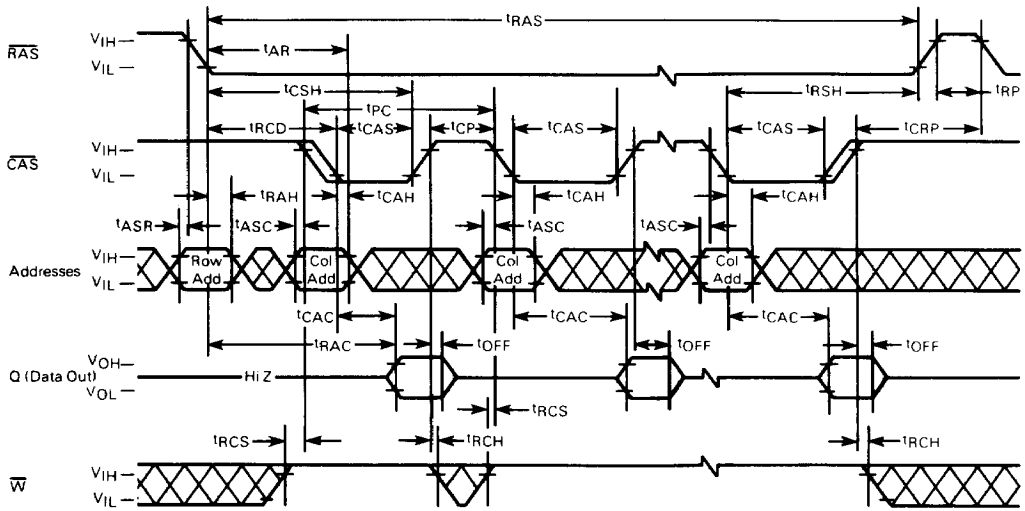
READ CYCLE TIMING



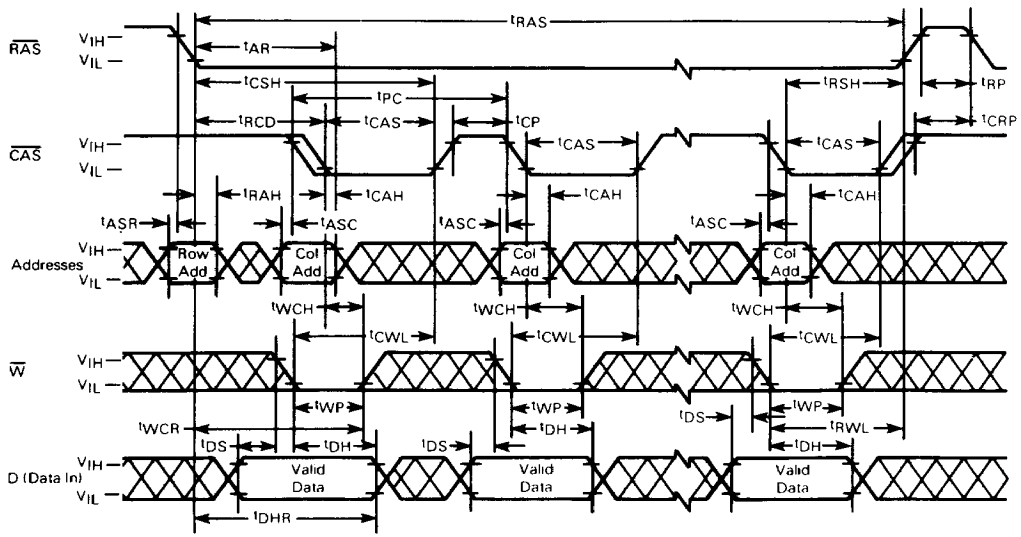
WRITE CYCLE TIMING



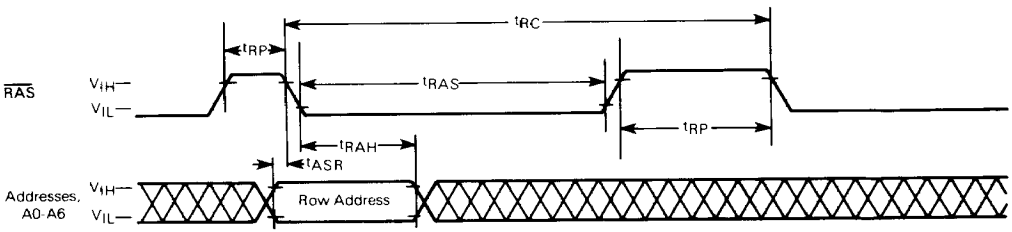
PAGE MODE READ CYCLE



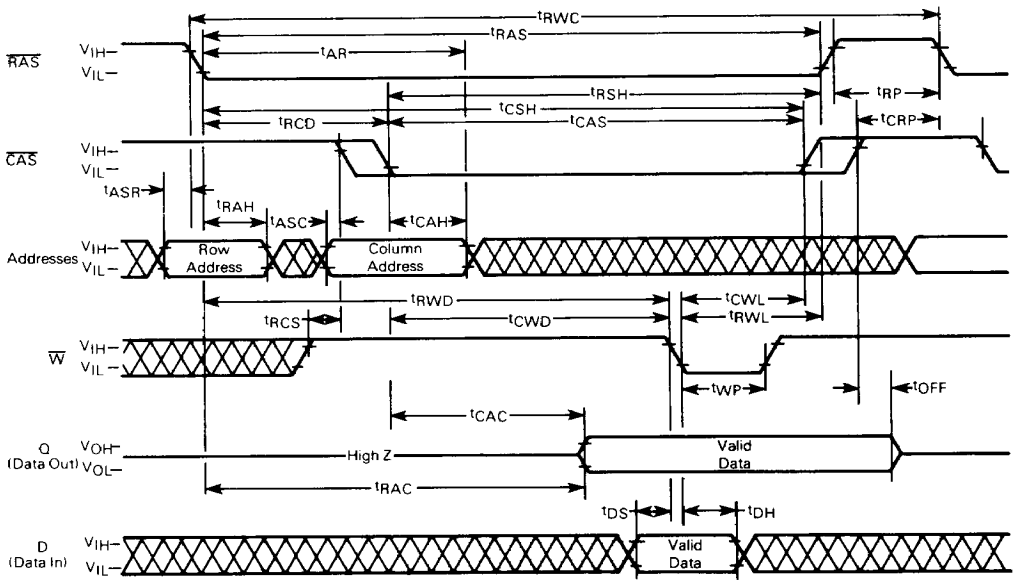
PAGE MODE WRITE CYCLE



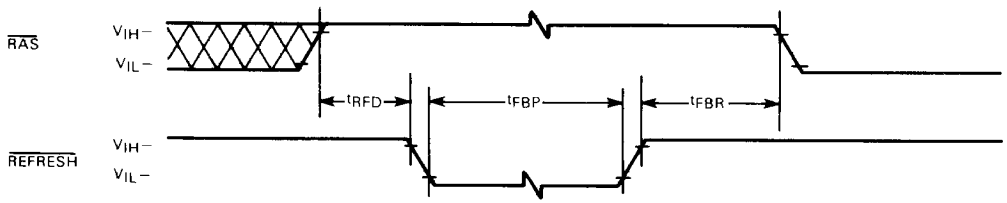
$\overline{RAS}$-ONLY REFRESH CYCLE
(Data-in and $\overline{WRITE}$ are Don't Care, $\overline{CAS}$ is HIGH)



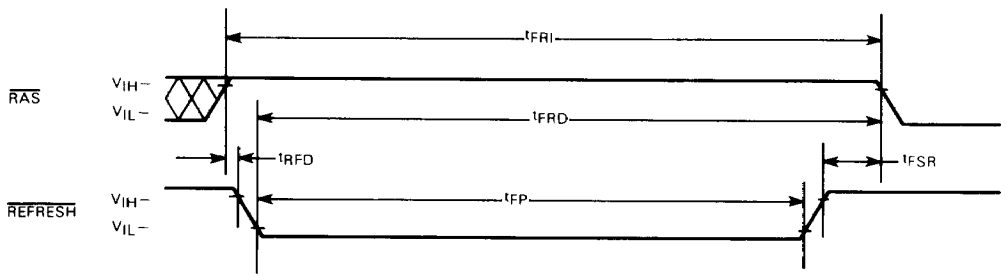
READ-WRITE/READ-MODIFY-WRITE CYCLE



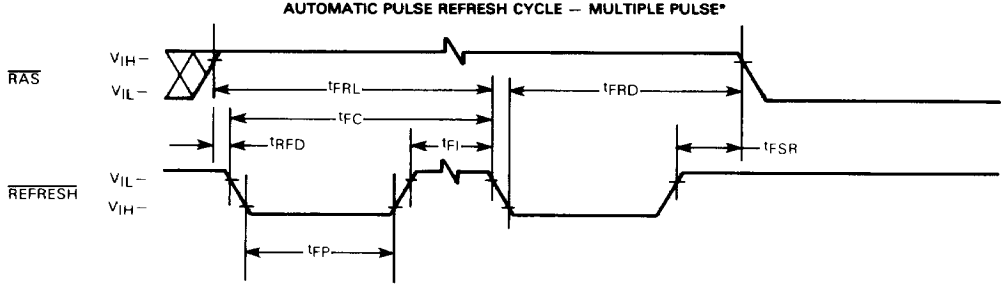
SELF REFRESH MODE (Battery Backup)*



AUTOMATIC PULSE REFRESH CYCLE — SINGLE PULSE*



AUTOMATIC PULSE REFRESH CYCLE — MULTIPLE PULSE*



*Addresses, data-in and $\overline{\text{WRITE}}$ are don't care, $\overline{\text{CAS}}$ is high.

TYPICAL CHARACTERISTICS

FIGURE 2 — $\overline{RAS}$ ACCESS TIME versus SUPPLY VOLTAGE

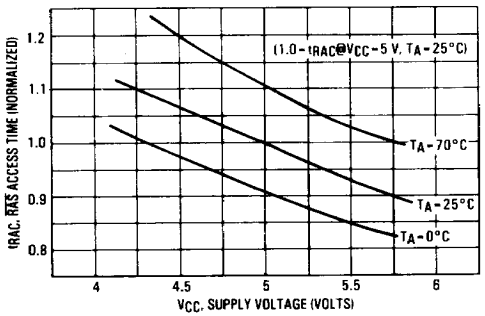


FIGURE 3 — $\overline{CAS}$ ACCESS TIME versus SUPPLY VOLTAGE

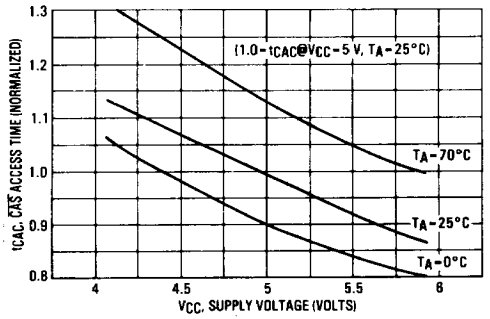


FIGURE 4 — $\overline{RAS}$ ACCESS TIME versus AMBIENT TEMPERATURE

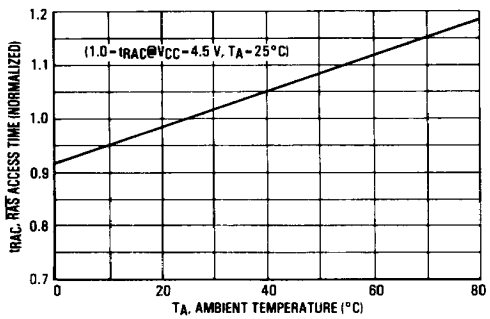


FIGURE 5 — $\overline{CAS}$ ACCESS TIME versus AMBIENT TEMPERATURE

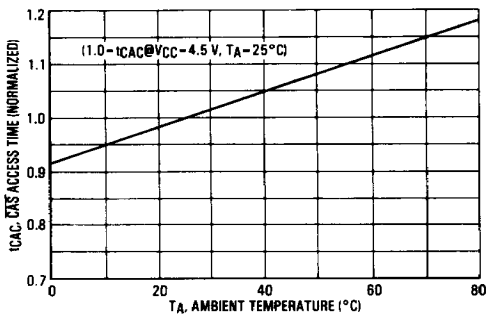


FIGURE 6 — $\overline{RAS}$, $\overline{W}$ INPUT LEVEL versus SUPPLY VOLTAGE

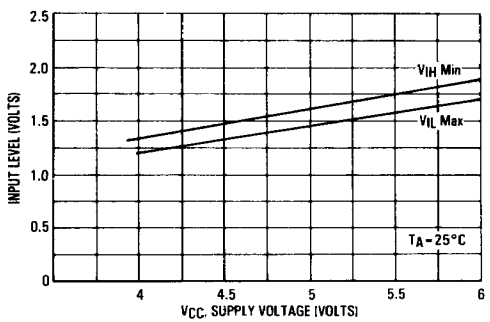
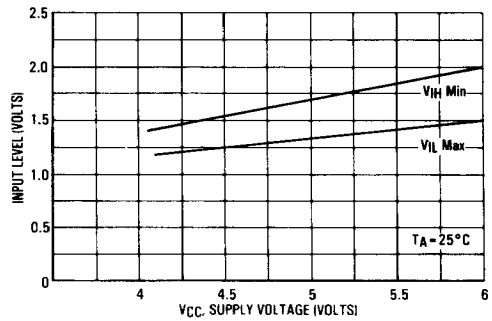


FIGURE 7 — $\overline{CAS}$, $\overline{W}$ INPUT LEVEL versus SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 8 — I_{CC1} SUPPLY CURRENT versus CYCLE RATE

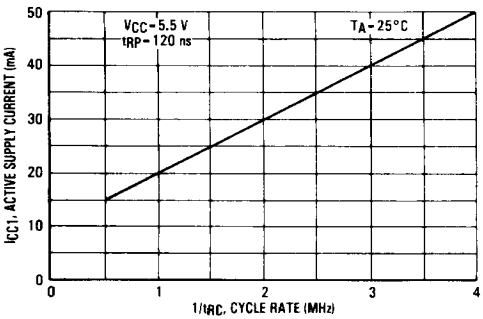


FIGURE 9 — I_{CC1} SUPPLY CURRENT versus SUPPLY VOLTAGE

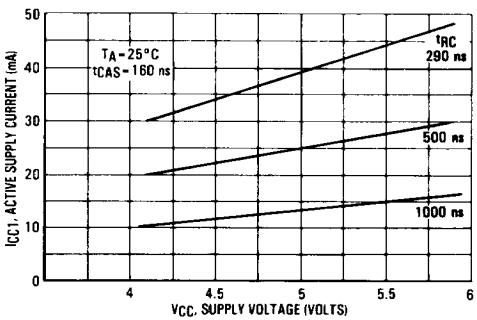


FIGURE 10 — I_{CC1} SUPPLY CURRENT versus SUPPLY VOLTAGE

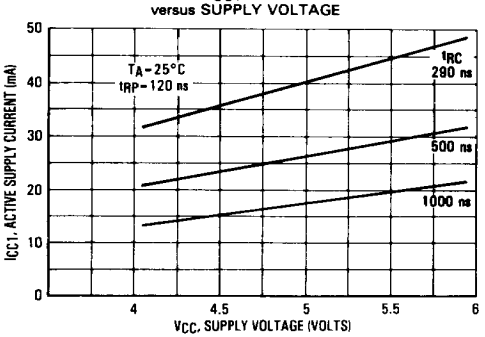


FIGURE 11 — I_{CC1} SUPPLY CURRENT versus AMBIENT TEMPERATURE (min t_{RP})

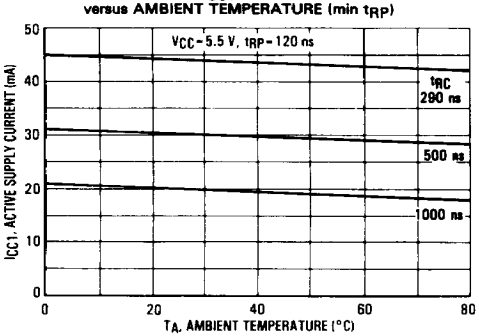


FIGURE 12 — I_{CC1} SUPPLY CURRENT versus AMBIENT TEMPERATURE (min $\overline{RAS}$)

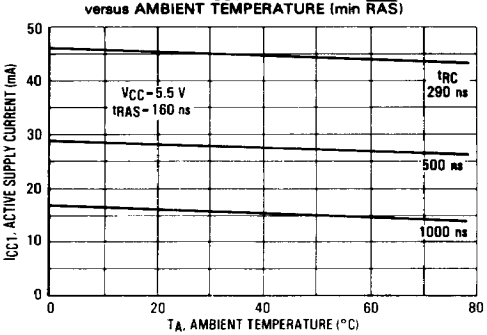
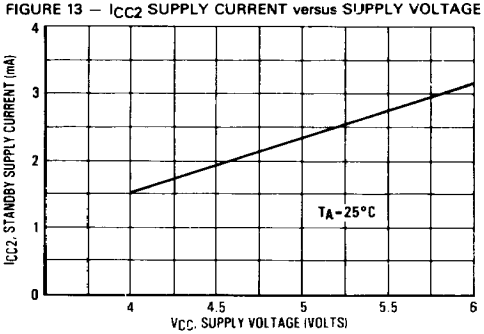


FIGURE 13 — I_{CC2} SUPPLY CURRENT versus SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 14 – I_{CC2} STANDBY CURRENT versus AMBIENT TEMPERATURE

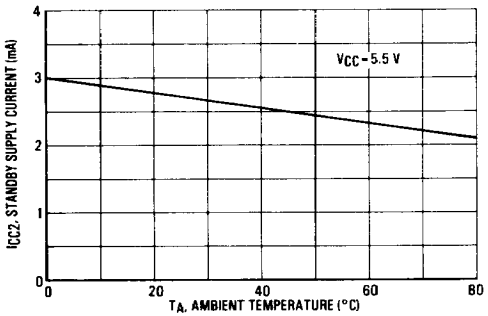


FIGURE 15 – I_{CC3} SUPPLY CURRENT versus CYCLE RATE

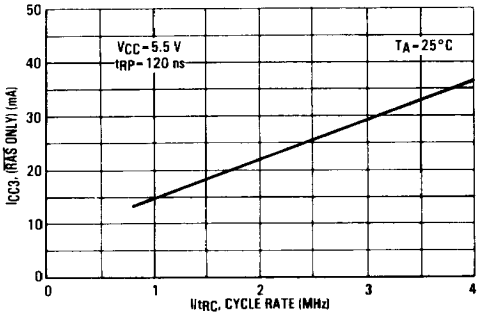


FIGURE 16 – ADDRESS INPUT LEVEL versus SUPPLY VOLTAGE

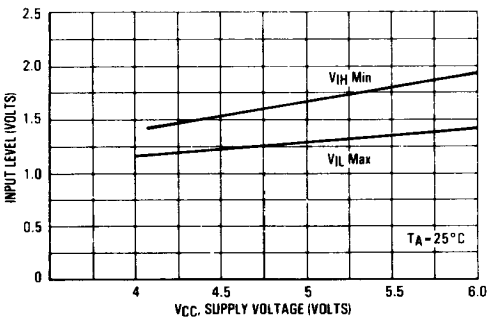
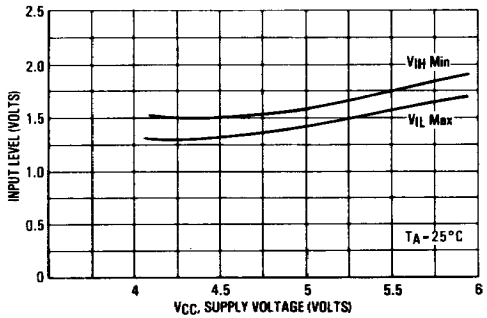


FIGURE 17 – DATA INPUT LEVEL versus SUPPLY VOLTAGE



SOFT ERROR TESTING

The storage cell depletion regions as well as the sense amplifier and its associated bit lines are susceptible to charge collection of electrons from an alpha "hit." However, the susceptibility of these vulnerable regions varies. Depleted storage cells are vulnerable at all times, whereas the sense amplifiers and associated bit lines are susceptible only during the small portion of the memory cycle just prior to sensing. Hence, an increase in the frequency of dynamic RAM access will cause a corresponding increase in the soft error rate.

To take this memory access dependency into account, the total soft error rate profile includes a cycle time component. The soft error rate due to bit line hits at the system's memory cycle rate is added to the soft error rate due to storage cell hits which are not frequency dependent. Figure 18 illustrates the impact that frequency of access has on the MCM6664A/MCM6665A overall soft error rate.

Under normal operating conditions, the die will be exposed to radiation levels of less than 0.01 alpha/cm^2/hr. Accelerated soft error testing data is generated from at least three high-intensity sources having an Alpha Flux Density range of 1×10^5 to 6×10^5 (alpha/cm^{2}hr) placed over uncoated die. Figure 19 shows the soft error rate for a given alpha flux density at a cycle rate of 100 kHz. The accelerated data of Figures 18 and 19 project that the soft error rate for package level radiation will be less than 0.1%/1000 hours.

SYSTEM LIFE OPERATING TEST CONDITIONS

1) Cycle time: 1 microsecond for read, write and refresh cycles
2) Refresh Rate: 1 millisecond
3) Voltage: 5.0 V
4) Temperature: 30° C ±2° C (ambient temperature inside enclosure)
5) Elevation: Approximately 620 feet above mean sea level
6) Data Patterns: Write the entire memory space sequentially with all "1"s and then perform continuous sequential reads for 6 hours. Next, write the entire memory space with all "0"s sequentially and then perform continuous sequential reads for 6 hours. Next, go back to the all "1"s pattern and repeat the sequences all over again.

FIGURE 18 — ACCELERATED SOFT ERROR versus CYCLE TIME

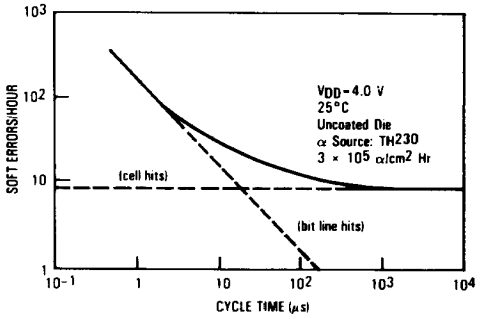
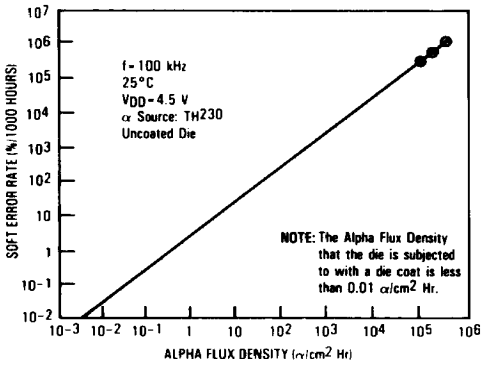


FIGURE 19 — SOFT ERROR RATE versus ALPHA FLUX DENSITY



CURRENT WAVEFORMS

FIGURE 20 — $\overline{RAS}/\overline{CAS}$ CYCLE

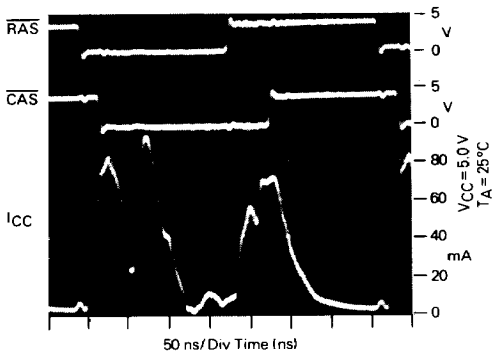


FIGURE 21 — LONG $\overline{RAS}/\overline{CAS}$ CYCLE

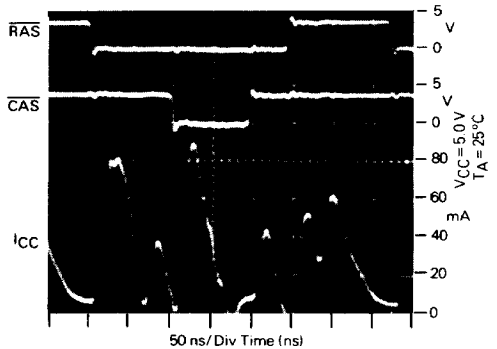


FIGURE 22 — $\overline{RAS}$ ONLY CYCLE

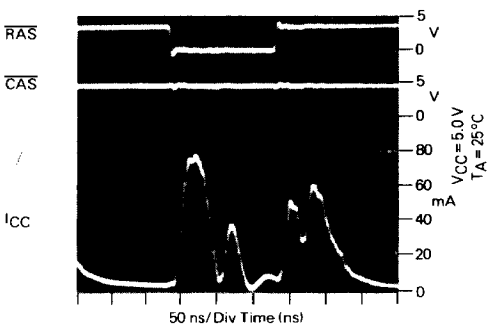


FIGURE 23 — PAGE MODE CYCLE

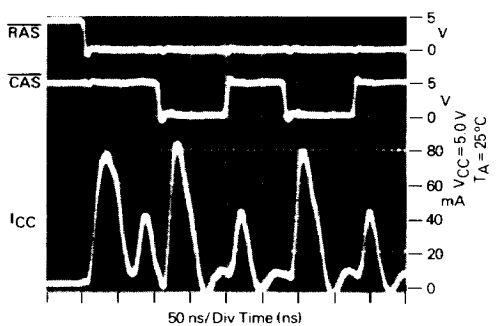
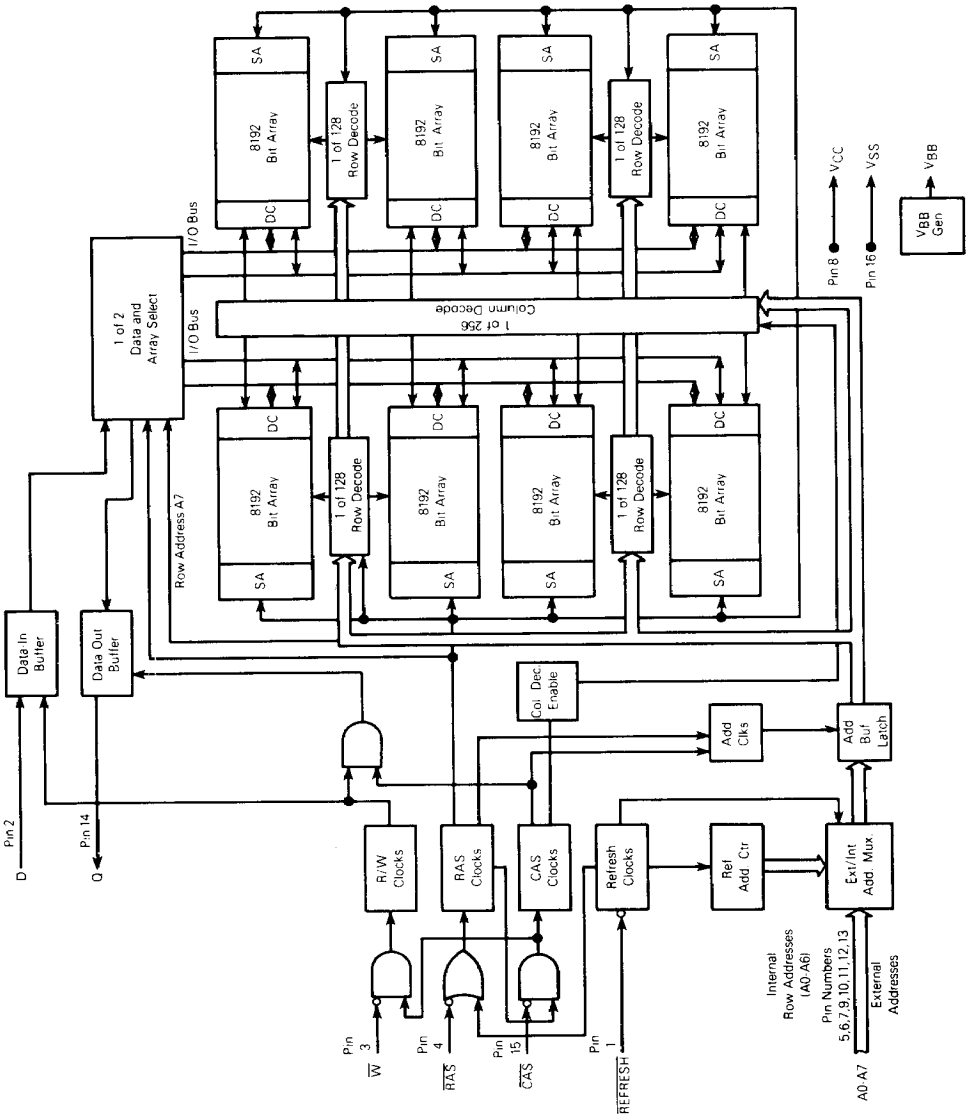


FIGURE 24 — FUNCTIONAL BLOCK DIAGRAM



DEVICE INITIALIZATION

Since the 64K dynamic RAM is a single supply 5 V only device, the need for power supply sequencing is no longer required as was the case in older generation dynamic RAMs. On power-up an initial pause of 100 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 2 ms with device powered up) the wake up sequence (8 active cycles) will be necessary to assure proper device operation. See Figures 25 and 26 for power on characteristics of the RAM for two conditions (clocks active, clocks inactive).

The row address strobe is the primary "clock" that activates the device and maintains the data when the RAM is in the standby mode. This is the main feature that distinguishes it as a dynamic RAM as opposed to a static RAM. A dynamic RAM is placed in a low power standby mode when the device receives a positive-going row address strobe. The variation in the power dissipation of a dynamic RAM from the active to the standby state is an order of magnitude or more for NMOS devices. This feature is used to its fullest advantage with high density mainframe memory systems, where only a very small percentage of the devices are in the active mode at any one time and the rest of the devices are in the standby mode. Thus, large memory systems can be assembled that dissipate very low power per bit compared to a system where all devices are active continuously.

ADDRESSING THE RAM

The eight address pins on the device are time multiplexed with two separate 8-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe and the column address strobe. A total of sixteen address bits will decode one of the 65,536 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 64K RAM, one is called the page mode cycle (described later) where an 8-bit column address field is presented on the input pins and latched by the $\overline{CAS}$ clock; and the other is the $\overline{RAS}$ only refresh cycle (described later) where a 7-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. In the latter case, the most significant bit on Row Address A7 (pin 9) is not required for refresh. See bit address map for the topology of the cells and their address selection.

NORMAL READ CYCLE

A read cycle is referred to as normal read cycle to differentiate if from a page-mode-read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at

CURRENT WAVEFORMS

FIGURE 25 — SUPPLY CURRENT versus SUPPLY VOLTAGE DURING POWER UP, $\overline{RAS}$, $\overline{CAS}$ = V_{CC}

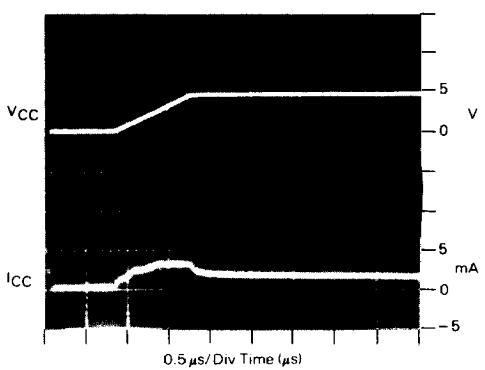
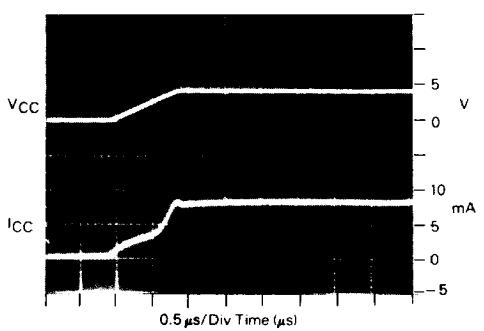


FIGURE 26 — SUPPLY CURRENT versus SUPPLY VOLTAGE DURING POWER UP, $\overline{RAS}$, $\overline{CAS}$ = V_{SS}



the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available, as noted in the functional block diagram, Figure 24. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. The $\overline{CAS}$ clock can remain active for a maximum of 10 ns (t_{CRP}) into the next cycle. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as a early write cycle. In an early write cycle, the write clock and the data in is referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CAS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write (W) clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds – ($t_{RWL} + t_{RP} + 2T_t$).

At the start of a write cycle, the data out is in a three-state condition and remains inactive throughout the cycle. The data out remains three-state because of the active transition of the write ($\overline{W}$) clock prevents the $\overline{CAS}$ clock from enabling the data-out buffers as noted in Functional Block Diagram. The three-state condition (high impedence) of the Data Out Pin during a write cycle can be effectively utilized in systems that have a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYLES

As the name implies, both a read and a write cycle is accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, the following parameters (t_{RWD}, t_{CWD}) play an important role. A read-while-write cycle starts as a normal read cycle with the write ($\overline{W}$) clock being asserted at minimum t_{RWD} or minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out occurs. The minimum specification on t_{RWD} and t_{CWD} assure that data out does occur. In this case, the data in is set up with respect to write ($\overline{W}$) clock active edge.

PAGE-MODE CYCLES

Page mode operation allows faster successive data operations at the 256 column locations. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 64K dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 8-bit column address field. There are two controlling factors that limit the access to all 256 column locations in one $\overline{RAS}$ clock active operation. These are the refresh interval of the device (2 ms/128 = 15.6 microseconds) and the maximum active time specification for the $\overline{RAS}$ clock (10 microseconds). Since 10 microseconds is the smaller value, the maximum specification of the $\overline{RAS}$ clock on time is the limiting factor of the number of sequential page accesses possible. Ten microseconds will provide approximately 50 successive page accesses (10 microseconds ÷ page mode cycle time) for each row address selected before the $\overline{RAS}$ clock is reset.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In addition to read and write cycles, a read-modify-write cycle can also be performed in a page mode operation. For a read-modify-write or read-while-write type cycle, the conditions normal to that mode of operation will apply in the page mode also. The page mode cycle illustrated show a series of sequential reads separated by a series of sequential writes. This is just one mode of operation. In practice, any combination of read, write and read-modify-write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to

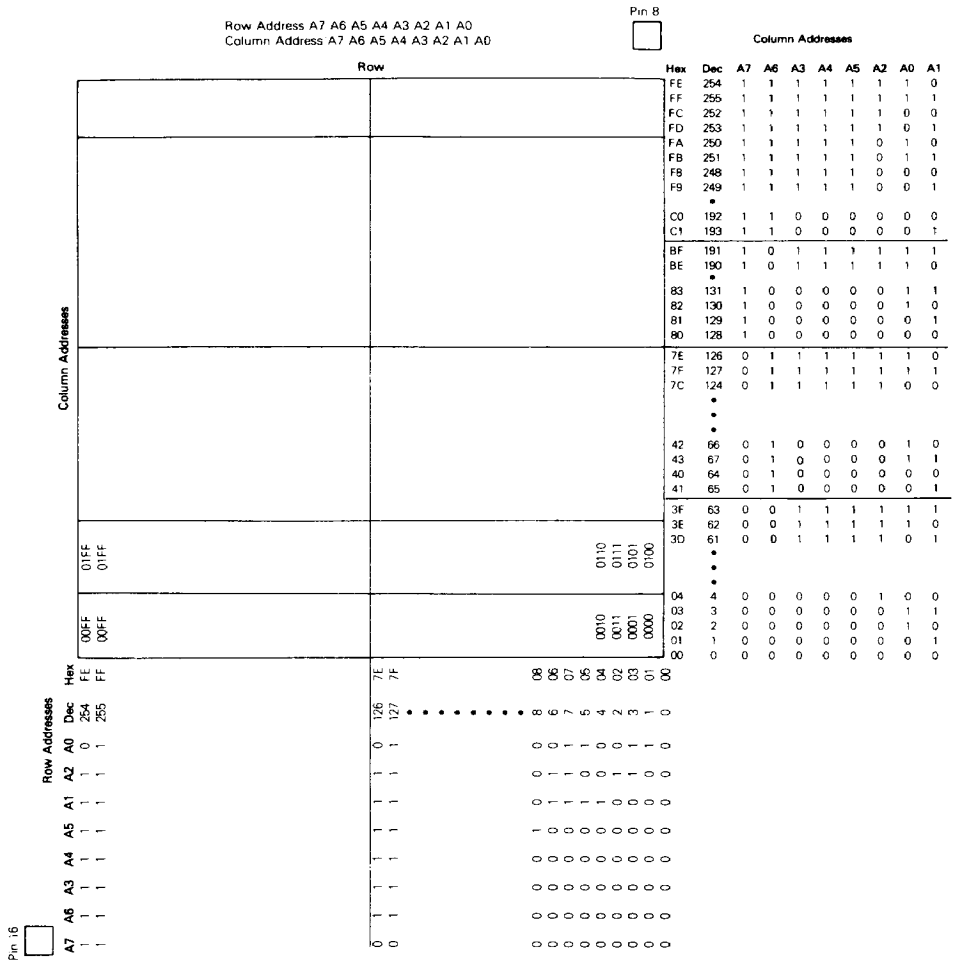
degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 2 ms. This is accomplished by sequentially cycling through the 128 row address locations every 2 ms, or at least one row every 15.6 microseconds. A normal read or write operation to the RAM will serve to refresh all the bits (256) associated with that particular row decoded.

$\overline{\text{RAS}}$ Only Refresh – When the memory component is in standby the $\overline{\text{RAS}}$ only refresh scheme is employed. This refresh method performs a $\overline{\text{RAS}}$ only cycle on all 128 row addresses every 2 ms. The row addresses are latched in with the $\overline{\text{RAS}}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{\text{CAS}}$ clock is not required and should be inactive or at a V_{IH} level to conserve power.

Auto Refresh Mode and Self Refresh mode (MCM6664A only) – With the MCM6664A, two additional refresh methods are available to the user. These special functions are incorporated on pin 1 of the device and have been approved by JEDEC as an alternative function for that pin on the 64K dynamic memory. The auto refresh mode is accomplished by asserting pin 1 active (V_{IL} level) during the time interval when there are no memory cycles. In the auto refresh mode, the $\overline{\text{REFRESH}}$ active pulse (t_{FP}) must be limited to 2 microseconds or less. The 2 microsecond time is specified to prevent the device from transitioning into the self refresh mode. Auto refresh can be performed in a distributed mode (refresh cycle every 15.6 microseconds) and in a burst mode where all 128 refresh cycles are done one after the other until complete. An onboard address counter generates the internal row address to refresh a particular row and increments itself at the end of each cycle.

Another variation of refresh is the self refresh mode. This mode is similar to the auto refresh method except that the active pulse width (t_{FBP}) must be greater than 2 microseconds or held down active indefinitely. With pin 1 in the self refresh mode, an internal row address is generated by the internal refresh counter approximately every 15.6 microseconds. This mode of refresh is used for systems requiring battery back-up, and saves additional system power by not requiring an external refresh address counter and address buffers. The power dissipation for either $\overline{\text{REFRESH}}$ mode is the same.

MCM6664A BIT ADDRESS MAP



Hex	Dec	A7	A6	A5	A4	A3	A2	A1	A0
FE	254	1	1	1	1	1	1	1	0
FF	255	1	1	1	1	1	1	1	1
FC	252	1	1	1	1	1	1	0	0
FD	253	1	1	1	1	1	1	0	1
FA	250	1	1	1	1	1	0	1	0
FB	251	1	1	1	1	1	0	1	1
F8	248	1	1	1	1	1	0	0	0
F9	249	1	1	1	1	1	0	0	1
•									
C0	192	1	1	0	0	0	0	0	0
C1	193	1	1	0	0	0	0	0	1
BF	191	1	0	1	1	1	1	1	1
BE	190	1	0	1	1	1	1	1	0
•									
83	131	1	0	0	0	0	0	1	1
82	130	1	0	0	0	0	0	1	0
81	129	1	0	0	0	0	0	0	1
80	128	1	0	0	0	0	0	0	0
7E	126	0	1	1	1	1	1	1	0
7F	127	0	1	1	1	1	1	1	1
7C	124	0	1	1	1	1	1	0	0
•									
•									
•									
42	66	0	1	0	0	0	0	1	0
43	67	0	1	0	0	0	0	1	1
40	64	0	1	0	0	0	0	0	0
41	65	0	1	0	0	0	0	0	1
3F	63	0	0	1	1	1	1	1	1
3E	62	0	0	1	1	1	1	1	0
3D	61	0	0	1	1	1	1	0	1
•									
•									
•									
04	4	0	0	0	0	0	0	1	0
03	3	0	0	0	0	0	0	1	1
02	2	0	0	0	0	0	0	1	0
01	1	0	0	0	0	0	0	0	1
00	0	0	0	0	0	0	0	0	0

Data Stored = $D_{in} \oplus A_{0X} \oplus A_{1Y}$

Column Address A1	Row Address A0	Data Stored
0	0	True
0	1	Inverted
1	0	Inverted
1	1	True