

# DRAM

# 64K x 1 DRAM

## PAGE MODE

DRAM

### FEATURES

- Industry standard pinout, functions and timing
- Single +5V ±10% power supply
- Low power, 15mW standby; 75mW active, typical
- Common I/O using EARLY-WRITE
- Q held indefinitely by  $\overline{\text{CAS}}$
- 256-cycle refresh in 4ms
- Fully compatible with MT1259 (256K)
- Optional PAGE MODE access cycle

### OPTIONS

- Timing
  - 100ns access
  - 120ns access
  - 150ns access
  - 200ns access
- Packages
  - Plastic DIP
  - Ceramic DIP

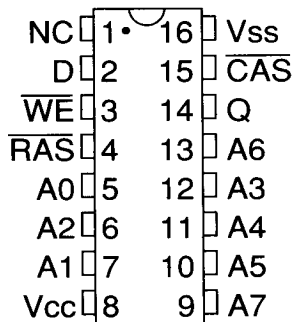
### MARKING

- 10
- 12
- 15
- 20

None  
C

### PIN ASSIGNMENT (Top View)

16-Pin DIP  
(A-1, B-1)



### GENERAL DESCRIPTION

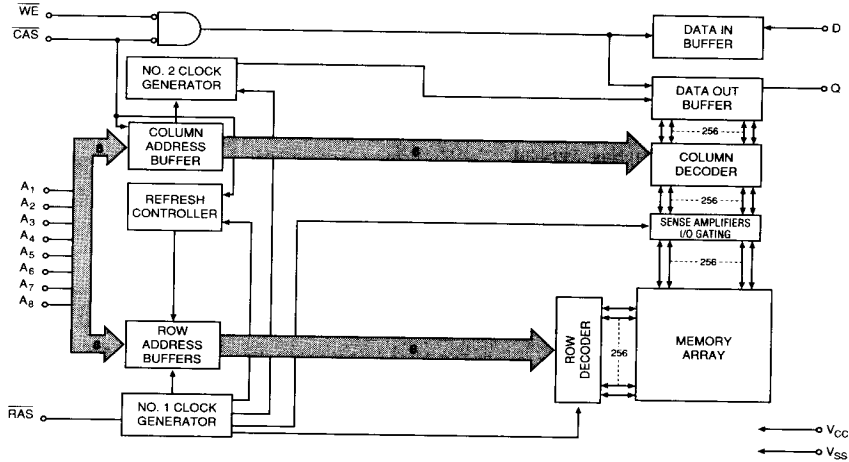
The MT4264 is a randomly accessed solid-state memory containing 65,536 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 16 address bits, which are entered 8 bits (A0-A7) at a time.  $\overline{\text{RAS}}$  is used to latch the first 8 bits and  $\overline{\text{CAS}}$  the latter 8 bits. A READ or WRITE cycle is selected with the  $\overline{\text{WE}}$  input. A logic HIGH on  $\overline{\text{WE}}$  dictates READ mode while a logic LOW on  $\overline{\text{WE}}$  dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever occurs last. If  $\overline{\text{WE}}$  goes LOW prior to  $\overline{\text{CAS}}$  going LOW, the output pin(s) remain open (High-Z) until the next  $\overline{\text{CAS}}$  cycle. If  $\overline{\text{WE}}$  goes LOW after data reaches the output pin(s), data out (Q) is activated and retains the selected cell data as long as  $\overline{\text{CAS}}$  remains LOW (regardless of  $\overline{\text{WE}}$  or  $\overline{\text{RAS}}$ ). This late  $\overline{\text{WE}}$  pulse results in a READ-WRITE cycle.

PAGE MODE operations allow faster data operations

(READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A7) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed-in by  $\overline{\text{RAS}}$  followed by a column address strobed-in by  $\overline{\text{CAS}}$ .  $\overline{\text{CAS}}$  may be toggled-in by holding  $\overline{\text{RAS}}$  LOW and strobing in different column addresses, thus executing faster memory cycles. Returning  $\overline{\text{RAS}}$  HIGH terminates the PAGE MODE operation.

Returning  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the  $\overline{\text{RAS}}$  HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any  $\overline{\text{RAS}}$  cycle (READ, WRITE,  $\overline{\text{RAS}}$ -ONLY or HIDDEN REFRESH) so that all 256 combinations of  $\overline{\text{RAS}}$  addresses (A0-A7) are executed at least every 4ms, regardless of sequence.

**FUNCTIONAL BLOCK DIAGRAM  
PAGE MODE**



**TRUTH TABLE**

Function	RAS	CAS	WE	Addresses		
				'R	'C	
Standby	H	X	X	X	X	High Impedance
READ	L	L	H	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In
PAGE-MODE READ	L	H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out
PAGE-MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In
RAS-ONLY REFRESH	L	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out
CAS-BEFORE- RAS REFRESH	H→L	L	X	X	X	High Impedance

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc supply relative to Vss ..... -1.0V to +7.0V  
 Operating Temperature, TA(Ambient) ..... 0°C to +70°C  
 Storage Temperature (Ceramic) ..... -65°C to +150°C  
 Storage Temperature (Plastic) ..... -55°C to +150°C  
 Power Dissipation ..... 1W  
 Short Circuit Output Current ..... 50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

(Notes: 1, 2, 3, 4, 6) (0°C ≤ T<sub>A</sub> ≤ 70°C; V<sub>cc</sub> = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V <sub>cc</sub>	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V <sub>IH</sub>	2.4	V <sub>cc</sub> +1	V	1
Input Low (Logic 0) Voltage, All Inputs	V <sub>IL</sub>	-1.0	0.8	V	1
<b>INPUT LEAKAGE</b> Input leakage current, any input (0V ≤ V <sub>IN</sub> ≤ V <sub>cc</sub> ); I all other pins not under test = 0V	I <sub>I</sub>	-10	10	μA	
<b>OUTPUT LEAKAGE</b> Output leakage current (Q is disabled; 0V ≤ V <sub>OUT</sub> ≤ V <sub>cc</sub> )	I <sub>OZ</sub>	-10	10	μA	
<b>OUTPUT LEVELS</b> Output High (Logic 1) Voltage (I <sub>OUT</sub> = -5mA) Output Low (Logic 0) Voltage (I <sub>OUT</sub> = 5mA)	V <sub>OH</sub> V <sub>OL</sub>	2.4	0.4	V V	1

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
<b>STANDBY CURRENT</b> (R <sub>AS</sub> = C <sub>AS</sub> = V <sub>IH</sub> after 8 R <sub>AS</sub> cycles)	I <sub>cc1</sub>		4	mA	
<b>OPERATING CURRENT</b> (R <sub>AS</sub> and C <sub>AS</sub> Cycling)	I <sub>cc2</sub>		30	mA	2
<b>R<sub>AS</sub>-ONLY REFRESH CURRENT</b> (C <sub>AS</sub> = V <sub>IH</sub> )	I <sub>cc3</sub>		20	mA	2
<b>PAGE MODE CURRENT</b> (R <sub>AS</sub> = V <sub>IL</sub> ; C <sub>AS</sub> = Cycling)	I <sub>cc4</sub>		30	mA	2

**CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A7, D	C <sub>I1</sub>		5	pF	18
Input Capacitance: R <sub>AS</sub> , C <sub>AS</sub> , WE	C <sub>I2</sub>		8	pF	18
Output Capacitance: Q	C <sub>O</sub>		8	pF	18

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

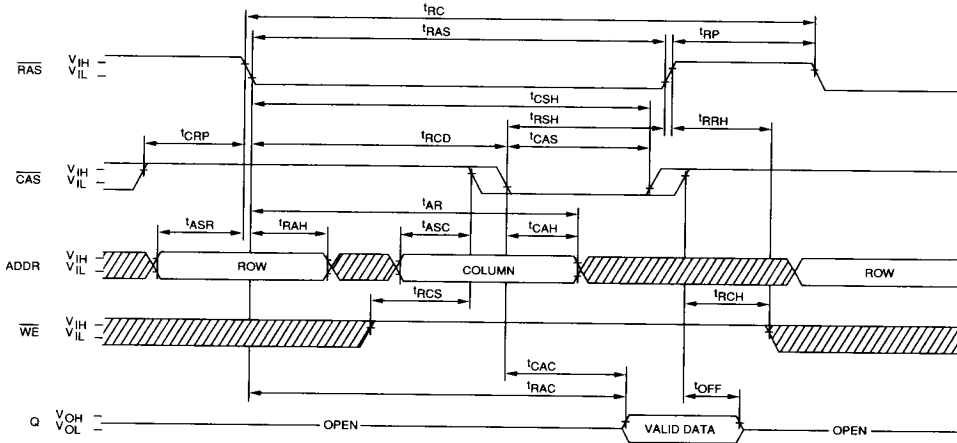
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T<sub>A</sub> ≤ 70°C; V<sub>cc</sub> = 5.0V ±10%)

A.C. CHARACTERISTICS		-10		-12		-15		-20		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Random READ or WRITE cycle time	<sup>1</sup> RC	195		230		260		330		ns	6, 7
READ-MODIFY-WRITE cycle time	<sup>1</sup> RWC	220		255		295		370		ns	
PAGE-MODE cycle time	<sup>1</sup> PC	90		100		120		170		ns	6, 7
Access time from RAS	<sup>1</sup> RAC		100		120		150		200	ns	7, 8
Access time from CAS	<sup>1</sup> CAC		50		60		75		120	ns	7, 9
RAS pulse width	<sup>1</sup> RAS	100	10,000	120	10,000	150	10,000	200	10,000	ns	
RAS hold time	<sup>1</sup> RSH	50		60		75		100		ns	
RAS precharge time	<sup>1</sup> RP	80	20,000	90	20,000	100	20,000	120	20,000	ns	
CAS pulse width	<sup>1</sup> CAS	50	10,000	60	10,000	75	10,000	120	10,000	ns	
CAS hold time	<sup>1</sup> CSH	100		120		150		200		ns	
CAS precharge time	<sup>1</sup> CPN	25		25		30		35		ns	19
CAS precharge time (PAGE MODE)	<sup>1</sup> CP	30		30		35		40		ns	
RAS to CAS delay time	<sup>1</sup> RCD	25	50	25	60	25	75	30	80	ns	13
Row address setup time	<sup>1</sup> ASR	0		0		0		0		ns	
Row address hold time	<sup>1</sup> RAH	15		15		20		25		ns	
Column address setup time	<sup>1</sup> ASC	0		0		0		0		ns	
Column address hold time	<sup>1</sup> CAH	20		20		25		50		ns	
Column address hold time referenced to RAS	<sup>1</sup> AR	70		80		100		130		ns	
READ command setup time	<sup>1</sup> RCS	0		0		0		0		ns	
READ command hold time referenced to CAS	<sup>1</sup> RCH	0		0		0		0		ns	14
READ command hold time referenced to RAS	<sup>1</sup> RRH	0		0		0		0		ns	
Output buffer turn-off delay	<sup>1</sup> OFF	0	30	0	30	0	35	0	40	ns	12
WE command setup time	<sup>1</sup> WCS	0		0		0		0		ns	16
WRITE command hold time	<sup>1</sup> WCH	35		40		45		60		ns	
WRITE command hold time referenced to RAS	<sup>1</sup> WCR	85		100		120		140		ns	
WRITE command pulse width	<sup>1</sup> WP	35		40		45		50		ns	
WRITE command to RAS lead time	<sup>1</sup> RWL	35		40		45		55		ns	
WRITE command to CAS lead time	<sup>1</sup> CWL	35		40		45		55		ns	
Data-in setup time	<sup>1</sup> DS	0		0		0		0		ns	15
Data-in hold time	<sup>1</sup> DH	35		40		45		55		ns	15
Data-in hold time referenced to RAS	<sup>1</sup> DHR	85		100		120		135		ns	
CAS to WE delay	<sup>1</sup> CWD	40		50		60		100		ns	16
RAS to WE delay	<sup>1</sup> RWD	90		110		135		180		ns	16
Transition time (rise or fall)	<sup>1</sup> T	3	100	3	100	3	100	3	100	ns	5, 17
Refresh period (256 cycles)	<sup>1</sup> REF		4		4		4		4	ms	
CAS to RAS setup time	<sup>1</sup> CRP	10		15		20		20		ns	

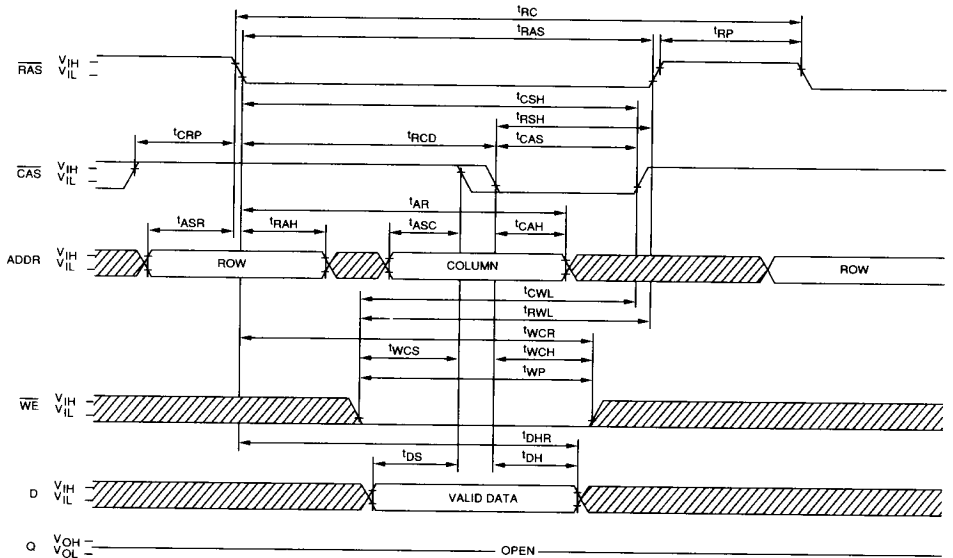
**NOTES**



1. All voltages referenced to Vss.
2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
4. AC characteristics assume tT = 5ns.
5. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ TA ≤ 70°C) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that tRCD < tRCD (MAX). If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
9. Assumes that tRCD ≥ tRCD (MAX).
10. If CAS = VIH, data output is high impedance.
11. If CAS = VIL, data output may contain data from the last valid READ cycle.
12. tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
13. Operation within the tRCD (MAX) limit ensures that tRAC (MAX) can be met. tRCD (MAX) is specified as a reference point only; if tRCD is greater than the specified tRCD (MAX) limit, then access time is controlled exclusively by tCAC.
14. tRCH is referenced to the first rising edge of RAS or CAS.
15. These parameters are referenced to CAS leading edge in early WRITE cycles and WE leading edge in late WRITE or READ-WRITE cycles.
16. tWCS, tRWD and tCWD are restrictive operating parameters in late READ-WRITE and READ-MODIFY-WRITE cycles only. If tWCS ≥ tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If tCWD ≥ tCWD (MIN) and tRWD ≥ tRWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of Q (at access time and until CAS goes back to VIH) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
18. This parameter is sampled. Capacitance is calculated from the equation C = I dt/dv with dv = 3V and VCC = 5V.
19. If CAS is LOW at the falling edge of RAS, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for tCPN.

READ CYCLE

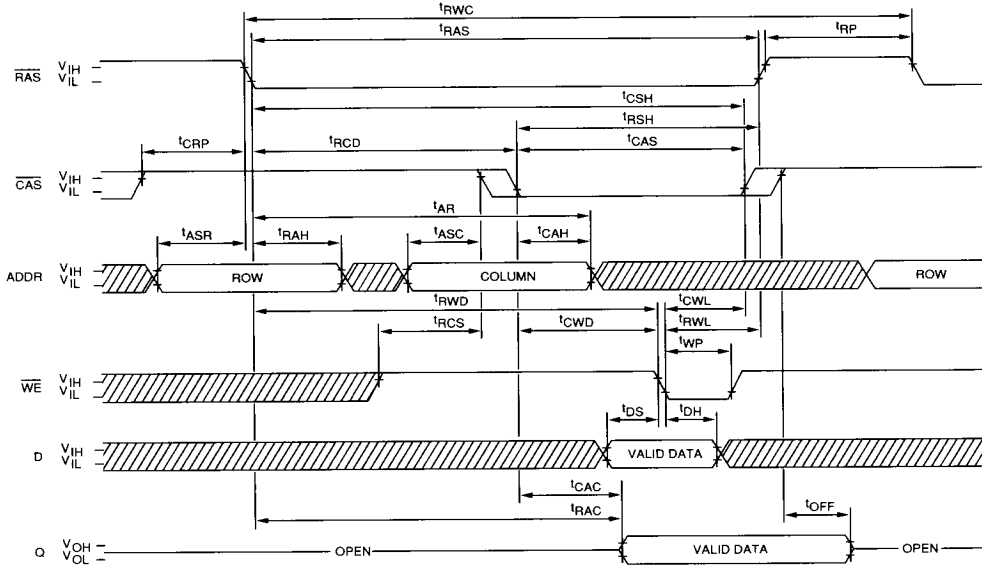


EARLY-WRITE CYCLE

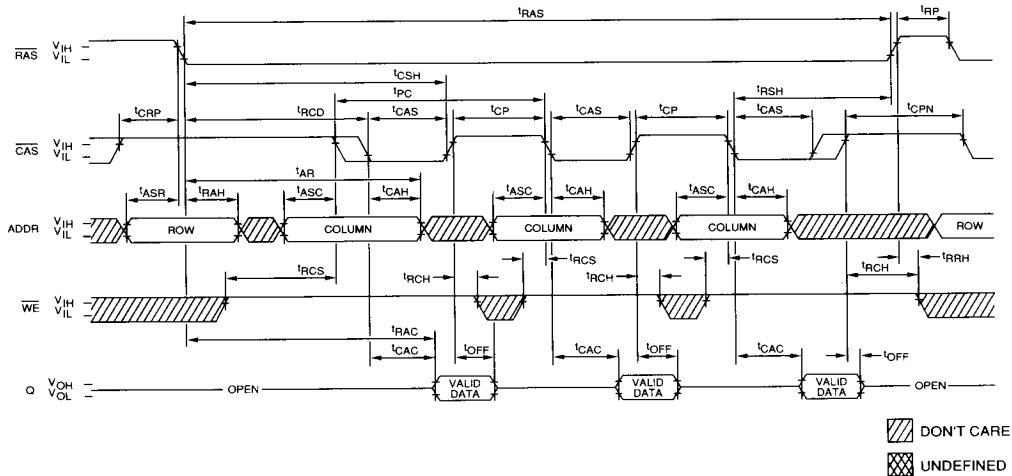


 DON'T CARE  
 UNDEFINED

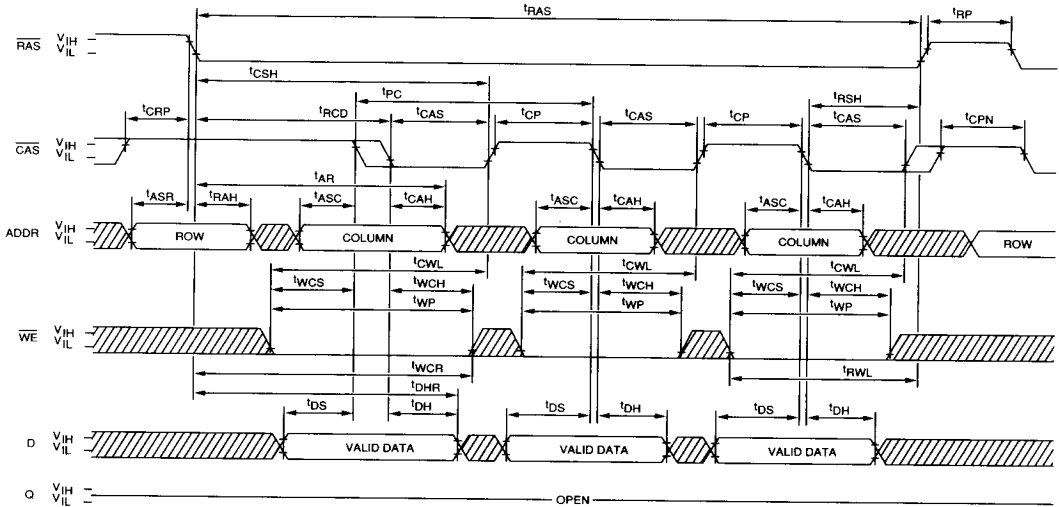
**READ-WRITE CYCLE**  
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



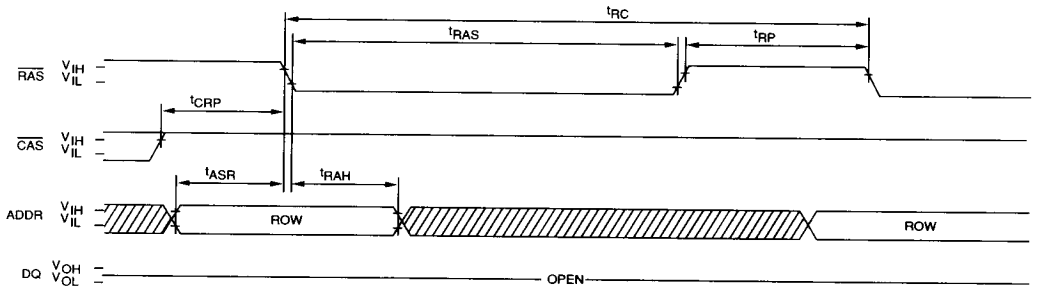
**PAGE-MODE READ CYCLE**




PAGE-MODE EARLY-WRITE CYCLE



RAS-ONLY REFRESH CYCLE  
(ADDR = A<sub>0</sub> - A<sub>7</sub>)



 DON'T CARE  
 UNDEFINED