

MOTHERBOARD PARTS LIST

R1 - R8	22K	1/4 Watt Resistors
R9, R17, R19	5.6K	1/4 Watt Resistors
R10	1K	1/4 Watt Resistors
R11, R14, R15, R18	3.3K	1/4 Watt Resistors
R12	270 Ohms	1/4 Watt Resistors
R13, R16	100 Ohms	1/2 Watt Resistors
R20	100 Ohms	1 Watt Resistor
C1 - C3	22 MFD	15V Dipped Tantalum Capacitors
C4, C5	10 PFD	Dipped Mica Capacitors
C7, C8, C9,	.1 ceramic UK16-104 CRL	
C6	0.47 MFD	Paper Capacitor
	280 AE/A470K	Philips or equivalent
XTAL	2 MHz	Crystal (Wire Leads, HC6/U casing)
Q1	2N4402	PNP Silicon
D1	1N914	Silicon Diode
3850	F8-CPU	3850 PC Fairchild
3853	F8-SMI	3853 PC Fairchild

4050	C-MOS Buffer	4050 PC Fairchild or similar
40097	C-MOS Buffer	40097 PC Fairchild or similar
4023	C-MOS Gates	4023 PC Fairchild or similar
4001	C-MOS Gates	4001 PC Fairchild or similar
CARD SOCKETS		00-6022-044-981-028 ELCO or similar
J1, J2		These jumpers must be installed for proper operation of the 3853 SMI. When removed, they will allow a 3852 DMI to be substituted in place of the 3853 SMI for interfacing to dynamic RAM's.

MOTHERBOARD CONNECTOR

Along one edge of the motherboard is a 44 pin card edge, which allows access to PORT 00 and PORT 01 (which are located in the 3850 CPU chip) as well as the various control and interface lines.

COMPONENT SIDEFOIL SIDE

1	GND	A	GND
2	+5V	B	+5V
3	+12V	C	+12V
4	-5V (optional)	D	-5V (optional)
5		E	
6	EXT. INT.	F	EXT. INT. GND.
7		H	
8	EXT. RESET	J	EXT. RESET GND.
9		K	
10	I/O 00	L	I/O 10
11	I/O 01	M	I/O 11
12	I/O 02	N	I/O 12
13	I/O 03	P	I/O 13
14	I/O 04	R	I/O 14
15	I/O 05	S	I/O 15
16	I/O 06	T	I/O 16
17	I/O 07	U	I/O 17
18		V	
19		W	
20	FAIRBUG SWITCH	X	FAIRBUG SWITCH
21	PRINTER RTN.	Y	KEYBOARD RTN.
22	KEYBOARD	Z	PRINTER

A momentary pushbutton, normally open, is connected between pins 8 and J. Closing of this switch actuates the EXTERNAL RESET mechanism of the CPU.

A single pole, single throw, toggle switch is connected between pins 20 and X. Closure of these controls will allow the EXTERNAL RESET to cause entry to FAIRBUG (8080). If this switch is "open", the EXTERNAL RESET will operate normally (reset to 0000).

NOTE: In some cases a heavy noise environment can cause spontaneous actuation of the external RESET. If this occurs a small capacitor (.01 MFD) wired between pins 8 and J (EXTERNAL RESET PAIR) should correct this problem.

CONNECTING A TELETYPE MODEL 33

The CPU-8 system can easily interface with a Teletype Model 33 teleprinter. The teletype interface of the microcomputer provides signals for a 20 mA full duplex loop.

The recommended teletype is a Teletype Model 33 ASR, with automatic reader on/off control. Other Model 33 Teleprinters can also be used.

Teletype Strapping Options

No modifications of the teletype are necessary. Strapping options should be selected to provide 20 mA loops, and to provide full duplex operation in place of half duplex operation. The options are described in the following paragraphs:

1. **Parts Location:** All option points are on the teletype power supply assembly. The power supply assembly is rightmost in the teletype; prominent are the LINE/OFF/LOCAL switch in the front of it, and a row of three fuse holders in the rear. Changes are made on a ten terminal strip (part #151411) that is at the lower rear of the power supply assembly. The other change is made on a large flat multi-tap power resistor (part #181816) that is about three inches behind the LINE/OFF/LOCAL switch.
2. Select 20 mA loop currents by performing Note 2 of the TTY Drawing Number 6353WD which states: "For the .020 amp, neutral signal line, move the purple wire from Terminal 8 to Terminal 9 of the 151411 terminal strip. Also move the blue wire from Terminal 3 of the power resistor 181816 to Terminal 4."

3. Select full duplex operation by performing Note 3 of TTY Drawing Number 6353WD which states: "Move the white-blue wire from Terminal 4 to 5 and the brown-yellow wire from Terminal 3 to 5 on the 151411 terminal strip."

Caution: The 110V cord terminates on the terminal strip. Unplug power cord from the AC source before working on the teletype.

Teletype Model 33 machines provide two alternative places for attaching an interface cable. One location is the 10 terminal strip that is at the rear of the power supply assembly (the same place as where the option changes were made). The optional location is at the 15 pin connector #2, which is just above the terminal strip. One mating plug for connector is:

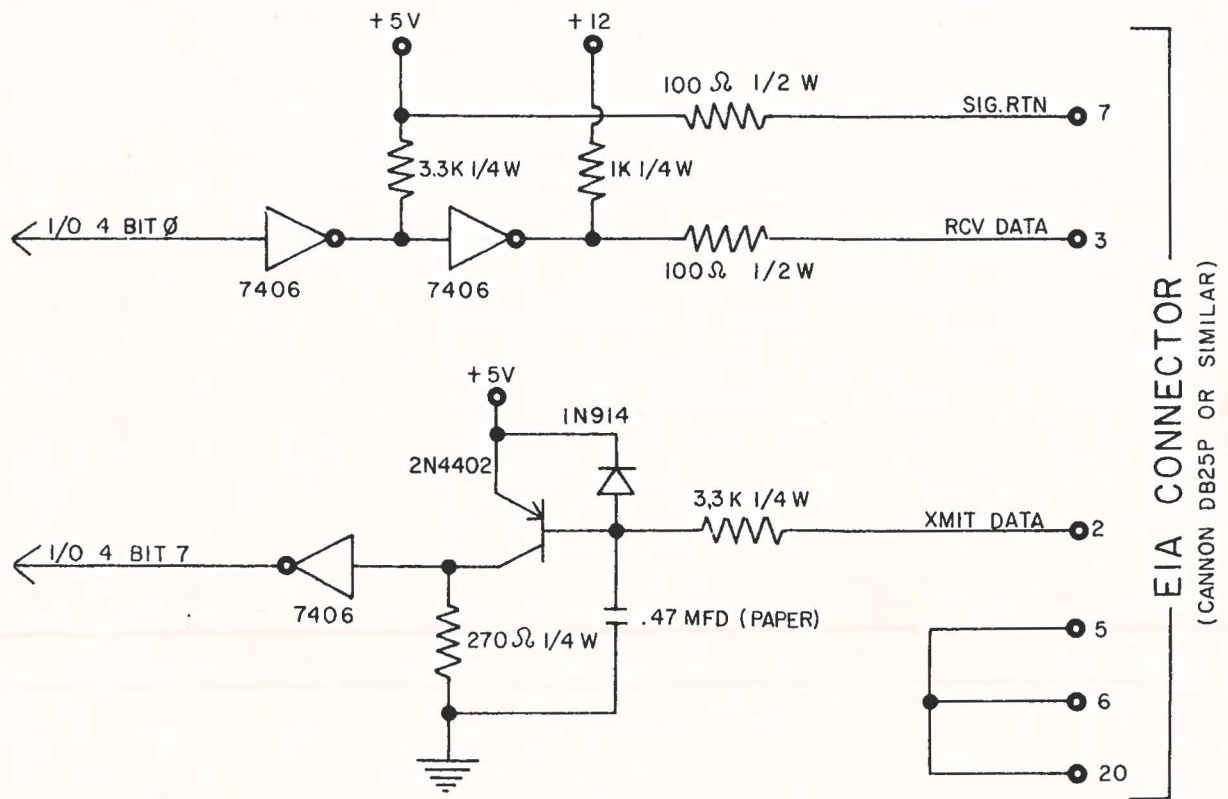
MOLEX Part # P(03-09-2151) housing  
with MOLEX Part # (02-09-2118) terminals

The connections between teletype and microcomputer are:

<u>Teletype</u>	<u>CPU-8</u>
TS-4 or J2-6	Keyboard
TS-3 or J2-5	Keyboard Return
TS-7 or J2-8	Printer
TS-6 or J2-7	Printer Return

### EIA Interface

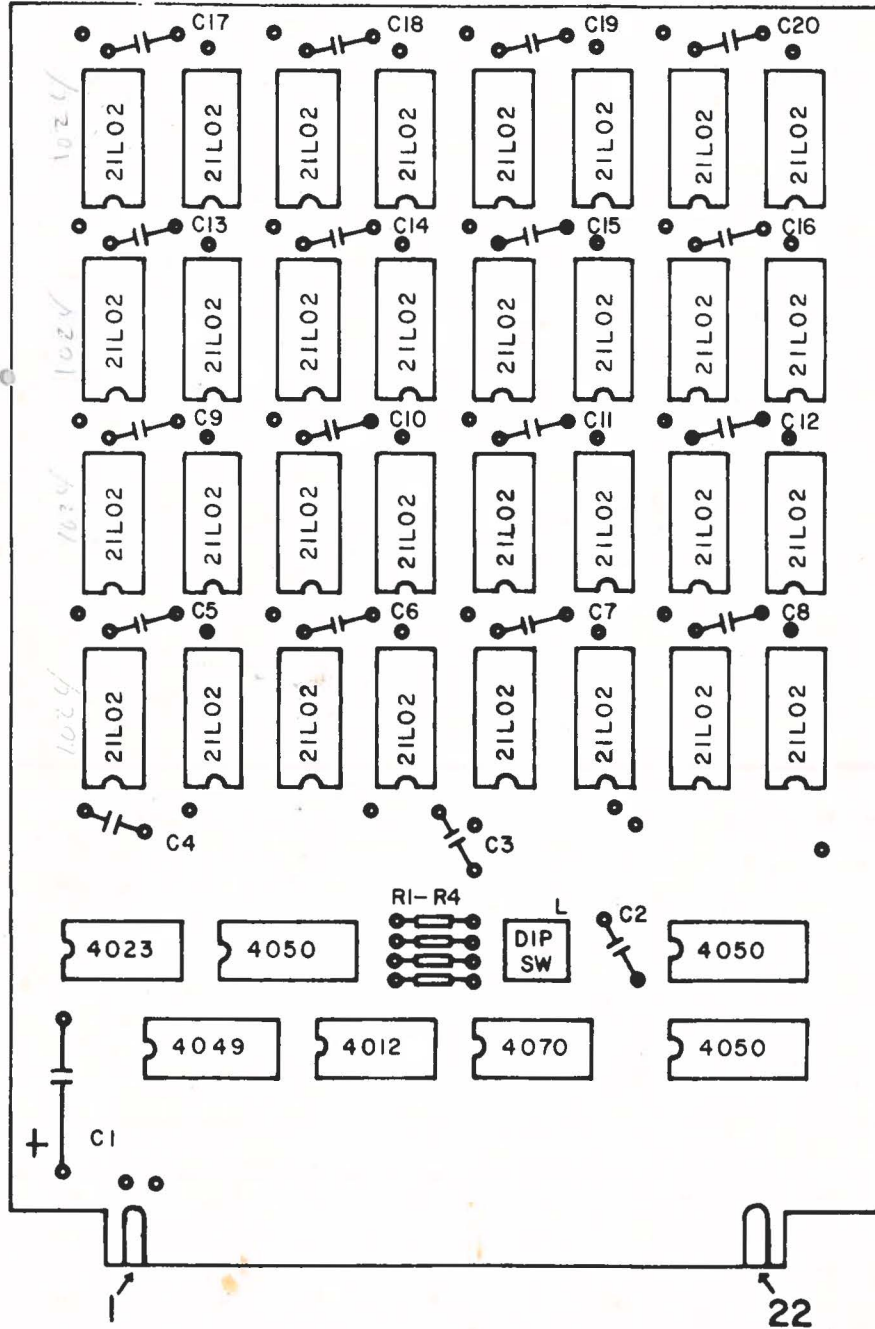
The following schematic shows an alternate TTY convertor circuit for interface with an EIA connector. Note that the terminal ground (SIG. RTN) is connected to the +5V line of the CPU-8.



EIA INTERFACE FOR CPU-8

# CPU SYSTEMS

## 4K STATIC RAM COMPONENT PLACEMENT





4K RAM PARTS LIST

R1 - R4	10K 1/4 W Resistors
C1	22 MFD 10V Tubular Tantalum Capacitor
C2 - C20	0.1 MFD Ceramic Capacitors UK16-104 CRL
DIP SW.	4 Position Dip Switch 76B04 Grayhill or similar
21L02	Memory Chips 21L02 Fairchild or similar
4023	C-MOS Gates 4023 PC Fairchild or similar
4070	C-MOS Gates 4070 PC Fairchild or similar
4049	C-MOS Buffers 4049 PC Fairchild or similar
4050	C-MOS Buffers 4050 PC Fairchild or similar

4K RAM CONNECTORCOMPONENT SIDEFOIL SIDE

1	+5V	A	+5V
2	GND	B	GND
3		C	
4	WRITE	D	
5	DI 0	E	DO 0
6	DI 1	F	DO 1
7	DI 2	H	DO 2
8	DI 3	J	DO 3
9	DI 4	K	DO 4
10	DI 5	L	DO 5
11	DI 6	M	DO 6
12	DI 7	N	DO 7
13		P	
14		R	
15	ADD 7	S	ADD 15
16	ADD 6	T	ADD 14
17	ADD 5	U	ADD 13
18	ADD 4	V	ADD 12
19	ADD 3	W	ADD 11
20	ADD 2	X	ADD 10
21	ADD 1	Y	ADD 9
22	ADD 0	Z	ADD 8

All input lines to the 4K RAM boards are fully BUFFERED and present only one or two C-MOS unit loads to the motherboard. If 4K RAM's are installed in all four possible memory slots, the CPU-8 will directly interface 16K of memory (128 21L02 chips) without further buffering. Because the drive lines on the motherboard are themselves buffered, the number of memory cards may be increased

## 4K Ram Connector (continued)

to as many as sixteen (with suitable power supply), allowing usage of the full memory interface capability of the processor (64K). If this is done, the 1K of memory located at 8000-83FF will overlap the FAIRBUG location. However, because the F8 essentially "turns off" the RAM locations when accessing a PSU location, no special operations are required to overcome this overlap. The 1K of RAM at this location is simply not used by the processor, no conflict of data from the two sources RAM and PSU are possible.

Dip Switch

The designation "L" on the assembly drawing indicates the LSB of the coding for the UPPER FOUR BITS of the MEMORY ADDRESS SELECT setting. This card may be positioned at any of the 4K steps, starting from 0000. (i.e. - 0000, 1000, 2000, 3000, up to F000)

SWITCH CLOSED	=	1
SWITCH OPEN	=	0

SPECIAL NOTES

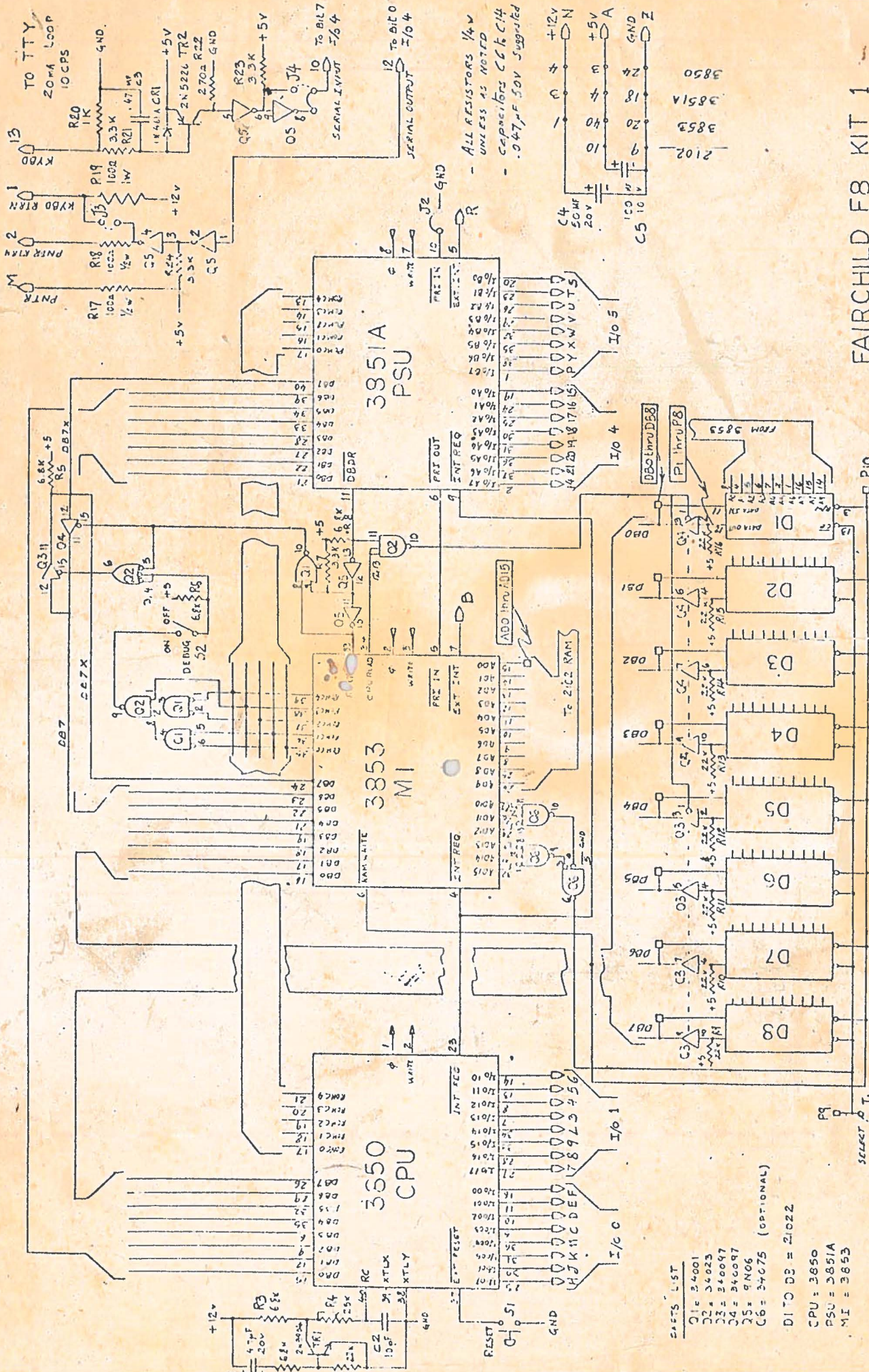
1. STATIC - Most of the devices used on the CPU-8 boards are some form of MOS logic. While all are protected against normal handling, protection from STATIC ELECTRICITY is the responsibility of the USER. Where possible, a grounded soldering iron is recommended and chip handling should be kept to a minimum (after removal from their protective carriers). MOST IMPORTANT, however, is to not handle or assemble chips under conditions of extreme low humidity. Do not wear heavy wool sweaters or walk across rugs wearing leather shoes, etc. If the user should happen to draw a static discharge between himself and one of the chips, THAT'S IT. The chip can only be thrown in the garbage.
  
2. All MEMORY AND PIO cards are to be installed on the motherboard FACING THE CENTRE. The Memory and PIO cards will, therefore, face each other as well. If this is not clear, an examination of the POWER BUS lines on the motherboard should indicate proper placement of the cards. BE PARTICULARLY CAREFUL to install the PIO Boards right-side-up. Although no immediate damage seems to result from plugging this board in upside-down, (i.e. - Port connector side to motherboard) freedom from device destruction cannot be guaranteed (and, of course, the microcomputer will not function if the board is upside-down).
  
3. All MEMORY CHIPS must have a 650 NS access time or better. 2102 types may be substituted for the low power 21L02 but should be 2102-1 or 2102-2 types. Care should also be taken not to exceed the power supply capability of the system as 2102 types may draw 60% more current than 21L02 types.

PS-2 POWER SUPPLY PARTS LIST

VR-1	✓ 78H05KC FSC REGULATOR Mounted on a 641A WAKEFIELD HEAT SINK	
VR-2	✓ 7812UC FSC REGULATOR	
D1, D2	✓ 1N4001 1 AMP DIODES	
D3, D4	✓ 60S1 IR 6 AMP DIODES	
C1	<sup>4,700</sup> 2,200 MFD 25 VDC CAPACITOR G. E. MEA25V2200	208-211, 216-221 238-240
C2-C5	<sup>4,700</sup> 3,300 MFD 16 VDC CAPACITORS G. E. MEA16V3300	
C6	<sup>13,000</sup> ✓ 0.1 MFD 16VDC CERAMIC CAPACITOR UK16-104 CRL	15DC 722 IL
TS-1	6-176-2 JONES TERMINAL STRIP	464-470, 508, 522,
TS-2	3-176-2 JONES TERMINAL STRIP	489, 492-93

For persons assembling the PS-2B0 board only version the following order of component installation is recommended.

1. Mount the terminal strips TS-1 and TS-2
2. Mount VR-1 and the associated heat sink
3. Mount VR-2. An additional 1/8" hole must be drilled in the heat sink to mount this component. This is best done by using the mounting hole in the P.C. board as a drilling guide after the heat sink is mounted. Be sure to use heat sink compound on both regulators.
4. The balance of the components may then be installed in any order.



- ALL RESISTORS 1/4W  
 - UNLESS AS NOTED  
 - CAPACITORS C66, C14  
 - .047µF 50V SUGGESTED

2102  
 3853  
 3851A  
 3850

# FAIRCHILD F8 KIT 1

REVISION C, SEPT 25, 1975

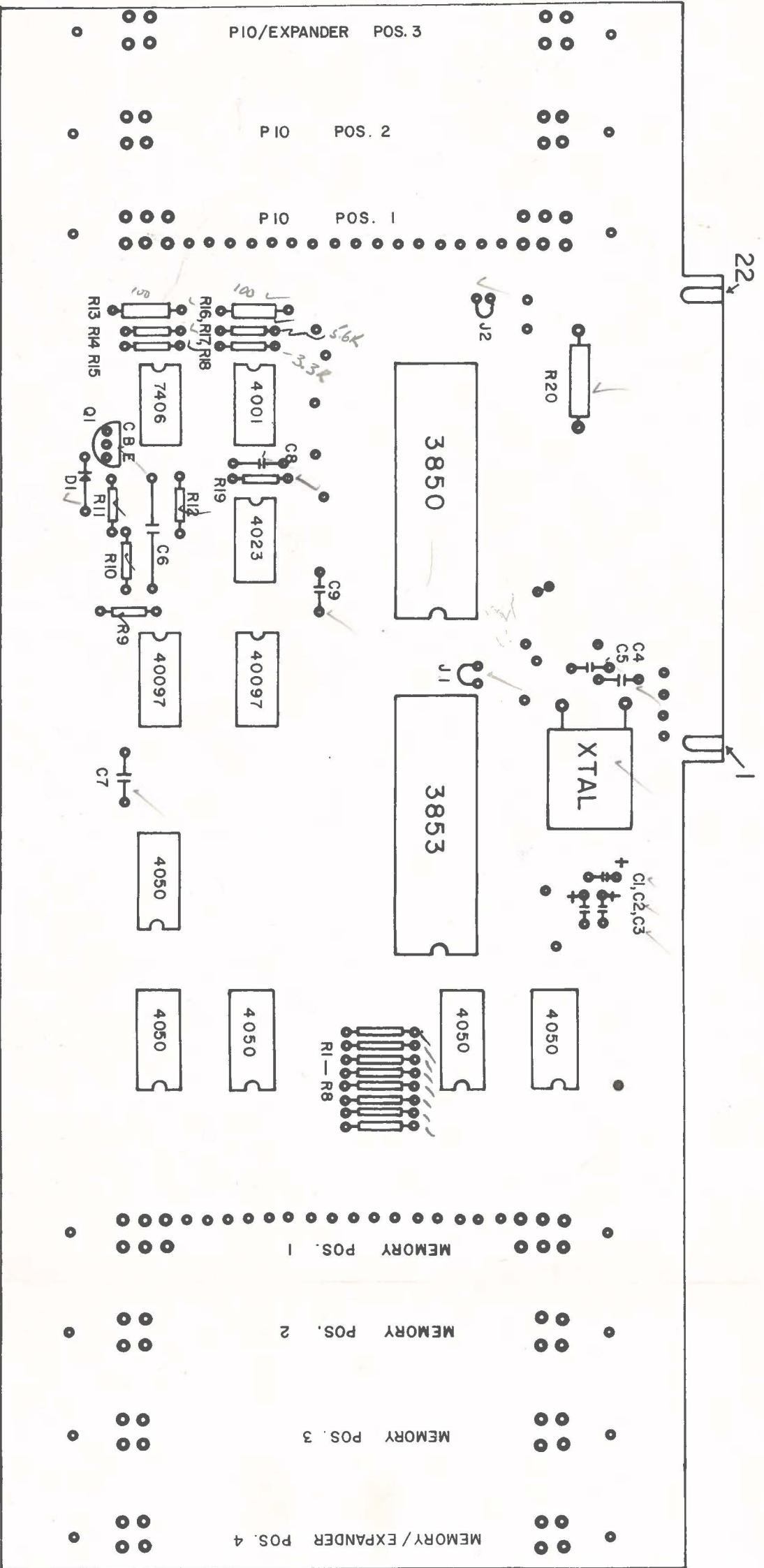
- PARTS LIST**
- D1 = 34001
  - D2 = 34023
  - D3 = 34007
  - D4 = 34007
  - D5 = 4N66
  - D6 = 34075 (OPTIONAL)

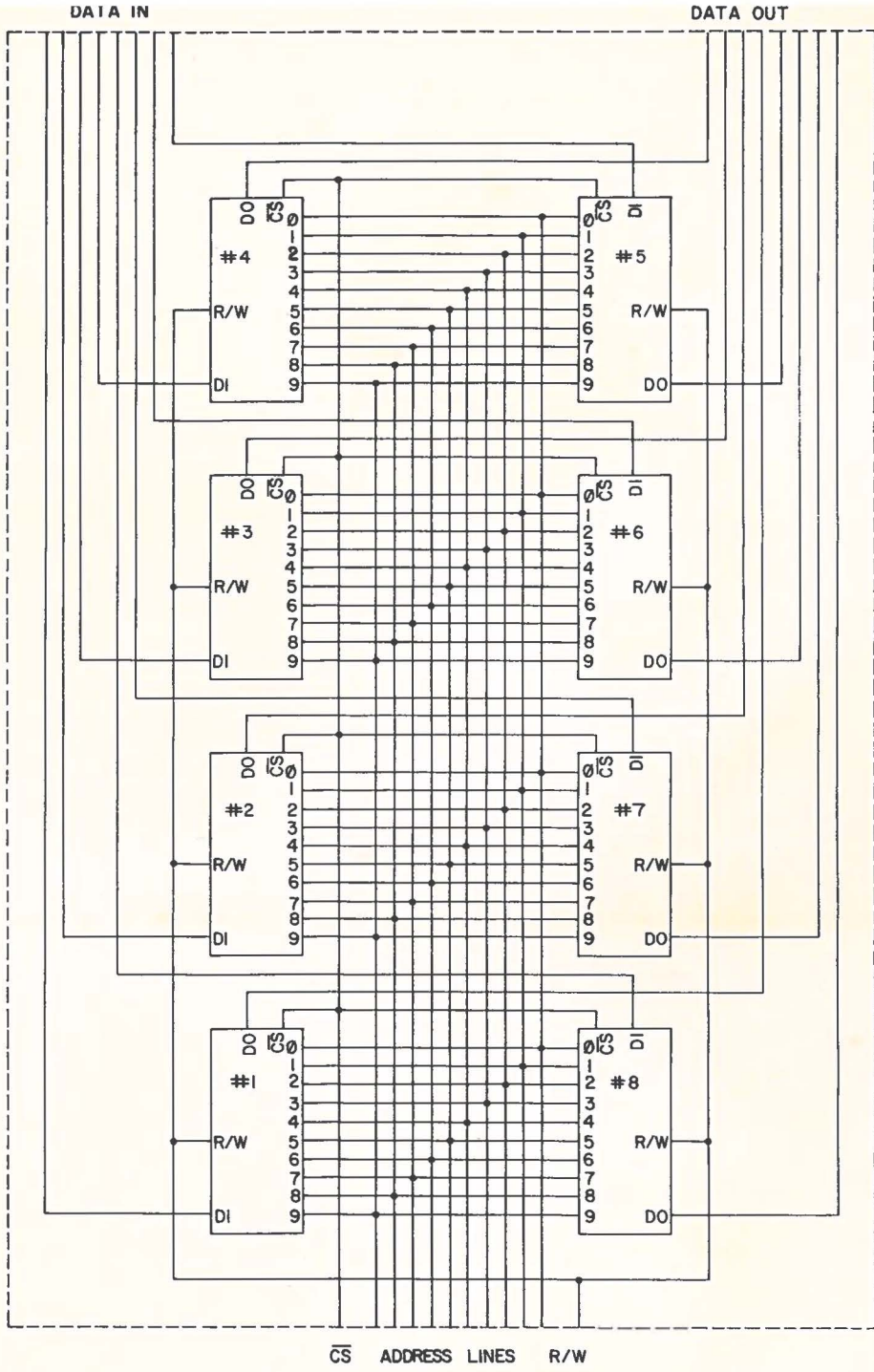
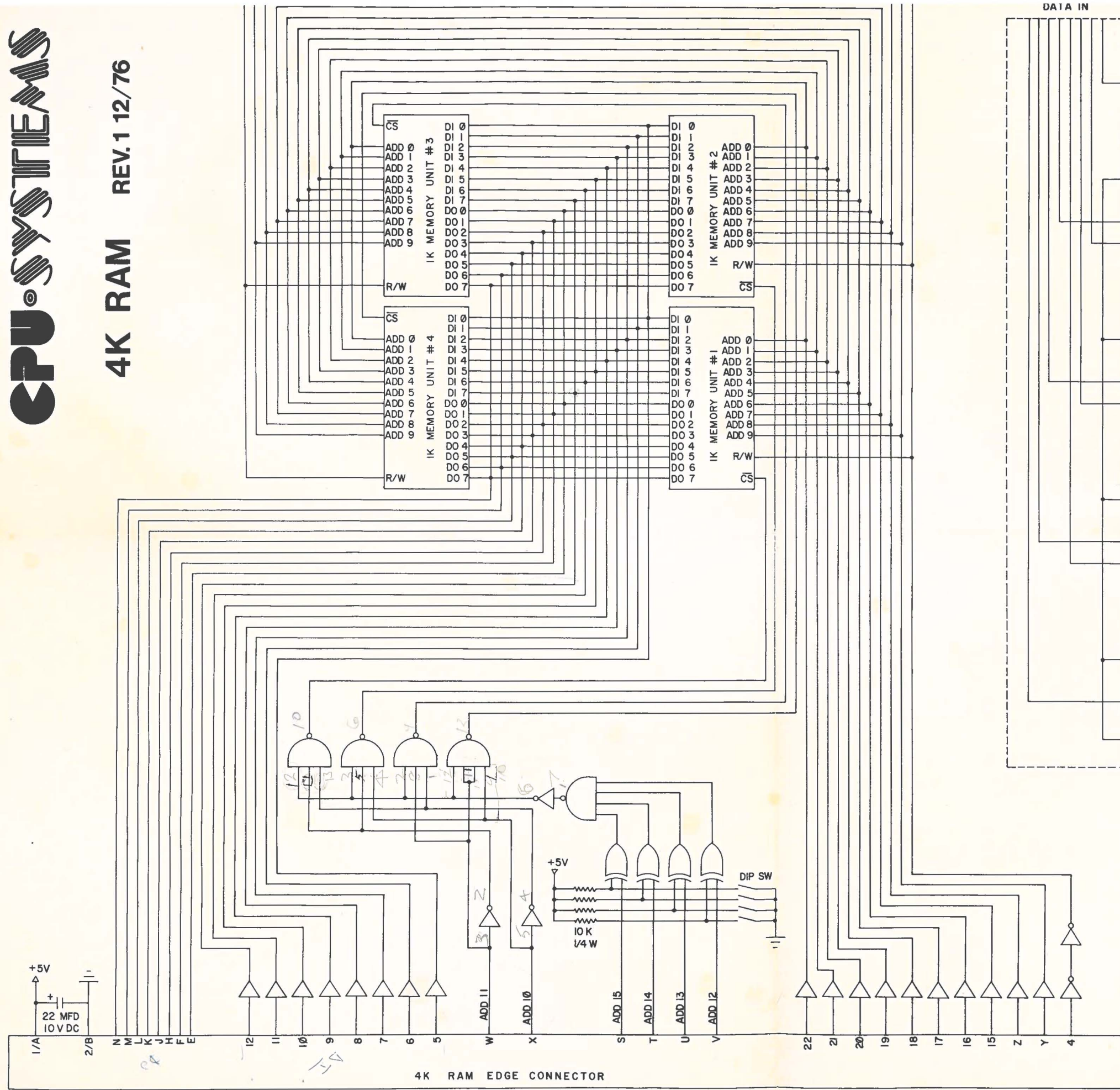
D1 TO D8 = 21022  
 CPU = 3650  
 PSU = 3851A  
 MI = 3853

SELECT  
 OPTION  
 GND

# CPU SYSTEMS

## CPU8 MOTHERBOARD COMPONENT PLACEMENT





— 1K MEMORY UNIT —  
ALL CHIPS 2102 OR 21L02

