

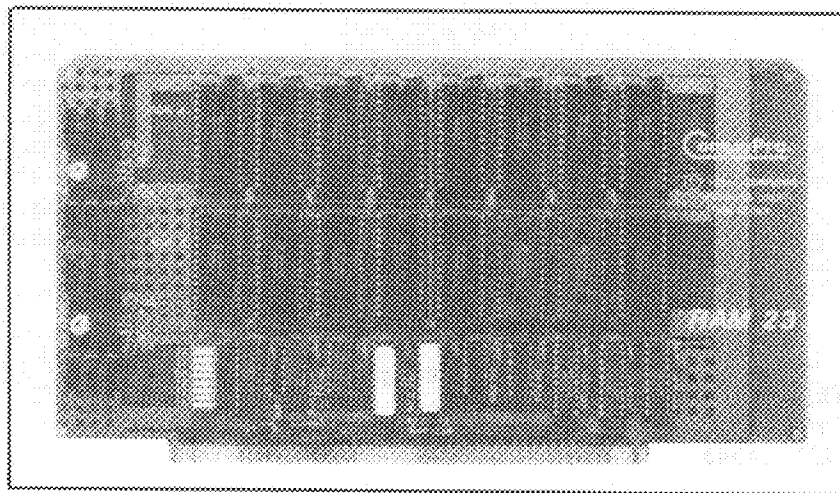
**COMPUTRO**

# RAM 23

TECHNICAL MANUAL

# RAM 23

## Technical Manual



STATIC MEMORY  
128K x 8 / 64K x 16  
or  
64K x 8 / 32K x 16

RAM 23 TECHNICAL MANUAL  
Copyright 1984 CompuPro  
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# CONTENTS

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- About RAM 23 . . . . . 1
- Technical overview . . . . . 1
- How to configure the RAM 23 for your system . . . . . 2
- Switch settings for S1 - address selection . . . . . 2
- Jumper settings . . . . . 2
- Theory of operation . . . . . 3
- Locating RAM ICs by address and bit . . . . . 3
- Logic diagram . . . . . 4-9
- Parts list . . . . . 10
- Component layout . . . . . 11
- Customer service/limited warranty information . . . . . 12

# RAM 23 TECHNICAL MANUAL

## ABOUT RAM 23

The RAM 23 from CompuPro represents one of the most advanced RAM boards ever produced for the IEEE 696/S-100 Bus. By combining state-of-the-art static CMOS RAM technology with CompuPro's design excellence the RAM 23 offers the most versatile, efficient and reliable performance available today. The board works as "byte-wide" memory in 8-bit systems and automatically switches to "word-wide" mode for today's newer 16-bit systems. It is available in two versions, 64K or 128K.

## TECHNICAL OVERVIEW

The RAM 23 uses 16 high performance 8K X 8 CMOS RAM chips to provide a total of 128K bytes or 64K words of storage. It is also available in a version with eight high performance 8K X 8 CMOS RAM chips to provide a total of 64K bytes or 32K words of storage. The RAM 23 is addressable on any 128K byte boundary for the 128K byte version, or any 64K byte boundary for the 64K byte version in the 16 megabyte address space specified by the IEEE 696 standard.

The RAM 23 also dynamically switches between "byte-wide" or "word-wide" modes per the state of the sXTRQ\* signal on the S-100 bus (see the Theory of Operation section for a complete discussion of how this protocol works).

CompuPro designed the board to work with our CPU 286/287 at 6 MHz, our 68K at 10 MHz, our 8086 at 10 MHz, our 8088 at 8 MHz, our CPU-Z at 6 MHz and our CPU 32016 at 6 MHz. The RAM 23 will also work with 8086/88 type CPUs at 12 MHz when these chips become available. It also handles high-speed DMA flawlessly, a feature few memory boards can boast.

To reduce the number of support ICs required to pack all this performance and capacity onto a standard height S-100 board, two PAL (programmable-array-logic) elements are used. The PALs select the proper memory chips and control the complicated data bus switching scheme required to mix 8- and 16-bit operations.

We also use a high-quality double-sided circuit board design that has a full solder-mask and legend. Sockets are provided for all ICs for ease of maintenance. All edge connector contacts are gold on a nickel substrate to insure long and reliable operation.

## HOW TO CONFIGURE THE M 23 FOR YOUR SYSTEM

The RAM 23 requires only that the starting address of the board be set using switch S1, and that Jumper J1 be set for either 64K or 128K. All other features such as PHANTOM and byte (8-bit)/word (16-bit) transfers are handled automatically by onboard logic. This board responds to the upper eight address lines (A16-23) as provided for by the IEEE 696/S-100 standard.

The starting address of the board is selected by setting paddles 1-8 of dip-switch S1 for a RAM 23 with 64K bytes and paddles 1-7 for a board with 128K bytes. S1 is located near the bottom left corner of the board. The address is set in a binary fashion with each paddle of S1 representing an address bit. An "ON" paddle represents a binary "zero" and an "OFF" paddle represents a binary "one". The paddle to address bit relationship is shown in the following table:

### SWITCH SETTINGS FOR S1 - ADDRESS SELECTION

ADDRESS BIT	PADDLE NUMBER	
A23 .....	1	
A22 .....	2	
A21 .....	3	
A20 .....	4	
A19 .....	5	ON = 0
A18 .....	6	OFF = 1
A17 .....	7	
A16 .....	8	

Paddle 8 has no effect on boards jumpered for 128K byte operation. Paddle 8 must be set on RAM 23 boards made to run at 64K bytes.

EXAMPLE: If this is the first RAM board in your system and you want 128K starting at address 000000H, set paddles 1 through 7 of S1 ON.

EXAMPLE: If this is the second 128K RAM board in your system and you want it addressed at 020000H, set paddles 1 through 6 ON and paddle 7 OFF.

EXAMPLE: If you want this board to reside at the top of the first megabyte of address space (i.e., starting address 0E0000H), set paddles 1 through 4 ON and paddles 5 through 7 OFF. This would put the board at the highest 128K address which an 8086 or an 8088 can directly address.

### JUMPER SETTINGS

To make this board work as either 64K or 128K, you have to set a shunt on Jumper J1. Jumper 1 is located near the bottom edge of the board to the left of center. If you want to use the board as 64K, set the shunt on the right-most position (next to the 64K mark on the legend). To use the board as 128K, set the shunt on the left-most position of the jumper.

## **THEORY OF OPERATION**

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The RAM 23 is designed to work in 8- and 16-bit systems per the protocol established by the IEEE 696/S-100 standard. The DATA IN and DATA OUT buses operate as a bidirectional 16-bit data path when word transfers are performed. The two buses remain uni-directional during byte operations.

Here's how the protocol works: The bus master requests a 16-bit transfer by asserting sXTRQ\*. If the slave (in this case the RAM 23) is capable of performing word transfers, it acknowledges this fact to the master by asserting SIXTN\*. Sometimes, even a 16-bit master may only want to transfer one byte rather than a whole word. In this case, the master does not assert sXTRQ\* but instead uses the data buses as an 8 bit master would, that is, data from the master would be transferred on the DO bus and data to the master would be transferred on the DI bus.

The RAM 23 handles this multiplexing of the data buses with two bi-directional bus buffers (U10 and U11) and one intermediate buffer (U12). This complicated algorithm is executed by PAL (programmable array logic) element U6. A second PAL (U7) acts as the array decoder along with U4. The RAM is configured as two arrays of 64K by 8 bits. The bit/address decode scheme is covered in the next section. The decoder PAL only generates select signals, which enable the RAM chips only during memory reference operations. This feature, coupled with the use of RAM chips which power down when not selected makes the RAM 23 consume less power than most dynamic RAM designs while providing the speed of operation and reliability that only static RAM delivers.

The base address of the board is set with dip-switch S1. Octal comparator (U3) generates signal ASEL\* when the address present on bus lines A16 through A23 matches that set in S1-1 through S1-8. A16 has no effect if the board is jumpered for 128K byte operation.

ESXT\* is the signal generated in the PAL (U6) which causes the RAM 23 to acknowledge requests for word transfers when the board is selected. Transistor Q1 provides the open collector output required to drive bus signal SXTN\* (line 60).

Parallel decoding speeds up the response time. An onboard generated early write signal (OBG) is used to take advantage of the speed of the S-100 bus. The write signal is started early and stretched out as long as possible.

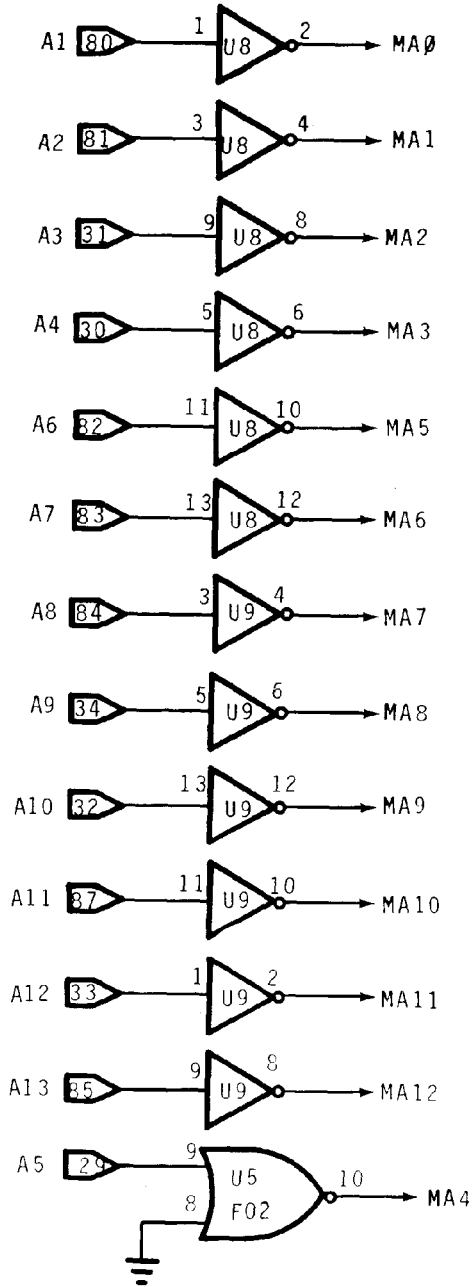
### **LOCATING RAM ICs BY ADDRESS AND BYTE**

The COMPONENT LAYOUT in this manual may be used as a map to locate RAM ICs by address and byte. Each RAM chip is identified by address and high or low byte position as written in each RAM location.

NOTE: The dotted line around the eight center most RAM chips on the COMPONENT LAYOUT indicates the RAM chips present in a 64K board.

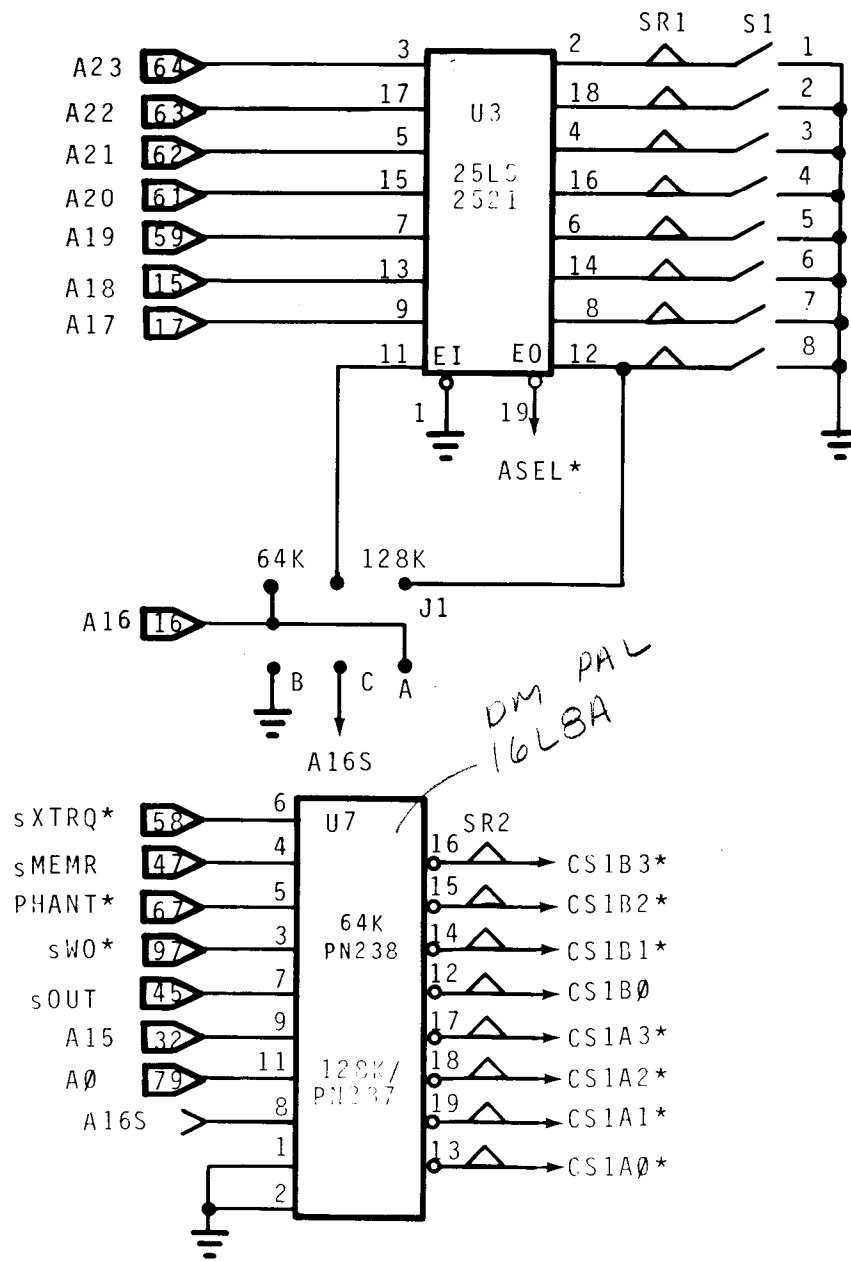
# LOGIC DIAGRAM

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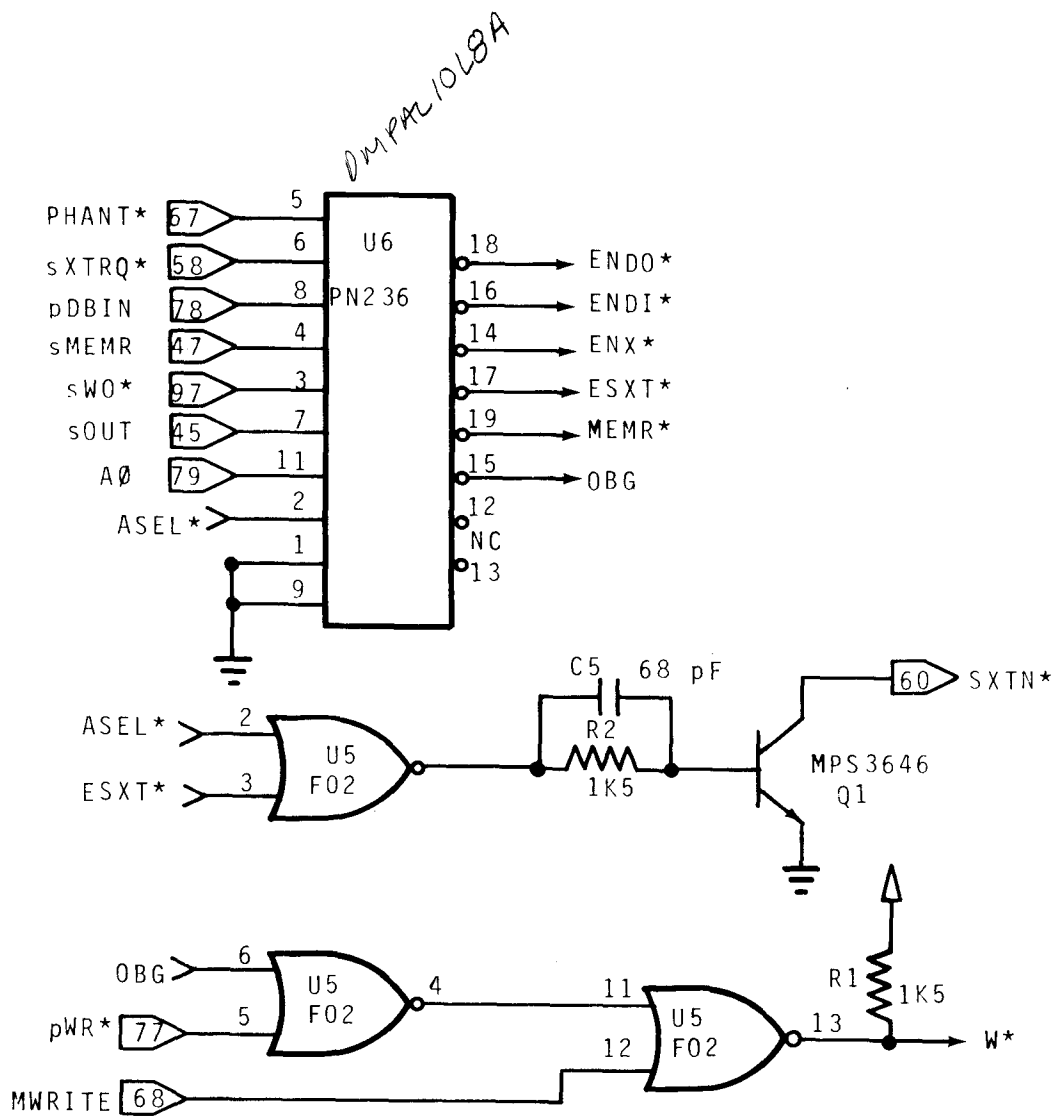


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235A  
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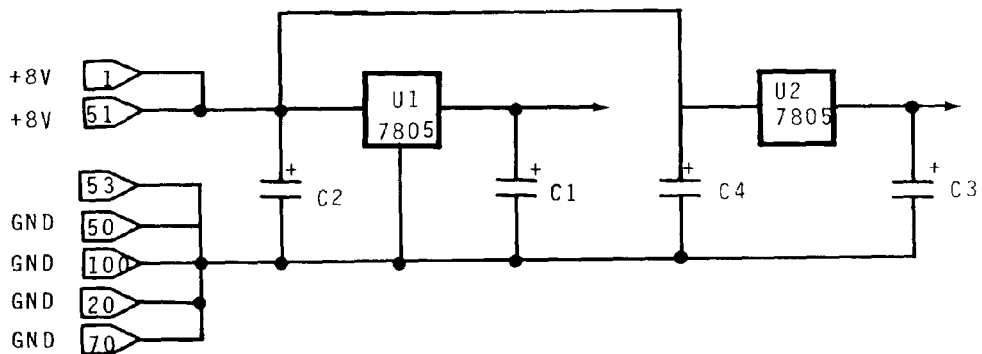
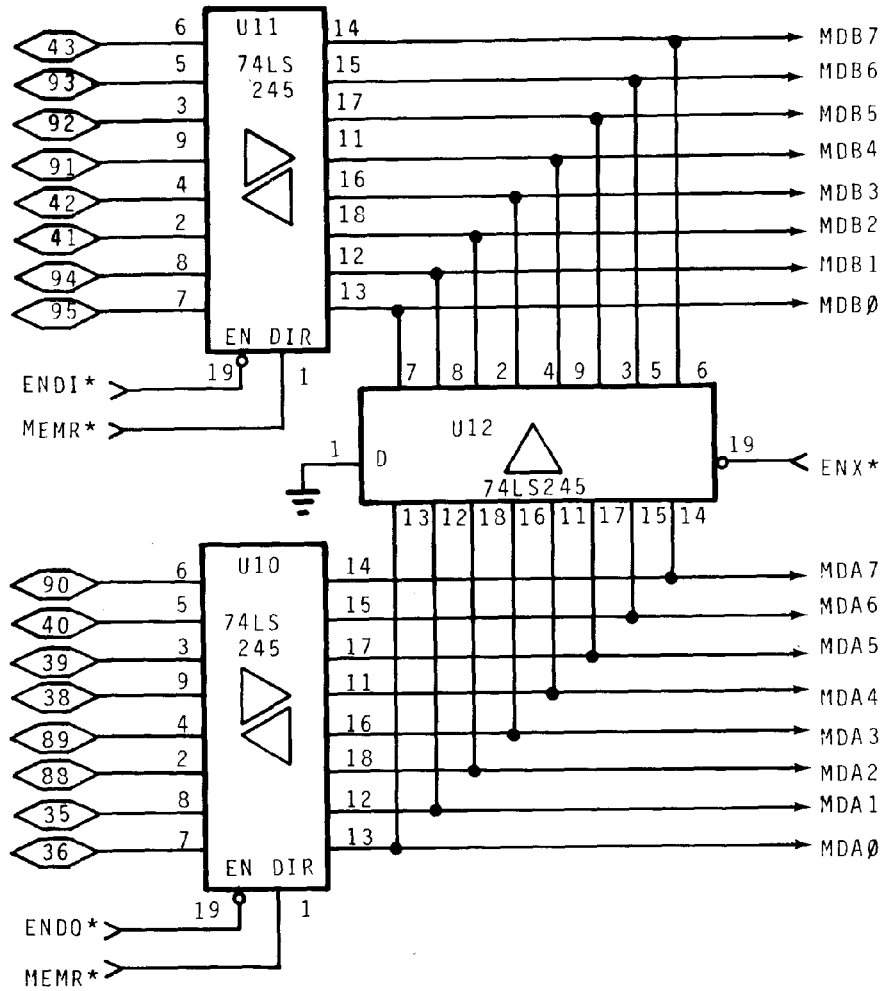




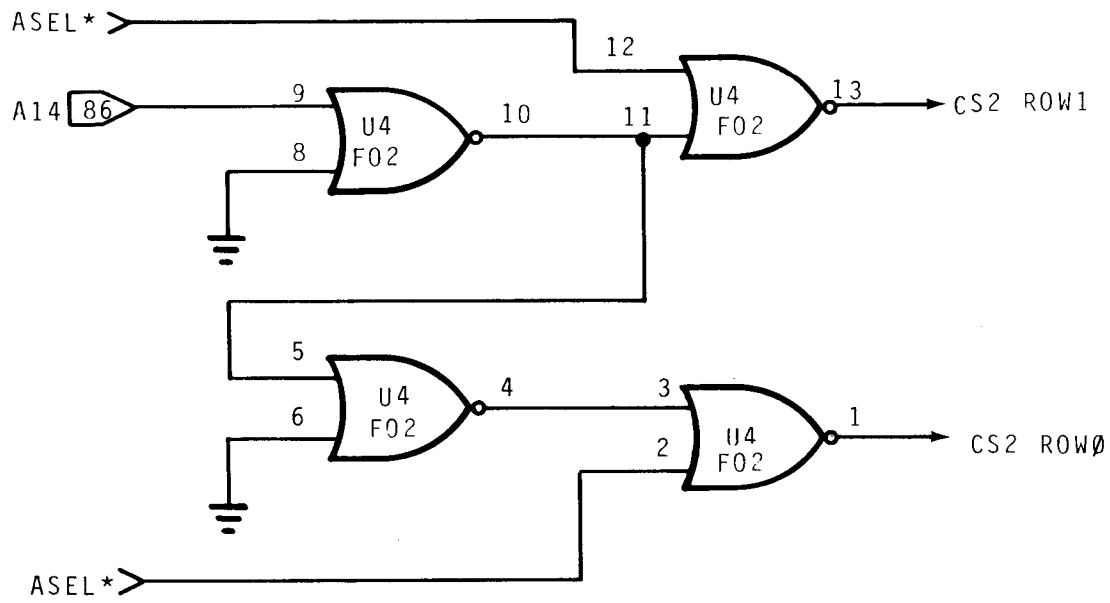
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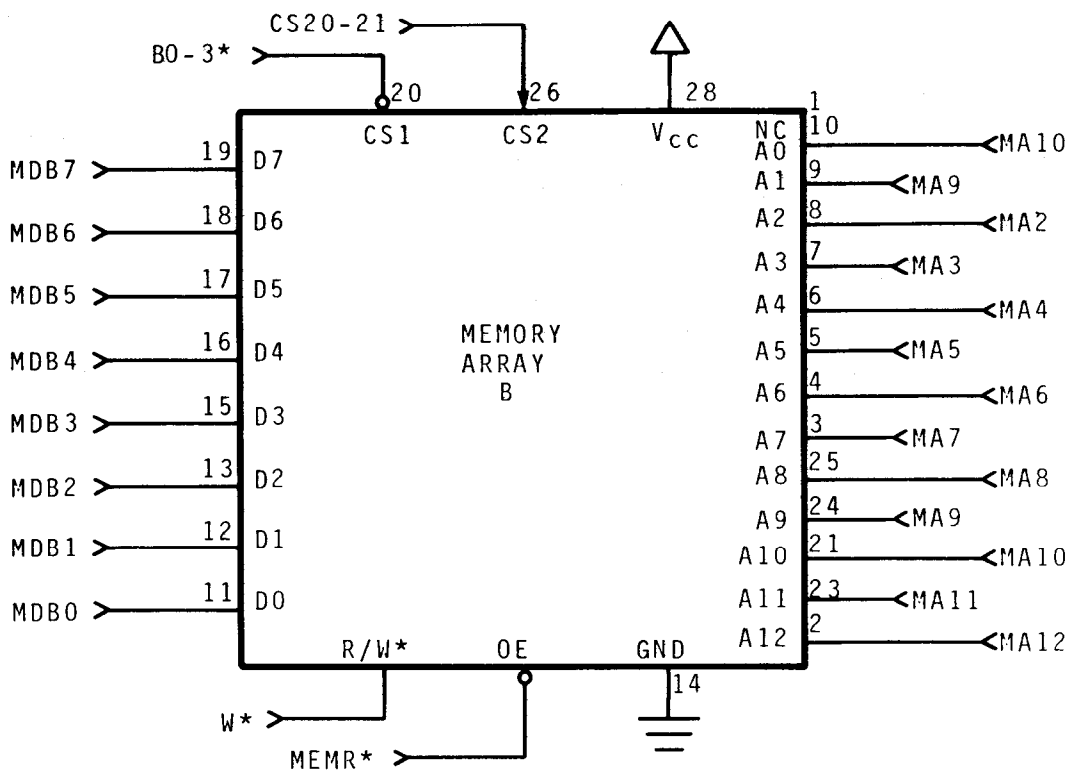
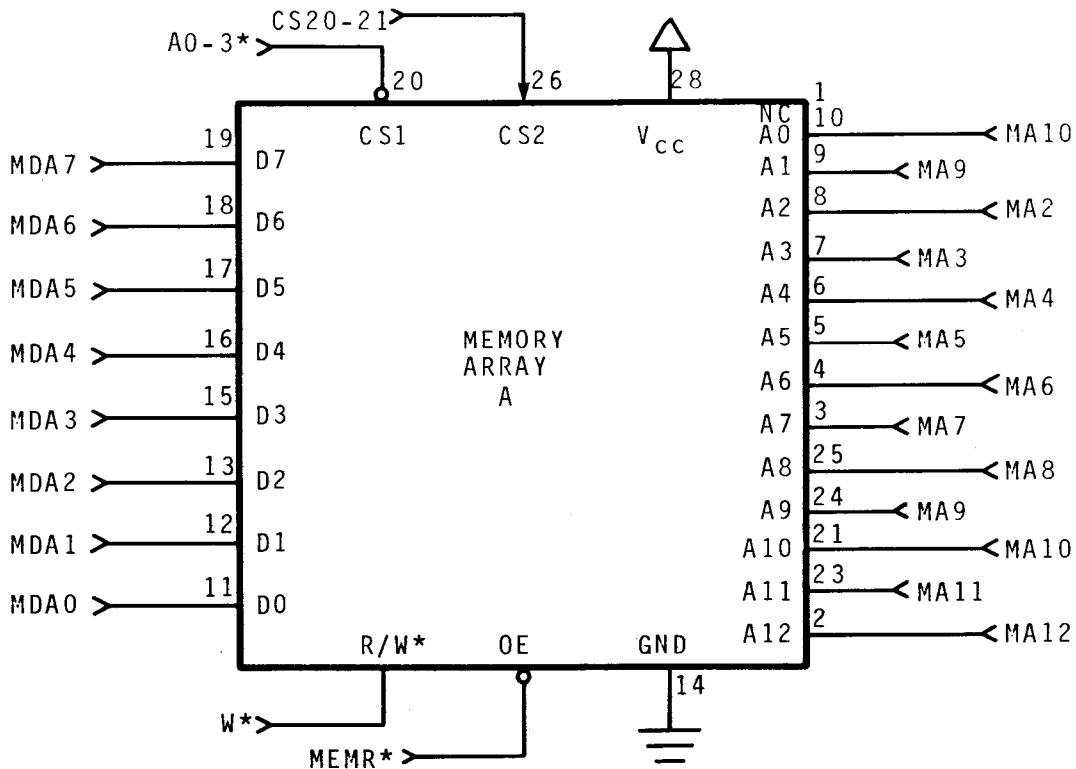
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# PARTS LIST

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## SEMICONDUCTORS

QTY	Description	Location
16	6264P-12	U13 thru U28 (128K bytes version)
8	6264P-12	U15 thru U18, U23 thru U26 (64K bytes version)
1	25LS2521	U3
2	74F02	U4, U5
2	74LS04	U8, U9
3	74LS245	U10, U11, U12
1	CompuPro #236	U6 (Programmable Logic Array, PAL)
1	CompuPro #237	U7 (PAL - 128K version)
1	CompuPro #238	U7 (PAL - 64K version)
2	7805	U1, U2 (5 Volt regulator)
1	MPS3646	Q1

## CAPACITORS

		Location
26	Bypass Caps	unmarked
1	68 pF silver Mica	C5
2	1.5 uF 6 volt (min.)	C1, C3
2	1.5 uF 10 volt (min.)	C2, C4

## RESISTORS

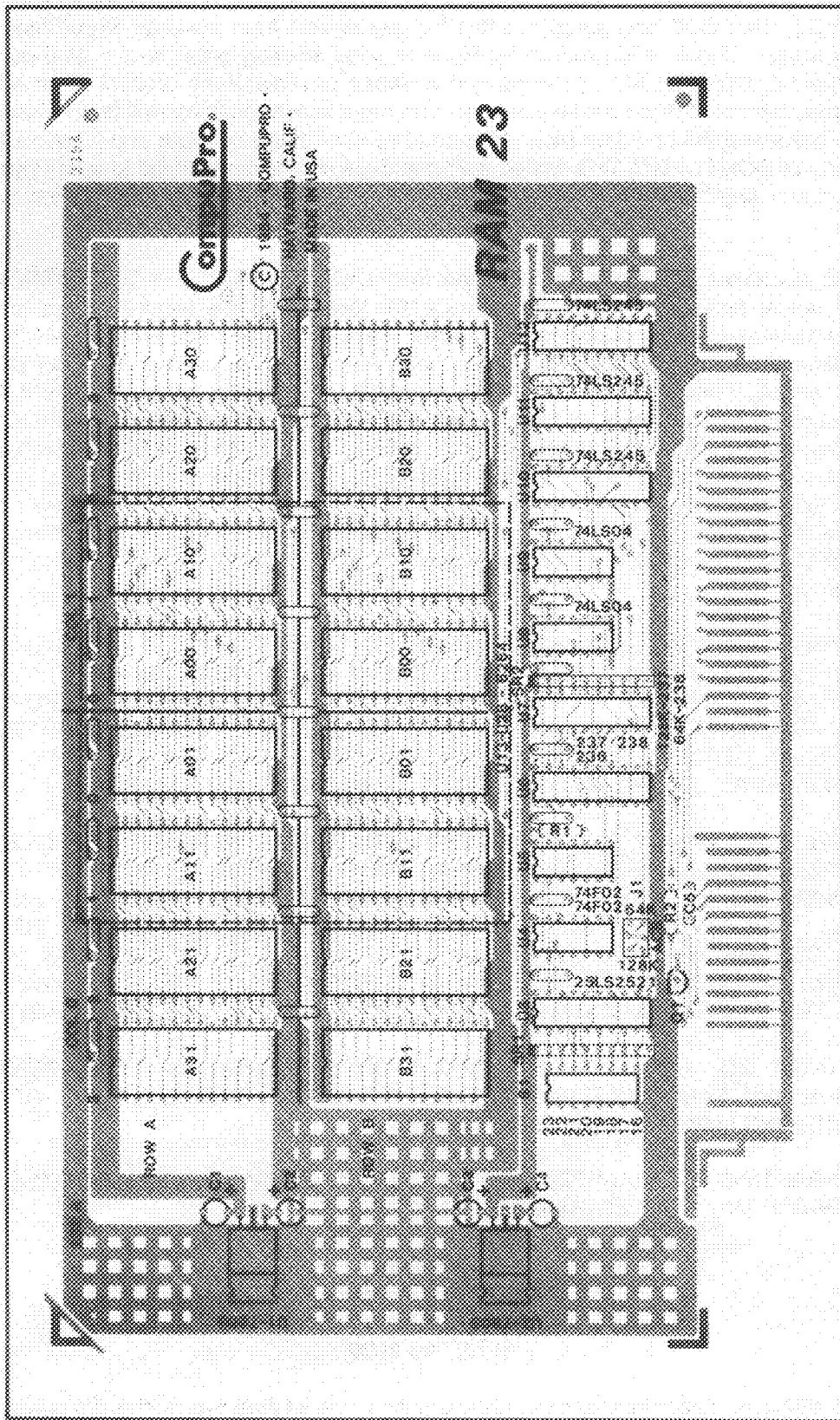
		Location
1	5K1 Ohm 1/4 W 5%	R1
1	1K5 Ohm 1/4 W 5%	R2
2	5K1 SIP	SR1, SR2

## SOCKETS

		Location
4	14 pin	U4, U5, U8, U9
6	20 pin	U3, U6, U7, U10, U11, U12
16	28 pin	U13 thru U28

## MISC. HARDWARE

		Location
2	Large Heatsinks	U1, U2
2	6-32 panhead, 5/16"	U1, U2
2	#6 lockwasher	U1, U2
2	6-32 1/4" nut	U1, U2
1	8 position dip switch	S1
2	Card Extractors	Upper corners
2x3	Double row pins	J1
2	Low profile shunts	J1



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 CALIF.  
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**RAM 23**

**COMPONENT LAYOUT**

□ First 64K Bytes



## LIMITED WARRANTY

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