Twenty Dollars

Cromemco

16FDC

Floppy Disk Controller

Instruction Manual

Cromemco™

16FDC

INSTRUCTION MANUAL

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This manual was produced on a Cromemco System Three computer utilizing a Cromemco HDD-22 Hard Disk Storage System running under the Cromemco Cromix™ Operating System. The text was edited with the Cromemco Cromix Screen Editor. The edited text was formatted using the Cromemco Word Processing System Formatter II. Final camera-ready copy was printed on a Cromemco 3355A printer.

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INTRODUCTION

The 16FDC is Cromemco's second generation floppy disk controller board. The 16FDC provides a complete system for floppy disk operation including serial I/O for an RS-232 terminal, a pre-programmed Read Only Memory with system bootstrap and diagnostic routines, and of course full read/write/format capability for any combination of single or double sided, single or double density, 5" (mini) or 8" (maxi) floppy disks. The 16FDC normally handles up to 4 drives in a daisy chain configuration, although 16 drives may be chained if the drives decode the 4 drive select lines.

The 16FDC includes an 8 channel interrupt system which is connected to the flag bits of the disk controller, serial I/O, and a set of interval timers. One of the interrupt inputs can optionally be connected to a 512 millisecond crystal controlled clock for real time interrupt capability.

All timing on the 16FDC is referenced to an onboard crystal clock. This includes the head load delay (which is switched according to the size of the diskette), the head stepping rate, the motor turnoff timer, and the watchdog timer in the autowait circuit.

The data recovery circuit uses a unique phase locked loop (pat. pending) to optimize performance for each size and density diskette. Single density data is recorded in the FM format while double density data uses the MFM format. Density on a given diskette may vary from track to track. Such dual density diskettes often require the first track to contain a label, written in single density, which informs the operating system of the density and number of sides of the remainder of the diskette.

The phase locked loop circuitry incorporates an adjustable trim capacitor which is clearly visible on the circuit board. This trim cap is adjusted at the factory. Special test equipment must be operated by trained personnel to adjust the setting of this capacitor.

THE USER MUST NOT MAKE ANY ATTEMPT TO ADJUST THE TRIM CAPACITOR.

Chapter 1

GETTING STARTED WITH THE 16FDC

Most users of the 16FDC will be running under the Cromemco Disk Operating System (CDOS) or the Cromemco Cromix Operating System. For these users, getting started with the 16FDC is simple -- a matter of plugging in the cables and setting the switches. These operations are explained below.

SWITCHES

The first four switches on the 16FDC are important to CDOS and Cromix Operating System users.

The first switch (numbered 1, located at the top of the rank of switches) is the RDOS-II DEFEAT control. The operating system uses the RDOS-II program for bootstrap when the system is turned on, so be sure that switch 1 is OFF (pushed to the left).

Switch 2 is the control for DISABLE RDOS-II AFTER BOOT. This switch should be ON (pushed to the right) to clear all 64k bytes of memory space for the operating system after RDOS has performed the bootstrap.

Switch 3 is the AUTOMATIC BOOT control. Set it ON to make your system load the operating system. If the switch is OFF, RDOS-II enters a diagnostic monitor mode and waits for further commands.

Switch 4 INHIBITS INITIALIZATION. When on, Cromemco initialization programs will not allow diskettes to be formatted. Turn the switch OFF if you are expecting to format double density (or any) diskettes.

Table of Standard Switch Settings

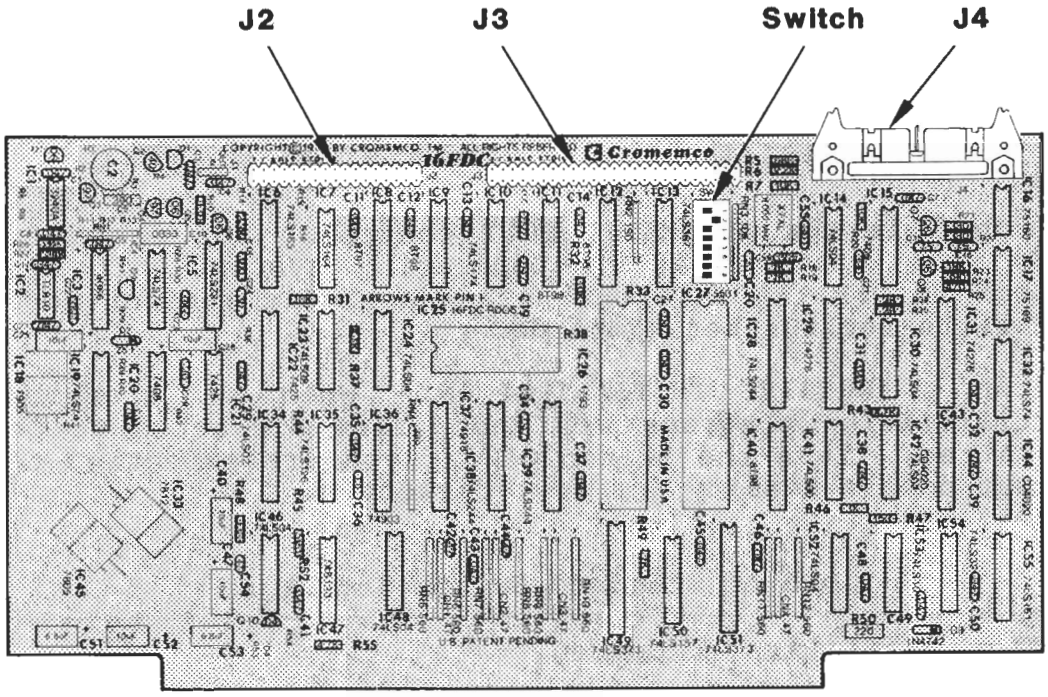
Switch	Position	Function
1	OFF	RDOS-II is not defeated
2	ON	RDOS-II disabled after boot
3	ON	operating system loads automatically
4	OFF	operating system can format diskettes
5	OFF	baud rate not pre-set
6-8	N/A	reserved

CABLES

A 26 wire ribbon cable connects the RS-232 socket at the back of the computer to the 16FDC. This cable should be plugged into the serial connector (J4) of the 16FDC. The cable has a stripe along one edge. This stripe face left, towards the center of the 16FDC.

Now find the disk signal cables. If you have 8" drives, the cable will have 50 wires; if you have 5" drives, the cable will have 34 wires. Connect these cables to their jacks (J3 and J2 respectively). Ensure that the cable stripe is to the left.

Finally, connect the interrupt daisy chain to connector J1. This step is necessary if you have a WDI, PRI, TU-ART, or other cards capable of generating interrupts or if you are running the Cromix Operating System. If these cards are not present, or if interrupts will not be used, the daisy chain cable need not be connected.



16FDC CABLE CONNECTIONS

INITIALIZATION OF DISKETTES

The initialization format of the 16FDC is more restrictive than that required by the 4FDC. The 16FDC may not be able to read small (5-1/4 inch) diskettes which were initialized using versions of the Cromemco **Init** program prior to version 2.15. It also may not be able to read large (8 inch) diskettes which were initialized around the wrong index hole. The following procedures will assist users who encounter either of these problems.

Floppy diskettes which cannot be read by the 16FDC because of improper initialization must be copied to properly initialized diskettes using the 4FDC. A properly initialized small diskette is one which has been initialized using the **Init** program, version 2.15 or higher. A properly initialized large diskette is one which has been initialized using the **Init** program, version 2.15 or higher, with the proper index hole exposed (refer to the following paragraph on index holes). After it has been determined that the copied diskettes can be read by the 16FDC, the old diskettes may be reinitialized using the 16FDC.

Index Holes

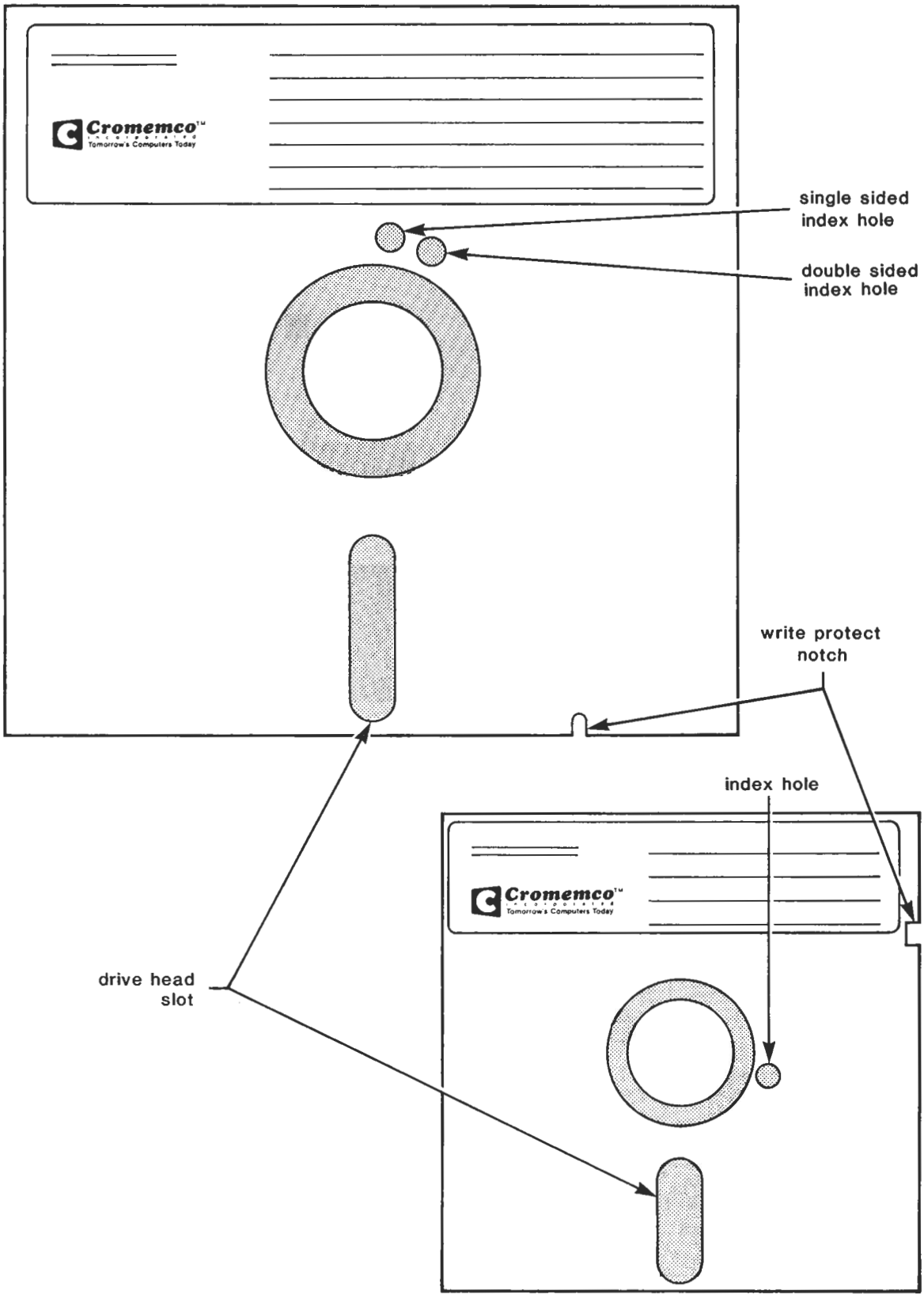
Cromemco large (8 inch) double sided, double density floppy diskettes have two index holes. The hole closest to the top of the diskette should be **exposed** when using the diskette as single sided. The hole to the right should be **exposed** when using the diskette as double sided.

Cromemco strongly recommends that only the correct index hole be exposed before using an 8 inch diskette. Cromemco supplies special labels for this purpose.

Write Protection

The 16FDC, when used in conjunction with a Cromemco floppy disk drive, provides write protection.

An 8 inch diskette is write protected if the write protect notch is **not** covered. A 5-1/4 inch diskette is write protected if the write protect notch **is** covered.


Cromemco™
Tomorrow's Computers Today
single sided
index hole
double sided
index hole
write protect
notch
index hole
Cromemco™
Tomorrow's Computers Today
drive head
slot

STARTING THE SYSTEM

With all cables installed and the switches set, the 16FDC is ready for operation. Set the ZPU power on jump (refer to the Cromemco ZPU manual, part number 023-0012) so that execution will begin at C000 hex (start of RDOS-II). Set the switches on the RAM card(s) so that memory at C000 to D000 hex is disabled and memory from 0000 to 1000 hex (or more) is enabled.

Now apply power to the system and insert a disk containing the operating system into drive A. RDOS-II will print out a sign-on message after determining the baud rate of the terminal. (Note: if you are not using a Cromemco 3102 Video Terminal it will be necessary to press the **RETURN** key on your terminal several times so that the 16FDC can determine the baud rate.)

After the sign-on is complete, RDOS-II will try to load the operating system from drive A. The light on the drive will come on, indicating that the 16FDC is accessing the drive.

If you would prefer not to load the operating system, press the **ESC** key immediately after the RDOS-II sign-on appears. This instructs RDOS-II to abort the bootstrap procedure.

Chapter 2

RDOS-II

The Cromemco Resident Disk Operating System II (RDOS-II) is a 4K byte program supplied in ROM with each Cromemco model 16FDC disk controller card. The RDOS program is designed to execute beginning at memory location C000h.

COMMAND FORMAT

All commands must be terminated by a carriage **RETURN** character. RDOS-II will not respond to any command until the command is properly terminated with a **RETURN.**

The normal prompt of the monitor is a semicolon (;). If a disk drive is selected, the prompt changes in order to remind the user which drive is current. All disk commands refer to the drive most recently selected.

Spaces within the command string are ignored, but spaces must not be embedded inside numeric arguments. Thus, the command format is generally free form with respect to spaces.

Wherever a numeric value is expected, a decimal integer may be specified by following the number with a decimal point (e.g., **123.**). If no decimal point is present, the number is assumed to be hexadecimal.

Console input is line buffered thus allowing use of the following edit commands:

Backspace	Deletes previous character
CNTRL-U	Deletes current input line
Backarrow or Underline	Same as Backspace
Delete or Rubout	Same as Backspace

CNTRL-P may be selected at any time to start or terminate the echoing of terminal output to the printer. The printer must be a dot matrix printer, such as the Cromemco Model 3703. RDOS-II does not support the use of fully formed character printers, such as the Cromemco Model 3355A.

CNTRL-S may be used to suspend the display, with another

CNTRL-S (or any other character) used to resume the display.

ESC or **RETURN** may be used to abort the display and return control to RDOS-II.

SWATH OPERATOR

Commands requiring multiple address arguments may be specified in one of two ways: either by explicitly declaring the start & stop addresses, or by declaring the start address and the swath (or width). This is done by following the start address with the letter **S** and the swath width. For example, the following two commands are identical in function:

DM 100 142	Display memory starting at 100h through 142h
DM 100 S 43	Display memory starting at 100h for 43h bytes

ALIGNMENT OPTION

A ON
A OFF

This command is used to force disk select on a continuous basis. **A ON** enables the option, **A OFF** disables it. This command is used when aligning disk drives. When the option is enabled, the current drive will be selected and stay selected until the option has been disabled. In this mode the user may perform all of the usual disk operations.

BOOT

B

Upon receiving the boot command, RDOS-II will print the message:

Preparing to BOOT, ESC to Abort

indicating the boot command has been received.

After this, RDOS-II will wait one second before reading the boot sector. The disk is then read. If the boot sector can be read, RDOS-II will check to see if an **ESC** has been typed at the console. If it has, the boot will be aborted. If not, RDOS-II will print:

```
Standby
```

and jump to the boot. This will allow the user to abort the boot during the boot preparation by typing **<ESC>**. If the boot is not aborted, then the operating system will display its sign on message and prompt.

Note that if the disk controller board is set for power on boot, the boot may be aborted by typing **<ESC>** as described above, allowing the user to go into RDOS-II without having to reset the power on boot switch on the 16FDC.

DISPLAY MEMORY

```
DM
DM start
DM start finish
DM start S swath
DM S swath
```

The contents of memory is displayed in hexadecimal and ASCII. Each line of the display is preceded by the address of the first byte. The ASCII portion is displayed to the right of the hexadecimal part, with bit 7 set to 0. Any nonprinting ASCII characters are displayed as a period (.).

The first form of the command will display 80h bytes starting with the ending address of the previous DM command plus 1, or 100h if no DM command has been given yet. The second form will display 80h bytes from the address specified. The third form will display from start to finish as specified. The fourth form will display swath bytes beginning at start. The last form will display swath bytes starting with the ending address as above.

The default swath width for the DM command is 80h (128 decimal) bytes. The letter M following the D is optional.

EXAMINE INPUT PORT

E port

Displays the current contents of the specified input **port.**

GO

G addr

Begins execution starting at addr.

INITIALIZE BAUD RATE

I

After the **I** command and the following **RETURN** are typed, change the baud rate of the terminal to the desired value and then type **RETURNs** until the monitor responds with its prompt. On Cromemco 3102 terminals, RDOS-II establishes the baud rate by sending a <BREAK> to the terminal, thus eliminating the need for the user to type **RETURNs** to set the baud rate. The monitor is capable of selecting 19200, 9600, 4800, 2400, 1200, 300, 150, or 110 baud. The maximum number of **RETURNs** required is four. During this process, any character other than the **<CR>** is ignored. If switch 5 is set, then the baud rate will be automatically set to 300 baud. This is so a modem can be used instead of a terminal, not requiring the use of **<CR>**s to initialize the baud rate.

LIST ALL DISKS LOGGED IN

L

List details of all disks logged in, in the following format:

Drive $1, Size $2, $3 Sided, $4 Density, $5 Seek, Cromix

where:
$1 is drive letter **A** through **D**
$2 is **L** or **S** for Large or Small
$3 is **S** or **D** for Single or Double
$4 is **S** or **D** for Single or Dual
$5 is **F**, **M**, or **S** for Fast, Medium, or Slow
Cromix is printed if the disk is formatted for use with the Cromix Operating System.

MOVE

M source finish dest
M source S swath dest

Move (or copy) the contents of memory beginning with source and ending with finish to memory beginning at dest. After the move, the monitor will verify that the source and destination are the same. This will result in a display of discrepancies which are not really errors after certain types of overlapping moves. This printout can be terminated by depressing **<ESC>**.

The move command can be used to fill a block of memory with a constant. For example, to enter zeros between locations 100h and 108h, use the **SM** command to enter 0 at location 100h, and then move 100h through 107h to 101h:

M 100 107 101 or
M 100 S 8 101

OUTPUT

O byte port

Writes **byte** to the output **port** specified.

QUERY

Q start finish string of bytes
Q start S swath string of bytes

This command is used to search memory specified for a certain string of bytes. The string of bytes is in the same format as in the **SM** command. If the string of bytes is found, 16 bytes starting at the first byte which matches are displayed as in the **DM** command.

READ DISK

RD start finish sector
RD start S swath sector

Before this command will be accepted, the disk drive, side number, and track number must have been specified. (See the Select Disk, Seek and Set Side commands.)

This command reads enough sectors from disk to fill the specified memory area, starting with the specified sector of the current track. The first track, sector and side and the last track, sector and side read are then displayed (e.g., 1D01 0 1D02 0).

If the last sector on the last track is read before the memory area is filled then the message is displayed:

Next Memory: nnnn
End of Disk

where nnnn is the next location to be read into. The command is terminated.

The command is also terminated if an error occurs in reading a sector. In this case the message **Rnn** is printed, where nn is a hex number which indicates the status:

Bit	Indication
7	Not Ready
6*	0
5*	Record Type
4	Record Not Found
3	CRC Error
2	Lost Data
1*	Data Request
0*	Busy

*are not really errors

SET DISK SIDE

SX side

The current drive is set to the side specified. If the current drive is single sided a question mark will be displayed and the command terminated.

SEEK

S track	e.g.,	S 28. Seek track 28 (decimal)
S track side	e.g.,	S 1C 1 Seek track 1C (hex) on side 1
SS side	e.g.,	SS 1 Set side to 1

Before this command will be accepted the disk drive must be specified. (See the Select Disk command.)

This command seeks the specified track of the current drive. The first form will seek on the current side; the second form will select the side before seeking.

If the second form is specified with a single sided drive or disk, an error message will be printed and the operation terminated.

In the third form the current drive is set to the side specified. If the current drive is single sided a question mark will be displayed and the command terminated.

Bit	Indication
7	Not Ready
6*	Write Protect
5*	Head loaded
4	Record Not Found
3	CRC Error
2*	Track 0
1*	Index
0*	Busy

*are not really errors

SELECT DISK DRIVE

The 16FDC will control up to 4 disk drives labelled **A, B, C,** and **D.** It can handle seeks from the slow seek appropriate to the mini floppy to the fast seek of Cromemco's large floppy. It can also handle the medium seek of some other large floppies.

It can handle single or dual density format, double sided as well as single sided drives and disks, including Cromemco Cromix Operating System format disks.

To select a drive, type the drive name followed by 1 semicolon for large disk and fast seek, 2 semicolons for large disk and medium seek, and 3 semicolons for small disk and slow seek, followed optionally by the sides/density/Cromix configuration. These options are specified as follows:

d;xyz

where:
d is the drive name
x is **S** or **D** for Single/Double sided
y is **S** or **D** for Single/Dual density
z is **C** for Cromix (optional)

Side/Density options **must** be specified together. Cromix may be specified only if Side and Density are specified.

Examples:

A;DS	Specifies drive A with fast seek, double sided, single density:
D;;;SDC	Specifies drive D with slow seek, single sided, dual density, Cromix

If no options are given, RDOS-II will read the label from the disk and log it in with the specification given on the label.

Disk selection also restores the disk drive head to home, track 0. If an error is made in doing this the message **Hnn** is printed where nn is a hex number indicating the status:

Bit	Indication
7	Not Ready
6*	Write Protect
5*	Head loaded
4	Record Not Found
3	CRC Error
2*	Track 0
1*	Index
0*	Busy

*are not really errors

SUBSTITUTE MEMORY

SM
SM addr

This command is used to substitute memory. The first format will substitute memory at the last location substituted plus 1, (100h if no **SM** command has been given yet); the second form will substitute at the address specified. RDOS-II displays the address followed by the contents of the memory byte. One of the following may then be entered:

1. A data byte value followed by a **RETURN.** The data byte value is stored at the address of the prompt. The address is then incremented by 1 and displayed on the next line.

2. A string enclosed between apostrophes (') followed by a **RETURN.** The string is stored beginning at the

address of the prompt. The address is then incremented past the string and displayed on the next line.

3. Any number of 1 and 2 above can be entered on one line with just one **RETURN** terminating the line. The address is then incremented past the bytes that were stored and the new address is displayed on the next line.

4. A minus sign (-). A minus sign does not store a byte. The address will be decremented to the previous address. The minus sign can be used to back up to a previous location in case an error was made.

5. A **RETURN** only. If no entry is made on the line, the memory byte remains unchanged. The address is incremented by 1 and displayed on the next line.

6. A Period (.). A period ends the input mode and returns control to RDOS-II.

Wherever a numeric value is expected, a decimal integer may be specified in place of a hexadecimal value by following the number with a decimal point (e.g. **123.**).

TEST SYSTEM

```
T
TZ
```

The first command moves RDOS-II out of ROM into the bottom of RAM (lower 16K), enables the upper block of RAM, and moves RDOS back into RAM at C000h. It then performs a routine check of the system memory and the operation of the 16FDC. The memory check will display a map of all 4K blocks of available memory, followed by a map of which blocks have errors or no errors. A check is then made of the 16FDC seek, read, and write operations, with progress reports being displayed on the console. The drive used in the test is prompted for by the test command, and remains selected when the test terminates.

The second command does not move RDOS-II into RAM and may be used to test systems with no RAM at C000h.

Note that after executing the first command, RDOS-II resides in RAM. The user should exercise caution so as not to overwrite this part of RAM.

VERIFY

V source finish dest
V source S swath dest

Verify that the block of memory starting at source through finish (or for length swath) is the same as the block starting at dest. The addresses and contents are displayed for each discrepancy found.

The command works by reading bytes from the source and destination and comparing them. If a discrepancy is found it is displayed on the following order: source address, source contents, dest contents, dest address.

WRITE DISK

WD start finish sector
WD start S swath sector

Before this command will be accepted the disk drive, side number, and track number must have been specified. (See the Select Disk, Seek, and Set Side commands.)

This command writes the contents of the specified memory area to the current drive, starting with the specified sector of the current track. The first track, sector and side and the last track, sector and side written are then displayed (e.g., 2045 1 2503 1).

If the last sector on the last track is written before the memory area has been read then the message is displayed:

Next Memory: nnn
End of Disk

where nnn is the next location to be written from. The command is terminated.

The command is also terminated if an error occurs in writing a sector. In this case the message **Wnn** is printed, where nn is a hex number which indicates the status:

Bit	Indication
7	Not Ready
6	Write Protect
5	Write fault
4	Record Not Found
3	CRC Error
2	Lost Data
1*	Data Request
0*	Busy

*are not really errors

Chapter 3

REGISTER DESCRIPTIONS

The registers of the 16FDC will be discussed in numerical order according to their I/O addresses shown below:

I/O Address (hex)	INPUT	OUTPUT
00	UART status register	UART baud rate
01	UART receiver data register	UART data
02	not assigned	UART command
03	Interrupt address	Interrupt mask
04	Auxiliary disk status	Auxiliary disk command
05	not assigned	Timer 1
06	not assigned	Timer 2
07	not assigned	Timer 3
08	not assigned	Timer 4
09	not assigned	Timer 5
30	DISK status	DISK command
31	DISK track	DISK track
32	DISK sector	DISK sector
33	DISK data	DISK data
34	DISK flags	DISK control
40	not assigned	Bank select

00 IN STATUS REGISTER:

Status flags from the TMS5501 UART.

D7 Transmitter Buffer Empty
D6 Receiver Data Available
D5 Interrupt Pending
D4 Start Bit Detect

D3 Full Bit Detect
D2 Serial Receive
D1 Overrun Error
D0 Frame Error

The functions of these flags are indicated in the following sections.

D7 Transmitter Buffer Empty (TBE):

A high in bit 7 indicates that the transmitter data buffer is ready to accept a new byte. TBE goes high as soon as the serial transmitter begins to send the byte currently in the buffer. Since the transmitter is "double buffered", the user may respond to the TBE signal and load the buffer even before the previous byte has been totally transmitted. TBE also activates interrupt request bit 5 (refer to the Interrupt Mask). TBE is cleared when the buffer is loaded and is set by the RESET command.

D6 Receiver Data Available (RDA):

A high in bit 6 indicates that a byte of data is available from the receiver buffer. This flag remains high until the buffer is read. A RESET command clears the flag. If the buffer is not read by the time the next byte from the receiver is ready, the new byte will write over the old byte and the overrun error flag will be set. RDA also activates interrupt request bit 4 (refer to the Interrupt Mask).

D5 Interrupt Pending (IPG):

A high in bit 5 indicates that one or more of the eight interrupt request sources has become active. This flag goes high at the same time as the interrupt request pin of the TMS 5501 UART.

D4 Start Bit Detect (SBD):

A high in bit 4 indicates that the serial receiver has detected a start bit. This bit remains high until the full character has been received. SBD is cleared by RESET command. This bit is provided for test purposes.

D3 Full Bit Detect (FBD):

The FBD flag in bit 3 goes high one full bit time after the start bit has been detected. This bit remains high until the full character has been received. FBD is cleared by a RESET command. This bit is provided for test purposes.

D2 Serial Receive (SRV):

A high in bit 2 indicates high level on the serial data input line. A low in bit 2 indicates a low level on the serial data input line. SRV is high when no data is being received. This bit is provided for break detection and for test purposes.

D1 Overrun Error (ORE):

A high in bit 1 indicates that the receiver has loaded the receiver data buffer before the previous contents were read. ORE is cleared after the status port is read or by the RESET command.

D0 Frame Error (FME):

A high in bit 0 indicates an error in one or both of the stop bits which "framed" the last received data byte. FME remains high until a valid character is received.

00 OUT BAUD RATE REGISTER:

Loading this register sets the baud rate and stop bits for serial receive and transmit data. The bits are assigned as follows:

D7 STOP BITS
D6 9600
D5 4800
D4 2400

D3 1200
D2 300
D1 150
D0 110

D7 Stop

A high in bit 7 selects one stop bit for serial receive and transmit data. A low in bit 7 selects two stop bits.

D6-D0 Baud Rate

A high in one of the lower seven bits selects the corresponding baud rate. If more than one bit is high, the highest rate selected will result. If none of the bits are high, the serial transmitter and receiver will be disabled. (For special purposes, the baud rates can be octupled -- see the description of HBD in the command register.)

01 IN **RECEIVER DATA:**

This register contains an assembled byte of data from the serial receiver.

01 OUT **TRANSMITTER DATA:**

This register is loaded with data for the serial transmitter.

02 IN **Not Assigned:**

Reading this port causes no response from the 16FDC. This address is available for other parts of the computer system.

02 OUT COMMAND REGISTER:

The command register format is shown below.

D7	Not Used	
D6	Not Used	
D5	Test	Latched
D4	HIGH BAUD	Latched
D3	INTA Enable	Latched
D2	RST7 Sel.	Latched
D1	Break	Latched
D0	Reset	

D5 Test Bit (TB5):

A high in bit 5 disables the internal interrupt priority logic and then enables the internal clock. Thus, the signal on the INT pin of the 5501 becomes a TTL level clock of 1562.5 Hz (12.5 kHz if HBD is high -- see D4 High Baud below). TB5 should be low for normal operation.

D4 High Baud (HBD):

A high in bit 4 octuples the rate of the internal clock. This causes the interval timers to count eight times faster and the serial data rates to increase eight-fold. When bit 4 is high, baud rates up to 76.8k are available for high speed data transfers.

D3 INTA Enable (INE):

A high in bit 3 allows the 5501 to respond to an Interrupt Acknowledge by gating a Restart instruction onto the data bus at the correct time and resetting its internal interrupt request latch.

A low in bit 3 prevents the 5501 from detecting an INTA cycle.

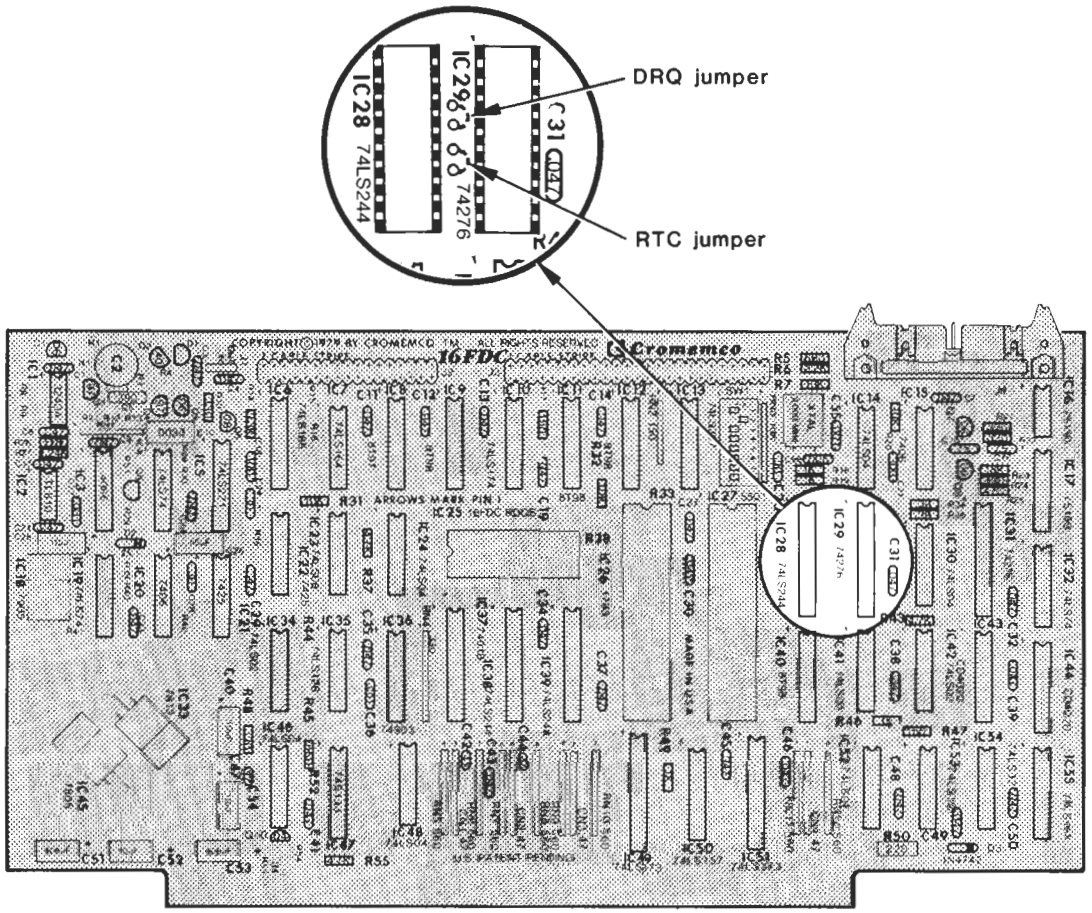
D2 RST7 Select (RS7):

A high in bit 2 connects the MSB of the parallel input port to the interrupt request latch for the lowest priority interrupt (interrupt 7). A low-to-high transition on the MSB of the parallel input port (XI7) will activate the interrupt request latch. The 16FDC provides an optional jumper to connect DRQ from the disk to XI7. When the jumper is inserted and RS7 is high, DRQ's from the disk will generate interrupts.

Another optional jumper connects a 512 millisecond clock to XI7. When this jumper (RTC) is inserted and RS7 is high, interrupts will be generated every 512 milliseconds.

Either the DRQ or the RTC jumper may be connected, **but not both.**

A low in bit 2 connects the output of Timer 5 to the interrupt request latch for the lowest priority interrupt (interrupt 7). When the timer count reaches zero, the interrupt request latch will be activated.



DRQ AND RTC JUMPER LOCATIONS

D1 Break (BRK):

A high in bit 1 holds the serial transmitter output in the low state (spacing). RES will override (see DO Reset below).

BRK should be low for normal operation.

D0 Reset (RES):

A high in bit 0 causes the following actions:

1. The Serial Receiver goes into search mode; RDA, SBD, FBD, and ORE are set to zero. The contents of the receiver buffer are not affected.

2. The Serial Transmitter output is set high (marking). If D0 (RES) and D1 (BRK) are both high, the RES function will override. RES sets TBE high.

3. The interrupt register is cleared except for the TBE interrupt request which is set high.

4. The interval timers are cleared. RES is not latched.

03 IN INTERRUPT ADDRESS:

This register contains the encoded address of the highest priority interrupt currently requesting service. This address is identical to the "Restart" instruction opcode for the interrupt acknowledge. Thus, the register contents may be (in order of service priority):

HEX	SOURCE
C7	Timer 1
CF	Timer 2
D7	End of job (From disk)
DF	Timer 3
E7	Receiver Data Available
EF	Transmitter Buffer Empty
F7	Timer 4
FF	Timer 5 or DRQ from disk or real time clock

This register is provided for servicing interrupts via polling. After the register is read, the corresponding bit in the interrupt request register is reset. If the register is read when no interrupt is pending, it will read 0FFH.

03 OUT INTERRUPT MASK:

The contents of this register are logically "And"-ed with output from the interrupt request register on the 5501. A high bit in the interrupt mask allows the corresponding request to pass on into the priority encoder. A low bit in the interrupt mask inhibits the corresponding interrupt from passing any further. Since the interrupt requests are latched independently of the state of the mask, an interrupt may be requested while the mask bit is low. The request will be retained until the mask is changed and the request allowed to pass on (assuming no RES command in the interim). The mask bit assignments are:

D7 Timer 5 or DRQ or real time clock
D6 Timer 4
D5 TBE (Transmitter Buffer Empty)
D4 RDA (Read Data Available)

D3 Timer 3
D2 EOJ (End of Job)
D1 Timer 2
D0 Timer 1

04 IN AUXILIARY DISK STATUS:

This register contains the following bits:

D7 DRQ or RTC
D6 Seek in progress
D5 X
D4 X

D3 Switch 5
D2 Switch 6
D1 Switch 7
D0 Switch 8

D7 Data Request (DRQ) or Real Time Clock (RTC) (jumper option)

A high in bit seven indicates the DISK data register, PORT 33H, is requesting service. This signal is also available at ports 30H and 34H. DRQ is provided at bit seven of port 04 so that the RS7 mode of the UART may be selected (see description of RS7; bit 2 of port 2) if interrupt driven disk routines are required. When shipped, the 16FDC does **not** have the enabling jumper inserted.

When the real time clock (RTC) jumper is inserted, D7 will be connected to a 512 millisecond square wave. This signal can be used to generate an interrupt when the RS7 mode of the UART is selected.

D6 Seek In Progress

A high in bit six indicates the voice coil motor in the currently selected drive is in motion.

A low in bit six indicates the voice coil motor has stopped moving in the currently selected drive.

This signal is only meaningful when the currently selected drive has a voice coil head stepper motor (e.g. PERSCI 277 or 299B). In all other cases, it will float high through the 150 ohm pullup to +5 volts.

D5-D4 Not assigned

D3-D0 Sense Switches

Bits D3 through D0 reflect the state of switch sections 5-8. A zero bit corresponds to a switch being ON.

04 OUT AUXILIARY DISK COMMAND:

This register contains the data which drives the parallel output buffers. The options which pertain to the Cromemco 299B disk drive follow.

D7 X
D6 -EJECT
D5 -DRIVE SELECT OVERRIDE
D4 -FAST SEEK

D3 -RESTORE
D2 -CONTROL OUT
D1 -SIDE SELECT
D0 X

D7 Not assigned

D6 Eject

A one in bit six causes no action. A zero in bit six activates the eject line of J2. This bit only affects PerSci drives with remote eject option. This bit is normally high.

D5 Drive Select Override

A one in bit five causes no action. A zero in bit five activates four drive select outputs from the 16FDC. Normally these outputs are controlled by the 1793; this bit is provided for testing and reading drive status in multiplex applications. This bit is normally high.

D4 Fast Seek

A one in bit four causes no action. A zero in bit four puts the FD 1793 into fast step mode as needed by voice coil drives. D4 should be returned to logic 1 after the drive has signalled seek complete. This bit is normally high.

D3 Restore

A one in bit four causes no action. A zero in bit four causes the currently selected drive to return to Track 00. This bit is normally high.

D2 $\overline{\text{Control OUT}}$

A zero in bit two activates the Control $\overline{\text{OUT}}$ pin of J1. This bit is provided for testing and is normally set to one.

D1 $\overline{\text{Side Select}}$

A zero in bit one selects the opposite side (side 1) of the currently selected diskette. A one in bit one selects the normal side of the diskette (side 0). This bit should be switched in accordance with the head select delays of the drive used.

D0 Not assigned

05 IN Not Connected:

Addressing this port causes no response from the 16FDC. This address is available for use by other parts of the computer system.

05 OUT TIMER 1:

This register contains the count used to start Timer 1. This count is decremented by 1 every 64 microseconds after initial loading. When the count reaches zero, bit 0 of the interrupt request register is set and the timer disabled. Since the maximum count is 255, the longest interval is 255x64 microseconds = 16.32 milliseconds. Accuracy is plus 0 and minus 64 microseconds. Loading a count of zero causes an immediate interrupt request to the interrupt request register. Loading a new count while the timer is counting reinitializes the timer without an interrupt request. If HBD is high in the command register, the timers will count eight times as fast.

06 IN Not Connected:

Same as Input 05.

06 OUT TIMER 2:

Operates in the same fashion as timer 1.

07 IN Not Connected:

Same as Input 05.

07 OUT **TIMER 3:**

Operates in the same fashion as timer 1.

08 IN **Not Connected:** Same as Input 05.

08 OUT **TIMER 4:**

Operates in the same fashion as timer 1.

09 IN **Not Connected:**

Same as Input 05.

09 OUT **TIMER 5:**

Operates in the same fashion as timer 1.

30 IN DISK STATUS:

This register's bit assignment varies according to the last command loaded into the disk command port. There are six possible assignments:

Last Command	D7	D6	D5	D4	D3	D2	D1	D0
SEEK,	Not	Write	Head	Not	CRC	TK	Index	Busy
STEP, or RESTORE	Ready	Protect	Down	Found	Error	00		
READ RECORD(S)	Not Ready	0	Record Type	Not Found	CRC Error	Lost Data	DRQ	Busy
WRITE RECORD(S)	Not Ready	Write Protect	0	Not Found	CRC Error	Lost Data	DRQ	Busy
READ ADDRESS	Not Ready	0	0	Not Found	CRC Error	Lost Data	DRQ	Busy
READ TRACk	Not Ready	0	0	0	0	Lost Data	DRQ	Busy
WRITE TRACK	Not Ready	Protect	0	0	0	Lost Data	DRQ	Busy

D7 Not Ready

A one in bit 7 indicates the drive is unable to execute the command (e.g., the door is open). This bit is an inverted copy of the signal from the currently selected drive.

D6 Write Protect

During WRITE or head moving operations, this bit is set to one if the diskette in the currently selected drive has been write protected.

D5 Head Down or Record Type or Write Fault

During head movement commands, this bit is set to one when the head is down and the setting time has elapsed.

During READ RECORD(S), a zero in this bit represents a Data Mark, a one in this bit represents a Deleted Data Mark.

During WRITE operations, this bit is a copy of the WRITE FAULT signal from the currently selected drive.

This bit is reset after being read.

D4 Not Found

A high in bit 4 indicates the desired track and/or sector were not verified. During READ ADDRESS, a high in bit 4 indicates no sector address field was encountered. This bit is cleared after the status register is read.

D3 CRC Error

A high in bit 3 indicates the internal CRC check did not agree with the diskette's CRC bytes. If bit 4 is set, the CRC error occurred in an address field; otherwise, it indicates an error in a data field.

D2 Track 00 or Lost Data

During head movement commands, a one in bit 2 indicates the head is positioned over TRACK 00 (farthest from the center). This signal is a copy of TK00 from the currently selected drive.

During data transfer commands, a one in bit 2 indicates that the computer did not respond to DRQ within one byte time. LOST DATA is cleared after being read.

D1 Index or DRQ

During head movement commands, a one in bit 1 indicates that the diskette in the currently selected drive is passing the INDEX or beginning of the track. This bit is a copy of IP from the drive.

During READ commands, a high in bit 2 indicates the 16FDC has a data byte from the disk ready to be read at port 33H. This bit is reset after being read.

During WRITE commands, a high in bit 2 indicates the 16FDC needs a data byte from the computer at port 33H.

This bit is reset after it is written.

D0 Busy

A high in bit 0 indicates the 16FDC is executing a disk command and cannot accept a new disk command yet (except a FORCE INTERRUPT command; see description of FORCE INTERRUPT).

30 OUT DISK COMMAND REGISTER:

The bit assignment varies with each command, therefore, each command will be discussed separately. A summary of the commands and bit assignments follow.

Command	D7	D6	D5	D4	D3	D2	D1	D0
RESTORE	0	0	0	0	1	v	r1	r0
SEEK	0	0	0	1	1	v	r1	r0
STEP	0	0	1	u	1	v	r1	r0
STEP IN	0	1	0	u	1	v	r1	r0
STEP OUT	0	1	1	u	1	v	r1	r0
READ RECORD(S)	1	0	0	m	s	E	c	0
WRITE RECORD(S)	1	0	1	m	s	E	c	a0
READ ADDRESS	1	1	0	0	0	1	0	0
READ TRACK	1	1	1	0	0	1	0	0
WRITE TRACK	1	1	1	1	0	1	0	0
FORCE INTERRUPT	1	1	0	1	I3	I2	I1	I0

Flags	=1	=0
v	Verify on last track	No verify
u	Update track register	No update
m	Multiple records	Single record
s	Compare for side 1	Compare for side 0
c	Enable side compare	Disable side compare
E	Enable head load delay	Assume head is down

Fields	=0	=1	=2	=3
r1r0	3 ms 6 ms	6 ms 12 ms	10 ms 20 ms	15 ms (8" Stepping Rate) 30 ms (5" Stepping Rate)
a0	FB(DATA MARK)	F8(DELETED DATA)		

INTERRUPT CONDITIONS	I3=1 IMMED-IATE	I2=1 INDEX	I1=1 WHEN NOT READY	I0=1 WHEN READY

COMMAND	DESCRIPTION
RESTORE	Upon receipt of this command, the Track 00 (TR00) input is sampled. If TR00 is active indicating the Read/Write head is positioned over track 0, the Track Register is loaded with zeroes and EOJ is set. If TR00 is not active stepping pulses are issued until the TR00 input is activated. At this time, the Track Register is loaded with zeroes and EOJ is set. If the TR00 input does not go active after 255 stepping pulses, the 16FDC terminates operation, sets EOJ, and sets the Not Found status bit. Note that the RESTORE command is executed after a RESET. A verification operation takes place if the V flag is set.
SEEK	This command assumes that the Track Register contains the track number of the current position of the Read Write head and the Data Register contains the desired track number. The 16FDC will update the Track Register and issue stepping pulses in the appropriate direction until the contents of the Track Register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. EOJ is set at the completion of the command.
STEP	Upon receipt of this command, the 16FDC issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the u flag is on, the Track Register is updated. EOJ is set at the completion of the command.
STEP IN	Upon receipt of this command, the 16FDC issues one stepping pulse in the direction towards the center of the diskette. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. EOJ is set at the completion of the command.
STEP OUT	Upon receipt of this command, the 16FDC issues one stepping pulse in the direction towards track 0. If the u flag is on, the Track Register is decremented by one. After a delay

determined by the r1r0 field, a verification takes place if the V flag is on. EOJ is set at the completion of the command.

These five commands have an optional verification flag. During verification, the first encountered ID field is read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, EOJ is set, and the BUSY status bit is reset. If there is not a match but there is a valid ID CRC, EOJ is set, the Not Found status bit (Status bit 4) is set, and the BUSY status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the disk, the 16FDC terminates the operation, sets EOJ, and sets the Not Found bit in the status register.

The STEP, STEP-IN, and STEP-OUT commands contain an UPDATE flag (u). When u = 1, the Track Register is updated by one for each step. When u = 0, the Track Register is not updated.

READ RECORD(S)

Upon receipt of the Read command the head is loaded and the BUSY status bit is set. When an ID field is encountered that has the correct side number (if side compare is enabled, s=1), correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 28 bytes of the correct field; if not, the Not Found status bit is set and the operation is terminated. When the first character or byte of the data field has been shifted, DRQ is generated. When the next byte is accumulated, another DRQ is generated. If the computer has not read the previous contents of the Data Register before a new character is transferred, that character is lost and the Lost Data status bit is set. This sequence continues until the complete data field has been input to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data

field is recorded in the Status Register (Bit 5) as shown below:

Status Bit 5	Data AM (HEX)
0	Data Mark
1	Deleted Data Mark

WRITE RECORD(S)

Upon receipt of the Write command, the head is loaded and the BUSY status bit is set. When an ID field is encountered that has the correct side number (if the side compare is enabled, s=1), the correct track number, correct sector number, and correct CRC, a DRQ is generated. The 16FDC counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the Data Register has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If this DRQ has been serviced, six bytes of zeroes in single density and 12 bytes in double density are written on the disk. The Data Address Mark is then written on the disk as determined by the a0 field of the Write Record(s) command as shown below. Refer to the Disk Command Register for additional information.

a0	DATA MARK (HEX)
0	Data Mark
1	Deleted Data Mark

The 16FDC then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing, the Lost Data Status Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte gap of logic ones.

The two commands which READ RECORD(S) and WRITE RECORD(S) determine the sector size by examining the Sector Length byte in the ID field. The numbers of bytes in the data field (sector) is then 128 x 2^n where n=0,1,2,3.

Sector Length Field (hex)	Number of bytes in sector (decimal)
00	128
01	256
02	512
03	1024

These two commands also contain a flag ,m, which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and EOJ is set at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The 16FDC will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track. At this point the NOT FOUND bit and EOJ are set.

READ ADDRESS

Upon receipt of the Read Address command, head is loaded and the BUSY status bit is set. The next encountered ID field is then read in from the disk and the six data bytes of the ID field are assembled. DRQ is generated for each byte. The six bytes of the ID field are:

	TRACK ADDR	SIDE NUMBER	SECTOR ADDR	SECTOR LENGTH	CRC 1	CRC 2
Byte	1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the 16FDC checks for validity and the CRC error status bit is set if there is a CRC error. The Sector Address of the ID field is written into the sector register. At the end of the operation, EOJ is set and the BUSY status bit is reset.

READ TRACK

Upon receipt of the Read Track command, the head is loaded and the BUSY status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled, it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. The accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, EOJ is set.

WRITE TRACK

Upon receipt of the Write Track command, the head is loaded and the BUSY status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse at which time EOJ is set. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the Data Register has not been loaded by the time the index pulse is encountered, the operation is terminated making the device Not Busy, the Lost Data status bit is set, and EOJ is set. If a byte is not present in the Data Register when needed, a byte of zeroes is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be written in single density, or by F5 in double density.

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	FD179X INTERPRETATION IN FM (DDEN\=1)	FD1791/3 INTERPRETATION IN MFM (DDEN\=0)
00 thru F4	Write 00 thru F4 with Clk=FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, clk=C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk=D7	Write FC in MFM
FD	Write FD with Clk=FF	Write FD in MFM
FE	Write FE, Clk=C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk=FF	Write FF in MFM

*Missing clock transition between bits 4 and 5
**Missing clock transition between bits 3 and 4

Note that one F7 pattern generates 2 CRC characters.

FORCE INTERRUPT

The command can be loaded into the command register at any time. If there is a current command under execution (BUSY status bit set), the command will be terminated and EOJ will be set when the condition specified in the I0 through I3 field is detected. The interrupt conditions are shown below:

I0 = Not-Ready-To-Ready Transition
I1 = Ready-To-Not-Ready Transition
I2 = Every Index Pulse
I3 = Immediate Interrupt

If I3 - I0 = 0, the command will be terminated but EOJ will not be set. The FORCE INTERRUPT commands above must be cleared in this manner before the 16FDC is given its next command.

31 IN/OUT TRACK REGISTER:

This register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. This register should not be loaded when the 16FDC is busy.

32 IN/OUT SECTOR REGISTER:

This register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. This register should not be loaded when the device is busy.

33 IN/OUT DATA REGISTER:

This register is used as a holding register during Disk Read and Write operations. In Disk Read operations, the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations, information is transferred in parallel from the Data Register to the Data Shift Register.

In Seek operations the desired track number is output to the Data Register.

34 IN DISK FLAGS:

This port provides four signals.

D7 DRQ
D6 $\overline{\text{BOOT}}$
D5 HEADLOAD
D4 $\overline{\text{INHIBIT INIT}}$

D3 MOTOR ON
D2 MOTOR TIMEOUT
D1 AUTOWAIT TIMEOUT
D0 EOJ

D7 Data Request (DRQ)

A high in bit 7 indicates the 16FDC has a byte from the disk or needs a byte for the disk according to the current operation.

D6 $\overline{\text{Boot}}$

A low in bit 6 indicates that SW3 is set to $\overline{\text{BOOT}}$. A high in bit 6 indicates SW3 is set to MON.

D5 Headload

A one in bit 5 indicates the 1793 is requesting the head to load. A zero in bit 5 indicates the 1793 is not asking the head to load.

D4 $\overline{\text{Inhibit Init}}$

A zero in bit 4 indicates that switch 4, $\overline{\text{INHIBIT INIT}}$, is ON. A one in bit 4 indicates that switch 4 is OFF.

D3 Motor On

A one in bit three indicates that the 16FDC is requesting the drive motors to turn on. A zero in bit three indicates that the 16FDC is no longer requesting the drive motors to turn.

D2 Motor Timeout

A one in bit 2 indicates that the motors have been turned off. The motors will turn off about 8 seconds after the last disk operation. A zero in bit 2 indicates the motors have not been turned off.

D1 Autowait Timeout

A one in bit 1 indicates that the autowait circuit has been turned off by the timer. This will occur about 4 seconds after autowait is turned on. A zero in bit 1 indicates that the autowait circuit has not timed out.

D0 End of Job (EOJ)

A one in bit 0 indicates the command has finished (end of job).

34 OUT DISK CONTROL:

D7 AUTO WAIT
D6 DOUBLE DENSITY
D5 MOTOR ON
D4 MAXI

D3 DS4
D2 DS3
D1 DS2
D0 DS1

D7 Auto Wait

A one in bit seven puts the 16FDC into Auto Wait mode which means that subsequent reading of Input port 34H will hold the CPU in a WAIT state until one of four things happen:

1. The 16FDC issues a DRQ (this is the normal use of the AUTO WAIT).

2. The 16FDC issues EOJ - this terminates the AUTO WAIT condition (the normal method of termination).

3. There is a hardware RESET.

4. The Autowait timer goes off (abnormal termination).

D6 Double Density

A one in bit six conditions the 16FDC to Read/Write/Format double density diskettes. A zero in bit six conditions the 16FDC for single density.

D5 Motor On

A one in bit 5 activates the motor-on signal to **all** disk drives and resets the motor timer. A zero in bit 5 deactivates the motor-on signal to all disk drives. The timer deactivates the motors automatically after about 8 seconds. This bit must be set to 1 to access the disk.

This bit is set by RESET.

D4 Maxi

A one in bit 4 conditions the 16FDC for an 8 inch disk drive (Maxi). A zero in bit 4 conditions the 16FDC for a 5 inch disk drive (Mini).

This bit is set by RESET.

D3-D0 Drive Select

A high in bits 3 through 0 selects the corresponding disk drive for all further operations. Only one drive should be selected at a given time.

RESET deselects all drives.

40 OUT BANK SELECT:

Outputting any byte to port 40H will disable the 4K ROM on the 16FDC if SW2 is on. The ROM may be reenabled by RESET.

Chapter 4

INTERFACE CHARACTERISTICS

The 16FDC appears on the S-100 bus as a 4K memory card and 15 I/O ports. The 16FDC is capable of generating interrupts and responding on a prioritized basis to the interrupt acknowledge cycle. Data exchange for the disk and serial I/O is programmed, not via direct memory access (DMA). This requires a minimum CPU speed of 4MHz and no memory wait states (at 4MHz) in the buffer memory.

The Bootstrap/Monitor ROM is addressed at C000-CFFFH. This address may be changed by cutting traces and inserting jumpers. Hold Acknowledge will temporarily disable the ROM. At 4MHz, the 16FDC inserts one wait state. There are no wait states at 2MHz. When switch one is on, the ROM is defeated and the 16FDC occupies no address space in memory. When switch 2 is on, the ROM is disabled as soon as a byte (any byte) is written to output port 40H, the bank select port. The ROM is reenabled by a hardware RESET.

The serial I/O channel requires 10 I/O addresses. CDOS requires these to start at I/O address 00, the way the 16FDC is shipped. The serial I/O channel is asynchronous because it uses the onboard clock. When one of the serial I/O channel's ports is addressed by the CPU, the 16FDC pulls down PRDY and holds it down until the 16FDC synchronizes with the CPU (up to 1 usec.)

The disk I/O ports are synchronous. CDOS assumes a base address of 30H. There are two cases in which the 16FDC will create wait states for the disk I/O ports:

1. if the ports 30-33H are read at 4 mHz there will be one wait state added for the FD1793 data to stabilize, or

2. if the Auto Wait mode has been selected an indefinite number of waits will be added to read or write operations on port 34H.

The CPU will stay in a WAIT state until the 16FDC issues a Data Request or an End of Job signal (or there is a hardware RESET).

SERIAL CHANNEL - INTERFACE CHARACTERISTICS

The 16FDC provides both RS-232 and 20 mA current loop interface. For RS-232 connect three wires from your terminal as follows:

16FDC J4	RS-232 terminal (e.g., CRT)
pin 7	**Signal** ground (not chassis)
pin 3	Receiver data (for display)
pin 2	Transmitter data (keyboard)

Some terminals may require additional modem control signals. With the Cromemco 3100, 3101, and 3102 the three signals given above are the only connections necessary. With other terminals, the 16FDC will provide primitive modem control signals in the usual location. Note that the 16FDC is acting as the data communications equipment (modem). The following signals will be held continuously in the on condition.

16FDC J4	RS-232 terminal
pin 5	clear to send
pin 6	data set ready
pin 8	data carrier detect

For 20 ma. teletype interface, solder jumpers into the four locations provided below J4. Make the following connections:

16FDC J4	ASR33 Terminal Strip "BL"*
pin 25	terminal 6(printer current out)
pin 24	terminal 3(keyboard current out)
pin 23	terminal 7(printer current in)
pin 17	terminal 4(keyboard current in)

*Caution: 120 VAC is also present on terminal strip **BL** at terminals **1** and **2.**

8" AND 5" DISK DRIVE - INTERFACE CHARACTERISTICS

The 16FDC drives J2 and J3, the Disk Drive Signal Cable Connectors, in parallel through separate sets of TTL bus drivers. The Signal cables should be terminated (150 ohm resistors to +5 volts) at the end of the cable only. If more than one disk drive **per cable** is used, only the last drive on the cable should use pull-ups. Signals from the drives back to the controller are terminated on the 16FDC with 150 ohm pullups.

OUTPUTS FROM THE 16FDC: (All active low)

$\overline{\text{DS1}}$
$\overline{\text{DS2}}$
$\overline{\text{DS3}}$
$\overline{\text{DS4}}$

These are four drive select signals. When a drive select signal is active the selected drive should enable its data and status drivers and load the read/write head.

All other drives should ignore signals until selected. When DRIVE SELECT is first asserted, the 16FDC waits a fixed amount of time for the head to LOAD before reading or writing the diskette. This time delay is 48 ms for 8" drives and 72 ms for 5" drives.

$\overline{\text{STEP}}$

This line goes active low for 16 microseconds to move the head of the selected drive in the direction specified by output DIRC. For multiple steps, the stepping rate is determined by the format of the command given to the 16FDC and will be 3, 6, 10, or 15 milliseconds per step for large floppies (except voice coil types like the PerSci 277 or 299B, in which case it is about 400 microseconds per step) or 6, 12, 20, or 30 milliseconds per step for small floppies. The 16FDC will wait one stepping period after the last step for the head to settle before attempting to read or write the diskette.

$\overline{\text{DIRC}}$

When this line is asserted (low) pulses on the STEP line should cause the head of the selected drive to advance one track per step towards the center of the diskette. If $\overline{\text{DIRC}}$ is high, pulses on the $\overline{\text{STEP}}$ line should cause the head of the selected drive to retreat on track per step towards the outer edge of the diskette (towards Track 00).

$\overline{\text{MOTOR ON}}$ This signal turns on the motors of all drives when low. When it is high it turns off the motors of all drives which are so equipped.

$\overline{\text{WRITE GATE}}$
This signal goes low to enable diskette write operations.

$\overline{\text{WRITE DATA}}$
This signal contains the intermingled clock and data pulses to be written on the diskette. Pulse width is 500 nanoseconds for 8" drives, 1 microsecond for 5" drives.

$\overline{\text{RESTORE}}$ This signal requests the head of the selected drive to return to TRACK 00.

$\overline{\text{EJECT}}$ This signal requests the currently selected PerSci 277 or 299B to eject its diskette.

INPUTS TO THE 16FDC

$\overline{\text{INDEX}}$ This line should go low for at least 10 useconds once per revolution of the diskette.

$\overline{\text{TRACK 00}}$ This signal should go low and stay low while the selected drive is on track 00, the outermost track.

$\overline{\text{READY}}$ This signal should be low when the disk drive is operable (i.e. door is closed, motor speed up, etc.) The 16FDC will always initiate a command regardless of the state of ready; the purpose of the signal is for detecting disk change operations using the Force Interrupt command.

$\overline{\text{WRITE PROTECT}}$
This signal goes low if a write protected diskette is in the currently selected drive.

$\overline{\text{READ DATA}}$
This signal is composite clock and data pulses from the disk drive. The line should go low for 1 microsecond for each flux reversal on the surface of the diskette.

SEEK COMPLETE

This signal should go low when the voice coil drive has positioned the read/write head over the desired track. This signal is gated with drive select and applies only to voice coil drives like the Persci 277 or 299B.

Chapter 5

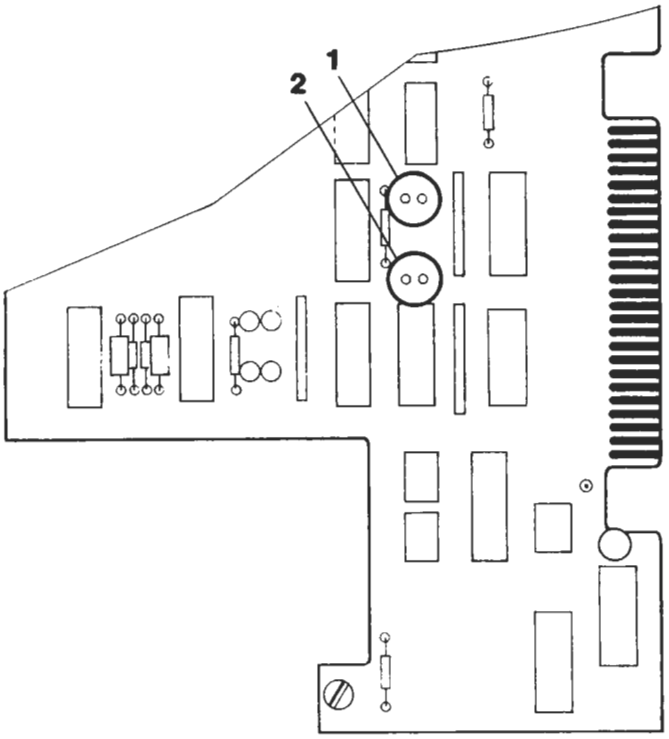
INITIAL SETUP

PERSCI 299B

Connect DC power to J3 on the 299B drive. Connect the 50 pin cable from J2 on the 16FDC to P1 on the 299B.

Assign drive numbers to the 299B by wiring the jumper in block C on the drive electronics PCB as indicated in the following diagram.

If the system uses two model 277 or 299B drives, the termination pack U1 should be removed from the drive electrically closer to the 16FDC on the 50 pin cable J2.



299B SETUP: 1=C/D, 2=A/B

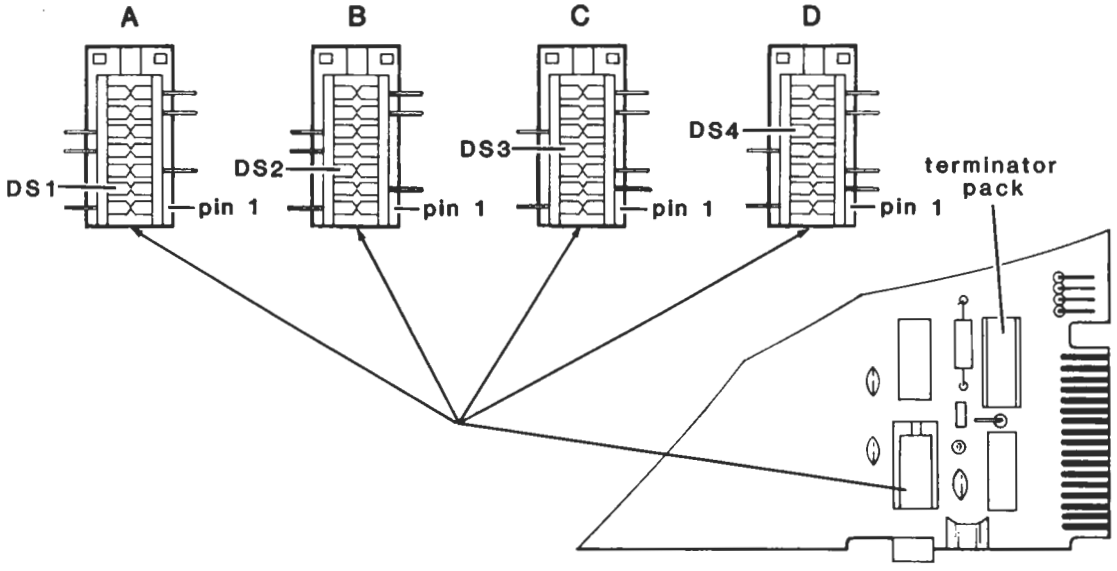
TANDON TM100

Locate the package of jumper straps (shunt 1E) just above the pc board edge connector. The jumper positions used for drive select are:

drive a - jumper pin 2 to 15 only
drive b - jumper pin 3 to 14 only
drive c - jumper pin 4 to 13 only
drive d - jumper pin 5 to 12 only

In older drives, it may be necessary to jumper from the land labelled 6 beside the 34 pin connector J1 to the land beside TP5. This provides continuity for the drive select signal for drive d, which enables it to be jumpered through the shunt at pins 5 and 12.

Cromemco recommends that only the drive select required be enabled and that all other connections **not** be jumpered. In a system with more than one small drive, remove the terminator packs from all but one of them. The drive with a terminator pack should be the one at the end of the interface cable. The drawing below shows the location of the terminator pack next to the edge connector.



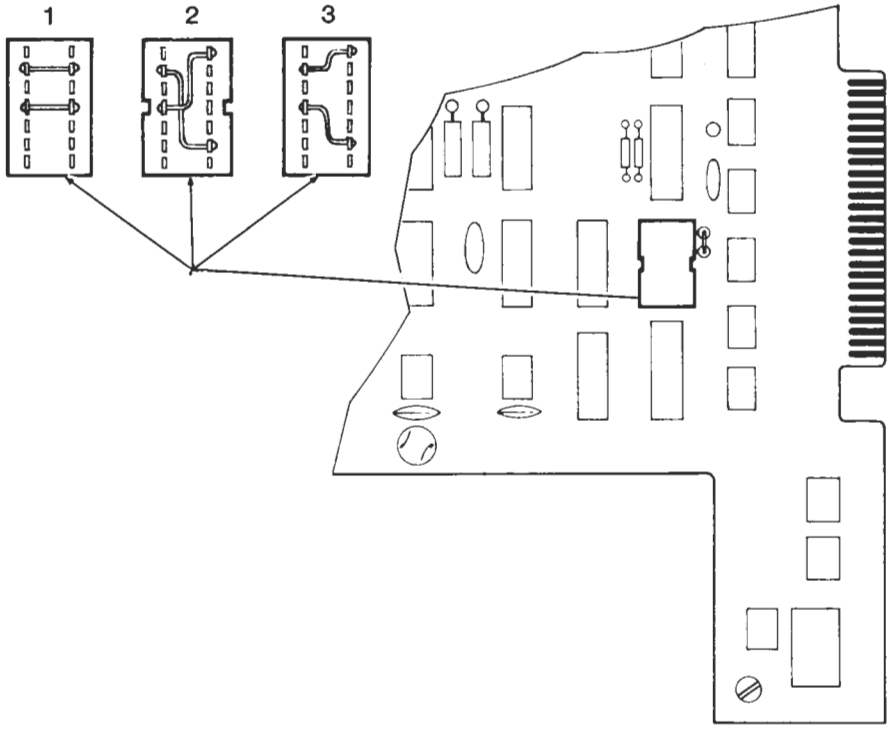
TM100 SETUP

PERSCI 277

Note that the PerSci Model 277 drive is not specified for double density operation. Connect DC power to J3 on the PerSci drive. Connect the 50 pin cable from J2 on the 16FDC to P1 on the PerSci.

Assign drive numbers to the PerSci 277 by wiring the 14 pin jumper inserted in U11 on the PerSci 277. See the following diagram. Jumper setup number 1 will cause the left side of the 277 to be drive A and the right side to be drive B. Jumper setup 3 will cause the left side of the 277 to be drive C and the right side to be drive D. This will work properly with the 16FDC or the newer 4FDC boards.

Notice that jumper setup number 3 is the opposite of the way that 277 drives were previously shipped as C/D drives. This change was caused by the redefinition of the signals coming from the drive through the 50 pin connector J2. This change was made for the 299B drives. The old connector setup will work. However, drive C and drive D will be reversed. The old style C/D jumper setup is number 2 in the diagram.



277 JUMPERS: 1=A/B, 2=C/D(OLD TYPE), 3=C/D

WANGCO 82

Cut the jumper wire on the PC board of the Wangco Model 82 labelled "MUX" (just above J4, the big blade connector in back).

Locate the package of jumper straps just above the PC board edge connector. The jumper positions, labelled "DS1", "DS2", "DS3", select DRIVE A, DRIVE B, or DRIVE C respectively. Cut the 2 jumpers that don't apply to your configuration (or simply bend out the pins on the jumper pack so they don't contact the socket). The 5 remaining jumpers connect line terminating resistors. For single drive setups, these jumpers are left intact. For 2 or more drives, the jumpers are left intact on the drive at the end of the control cable only; the other drives have these jumpers cut (or bent) out.

Finally, locate the spade lug ground on the rear chassis with a white wire under it. Remove the spade lug, disconnect the white wire, and replace the spade lug. Tape the white wire (or cut it off); it is no longer needed. This isolates chassis ground from logic ground.

When using the Wangco model 82 disk drive with the Cromemco model 16FDC disk controller the **MUX** strap must be disconnected. The frame ground strap must remain connected if the disk drive is a model WFD (stand alone). It must be cut only if the disk drive is used in a Z-2D system.

Chapter 6

THEORY OF OPERATION

POWER SUPPLIES

The unregulated bus power lines are converted to regulated supplies of +5, -5, and +12 volts by ICs 45, 18, and 33 respectively. The 16FDC requires 1.0 A at +8 unregulated, 0.100 A at +18 unregulated, and 0.100 A at -18 unregulated.

ADDRESS DECODE

The 16FDC decodes address and status signals on the bus to find the following conditions:

1. Memory read cycles in the address range C000-CFFFH,
2. Input/Output references in the address range 00-09,
3. Input/Output references in the address range 30-34H, and
4. Output references to port 40H.

In case 1, IC47P9 will go low, enabling the 4K prom IC25.

In case 2, the address decoding is done in two stages. First, the base address is decoded by IC37, then the offset is determined by IC36. Pin 9 of IC37 goes low for addresses in the range of 00-09H.

In case 3, IC37P14 goes low when the address base 30-34H is detected. Input or output references to port 34H are signalled by a low level at IC37P12 and IC37P13, respectively.

In case 4, IC37P8 goes low for address 40H.

DATA BUS

The 16FDC has a three state, bi-directional internal data bus. It is coupled to the Data In and Data Out buses on the S-100 bus through latch ICs 49 and 51. There are four cases of operation determined by the particular 16FDC function being addressed.

Case 1, Memory Read: When IC47P9 goes low selecting the RDOS-II ROM, data is presented to multiplexer IC50. The select pin IC50P1 is held high by a signal from IC36, so data passes straight through the multiplexer. Eight bits of data now are presented to the latch IC51. The gate of the latch, IC51P11, is held high by IC53P12 as long as the ROM is enabled, so data passes through the latch. The three-state output drivers of the latch are enabled during PDBIN.

Case 2, Input/Output references in the range 00-09H: When the TMS5501 IC27 is addressed, the 16FDC emulates an 8080 I/O cycle (M3). This is necessary to generate strobed status bits and to insure the correct read/write timing. The cycle begins when IC36P5 goes low presenting a high to the JK inputs of the first section of IC31. This section of IC31 is clocked by the falling edge of internal phase 2 and shifts a high level to IC31P5. This high level generates an internal SYNC pulse at IC42P13. This internal SYNC pulse enables status strobe drivers IC35P6 and IC35P3 (Write Output and Interrupt Acknowledge respectively), disables the incoming bus drivers and triggers the SYNC pin of the TMS5501. SYNC is terminated by the rising edge of phase 2 which clocks the next section of IC31 and presents a high level at IC31P12. During this period, the TMS5501 internally arranges data paths while the 16FDC idles. When phase 2 falls again, IC53P8 goes low which opens the gate of the output latch IC51 admitting the data from the TMS5501. Multiplexer IC50 passes the data straight through **except** when the 16FDC is in the process of reading the serial status port (Input port 00). In this case, IC36P7 goes low causing the multiplexer to switch D7 and D6 with D4 and D3 (producing the status bit assignment detailed in Chapter 3). The cycle finally terminates when phase 2 rises again shifting a high level to IC31P16.

Case 3, Input/Output references to ports 30-34H: During output cycles, data from the processor is latched into IC49 by $\overline{\text{PWR}}$. During input cycles, latch IC52 is read during PDBIN.

Case 4, Output reference to port 40H: Although the data bus is not examined by the 16FDC during bank select, the

data on the S-100 DO bus is latched into IC49 anyway.

WAIT STATE GENERATOR

The wait state generator, IC8P7, passes on wait requests when enabled by IC22. There are three enabling conditions:

1. 4MHz ROM access,
2. Disk references with Auto Wait mode selected, and
3. Any reference to the TMS5501 (ports 00-09).

There are three sources of wait request:

1. PSYNC,
2. Ready from wait IC20P12, and
3. Ready from TMS5501 (IC20P10).

The coincidence of an enabling condition and a wait request stops the processor in mid cycle.

CLOCKS

The 16FDC has an 8.000 MHz on board crystal clock which controls all internal board timing. IC29 conditions the clock for the TMS5501 and FD1793. 2MHz phase 1 and phase 2 signals are generated at IC41P3 and IC30P4 respectively. A 1MHz timing signal is generated IC29P15 and a switchable 2 or 1MHz clock is generated at IC29P16 (controlled by the maxi/mini signal at IC41P13).

BANK SELECT

The onboard ROM may be disabled through output port 40H if switch 2 (RES) is on. In this case, the ROM is deselected permanently after the first output to port 40H clocks flip-flop IC19 and forces IC19P5 low. This forces the memory address decoder IC47P9 high, deselecting the ROM. The ROM may be reenabled by a hardware RESET signal which sets IC19P5 high again.

TMS5501 INTERFACES

IC12 requires 12 volt clock levels at the phase 1 and phase 2 inputs. These are supplied by active pullups Q7 and Q8 which when triggered by a falling edge at the input edge at the input of open collector inverter package IC15 switch on briefly to pull the inverter outputs up to 12 volts.

The serial output IC27P40 is inverted and shifted from TTL levels to ±12 volts by IC16. IC15P12 provides an open collector current sink for current loops.

The serial input IC27P5 is controlled by IC17P3.

FD1793-1 INTERFACES

All signals from the drives are TTL buffered and have 150 ohm pullups. Maxi and mini signals are wire-anded at the pullup side of the buffers. READY is disabled and pulled high when the mini is selected.

Signals to the drives from the 1793 are TTL buffered with separate buffers for mini and maxi connectors. The HLD (head load) output does not go directly to the drives but rather enables the drive select lines through IC9P1. Thus, the actual drive select signal to the drive is the coincidence of a latched drive selection (done at port 34H) and HLD from the 1793. Head loading time is determined by counters IC43 and 55. Timeout is controlled by the count loaded into IC55.

Signals DRQ, HLD, and INTRQ (or EOJ) are available at input port 34H (IC28). Various control signals are assigned to output port 34H and are latched by ICs 10 and 4.

PRIORITY CHAIN

The 16FDC includes a ripple priority circuit which will defeat the interrupt acknowledge cycle if $\overline{\text{Priority IN}}$ is held low. If the 16FDC is allowed to perform the interrupt acknowledge, it will pull down its $\overline{\text{Priority Out}}$ line to signal others in the chain not to respond. This chain is compatible with the Cromemco TU-ART.

AUTO WAIT

An output to port 34 clocks D7 into IC4P2. When the auto wait is turned on, a read of port 34 will force IC22P6 high which puts the system into an extended wait state.

The wait state can end for one of four reasons. IC4P5 can be forced low by a system reset or by an interrupt request from the 1793. The Data Request output from the 1793 can raise IC22P5 forcing IC22P6 low. The auto wait timeout can pull IC22P2 high.

When the Auto wait is turned off shift register IC7 is held clear by IC4P5. Turning auto wait on permits IC7 to clock a one from the serial input to the last parallel output. It clocks approximately twice per second so after 8 clock cycles or four seconds, IC7 P13 goes high forcing IC22P6 low to end the wait state.

MOTOR TIMER

IC6 is an eight stage parallel load shift register clocking every four seconds. An output to port 34 causes it to load asynchronously. The first five stages load with logic zero. The final three stages are loaded with Data Bit 5, the motor on bit. The final stage at IC6P9 drives the motor on line on the interface through two buffers in IC11. If IC7 is not reloaded before a logic zero clocks through to the output, the drive motors will automatically turn off. Note that this feature will only function with drivers which are designated to have their motors turned off.

PHASE LOCKED LOOP

The 16FDC uses a Phase Locked Loop (PLL) to generate a square wave **READ CLOCK** (RCLK) for the 1793-B02 disk controller IC. The IC uses RCLK to separate clock bits from data bits and to shift the internal data shift register. The signal RCLK is synchronized to the data so that the data pulses from the drive occur close to the middle of the high or low portions of the square wave. If the data rate is different from the frequency of RCLK, the PLL adjusts itself via error feedback. This allows the 16FDC to compensate for minor variations in motor speed, etc.

When the 16FDC is idling, the PLL generates a free

running RCLK which is close to the normally expected data rate. This frequency depends upon the size and density of the diskette as specified by the control bits MAXI and DDEN of port 34H. RCLK is actually generated by a divide-by-two flipflop which is clocked by the sharp spikes used to reset the PLL's sawtooth oscillator. The following table shows free running frequencies:

MAXI	DDEN	RCLK	SAWTOOTH
1	1	500 KHz 2 uSec	1 MHz 1 uSec
1	0	250 KHz 4 uSec	500 KHz 2 usec
0	1	250 KHz 4 uSec	500 KHz 2 uSec
0	0	125 KHz 8 usec	250 KHz 4 uSec

The sawtooth is formed by discharging the timing capacitor, C5, and the trimmer, C2, through current-sink transistor Q3 until the buffered sawtooth voltage is less than the reference value at pin 3 of the comparator, IC2. Then the comparator switches on, causing the output of inverter IC24P4 to go low and turn on the reset switch, transistor Q2. This resets the timing capacitor to zero charge, clocks the RCLK flip flop, and switches the comparator off to begin a new cycle.

The frequency of the free running sawtooth is controlled by the collector current of Q3. At the maximum frequency, 1 MHz, this current is set by the voltage applied to the 1.00 KOhm resistor from the emitter of Q3 to ground. The voltage is essentially the same as at the non inverting input of the opamp, IC1P5, since the base-emitter voltage drop of Q3 is compensated for by feedback to the opamp. The current flowing through the resistor is supplied by the emitter of Q3 and, assuming negligible base current, this same current flows into the collector of Q3 from the timing capacitor. Since the voltage across the 1.00 KOhm resistor is held to .6 volts by the resistive divider at IC1P5, 600 uAmps flow through Q3 when the sawtooth is running at 1 MHz.

The sawtooth frequency is lowered by reducing the current in the collector of Q3. To go from 1 MHz to 500 KHz, the collector current is reduced from 600 uAmps to 300 uAmps. The reduction occurs when current from switch IC3P10 is allowed to flow through the 1.00 KOhm resistor to ground. If 300 uAmps are supplied through the switch, Q3's emitter need supply only 300 uAmp to bring the total up to 600 uAmp (recall that the voltage across the resistor is fixed to be .6 volt by the opamp,

and this requires a total current of 600 uAmp). Thus the collector current in Q3 is reduced by the amount of current supplied through the switch.

The lowest frequency is obtained by injecting 450 uAmps through the switch, IC3P10. The current through the switch is controlled by a current source made up of an opamp and transistor, with switched resistors in the emitter of the transistor. The opamp establishes a voltage at the emitter of Q1 which is equal to the voltage at IC1P3. The current flowing out of the collector of Q1 is equal to the voltage drop across the emitter resistor (half the analog supply voltage) divided by the selected emitter resistance.

The following table shows the relationship between currents:

Total Current through R11	Q3 Collector Current	Switch Current	Sawtooth Frequency
600	600	0	1 MHz
600	300	300	500 KHz
600	150	450	250 KHz

When a signal is applied to the PLL from the disk, the voltage at the opamp, IC1P5, is adjusted in the following manner so that the sawtooth frequency matches the data rate. Each incoming data pulse fires a pulse-shortening one-shot, IC5P12, which briefly strobes the sample-and-hold switch from IC3P4 and P9 to P3 and P8. This switch stores the voltage of the sawtooth on capacitor C22 at the end of the strobe pulse. If the data frequency and phase are matched to the PLL, each pulse will occur at the middle of the sawtooth. If the data pulse occurs early, it will strobe the sawtooth at a higher voltage than normal. This higher voltage causes the voltage at pin5 of the opamp, IC1, to rise which increases the current through Q3 and speeds up the sawtooth. Conversely, if the data pulse occurs later than normal, it will lower the voltage at the opamp and slow down the sawtooth. The rate of change is controlled by the loop filter, RN1P4 to P5 and C10, and the sensitivity of the sawtooth oscillator and sample-and-hold; the rate is set for rapid lockup. The PLL has been designed for rapid and stable lockup in all modes because the natural frequency and damping factor of the control loop are independent of the sawtooth frequency.

MODE 2 INTERRUPT ACKNOWLEDGE

When the 16FDC is used with a Z-80 CPU, it may be desirable to use the interrupt structure known as **Mode 2.** In this mode, the interrupting device supplies a one byte vector, rather than an instruction, to the CPU. The vector is appended to the Interrupt page, or I register in the Z80, and the resulting 16 bit value points to a location in memory which stores a two-byte address for the interrupt service routine.

Normally, the 16FDC supplies the opcode of a restart instruction when it is responding to an Interrupt Acknowledge cycle. In mode 0 (8080 compatible mode), these opcodes, C7, CF, D7, DF, ..., F7, and FF are intepreted by the Z80 as RST 0, RST 8, and so on. In mode 2, the Z80 interprets these opcodes as vectors, as described above. For example, if the I register is set to 01 and the 16FDC supplies a vector of D7, the Z80 will read locations 01D7 and 01D8 to get the pointer to the interrupt service routine. (In mode 0 the Z80 would have executed RST 10).

Since these opcodes are odd (i.e. bit zero is a one), they are mismatched to the normal form of mode 2 vectors, which are even. Recalling that these vectors form the low byte of a memory pointer, one can see that it is possible to get the most vectors per I-page if the vectors start at 00 and work up. This is why the normal form of mode 2 vectors is even.

The 16FDC can be converted to mode 2 (even) vectors by inserting a jumper which forces bit zero of the vectors to be zero. Once this jumper is inserted, the possible Interrupt Acknowledge vectors will be C6, CE, D6, DE, ..., F6, and FE. A 16FDC that has this jumper inserted is no longer compatible with the mode 0 (8080 compatible) interrupt structure. Also, the interrupt address register will not be affected and thus will still contain the restart op codes.

REAL TIME CLOCK

The 16FDC offers a highly accurate, 512 millisecond, real time clock interrupt which may be selected as an interrupt source through a jumper wire. If selected, interrupts will be generated when the 5501 is programmed to disable Timer 5 interrupts and enable the DRQ/RTC interrupt. The mask register must also be set properly.

Appendix A

TUNING THE DATA SEPARATOR

This procedure **MUST NOT BE PERFORMED BY THE USER.** Special test equipment must be used by trained personnel to make this adjustment. There is **no way** to tune the data separator without this equipment.

This adjustment requires a frequency counter. Nothing else is accurate enough to obtain reliable double density operation at the inner tracks. Connect the probe to pin 8 of IC4, and 74LS74. Reset the system and if necessary use the escape key to abort the boot. Adjust the trimmer capacitor near IC4 at the edge of the board for a frequency of 500 ± 1 KHz.

Use a series of RDOS commands to verify the other two free running frequencies. Verify the double density small drive setting by typing:

```
O 10 34
```

Note that the first character is the letter **"O"** not the numeral zero. The remainder of this RDOS output command is made up from hexadecimal digits. After RDOS accepts the command the frequency counter should read 250 ± 5 KHz. Large drives use this frequency for single density. Now verify the small drive single density frequency with this command:

```
O 00 34
```

The frequency counter should read 125 ± 10 KHz. Finally, verify the large double density frequency with:

```
O 50 34
```

It should still be 500 KHz.

Appendix B

PARTS LIST

Part No.	Description	Qty
Resistors		
001-0002	39.00 ohm 1/4W	2
001-0008	150.00 ohm 1/4W	3
001-0009	180.00 ohm 1/4W	1
001-0012	330.00 ohm 1/4W	5
001-0013	390.00 ohm 1/4W	2
001-0014	470.00 ohm 1/4W	1
001-0015	560.00 ohm 1/4W	1
001-0016	680.00 ohm 1/4W	1
001-0018	1.00 Kohm 1/4W	8
001-0021	2.20 Kohm 1/4W	2
001-0024	4.70 Kohm 1/4W	6
001-0026	5.60 Kohm 1/4W	2
001-0030	10.00 Kohm 1/4W	8
001-0032	18.00 Kohm 1/4W	1
001-0041	3.30 Kohm 1/4W	1
001-0086	1.00 Kohm 1/4W 1%	1
001-0103	1.24 Kohm 1/4W 1%	1
001-0106	3.92 Kohm 1/4W 1%	1
001-0107	25.50 Kohm 1/4W 1%	2
001-0108	20.00 Kohm 1/4W	1
001-0113	1.00 Kohm 1/4W 5%	1
001-0115	2.00 Kohm 1/4W	1
001-0126	220.00 ohm 1/2W	1
001-0128	2.67 Kohm 1/4W 1%	1
001-0187	5.49 Kohm 1/4W 1%	1
Resistor Networks		
003-0006	560 ohm 8 pin	8
003-0013	330 ohm 8 pin	1
003-0025	10 Kohm 8 pin	1
003-0042	16 FDC PLL 6 pin	1
003-0048	150 ohm 6 pin	1

Capacitors

004-0000	47 pF MONO	3
004-0003	30 pF CRDC	2
004-0007	75 pF CRDC	3
004-0008	100 pF CRDC	1
004-0018	560 pF DISC 1000V	1
004-0022	.001 CRDC	2
004-0025	.005 100V	2
004-0032	10 TANT 20V	4
004-0034	6.8 TANT	2
004-0061	.048 50V	32
004-0062	.001 POLY CARB	1
004-0063	.300 pF MICA 5%	1
004-0067	.0033 uF POLY CARB 5%	1
004-0068	5-120	1
004-0076	6.8 TANT 15V	1
005-0000	47 pF Network 8 pin	1

Diodes

008-0006	1N5231B	1
008-0008	1N4742	1
008-0020	LED GREEN MINI TIL-211	1
008-0029	ZENER DIODE 5.1V 1% 1WATT	1
009-0001	2N3904	1
009-0002	2N3906	5
009-0023	2N3640	1
009-0024	TIS97	2
009-0026	VN10KM VFET	1

ICs

010-0028	7406	2
010-0030	7404	1
010-0032	7425	2
010-0040	74LS221	1
010-0043	74LS164	1
010-0044	74LS161	1
010-0046	74LS157	1
010-0055	74LS74	3
010-0058	74LS32	1
010-0059	74LS30	1
010-0063	74LS10	1
010-0064	74LS08	1
010-0066	74LS04	5
010-0068	74LS02	2

010-0069	74LS00	1
010-0077	75189/1489	1
010-0080	74367	1
010-0089	74S133	1
010-0091	74276	2
010-0097	74LS174	1
010-0100	74LS244	3
010-0102	74LS373	2
010-0108	74LS367	1
010-0191	8T98N	4
010-0193	74LS165	1
010-0209	8T97N	1
010-0211	75150	1
010-0213	74LS126	1
011-0004	4066	1
011-0005	5501	1
011-0011	4020	2
011-0049	FD17938-02	1
011-0051	16FDC RDOS 2.1	1
012-0000	REG 7905/32OT-5	1
012-0001	REG 7805/34OT-5	1
012-0002	REG 7812	1
012-0006	72810/TL-810CP COMPARATOR 8PIN	1
012-0028	CA3240A RCA	1
502-0003	74903	1
502-0018	74918B	1

Miscellaneous

013-0002	8 POS DIP SWITCH	1
015-0013	6-32 HEX NUT SM PAT-1/4 CAD	5
015-0020	#6 SPLIT RING LOCK WASHER-CAD	5
015-0024	NYLON SHOULDER WASHER-WHITE	1
015-0044	6-32X1/2 PAN HD SLOT SCREW-CAD	3
015-0108	6-32X1/2" NYLON PAN HD SCREW	1
015-0134	6-32X5/8 PAN HD SLOT SCREW CAD	1
015-0142	6-32 HEX NUT, TEFLON	1
017-0000	SCKT 8 PIN BURNDY 8P-11T	3
017-0001	SCKT 14 PIN BURNDY 14P-11T	23
017-0002	SCKT 16 PIN BURNDY 16P-11T	15
017-0004	SCKT 20 PIN BURNDY 20P-11T	8
017-0005	SCKT 24 PIN TI C9324-02	1
017-0006	SCKT 40 PIN BURNDY 40P-11T	2
017-0022	SCKT 26 PIN HEADERS WITH HOOD	1
017-0033	50 PIN MALE CONNECTOR	1
017-0091	SCKT 34 PIN CA CONNECTOR	1
021-0017	LG HEATSINK	1
021-0109	SIL-PAD REG.	2
026-0001	CRYSTAL 8 MHZ	1

Cromemco 16FDC™

SCHEMATIC REV. 7

BOARD REV. F1

16FDC-040-0060

THIS SCHEMATIC CONTAINS CIRCUITS COVERED BY PENDING U S PATENTS

NOTE (UNLESS OTHERWISE SPECIFIED)

1 RESISTORS ARE 1/4W. 5%

2 CAPACITOR VALUES ≥1 ARE IN PICOFARADS. VALUES <1 ARE IN MICROFARADS.