Five Dollars

Cromemco

16KZ

Random Access Memory

Instruction Manual

Cromemco®

16KZ RAM

Instruction Manual

CROMEMCO, Inc.
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This manual was produced on a Cromemco System Three computer utilizing a Cromemco HDD-22 Hard Disk Storage System running under the Cromemco Cromix™ Operating System. The text was edited with the Cromemco Cromix Screen Editor. The edited text was proofread using the Cromemco SpellMaster™ Program and then formatted using the Cromemco Word Processing System Formatter II. Final camera-ready copy was printed on a Cromemco 3355A printer.

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INTRODUCTION

The Cromemco 16KZ is a high speed 16K RAM board designed for the S-100 microcomputer bus. The 16KZ can operate at **2 MHz** or **4 MHz** system clock rates with no wait states. The **Bank Select** feature incorporated on the 16KZ allows memory space to be organized into as many as eight banks of 64 Kbytes each. The memory banks in which the 16KZ resides are selected by switches on each 16KZ board; the active banks of memory are selected under software control. The 16KZ also contains Direct Memory Access Override circuitry that allows any DMA device to access different banks of memory during DMA operations.

The 16KZ was designed prior to the development and introduction of the Cromemco Cromix Operating System. Because the Cromix software uses a type of advanced bank switching which the 16KZ cannot perform, the 16KZ board cannot be used in a Cromix system.

Chapter 1

INITIAL SWITCH AND JUMPER SETUP

LOGICAL ADDRESS BLOCK SELECT

The 16KZ RAM board may be located in any one of four 16 Kbyte blocks of memory space. The Block Select switches, labeled A14 and A15, are part of an eight position DIP switch located in the upper middle of the board. These switches control address bits A14 and A15 respectively. Setting a switch to the UP position enables the board to respond to a high logic level in that address bit. The table below summarizes the switch settings for each block.

Origin Address	End Address	A15	A14
0	3FFF	0	0
4000	7FFF	0	1
8000	BFFF	1	0
C000	FFFF	1	1

MEMORY BANK MAPPING SELECT

With the software controlled Cromemco Memory Bank Select feature, the 16KZ board may be mapped to any combination of eight levels of 64K memory space. The eight position DIP switch in the upper middle of the board controls bank selection. The legend on the board next to this switch is labeled 7 6 5 4 3 2 1 0 with each number corresponding to a bank of memory. A switch in the UP position assigns the board to the specific memory bank.

On power-up, the active memory bank is Bank 0. Only memory boards mapped to this bank are immediately active after power-up. At this point, any bank or banks may be enabled under software control by addressing I/O port 40h dedicated to this function. The eight bits output from port 40h enable or disable the corresponding bank(s) in memory. A set bit **1** in the corresponding bit position will enable the memory bank. A reset bit **0** will disable it. A light emitting diode (D1) is used to indicate when the memory board is enabled.

BOARD SELECTION

When switch section 1 on the right hand DIP switch is OFF (out), the board will not be selected when the system is brought up or when a Power On Clear (reset) is performed. This allows RDOS to reside at memory location C000h. When the RDOS boot command is executed, RDOS will be disabled and this 16KZ board will automatically be enabled. Therefore, in systems with 64K of memory, only the card addressed with the highest origin (C000h) should have switch section 1 OFF. Switch sections 2 (A15) and 3 (A14) should be ON.

DIRECT MEMORY ACCESS OVERRIDE

The Cromemco 16KZ board also features Direct Memory Access (DMA) override, a powerful hardware feature which allows memory blocks residing in different memory banks, with identical or overlapping addresses, to be accessible to DMA transfer.

Switch sections 4 and 5 in the eight position DIP switch to the right at the middle top of the board control this function.

Switch section 5, when in the UP position, enables the DMA override for the entire block. When DOWN, the DMA override is disabled. Switch section 4, when in the UP position, locks out the block of memory during DMA transfer. When in the DOWN position, the memory is accessible to DMA regardless of whether or not it resides in the currently active memory bank. The setting of switch section 4 is only relevant if switch section 5 is UP, and then only during DMA operations. Normally both switch sections 4 and 5 are left in the DOWN position.

Chapter 2

THEORY OF OPERATION

BANK SELECT LOGIC

The bank select logic circuit decodes commands sent to output port 40h by the CPU to determine if the memory bank in question should be active. If the CPU sends a logic one to any bit position for which the bank select switch is ON, the board will be enabled. Otherwise, the board will be disabled. IC16 decodes the combination for SOUT, $\overline{PWR}$, and address 40h and sends a clock pulse to the bank select circuitry. The combination of open collector inverters IC3 and 4 does an AND-OR operation to detect the correct bank state. IC28 stores the current bank status, sends it to the LED DI for indication, and controls the board enable gate IC32. The AND gates IC31 in combination with some discrete components cause the bank 0 switch setting to control the board status whenever $\overline{PRESET}$ and $\overline{POC}$ are pulsed. Thus the bank 0 switch determines the state the board comes up in whenever a RESET occurs.

DIRECT MEMORY ACCESS OVERRIDE

IC13 in conjunction with the DMA ENABLE and DMA OFF switches allows DMA operations to override the current bank selection if desired. If the DMA ENABLE switch is DOWN, then the current bank select FF state governs the board state during DMA operations. In this case, the DMA OFF switch has no effect. If the DMA ENABLE switch is UP, then the DMA OFF switch determines whether the board is enabled during DMA operations. If the DMA OFF switch is DOWN, then the memory board is enabled for DMA operations when addressed. If the DMA OFF switch is UP, the memory board is unconditionally disabled during all DMA operations.

Proper use of the DMA ENABLE and DMA OFF switches will permit DMA devices, such as video graphic display generators, to remain "in contact" with their own dedicated memory area regardless of the current memory bank selection. This prevents loss of the image when banks are switched. All memory boards in an address range where bank switching is used in conjunction with DMA ENABLE must have the DMA ENABLE switching capability to prevent bus conflicts.

BOARD ENABLE DECODE

The overall board status is decoded by IC32. Address selection uses exclusive-OR Logic gates in conjunction with two dip switch sections to select the 16K address block for which the board is active. If any of the status lines SINP, SOUT, or SINTA goes high, the board is disabled. Also, any device pulling the MDSBL bus line (pin 67) low will disable the memory board. This permits a ROM bootstrap to overlap the memory area if desired. If the bank select and other conditions are met, then output of IC32 goes low to enable the 16KZ to perform memory cycles.

CHIP ENABLE GENERATION

The 16KZ uses a direct read process for generation of the RAM chip enable signals. In general, whenever the address and other conditions are correct for addressing a particular RAM, the chip enable (CE) input will go high (+12V) if a memory cycle request occurs. This is when either MWRITE, PDBIN, or SM1 go high, or when $\overline{\text{MREQ}}$ goes low. Since the bus signals are used directly to control the CE generation, all devices sending memory cycle signals on the bus must use a format similar to the 8080 and send only signals for complete memory cycles. Short pulses or address changes while CE is high will usually cause the RAM area addressed to fail to restore the data after reading it out. The data then changes state and is lost. Direct read operation was chosen to permit the shortest possible memory access operation and thereby allow operation at 4MHz with the Cromemco ZPU without wait states.

Decoding of the bus signal combinations giving valid CE operation occurs in IC47. Address line A0 determines whether the CE pulse will occur on pin 12 (A0=0) or pin 11 (A0=1). During CPU operations, CE pulse outputs can occur only if the address enable input is low and the gating pulse input H is high. During DMA operation the gating input H is held low. In general, gating input H is used to turn off the CE pulse whenever conditions requiring it occur. IC62 combines a number of these inhibiting conditions to produce the CE gating pulse. The signals of primary importance during CPU operation are the $\overline{\text{RFSH}}$ bus signal on pin 66, and the gating FF output from IC28 pin 7. The gating FF, IC28, takes pin 7 high whenever a CE pulse is allowed. If the current CE pulse lasts more than eight cycles of 02, then the QD output of IC29 goes high. This sets IC28 and its pin 7 goes low to terminate the CE pulse. This prevents the

CE pulse length from exceeding the RAM specifications if the CPU enters a wait state during a memory cycle. The wait state situation occurs primarily during front panel single step and reset operations, but could come from a hardware item elsewhere. Also, if a refresh cycle begins, CCDSBL goes low, or PHLDA goes high, IC28 goes low to prevent CE pulses from IC47. When normal CPU operation resumes, a logic low level output from IC30 pin 10 causes IC28 to take pin 7 high again.

CHIP ENABLE CONTROL LOGIC

The chip enable pulses from IC47 go first through IC48, which stretches the trailing edges to eliminate any low going glitches which may be generated in IC47. The CE signals then go to IC49 and IC50 for selection of the block of 4K bytes to be accessed. The NOR gate IC61 turns off the CE pulse when the board is unaddressed or during a refresh cycle. IC52 inserts the refresh pulse, and IC18 and IC35 amplify the TTL signal to logic levels of 0 and +12V for the RAMs. The 75332's employ an external PNP transistor to pull their outputs up to +12V.

The CE generation and control logic divides the RAM array into 4K blocks depending on the states of A0 and A8. This permits fast DMA devices such as the Cromemco Dazzler interface to use ripple addressing with either A0 or A8 as the most rapidly changing address. Minimum access times result, with the read process occurring in a manner similar to static RAMs. In order to use this mode, all addresses and control lines must change at the same time.

RAM ARRAY

The RAM array consists of four blocks or rows of 4K x 1 RAM chips, with like bit positions bussed together. All the similar address and control lines are tied together, with the CE pulse determining which row responds. Address data comes from multiplexers IC19, IC36, and IC53. These determine whether the RAMs use the CPU bus or the refresh counter for addressing. During write operations, IC64 transmits data from the CPU DO bus to the RAM chip data pins. The 3-state output of IC64 turns ON whenever an MWRITE pulse occurs. A stretching network with IC46 prolongs the MWRITE pulse trailing edge to allow for propagation delays through the CE logic. Data entry into IC64 is enabled whenever either

$\overline{PWR}$ or PRDY are low. This allows the memory write cycle to complete after the CPU changes DO for the next advanced status.

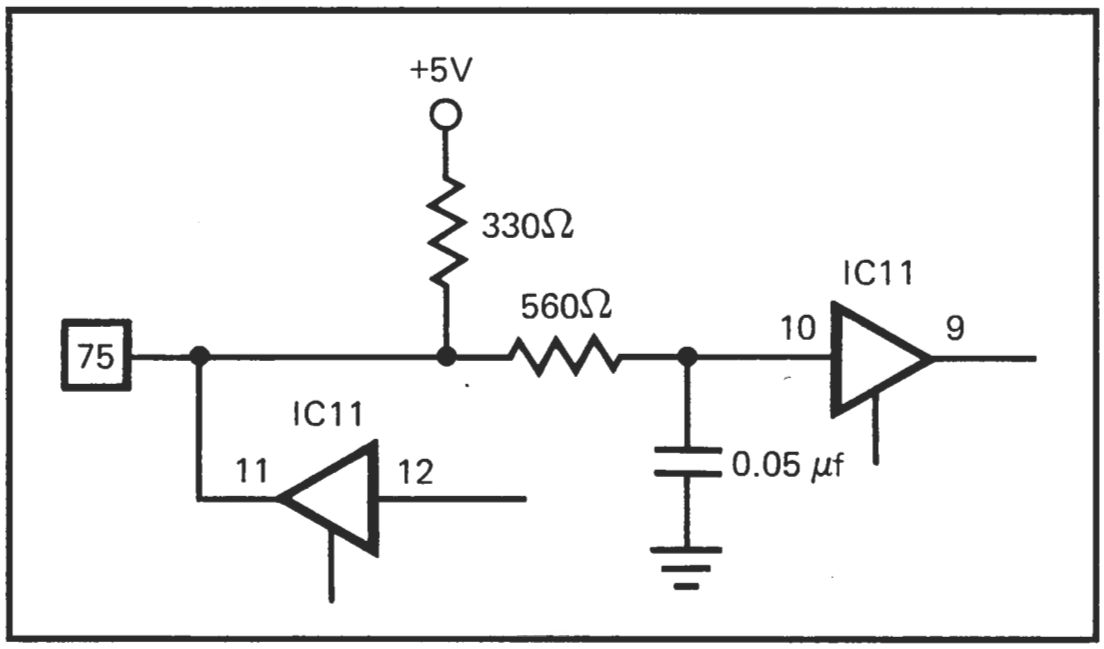
Data read out of the RAM array is latched into IC65. Thus it is available to the CPU and front panel after the memory completes its cycle. PDBIN, SMEMR, and board enable control gating of the data onto the DI bus. The latch enable signal comes from IC47 and goes high whenever the RAM array is read or written for data.

REFRESH CYCLE GENERATOR

This memory board uses an M1 refresh state process. Advantage is taken of the fact that 8080 and Z-80 CPUs use at least four clock cycles for their M1 states to fetch and decode instructions. The normal data fetch occurs during the first two clock cycles, and then memory refresh occurs during the 3rd and 4th clock cycles of M1. When a coincidence of SM1.PSYNC=1 occurs at a 02 positive going edge, IC27 pin 5 goes high to note this. One 02 cycle later, IC27 pin 9 goes high to begin a refresh sequence. During refresh, IC61 turns off any CE signals from IC47. At the first 02 negative going edge after refresh begins, IC44 pin 9 goes low to turn ON the CEs for all RAMs and refresh their data. One 02 cycle later, IC44 turns OFF, completing the refresh and incrementing the refresh address counter IC33. IC29 then turns OFF and returns the RAM to CPU control. If the RAM is used with a Z-80, IC14 uses the $\overline{RFSH}$ signal to prevent action by the CPU refresh pulse on $\overline{MREQ}$. Otherwise, some wait state conditions may cause the generation of CE glitches. When the refresh cycle begins, IC45 causes IC28 pin 7 to go low. It stays this way until the trailing edge of SM1 clocks IC44 pin 4, which causes IC30 to make IC28 pin 7 high again. IC44 clocks at the trailing edge of SM1 and PHLDA and the leading edges of MWRITE. During times when CPU operation is suspended, IC30 pin 9 goes high, causing IC29 to count. After eight cycles of 02, the CE outputs of the IC47 are disabled. After 16 cycles of 02, the CE outputs of IC47 are disabled. After 16 cycles of 02, IC29 pin 15 goes high, causing autonomous memory refresh cycles. These refresh cycles continue to occur once per 16 02 cycles until CPU operation resumes. Two sections of IC49 arbitrate between MWRITE and refresh pulses to prevent CE conflicts during front panel write operations with the CPU stopped.

RESET CIRCUITRY

The reset circuitry takes care of the special CE management problems that occur with dynamic memories using a direct read process. When the $\overline{\text{PRESET}}$ line goes low, IC13 and Q5 immediately pull down the PRDY line. This causes the CPU to halt during execution of the current memory cycle. The memory board then times out eight 02 cycles and IC28 pin 7 turns off the CE Pulse. The CPU board must have a 10 μsec delay network in series with its PRESET input. The current revision Cromemco ZPU board does have such a delay network, but older ZPU boards may need modification. In particular, ZPU REV A and ZPU REV B must have an RC network inserted in series with the reset line as shown in the schematic diagram below:



Provision of a 10 μsec delay permits the memory board to turn off before the CPU terminates the current operation.

When the $\overline{\text{PRESET}}$ line is released, IC14 produces a delay of about 50 μsec to allow for multiple switch bouncing. At the end of this time, IC13 and IC31 cause the data at memory location 0 to be read into the data latch IC65. After another 50 μsec, IC13 and Q5 release the PRDY line, allowing CPU operation to resume if in the run state. This procedure prevents the occurrence of partial memory cycles and resulting data loss caused by the reset switch bouncing.

16KZ PARTS LIST

INTEGRATED CIRCUITS		PART NO.
IC1	7812	012-0002
IC2	7805/340T-5	012-0001
IC3-4	74LS05	010-0065
IC5-12	4050/9050E	011-0002
IC13	74LS00	010-0069
IC14	74LS08	010-0064
IC15	74LS86	010-0052
IC16	74S133	010-0089
IC17	74LS158	010-0045
IC18	75322	010-0075
IC19-26	4050/9050E	011-0002
IC27	7474	010-0019
IC28	74109	010-0013
IC29	74161	010-0008
IC30	PROM 74902	502-0002
IC31	74LS08	010-0064
IC32	7430	010-0023
IC33	74393	010-0078
IC34	74LS158	010-0045
IC35	75322	010-0075
IC36-43	4050/9050E	011-0002
IC44	74109	010-0013
IC45	74LS00	010-0069
IC46	74265	010-0002
IC47	PROM 74901	502-0001
IC48	74S32	010-0090
IC49-50	74S10	010-0035
IC51	74LS158	010-0045
IC52	74S00	010-0036
IC53-60	4050/90500E	011-0002
IC61	74LS02	010-0068
IC62	74LS21	010-0060
IC63 (NON-TI)	74LS04	010-0066
IC64-65	74S373	010-0085

TRANSISTORS/DIODES		PART NO.
Q1	2N3646	009-0000
Q2-5	A5T4260	009-0020
D1	LED GRN TIL-211	008-0020
D2-7	1N914/1N4148	008-0002
D8	1N5231B	008-0006
D9	1N914/1N4148	008-0002

CAPACITORS		PART NO.
C1	.047 UF AXIAL	004-0061
C2	.001 UF DISK	004-0022
C3	.047 UF AXIAL	004-0061
C4	10 UF TANT	004-0032
C5	47 PF MONO	004-0000
C6	10 UF TANT	004-0032
C7-8	.047 UF AXIAL	004-0061
C9	22 UF TANT	004-0028
C10-37	.047 UF AXIAL	004-0061
C38	100 PF DISK	004-0008
C39-41	.047 UF AXIAL	004-0061
C42	220 PF DISK	004-0013
C43-54	.047 UF AXIAL	004-0061
C55	.001 UF DISK	004-0022
C56	47 PF DISK	004-0005
C57	100 PF DISK	004-0008
C58	10 UF TANT	004-0032
C59	6.8 UF TANT	004-0034
C60	.001 UF DISK	004-0022
C61-63	47 PF MONO	004-0000
C64-68	100 PF MONO	004-0009
C69-71	150 PF MONO	004-0010
C72-91	47 PF MONO	004-0000
C92	.047 UF AXIAL	004-0061

RESISTORS		PART NO.
R1	1 K	001-0018
R2	270	001-0011
R3-4	1 K	001-0018
R5	180	001-0009
R6	56	001-0040
R7-8	2.2 K	001-0021
R9	560	001-0015
R10-11	22	001-0001
R12	2.2 K	001-0021
R13	10 K	001-0030
R14	270	001-0011
R15	22	001-0001
R16	2.2 K	001-0021
R17	560	001-0015
R18	4.7 K	001-0024
R19	22	001-0001
R20	560	001-0015
R21	270	001-0011
R22	10	001-0000
R23	560	001-0015
R24	680	001-0067
R25-26	4.7 K	001-0024

R27	2.2 K	001-0021
R28-29	1.5 K	001-0020
R ACROSS C9	1.5 K	001-0020

RESISTOR NETWORKS		PART NO.
RN1	2.2K, 8 PIN	003-0008
RN2-4	33, 8 PIN	003-0000
RN5	270, 8 PIN	003-0003
RN6	560,8 PIN	003-0006
RN7	270, 8 PIN	003-0003
RN8	180, 8 PIN	003-0002
RN9-13	560, 8 PIN	003-0006
RN14	2.2K, 8 PIN	003-0008
RN15-16	100, 8 PIN	003-0001
RN17	1.5K, 8 PIN	003-0027

MISCELLANEOUS		PART NO.
2 EA.	SOCKETS, 20 PIN	017-0004
32 EA.	SOCKETS, 18 PIN	017-0003
10 EA.	SOCKETS, 16 PIN	017-0002
19 EA.	SOCKETS, 14 PIN	017-0001
2 EA.	SWITCH, 8 POSITION	013-0002
4 EA.	6-32X1/2 SCREW	015-0044
4 EA.	#6 LOCK WASHERS	015-0020
4 EA.	6-32 HEX NUTS	015-0013
1 EA.	LARGE HEAT SINK	021-0017
2 EA.	SILICON PADS	021-0109

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1. Your name, address and telephone number,
2. the return authorization number,
3. a description of the problem, and
4. proof of the date of retail purchase.

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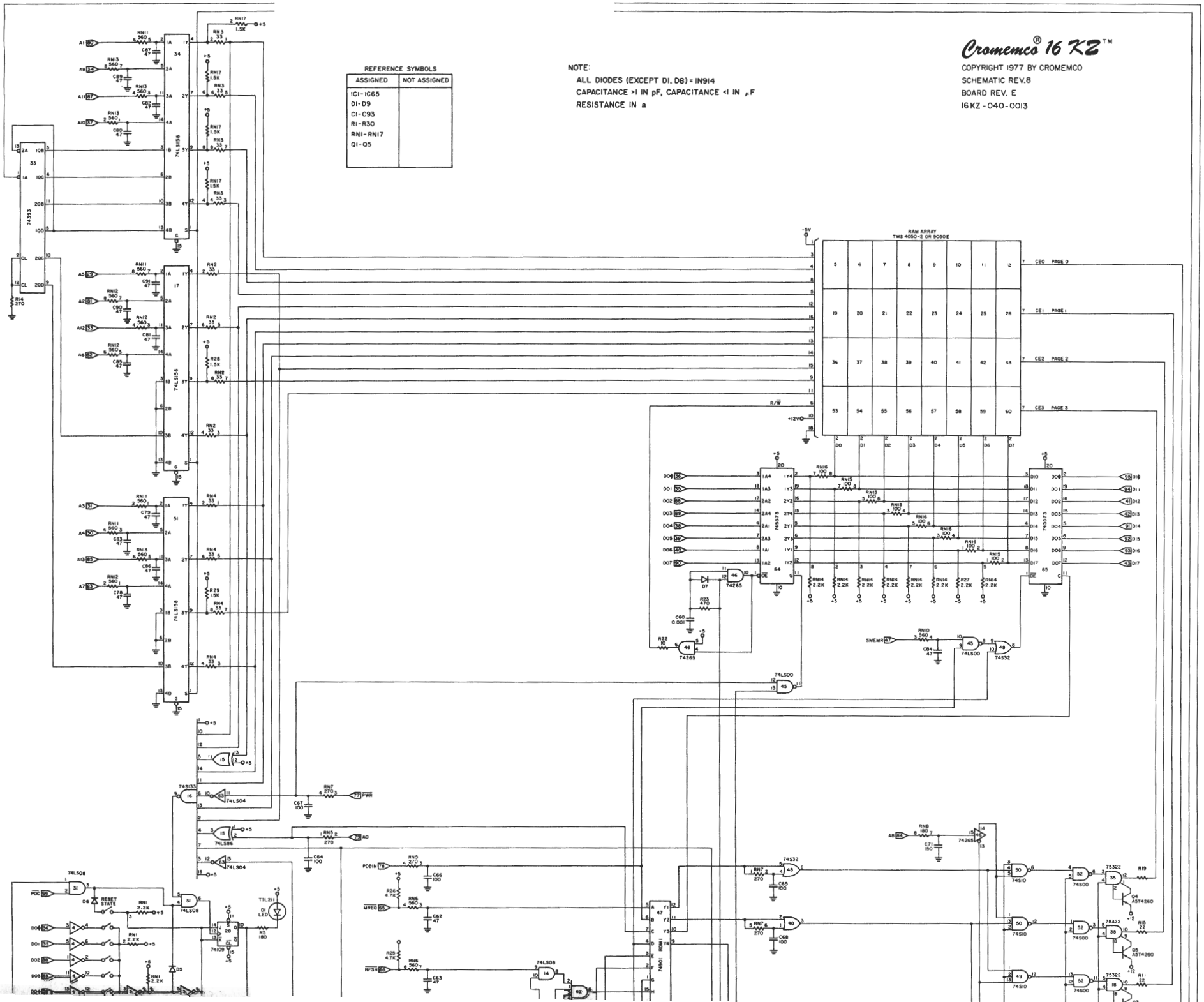
Cromemco® 16 KZ™
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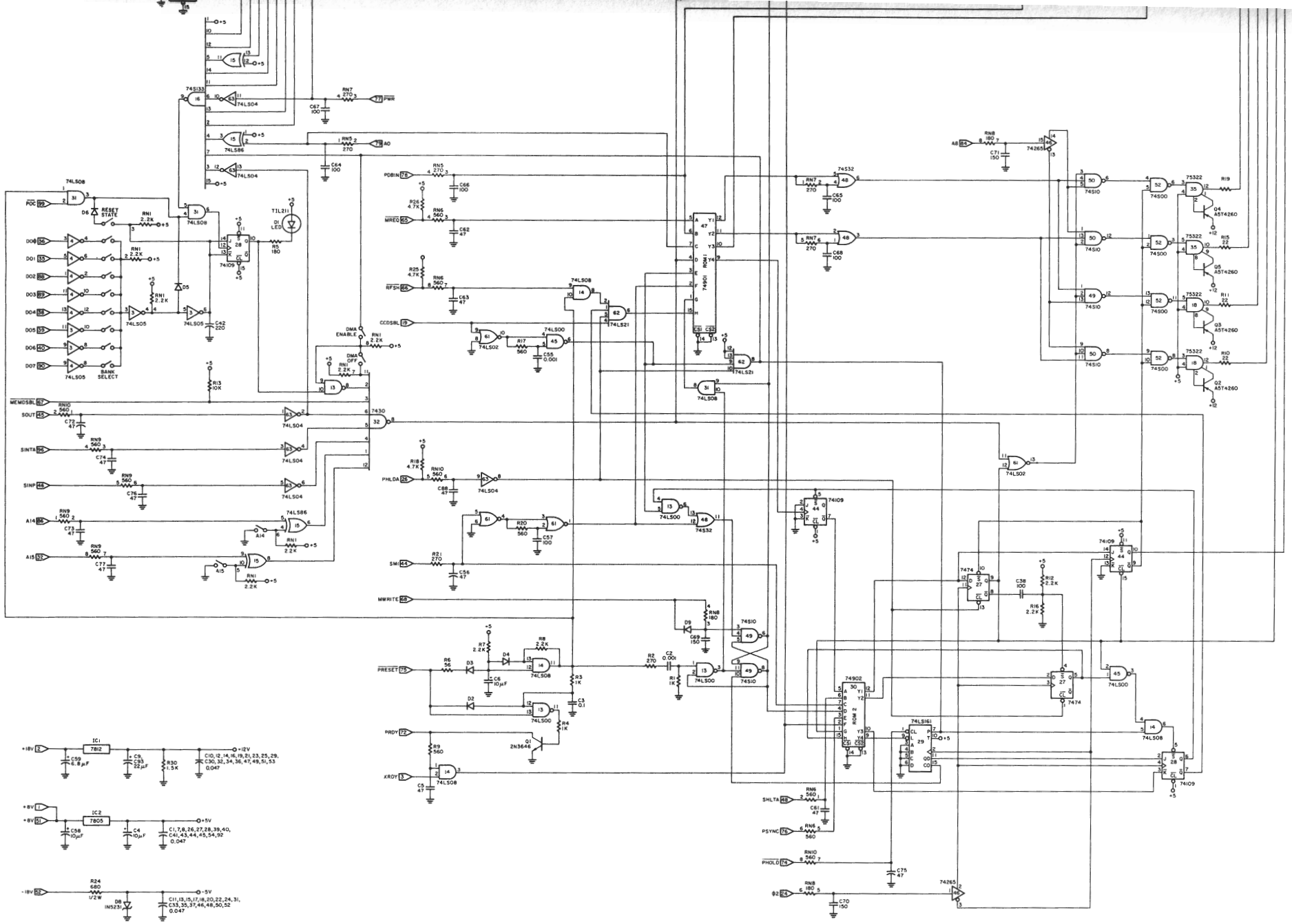
SCHEMATIC REV.8
BOARD REV. E
16KZ-040-0013
NOTE:
ALL DIODES (EXCEPT D1, D8) = IN914
CAPACITANCE >1 IN pF, CAPACITANCE <1 IN μF
RESISTANCE IN Ω
REFERENCE SYMBOLS
ASSIGNED
NOT ASSIGNED
IC1-IC65
D1-D9
C1-C93
R1-R30
RN1-RN17
Q1-Q5
RAM ARRAY
TMS 4050-2 OR 9050E
CE0 PAGE 0
CE1 PAGE 1
CE2 PAGE 2
CE3 PAGE 3
74393
74LS158
74LS373
74LS04
74LS86
74LS08
74LS00
74S32
74S10
74S00
74S22
74265
74S01
RESET STATE
PWR
SMEMR
PDBIN
WREQ
RFSH
A0
A8
+5V
+12V
R/W


74LS08
POC 99
RESET STATE
D6
RN1 2.2K
+5
D0 56
D1 55
D2 88
D3 89
D4 54
D5 53
D6 40
D7 90
74LS05
BANK SELECT
D5
74LS86
74LS04
74LS32
74LS00
74LS02
74LS21
74LS10
74LS08
74LS109
74LS153
74LS157
74LS161
74LS174
74LS283
74LS374
74LS244
74LS245
74LS273
74LS377
74LS393
74LS670
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