

ELECTRALOGICS 64k CMOS STATIC RAM BOARD

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2. GENERAL DESCRIPTION

Your 64k CMOS Static Ram Board uses state-of-the-art CMOS static memory devices and includes the following features:

Each of the 32 RAMs is addressable as a 2k block.

On-board Bank Select (Cromemco standard) is provided.

Extended-Addressing capability.

No wait-states necessary.

Phantom* (S-100 line # 67 capability).

All S-100 bus lines fully buffered.

Schmitt-triggered logic used to reduce sensitivity to noise.

Printed circuit board is solder-masked and silk screened.

All S-100 fingers are gold plated to ensure minimum contact resistivity and long life.

2716 EPROM compatibility. Each memory device can be replaced with a 2716 EPROM. Allows permanent allocation of monitors, etc.

Single voltage power supply requirements.

Low power dissipation. Typical active board consumption of 350 milliamps at 8 Volts. Inactive power consumption is less than 250 milliamps at 8 Volts.

2.0.1. Processor Compatibility

Electralogics Incorporated 64k CMOS Static Ram is guaranteed for use with the following processors and their slower versions:

CPU	MEM. ACC. TIME	INST. CYC. TIME	CLK.FREQ.
8080A-1	320 ns.	1.3 us.	3.2 Mhz.
8085A-2	230 ns.	0.8 us.	5.0 Mhz.
8088	340 ns.	0.8 us.	6.0 Mhz.
Z-80A	240 ns.	1.0 us.	4.0 Mhz.

Table 2-1: Micro-Processor Compatibility

The table above illustrates the relationship of memory access time, instruction cycle time and processor clock frequency. Clock frequency restrictions are often due to system bus, not memory, limitations.

The Hitachi 6116P-3 CMOS memory devices used on the 64k CMOS Static Ram Board have a very low power requirement which should result in total board consumption of less than 350 milliamps at 8 Volts. These 24-pin devices are internally organized in a "2k by 8" configuration and are 2716-compatible. Maximum Access Time is 150 nano-seconds.

Note: - Z-80 is the registered trademark of Zilog Corp.
 - 8080A, 8085A and 8088 are the registered trademarks of Intel Corp.

2.1. BASIC FEATURES

2.1.1. Basic Memory Size

Electralogics 64k CMOS Static Ram Board is available with a minimum population of 16k bytes of memory which can be upgraded in 2k byte increments to any capacity not exceeding 64k bytes.

2.1.2. Bank Selection

Bank Selection is provided, allowing the memory to be used with Multi-User systems such as Digital Research's M/PM.

2.1.3. Extended Addressing

Extended Addressing allows this board to be used in systems that have the ability to directly address up to 16 megabytes of memory (24 address bits).

2.1.4. Power Requirements

Electralogics 64k CMOS Static Ram Board typically requires 350 milliamps of current at 8 volts for the full complement of 64k bytes. Maximum current requirements will not exceed 400 milliamps.

2.1.5. Block Selection

Electralogics 64k CMOS Static Ram Board allows you to disable any 2k block of memory (at a 2k boundary) simply by turning off the appropriate Block Enable switch (switches 1 to 4). This flexibility is particularly suited to memory-mapped I/O or the use of EPROMs in which to locate a monitor or other firmware.

2.2. COMPATIBLE MEMORY

Electralogics 64k CMOS Static Ram Board is manufactured and shipped with Hitachi 6116P-3 CMOS or similar, compatible, memory devices. Other pin-for-pin compatible memory devices are:

SUPPLIER	MEMORY DEVICES		
	CMOS	NMOS	EPROM
Hitachi	6116P		
Intel			2716
Mostek		MK4802	
NEC	uPD446		
OKI	MSM5128	MSM2128	
TI	TMS4016		
Toshiba	TC5517AP	TMM2016P	

Table 2-2: Compatible Memory Devices

3. OPERATION

3.0.1. Block Enable Switches (SW1 to SW4)

The Block Enable Switches (SW1 to SW4) are located at the top right of the board nearest to the voltage regulator. (See Figure below) Switches of the "piano" type were selected for use, and mounted along the top edge of the board, because they allow the user to alter the system's memory configuration without removing the memory board from the system.

It is NOT necessary to turn power off when changing the Block Enable Switch settings.

Each of the four switch assemblies contains 8 individual switch positions. Each switch position is responsible for enabling or disabling one of the 32 2k blocks of memory. When any switch is in the "ON" position, its associated 2k block is enabled and will function normally. When any switch is set to the "OFF" position, its 2k block is disabled. If a memory-read operation is performed to that 2k block, the board will not drive the bus.

It is not necessary to remove the memory device when it is disabled but it can be removed if you wish. Since each device draws only about 1 microamp when de-selected, very little power will be saved by removing it.

Two Light Emitting Diodes (LED's) are located on the top of the board immediately to the left of the Block Select switches. The yellow LED identifies the selected memory board in a system containing multiple memory boards. The red LED indicates when an active memory block is read from or written to. The red LED will never turn on unless the yellow LED is on (board selected). For additional information, see the later paragraph covering Board Selection.

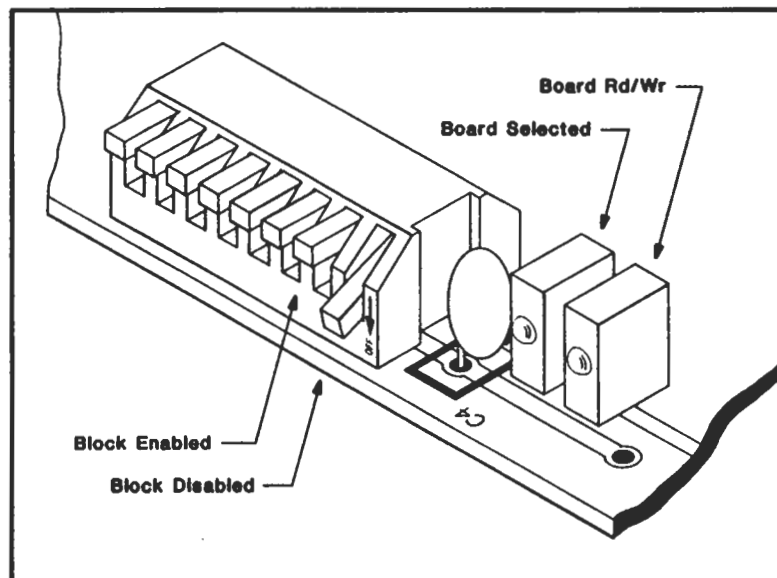


Fig. 3-1: Block Enable and Disable Switches

3.0.2. Phantom* Enable/Disable (Jumper J1-p)

The S-100 PHANTOM* line, when low, inhibits reading from all memory boards which have their Phantom Option enabled. Data can still be written to these same memory boards. This feature is useful when PROM-based bootstrap routines are used to perform system initialization. Plugging jumper J1-p enables the Phantom Option on the memory board. Removing jumper J1-p allows the board to function normally, ignoring the PHANTOM* line, permitting memory to be written to, or read from, at any time. This jumper is located along the bottom of the board just above, and between, S-100 contact fingers 19 and 20.

3.0.3. MWRT / PWR* (Jumpers J3-m,-w)

Some systems, usually those having front panels, require that all memory boards respond to the MWRT signal which is generated by the front panel. Systems without front panels do not usually generate the MWRT signal and therefore, PWR* must be used instead.

This option allows a memory board to be tailored to the system it is running in. If your system has a front panel, assume that this memory board should be strapped for MWRT and plug jumper J3-m. Otherwise, select PWR* by plugging J3-p. These jumpers are located along the bottom of the board, just above S-100 contact fingers 25 and 26.

3.0.4. Feature Selection (Jumpers J2-b,-x,-a)

Before any memory read or write may be successfully performed, the board must be selected by the processor.

Three options are available (jumper selectable) to perform this function. These jumpers are located along the bottom of the board, just above S-100 contact fingers 22 to 24. They are:

Jumper	Feature
J2-a)	Permanent Selection
J2-b)	Bank Select
J2-x)	Extended Addressing

Table 3-1: Feature Select Jumper Designation

3.0.5. Permanent Selection Mode

The Permanent Selection Mode (Jumper J2-a plugged) is most commonly used. When this Mode is selected, the board is always enabled and all memory read or write operations access the board. Only one memory board may be used in the system.

This mode is usually selected in systems whose addressing range is limited to 64k bytes. Whenever the Permanent Selection Mode is enabled, Extended Address and Bank Select features are ignored. Switch 5 is non-functional.

3.0.6. Bank Select Mode

Bank Select Mode (Jumper J2-b plugged) accomplishes board selection by having the user write one control byte of data to a "bank select" I/O port. This memory board recognizes the Cromemco standard for bank selection, that is, Port 40H as the Bank Select Control Port. Each bit of the control byte (when high) enables one 64k address space (one bank). By setting Switch 5's three high order positions to a binary value of 000 to 111, the board can be enabled for any one of 8 banks. When the control byte is written which corresponds to switch 5's setting, the board will be selected. Switch 5 settings are describes in appropriate sections of this manual.

On system initialization, a "write" to Port 40H should be performed to ensure that a bank is selected (Note: on power-up it is possible for more than one bank to be selected at the same time. Writing to Port 40H ensures that only the required bank will be enabled).

This mode is generally used in systems where more memory space is required and Extended Addressing is either not available or not desired. An example of such a system would be an 8080 or 8085 (or other 16 bit address bus) system running Digital Research's MP/M. A memory board containing 16k bytes of memory could be permanently enabled for running MP/M. Additional banks (up to 8 separate boards) of up to 48k bytes would be switched in and out as each user required service.

BANK SELECT MODE	
SW5	FUNCTION
1	Non-functional in this mode
2	Non-functional in this mode
3	Non-functional in this mode
4	Non-functional in this mode
5	Non-functional in this mode
6	LSB Bank Select Mode
7	Bank Select Mode
8	MSB Bank Select Mode

Table 3-2: Switch 5 - Active Positions For Bank Select

Bank Selected	SW5-8	SW5-7	SW5-6
0	ON	ON	ON
1	ON	ON	OFF
2	ON	OFF	ON
3	ON	OFF	OFF
4	OFF	ON	ON
5	OFF	ON	OFF
6	OFF	OFF	ON
7	OFF	OFF	OFF

Table 3-3: Switch 5 - Settings For Specific Banks

Note: Any switch "ON" = logical 0 "OFF" = logical 1

3.0.7. Extended Addressing Mode

The Extended Addressing Mode (Jumper J2-x plugged) allows a direct memory address range of up to 16 megabytes (24 address bits). When using the Extended Addressing Mode, the 8 high-order address lines (IEEE 696 lines specified as A16 to A23) are compared to SW5 via U15 (74LS682). When the results of the comparison are equal, the board is selected and the yellow LED will be turned "ON". In this mode, all read and write operations will be ignored by the board unless it is selected.

This mode of operation is generally used by systems containing a processor board with extended addressing capabilities (that is, more address lines than the conventional 16) or, systems utilizing memory-management procedures (a means of extending the address range of a processor).

EXTENDED ADDRESSING MODE				
SW5	FUNCTION			
1	Compared to Address Line 23			
2	"	"	"	22
3	"	"	"	21
4	"	"	"	20
5	"	"	"	19
6	"	"	"	18
7	"	"	"	17
8	"	"	"	16

Table 3-4: Switch 5 Functions - Extended Addressing Mode

Note: Any switch ON = logical "0" OFF = logical "1"

Therefore, in order for the board to respond to addresses 000000H to 00FFFFH, set SW5 as follows:

	A23							A16
SW.5 POS'N	1	2	3	4	5	6	7	8
ON/OFF	ON	ON	ON	ON	ON	ON	ON	ON

For the board to respond to addresses C30000H to C3FFFFH, set SW5 as follows:

	A23							A16
SW.5 POS'N	1	2	3	4	5	6	7	8
ON/OFF	OFF	OFF	ON	ON	ON	ON	OFF	OFF

4. S-100 BUS LINE UTILIZATION

PIN #	NAME	INPUT/OUTPUT	CHARACTERISTICS
-----	-----	-----	-----
1	+8VDC	1 Amp. max.	-
15	A18	I	A
16	A16	I	A
17	A17	I	A
20	GND	-	-
29	A5	I	A
30	A4	I	A
31	A3	I	A
32	A15	I	A
33	A12	I	A
34	A9	I	A
35	D01	I	A
36	D00	I	A
37	A10	I	A
38	D04	I	A
39	D05	I	A
40	D06	I	A
41	DI2	O	B
42	DI3	O	B
43	DI7	O	B
45	SOUT	I	C
46	SINP	I	C
47	SMEMR	I	C
50	GND	-	-
51	+8VDC	(see pin 1)	(see pin 1)
53	GND	-	-
59	A19	I	A
61	A20	I	A
62	A21	I	A
63	A22	I	A
64	A23	I	A
67	PHANTOM*	I	C
68	MWRT	I	C
70	GND	-	-
77	PWR*	I	C
78	PDBIN	I	C
79	A0	I	A
80	A1	I	A
81	A2	I	A
82	A6	I	A
83	A7	I	A
84	A8	I	A
85	A13	I	A
86	A14	I	A
87	A11	I	A
88	D02	I	A
89	D03	I	A
90	D07	I	A

91	DI4	0	B
92	DI5	0	B
93	DI6	0	B
94	DI1	0	B
95	DIO	0	B
100	GND	-	-

Table 4-1: S-100 Bus Utilization

4.1. SIGNAL CHARACTERISTICS

4.1.1. (A) Input

- logical 1 input voltage => 2.0 V.
- logical 0 input voltage <= 0.8 V.
- input hysteresis voltage 0.4 V. typical
- logical 1 input current 20 uA. max.
- logical 0 input current -200 uA. max.

4.1.2. (B) Output

- logical 1 output voltage => 2.4 V.
- logical 0 output voltage <= 0.5 V.
- logical 1 output current => 3 mA.
- logical 0 output current => -24 mA.

4.1.3. (C) Input

- logical 1 input voltage => 2.0 V.
- logical 0 input voltage <= 0.8 V.
- logical 1 input current 20 uA. max.
- logical 0 input current -360 uA. max.

Table 4-2: S-100 Bus Signal Characteristics

Note: All inputs and outputs are IEEE - 696 compatible.

4.2. MEMORY MAP

In order to accommodate the necessary 32 memory and associated support devices on the printed circuit board in a logical and esthetically appealing manner, it was necessary to arrange the memory in two horizontal rows of 13 and an additional row of six, devices.

The following chart indicates the hexadecimal address, memory block switch number and location for each device.

Hex. Address	Block Sw. No.	Location
0000H	SW1-1	A1
0800H	SW1-2	A2
1000H	SW1-3	A3
1800H	SW1-4	A4
2000H	SW1-5	A5
2800H	SW1-6	A6
3000H	SW1-7	B1
3800H	SW1-8	C1
4000H	SW2-1	B2
4800H	SW2-2	C2
5000H	SW2-3	B3
5800H	SW2-4	C3
6000H	SW2-5	B4
6800H	SW2-6	C4
7000H	SW2-7	B5
7800H	SW2-8	C5
8000H	SW3-1	B6
8800H	SW3-2	C6
9000H	SW3-3	B7
9800H	SW3-4	C7
A000H	SW3-5	B8
A800H	SW3-6	C8
B000H	SW3-7	B9
B800H	SW3-8	C9
C000H	SW4-1	B10
C800H	SW4-2	C10
D000H	SW4-3	B11
D800H	SW4-4	C11
E000H	SW4-5	B12
E800H	SW4-6	C12
F000H	SW4-7	B13
F800H	SW4-8	C13

Table 4-3: Memory Address/Block Switch/Location

5. FRONT PANEL MODIFICATIONS

Some older system types, such as the MITS Altair 8800 and the IMSAI 8800, do not fully comply with the IEEE-696 S-100 Standard. Owners of these systems will not be able to "DEPOSIT" data into this memory board as shipped. All of the remaining front panel functions will perform normally.

In order to allow the front panel to perform all of its normal functions when using this memory board, locate the three jumper pads labelled "J4" in the lower right corner of the board just above the serial number. (See Figure below)

A printed circuit jumper is permanently connected between the centre and right hand pads. Cut this land, using a sharp knife. Make sure that you remove a short length of copper to prevent intermittent problems.

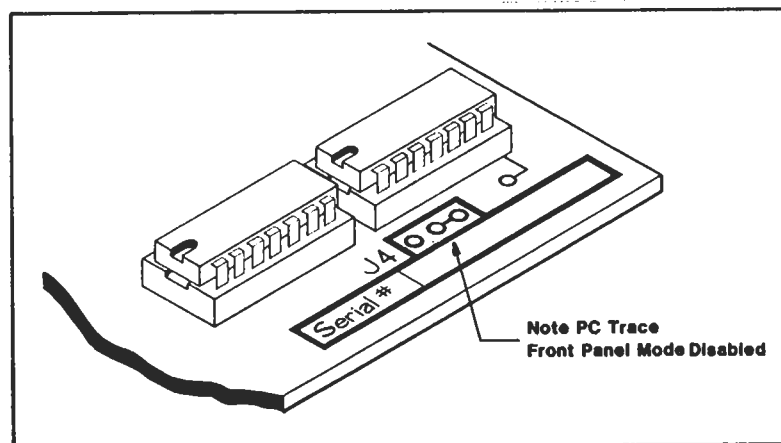


Fig. 5-1: Front Panel Mode Disabled

Then, using a fine-tipped soldering iron (25 to 35 Watts is best), install a jumper between pads 1 and 2 as shown.

The front panel will now function normally.

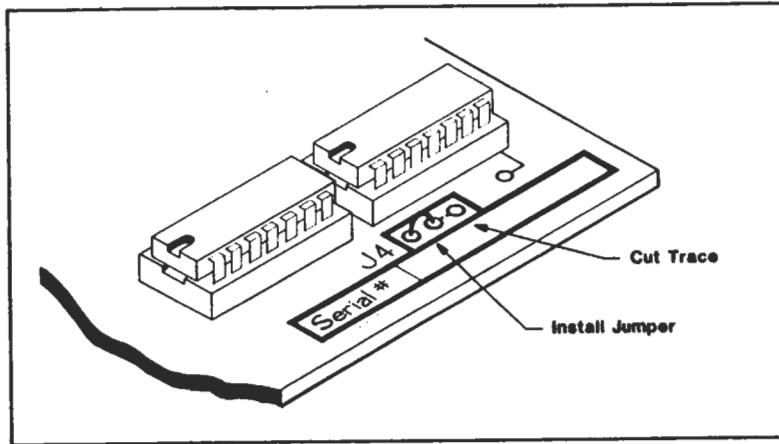


Fig. 5-2: Front Panel Mode Enabled

6. MEMORY TEST

Your 64k CMOS Static Ram Board was shipped assembled and extensively tested. Instructions are provided for board set-up which can be followed with little difficulty. Since short memory tests are of little benefit in detecting memory problems, we have decided to leave the selection of a memory test to the user for many reasons.

We will presume that a user ordering a 64k memory board does have a functional system. Memory tests can be performed by removing an existing memory board from the user's system and, by setting the proper Block Select switches, substituting the same amount of memory as the removed board provided. Existing user tests can then be run on those blocks selected.

An excellent memory test program, which we use to test our products, is MEMRS.ASM. This test is often available from a Remote CP/M (RCPM) system. If you are not aware of any RCPM, or other similar system, in your area, check with your local computer store for information.

Some magazines devoted to the micro-computer user have recently published address lists of these systems.

Canadian CP/M users may procure diskettes containing memory tests and other public domain software from the BDSC User's Group, the CP/M User's Group, RCP/M User's Group and the SIG/M User's Group from by sending \$10.00 Canadian, (for any single 8-inch diskette from the above groups), to the address below. The price includes a diskette and postal charges.

Toronto RCP/M,
c/o G.J. Newell,
4691 Dundas Street West,
Islington, Ontario M9A 1A7

CP/M User's Group diskettes are also available from:

CP/M User's Group,
1651 Third Avenue,
New York, N.Y. 10028

A. PARTS LIST

Description	Qty.	Identification
100k 5% 1/4 Watt Resistor	2	R1 R2
150 Ohm 5% 1/4 Watt Resistor	1	R3
2.2k 5% 1/4 Watt Resistor	2	R6 R7
470 Ohm 5% 1/4 Watt Resistor	2	R4 R5
Res. Network #4610X-101-332	4	R8-R11
0.01 uFd. 50V Ceramic Cap.	50	C13-C62
1.0 uFd. 35V Tantalum Cap.	5	C1-C3 C10 C11
10 uFd. 10V Tantalum Cap.	6	C4-C7 C9 C12
10 uFd. 25V Tantalum Cap.	1	C8
2N3904 NPN Signal Transistor	1	Q1
LED Red Dialco #555-2001	1	D1
LED Yellow Dialco #555-2401	1	D2
7805 Voltage Regulator 1.5 Amp.	1	VR1
7407 Hex Buffer (OC)	1	U13
74LS00 Quad 2-Input NAND	1	U21
74LS02 Quad 2-Input NOR	1	U20
74LS04 Hex Inverter	1	U10
74LS30 8-Input NAND	5	U5-U8 U22
74LS32 Quad 2-Input OR	1	U9
74LS123 Dual Single Shot	1	U11
74LS138 3-8 Line De-Mux	4	U1-U4
74LS241 Octal Buffer (TS)	2	U18 U19
74LS244 Octal Buffer (TS)	2	U16 U17
74LS354 8-1 Line Data Select.	1	U12
74LS682 Octal Comparator	2	U14 U15
HM6116P-3 2k*8 Static Ram	32	U23-U54
8 Pos'n Switch AMP #435640-5	1	SW5
8 Pos'n Switch Piano Type AMP #435802-1	4	SW1-SW4
Programming Shunt	3	
14 Pin IC Socket	10	U5-U10 U13 U20-U22
20 Pin IC Socket	7	U12 U14-U19
24 Pin IC Socket	32	U23-U54
Double Row 0.025 Post Header	1	J1
Double Row 4-Pin 0.025 Post	1	J3
Double Row 6-Pin 0.025 Post	1	J2

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4-40 X 5/16 Pan Head Screw	1
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4-40 Star Lockwasher	1
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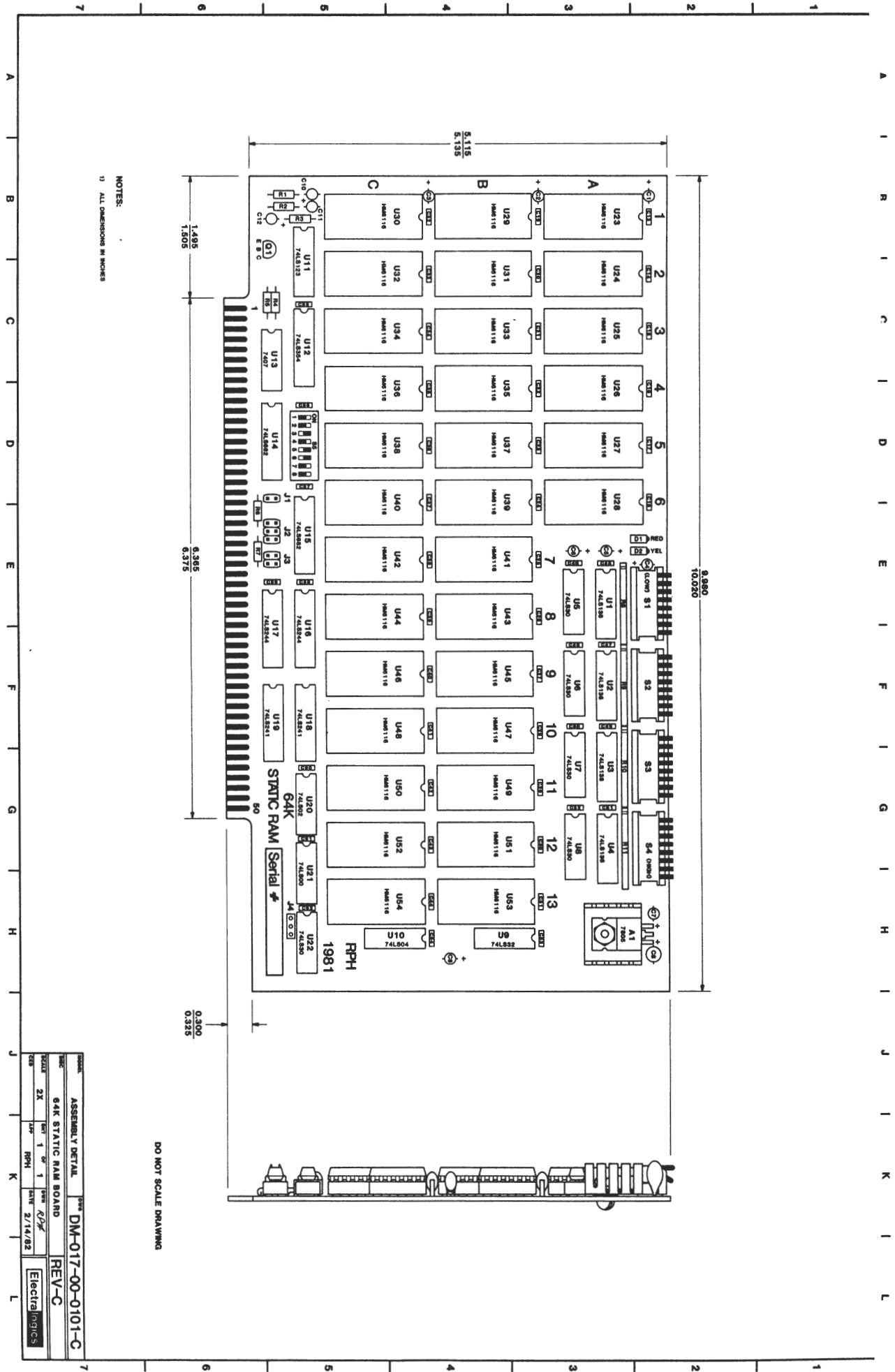
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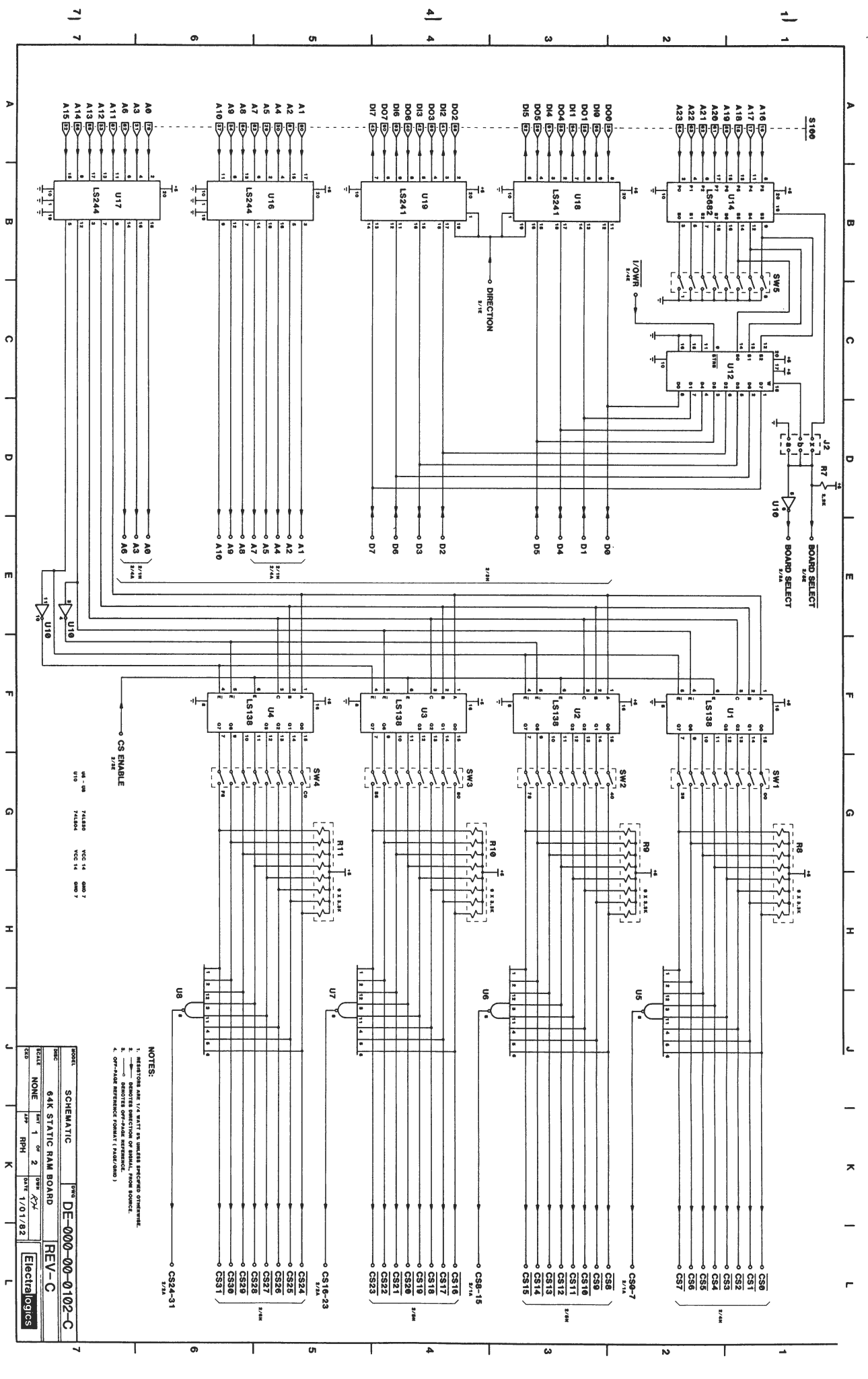
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NOTES:
 1) ALL DIMENSIONS IN INCHES

DO NOT SCALE DRAWING

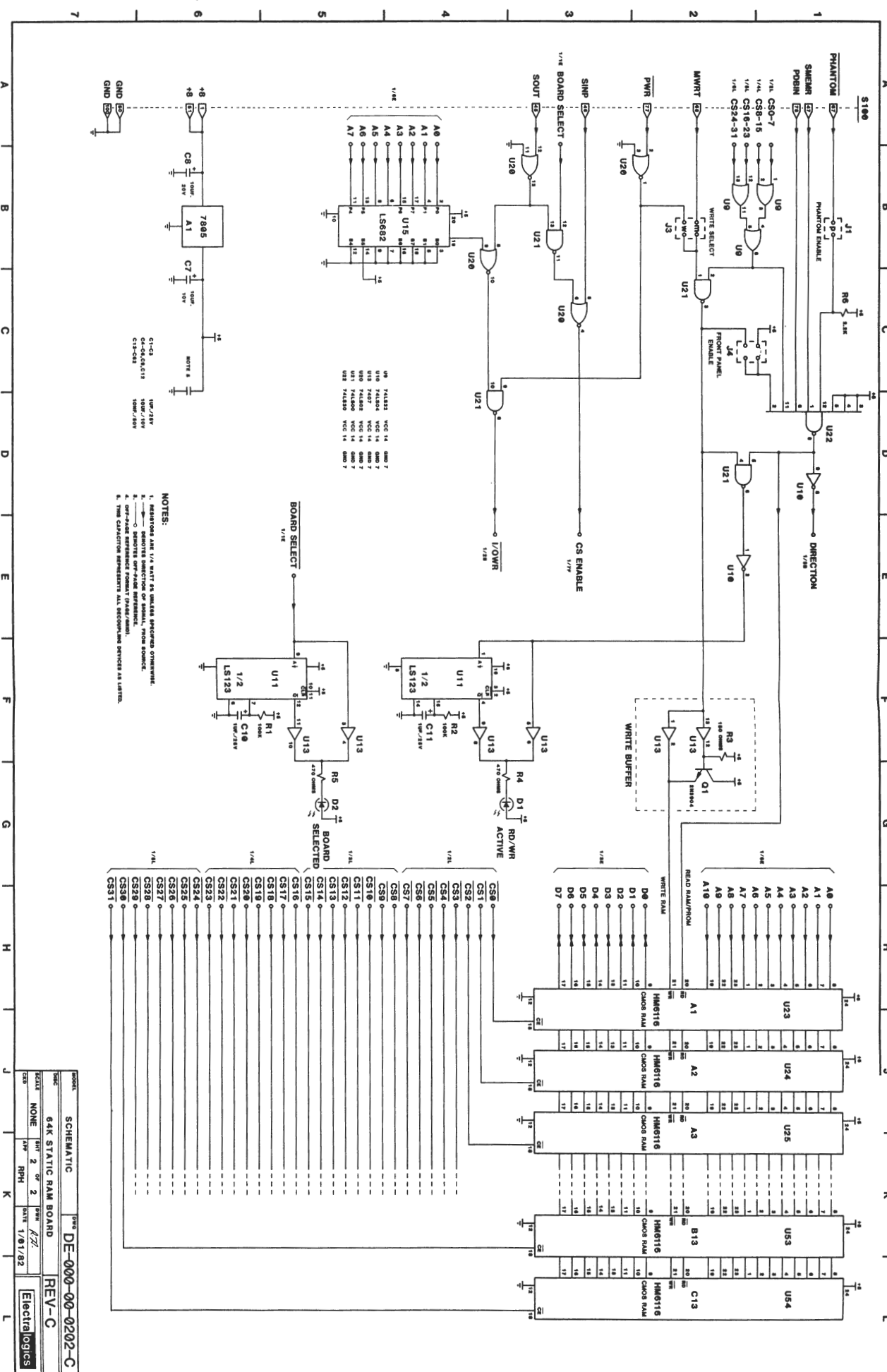
TITLE		PART		DATE	
ASSEMBLY DETAIL		DM-017-00-0101-C		2/14/82	
REV		DRAWN		CHECKED	
REV-C		RPH		2X	
ELECTRA LOGICS		DATE		DRAWN	
		2/14/82		RPH	



- NOTES:
1. REFERENCE AND 1/4 WATT 5% TOLERANCE DISCRETE COMPONENTS.
 2. DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.
 3. DIMENSIONS IN PARENTHESES ARE FOR MOUNTING HOLES.
 4. OFF-BOARD REFERENCE POINTS (PANEL MOUNT).

MODEL	SCHEMATIC		REV	DE-000-00-0102-C
DATE	NONE	REV	1	REV
SCALE	NONE	UNIT	1	OR
APP	RPH	DATE	1/01/82	
REP				

64K STATIC RAM BOARD
REV-C
Electronics



- NOTES:
1. RESISTOR AND 1/4 WATT OR LOWER POWERED COMPONENTS ARE TO BE USED UNLESS OTHERWISE SPECIFIED.
 2. CAPACITORS ARE TO BE 5% TOLERANCE UNLESS OTHERWISE SPECIFIED.
 3. UNLESS OTHERWISE SPECIFIED, ALL COMPONENTS ARE TO BE MIL-SPEC.
 4. OFF-PAGE REFERENCE FORMAT (PAGE/AMOUNT).
 5. UNLESS OTHERWISE SPECIFIED, ALL COMPONENTS ARE TO BE MIL-SPEC.
 6. THE CAPACITOR REQUIREMENTS ALL REQUIREMENTS SERVICES AS LISTED.

PROJECT	SCHEMATIC	REV	DE-000-00-0202-C
TITLE	64K STATIC RAM BOARD	REV	REV-C
DATE	1/9/82	DESIGNER	RZH
APPROVED	RPH	CHECKED	NONE
DATE	1/9/82	DATE	1/9/82
Electralogics			

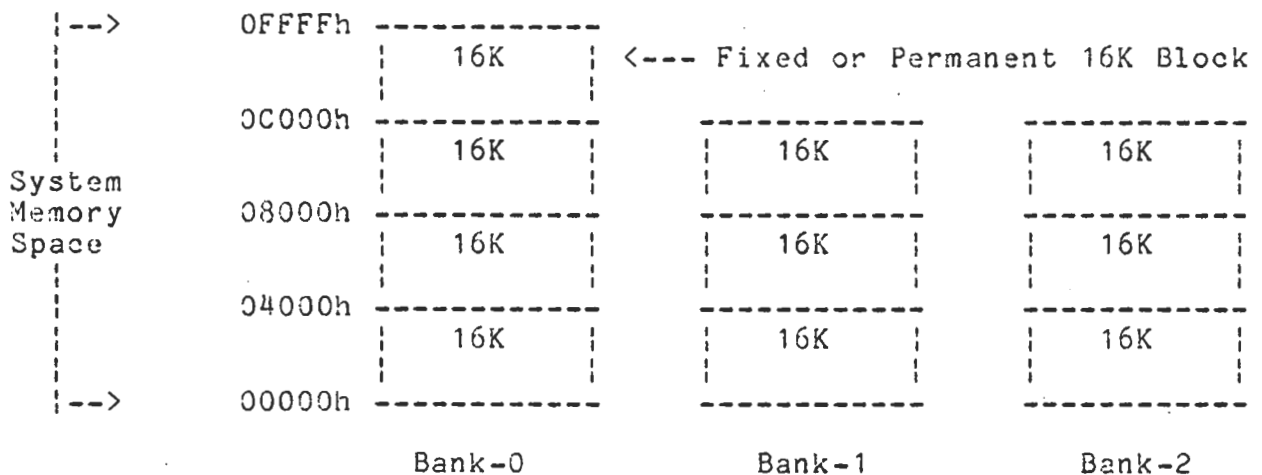
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☆☆☆ UPDATE ☆☆☆

APPLICATION NOTE #1

Title:- Configuring Your 64K CMOS Static Ram Board for MP/M(tm) and/or CP/M 3.0(tm) Systems.

Many of our customers using MP/M(tm) and possibly CP/M 3.0(tm) have requested a technique which will allow one of our 64K memory boards to contain both fixed or permanent and banked RAM. The figure below illustrates a typical system where such a requirement presents itself:



In the above diagram, the upper 16K of RAM must always be resident whereas the lower 48K must be bank selectable. Without the modifications which are to follow, 4 memory boards would be required to implement this system. The first board would contain the fixed 16K portion while the additional 3 boards would each be populated to 48K and be used to implement each of three banks. A technique is needed to allow one board to support not only the fixed portion of RAM, but also the memory for one bank.

The criteria for this modification were simple -

- Keep it simple.
- Don't destroy the product in the process.

Who knows, you may want to sell the board some day!

Modification:- Examining the schematics for your 64K RAM board will show that all the chip selects are generated by U1-U4 as follows: (These are the 74LS138's located below the dip switches)

U1 - 0000h to 3FFFh
U2 - 4000h to 7FFFh
U3 - 8000h to BFFFh
U4 - C000h to FFFFh

To make any of these 16K blocks of RAM fixed is as simple as:

- a) Locate the proper IC (U1-U4).
- b) Lift pin 6 on the selected device and bend it back over the top of the chip.
- c) Use a small piece of wire and jumper pin 6 to pin 16(+5).
- d) Replace the IC.

The following example may help illustrate such a modification.

EXAMPLE:- The goal is to implement a system with three 48K banks which are bank selectable and range from 0000h to BFFFh and has 16K of RAM fixed from C000h to FFFFh.

SOLUTION:- This system will require 3 memory boards, one populated with 64K of RAM and two populated with only 48K.

On the 64K board, lift U4 and modify the chip as listed above. Replace U4. This operation has fixed the top 16K of this board. Note that any block which is modified as shown will not respond to the jumper option J2-b. Since the lower 48K of this board is to be used as one of the 3 banks, the jumpers should be set as follows:

J1 - as required by user.
J2 - select "b" for bank select.
J3 - select "m" for MWRT.

Assuming this bank is to be bank 0, set SW5 as follows:

SW5-1 to SW5-5 = don't care.
SW5-6 to SW5-8 = "on".

(See page 10 of User's Manual)

Note that SW1 to SW4 must have all switches "on".

