# QX-10

## OPTION CARDS

# TECHNICAL MANUAL

Q8490026-0

EPSON

# INTRODUCTION

This Technical Manual provides technical information on the principles of operation of the QX-10 options and on trouble-shooting. Major technical modifications, if made in the future, will be notified through Service Bulletins, and the Technical Manual should be revised accordingly.

The details of the Manual are subject to change without notice. All the information given in the Manual concerns the QX-10 options, and we are not responsible for any problems with the industrial copyright of a third party that might arise from your application of the Manual to other products or from the connection of the QX-10 options to others.

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# CHAPTER 1 GENERAL

1.1. Outline of Options

1.2. Precautions on FCC Regulations

1.3. Maintenance

The QX-10 has five option card slots including the 8-bit parallel data bus. The following option cards are available for user support.

| Name | Application |
|---|---|
| Q10K1 | ROM card including JIS 1st level kanji character generator |
| Q10K2 | ROM card including JIS 2nd level kanji character generator |
| Q10MF | ROM card including 16 kinds of proportional characters |
| Q10RS | 2-channel RS-232C interface card |
| Q10IE | IEEE-488 interface card |
| Q10OF | Optical fiber interface card |
| Q10AD | 8-bit A/D-D/A converter |
| Q10CMS | Color monitor subboard |
| Q10UC | Universal card usable optionally by user |
| Q10LP | Light pen |

Table 1-1

## 1.2. Precautions on FCC Regulations

1) The FCC regulations require each option card to meet the regulated values when mounted in the QX-10 system. All EPSON brand option cards satisfy these regulations. However, when option cards are produced by the universal card (Q10UC) and sold under the EPSON brand, each of these option cards must be approved by FCC.
In such a case, samples of these cards shall be submitted to EPSON, System Design Section 1 for recognition by EPSON.
Application by the foreign corporation of EPSON or EPSON CORPORATION to FCC (FTZ) shall be considered each time the application is made.

2) Precautions on designing option cards to meet FCC Regulations

   (1) Use C-MOS IC as far as possible in option cards. If C-MOS IC cannot be used, use LS or normal TTL. Never use TTL of S, ALS.

   (2) Use thick GND and power supply pattern, and make the power supply impedance sufficientyly small.

   (3) Make the clock frequency as low as possible, and make the waveform as dull as possible in the leading and trailing edges.

   (4) When a connector is needed for external connection, use a connector with metallic case and connect FG (Frame Ground) to the metal plate on the rear panel of QX-10.

## 1.3. Maintenance

The following tool and test program are available for maintenance of option cards.

Tool: Q10 Extension Card (Y135211001)

As shown in Fig. 1-1, this card is inserted in the option slot to raise the option card position for ease of waveform observation and repair.

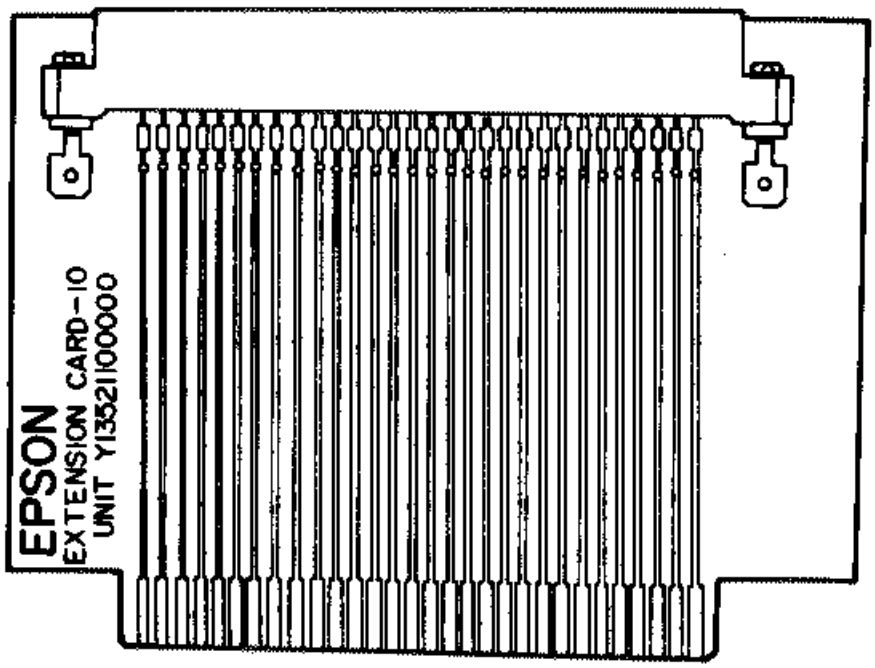



Fig. 1-1

Test Program: The test program is used for checking operation of option card.

# CHAPTER 2 SPECIFICATIONS OF OPTION SLOT SIGNALS

## 2.1. Location of Option Connector Signals

As shown in Fig. 2-1, there are five option slots on the Q10SYM circuit board under the option cover. Signal lines of 60 pins including the system data bus, address bus and power supply line are output to these slots. Each slot is different in interrupt level, etc. Pay attention to this point when using the slots.
The Table 2-1 shows the location of these option connector signals.

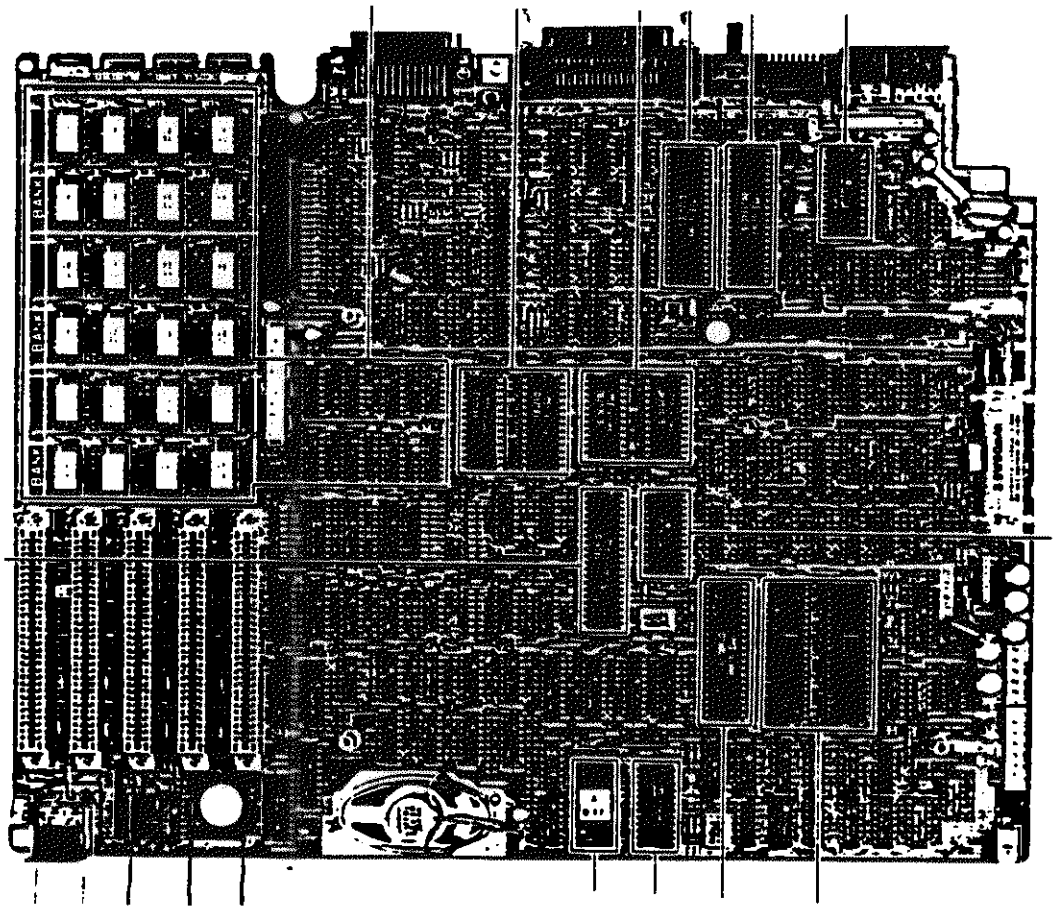


Fig. 2-1 Location of option slots

| Pin No. | Signal Symbol | Signal Direction | Description of Signal |
|---|---|---|---|
| 1 - 2 | GND | —— | Ground |
| 3 - 10 | DTBO-7 | IN/OUT | Data bus |
| 11 - 12 | -12 V | —— | -12 V |
| 13 - 28 | ADRO-15 | OUT | Address bus |
| 29 - 30 | GND | —— | Ground |
| 31 | CLK | OUT | System clock |
| 33 | $\overline{\text{BSAK}}$ | OUT | Bus acknowledge |
| 34 | $\overline{\text{MEMX}}$ | OUT | External memory select |
| 35 | $\overline{\text{IRD}}$ | OUT | I/O read |
| 36 | $\overline{\text{IWR}}$ | OUT | I/O write |
| 37 | $\overline{\text{MRD}}$ | OUT | Memory read |
| 38 | $\overline{\text{MWR}}$ | OUT | Memory write |
| 39 | $\overline{\text{RSIN}}$ | IN | Reset input |
| 40 | INT(H)1 | IN | High-priority external interrupt |
| 41 | INT(H)2 | IN | High-priority external interrupt |
| 42 | INT(L) | IN | Low-priority external interrupt |
| 43 | +5 V | —— | +5 V |
| 44 | $\overline{\text{RSET}}$ | OUT | Reset output |
| 45 - 46 | +5 V | —— | +5 V |
| 47 | $\overline{\text{DRQ(F)}}$ | IN | DMA request |
| 48 | $\overline{\text{DRQ(S)}}$ | IN | DMA request |
| 49 | $\overline{\text{RDY(F)}}$ | IN | DMA ready |
| 50 | $\overline{\text{RDY(S)}}$ | IN | DMA ready |
| 51 | $\overline{\text{WAIT}}$ | IN | Wait |

| Pin No. | Signal Symbol | Signal Direction | Description of Signal |
|---|---|---|---|
| 52 | $\overline{\text{IWS}}$ | OUT | I/O write short |
| 53 | $\overline{\text{DAK(F)}}$ | OUT | DMA acknowledge |
| 54 | $\overline{\text{DAK(S)}}$ | OUT | DMA acknowledge |
| 55 | $\overline{\text{EOP(F)}}$ | OUT | End of process |
| 56 | $\overline{\text{EOP(S)}}$ | OUT | End of process |
| 57 - 58 | +12 V | —— | +12 V |
| 59 - 60 | GND | —— | Ground |

## 2.2. Description of Signals

| Signal | Pin No. | Description |
|---|---|---|
| GND | 1, 2, 29, 30, 32, 59, 60 | Potential 0V. Return lines of respective power supplies (+5, +12, -12). All pins are connected to the signal ground on the main board. |
| DTB 0 \| DTB 7 | 3 - 10 | DATA BUS. Input/Output signals. These are buffered by the bidirectional buffer on the main board. All of these are output signals except for data input from the option slot. |
| ADR 0 \| ADR 15 | 13 - 28 | ADDRESS BUS. Output signals. These signals designate memory addresses and an input/output device. |
| CLK | 31 | SYSTEM CLOCK. Output signal. It is the main system clock (3.9936 MHz). The phase is the same as that supplied to the CPU. |
| $\overline{\text{BSAK}}$ | 33 | BUS ACKNOWLEDGE. Output signal. This is a bus acknowledgement signal for CPU. When LOW, this signal indicates that the DMA is operating. |
| $\overline{\text{MEMX}}$ | 34 | EXTERNAL MEMORY SELECT. Output signal. When LOW, this signal indicates that memory at the option slot has been selected. |
| $\overline{\text{IRD}}$ | 35 | I/O READ. Output signal. Set to LOW for data input from an I/O device; the CPU receives data at the rising edge of the signal. |
| $\overline{\text{IWR}}$ | 36 | I/O WRITE. Output signal. Set to LOW for data output to an I/O device. |
| $\overline{\text{MRD}}$ | 37 | MEMORY READ. Output signal. Set to LOW for data input from memory; the CPU receives data at rising edge of the signal. |

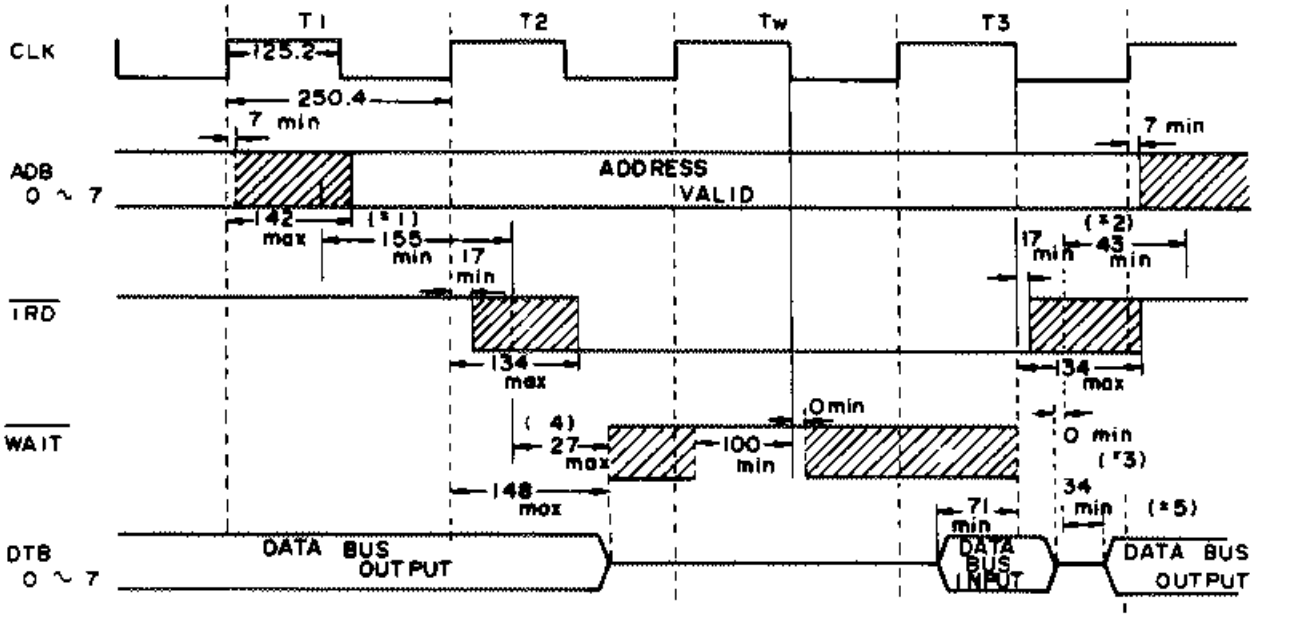
| Signal | Pin No. | Description |
|---|---|---|
| $\overline{\text{MWR}}$ | 38 | MEMORY WRITE. Output signal. Set to LOW level for data output to memory. |
| $\overline{\text{RSIN}}$ | 39 | RESET IN. Input signal. Input of this signal from the option side resets the CPU when the signal goes LOW, while the reset operation ends when the signal is set to HIGH. |
| INT(H) 1<br>INT(H) 2 | 40<br>41 | HIGH PRIORITY EXTERNAL INTERRUPT. Input signals. High priority interrupts applied when signals are set to HIGH.<br>These signals are connected to the 8259 on the main board. |
| INT(L) | 42 | LOW PRIORITY EXTERNAL INTERRUPT. Input signal. This signal is used in the same manner as INT(H), but the priority of the interrupt is low. |
| $\overline{\text{RSET}}$ | 44 | RESET. Output signal. This signal initializes the device at the option slot. When the system is in the reset condition, this signal is set to LOW. |
| $\overline{\text{DRQ(F)}}$<br>$\overline{\text{DRQ(S)}}$ | 47<br>48 | DMA REQUEST. Input signals. These signals are set to LOW to request DMA transfer from a device at the option slot. DRQ(F) has a higher DMA request level than DRQ(S). |
| $\overline{\text{RDY(F)}}$<br>$\overline{\text{RDY(S)}}$ | 49<br>50 | DMA READY. Input signals. WAIT can be applied to the DMA controller by setting these signals to LOW. RDY(F) and RDY(S) correspond to DRQ(F) and DRQ(S), respectively. |
| $\overline{\text{WAIT}}$ | 51 | WAIT. Input signal. CPU operation can be interrupted by setting this signal to LOW. |

| Signal | Pin No. | Description |
|---|---|---|
| $\overline{\text{IWS}}$ | 52 | I/O WRITE SHORT. Output signal. Used when the IWR signal does not provide sufficient time to write data from an external memory to an I/O device during a DMA transfer. |
| $\overline{\text{DAK(F)}}$<br>$\overline{\text{DAK(S)}}$ | 53<br>54 | DMA ACKNOWLEDGE. Output signals. When the DMA controller receives DRQ, these signals are set to LOW when the DMA is started. DAK(F) and DAK(S) correspond to DRQ(F) and DRQ(S), respectively. |
| $\overline{\text{EOP(F)}}$<br>$\overline{\text{EOP(S)}}$ | 55<br>56 | END OF PROCESS. Output signals. These signals indicate the end of 1 block during a DMA transfer. They are set to LOW together with DAK when the last byte is sent. EOP(F) and EOP(S) correspond to DRQ(F) and DRQ(S), respectively. |
| +5 V | 43, 45, 46 | +5 V power supply lines. (Up to 2 A.) |
| +12 V | 57, 58 | +12 V power supply lines. (Up to 0.2 A.) |
| -12 V | 11, 12 | -12 V power supply lines. (Up to 0.04 A.) |

## 2.3. I/O Port Access Timing

### (1) I/O Read Timing

[Unit: nsec]




(*1) Address stabilization prior to $\overline{IRD}$.

(*2) Address holding time after $\overline{IRD}$.

(*3) Data holding time after $\overline{IRD}$.

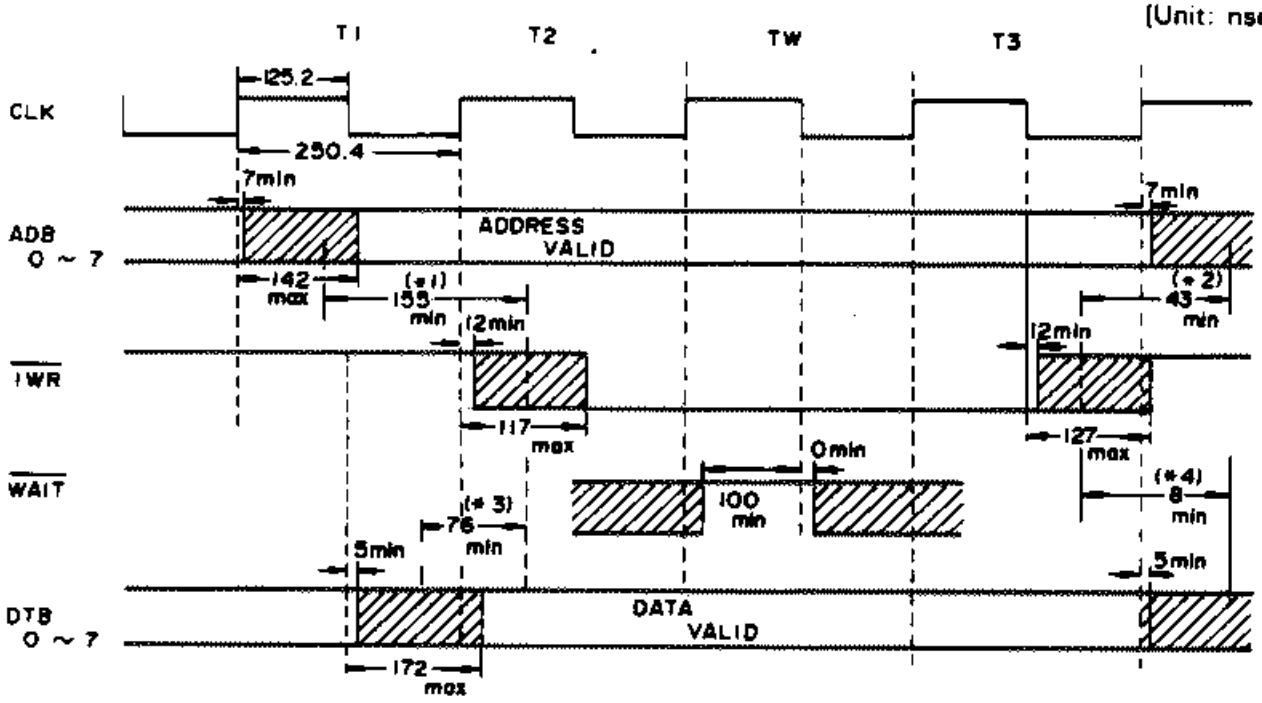
(*4) Delay before float after $\overline{IRD}$.

(*5) Floating hold time after $\overline{IRD}$.

Note: The data bus is normally in the output state, and serves as an input terminal only when data is output from the option side.

(2) I/O Write Timing

[Unit: nsec]




(*1) Address stabilization prior to $\overline{IWR}$.

(*2) Address holding time after $\overline{IWR}$.

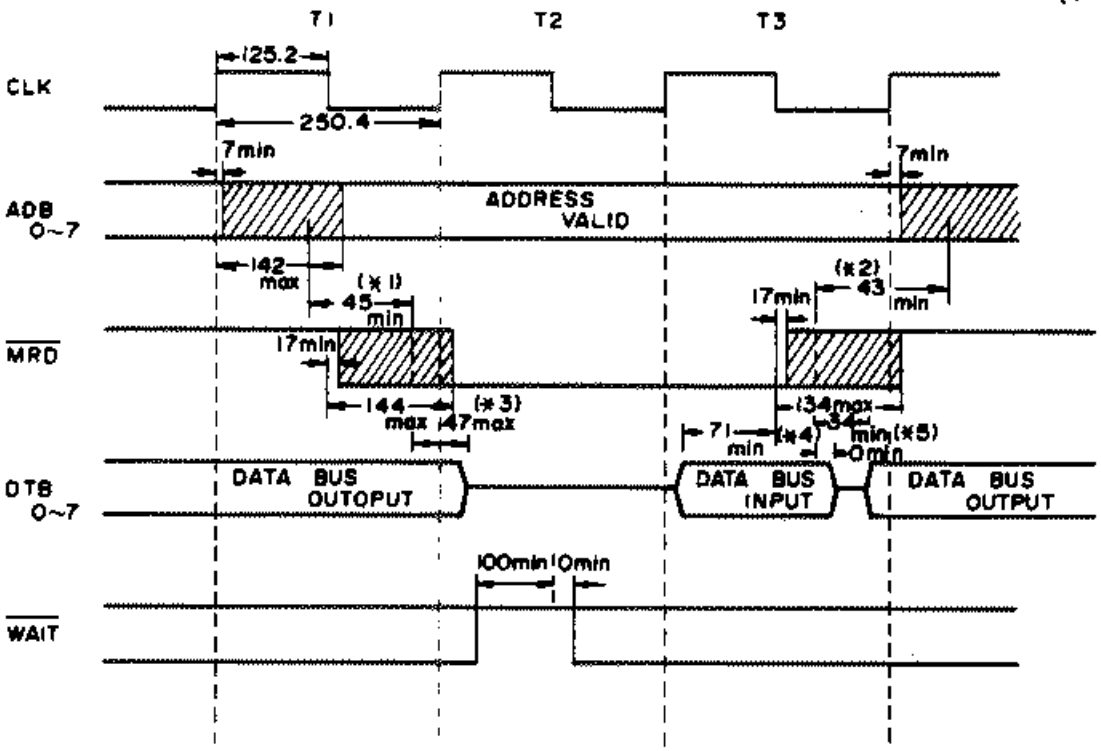
(*3) Data stabilization after $\overline{IWR}$.

(*4) Data holding timing prior to $\overline{IWR}$.

## 2.4. Memory Access Timing

### (1) Memory read timing

(Unit: nsec)




(*1) Address bus stabilization time preceding the falling edge of $\overline{MRD}$.

(*2) Address bus holding time following the rising edge of $\overline{MRD}$.

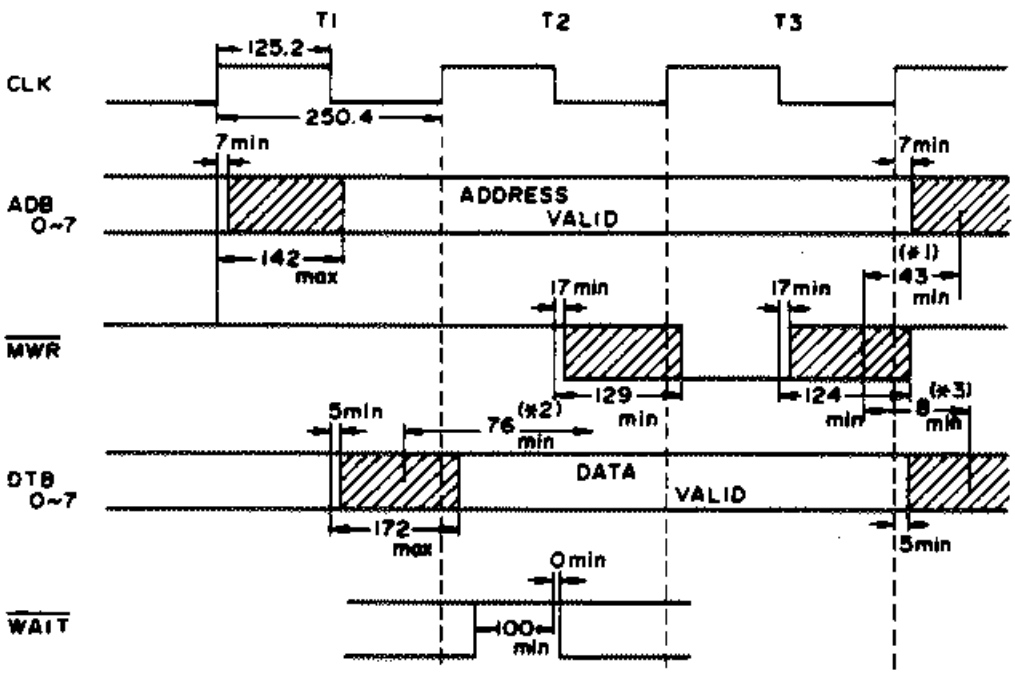
(*3) Time following the falling edge of $\overline{MRD}$ before the data bus starts floating.

(*4) Data bus holding time following the rising edge of $\overline{MRD}$.

(*5) Data bus floating time following the rising edge of $\overline{MRD}$.

(2) Memory write timing

[Unit: nsec]




(*1) Address bus holding time following the rising edge of $\overline{MWR}$.

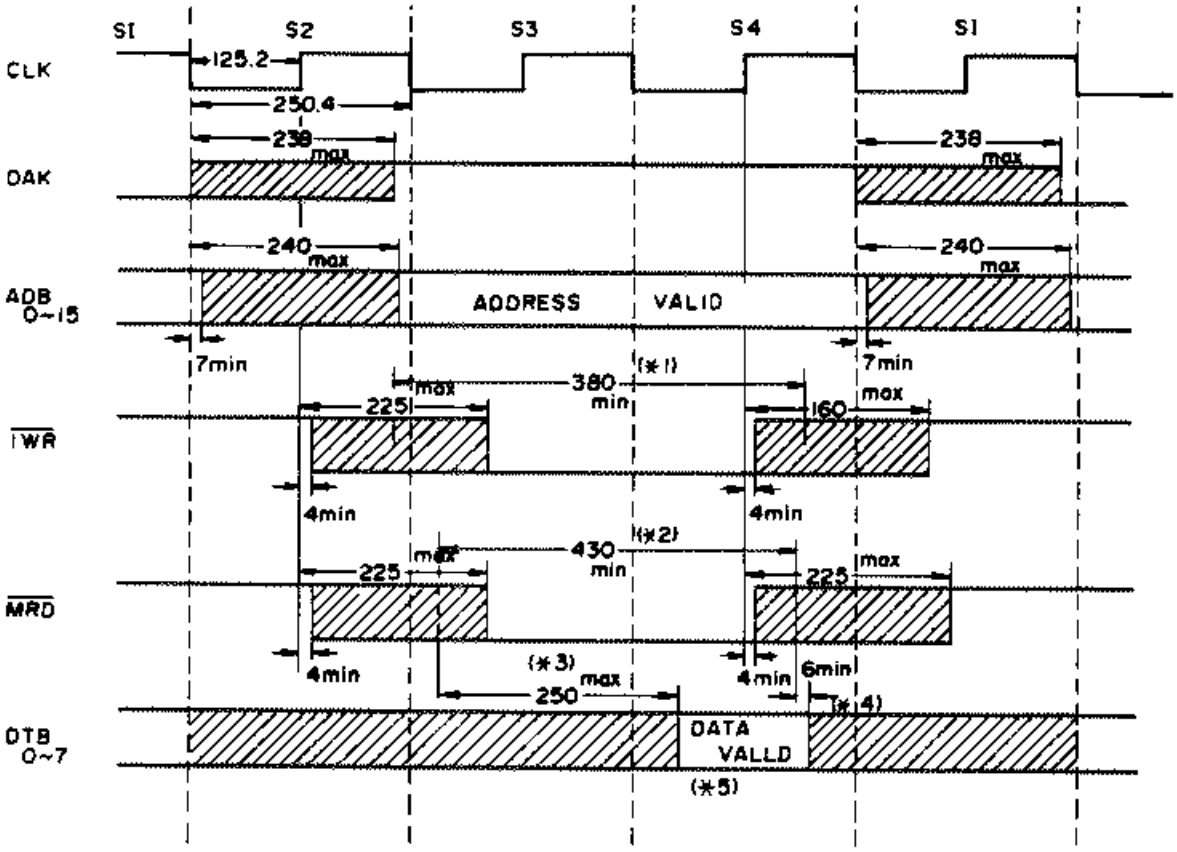
(*2) Data bus stabilization time preceding the falling edge of $\overline{MWR}$.

(*3) Data bus holding time following the rising edge of $\overline{MWR}$.

## 2.5. DMA Access Timing

### (1) Memory read, I/O write timing

[Unit: nsec]




(*1) Low level pulse width of $\overline{IWR}$.

(*2) Low level pulse width of $\overline{MRD}$.

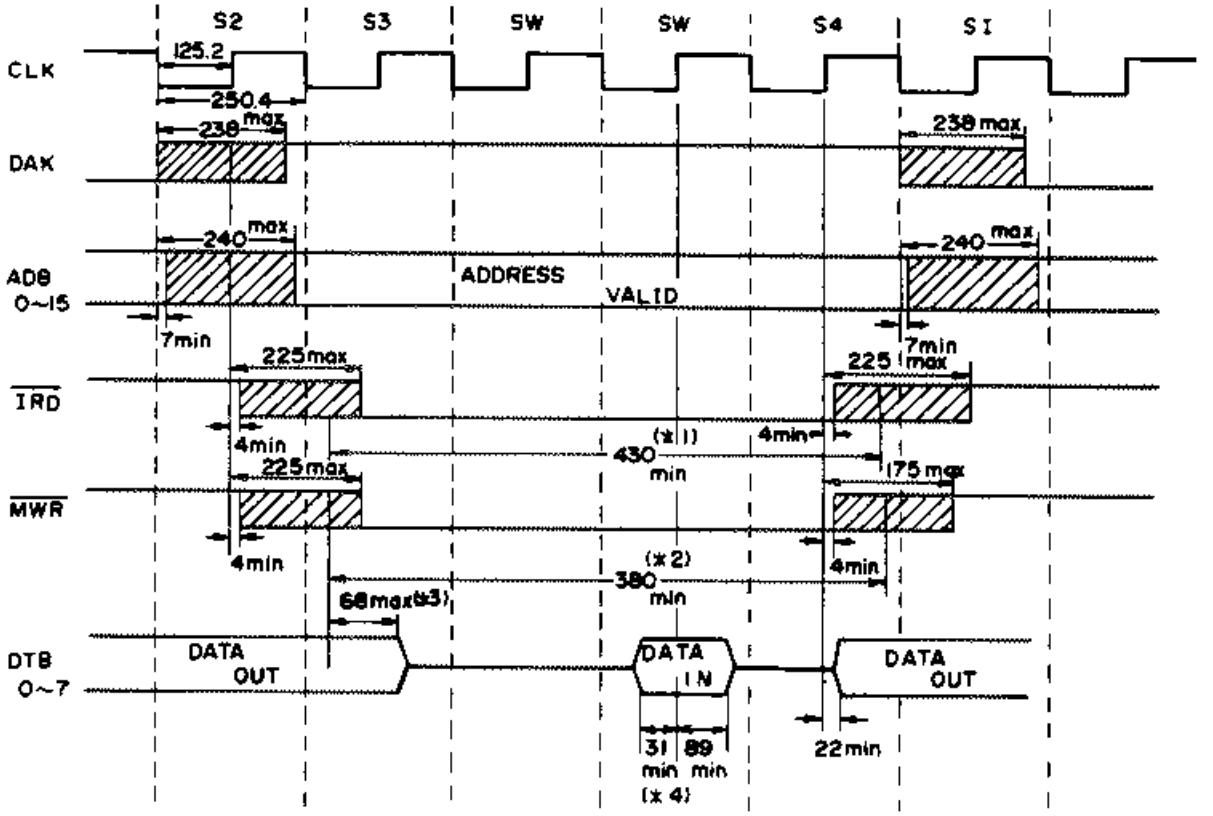
(*3) Data bus stabilization time following the falling edge of $\overline{MRD}$.

(*4) Data bus holding time following the rising edge of $\overline{MRD}$.

(*5) Data from internal memory to I/O in DMA.

(2) I/O read, memory write timing

[Unit: nsec]




(*1) Low level pulse width of $\overline{IRD}$.

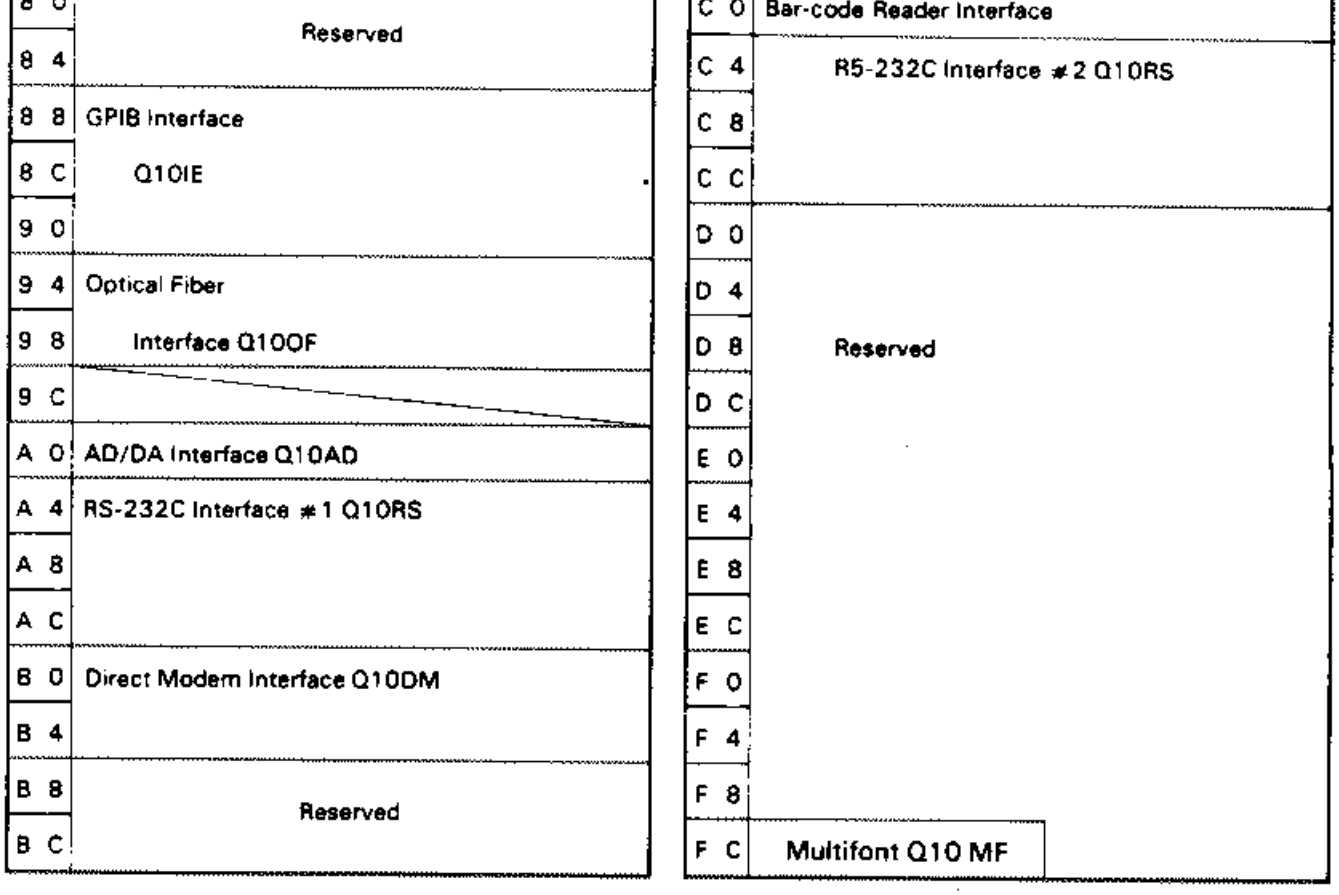
(*2) Low level pulse width of $\overline{MWR}$.

(*3) Time following the falling edge of $\overline{MWR}$ before the data bus starts floating.

(*4) Limitation of input data from I/O to internal memory.

## 2.6. I/O Port Address Map for Options

The addresses of I/O ports allocated for options are from 80H to FFH. Of these, some are already assigned to existing interface cards. Therefore, when other option cards are prepared, contact the Electronic Instruments Design Dept. of the EPSON Corporation for confirmation that the addresses are free. (This precaution must be observed to prevent the same port from being allocated to more than one option.)


8 0
Reserved
8 4
8 8
GPIB Interface
8 C
Q10IE
9 0
9 4
Optical Fiber
9 8
Interface Q10OF
9 C
A 0
AD/DA Interface Q10AD
A 4
RS-232C Interface #1 Q10RS
A 8
A C
B 0
Direct Modem Interface Q10DM
B 4
B 8
Reserved
B C
C 0
Bar-code Reader Interface
C 4
RS-232C Interface #2 Q10RS
C 8
C C
D 0
D 4
D 8
Reserved
D C
E 0
E 4
E 8
E C
F 0
F 4
F 8
F C
Multifont Q10 MF

## 2.7. Precautions on Making Interface

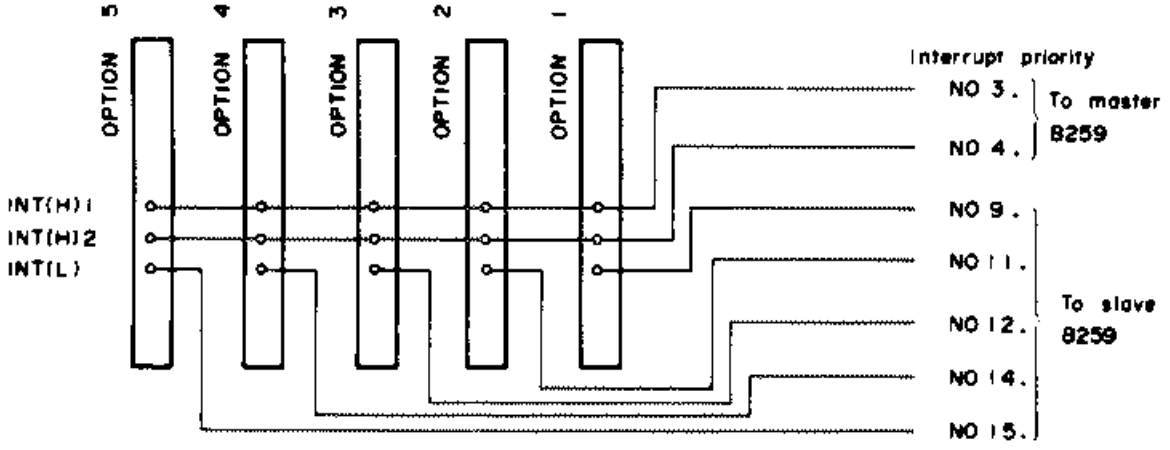
Take note of the following when preparing option cards.

(1) $\overline{\text{RSIN}}$ (Reset signal)

$\overline{\text{RSIN}}$ is the input signal for system reset. Since this signal is directly input to the CPU reset terminals with no particular synchronization, it is recommended that it be synchronized with the rising edge of the read/write pulse and that the pulse width be held to less than 1 mS when D-RAM data is to be saved, however, note that the pulse width must be greater than three clocks.

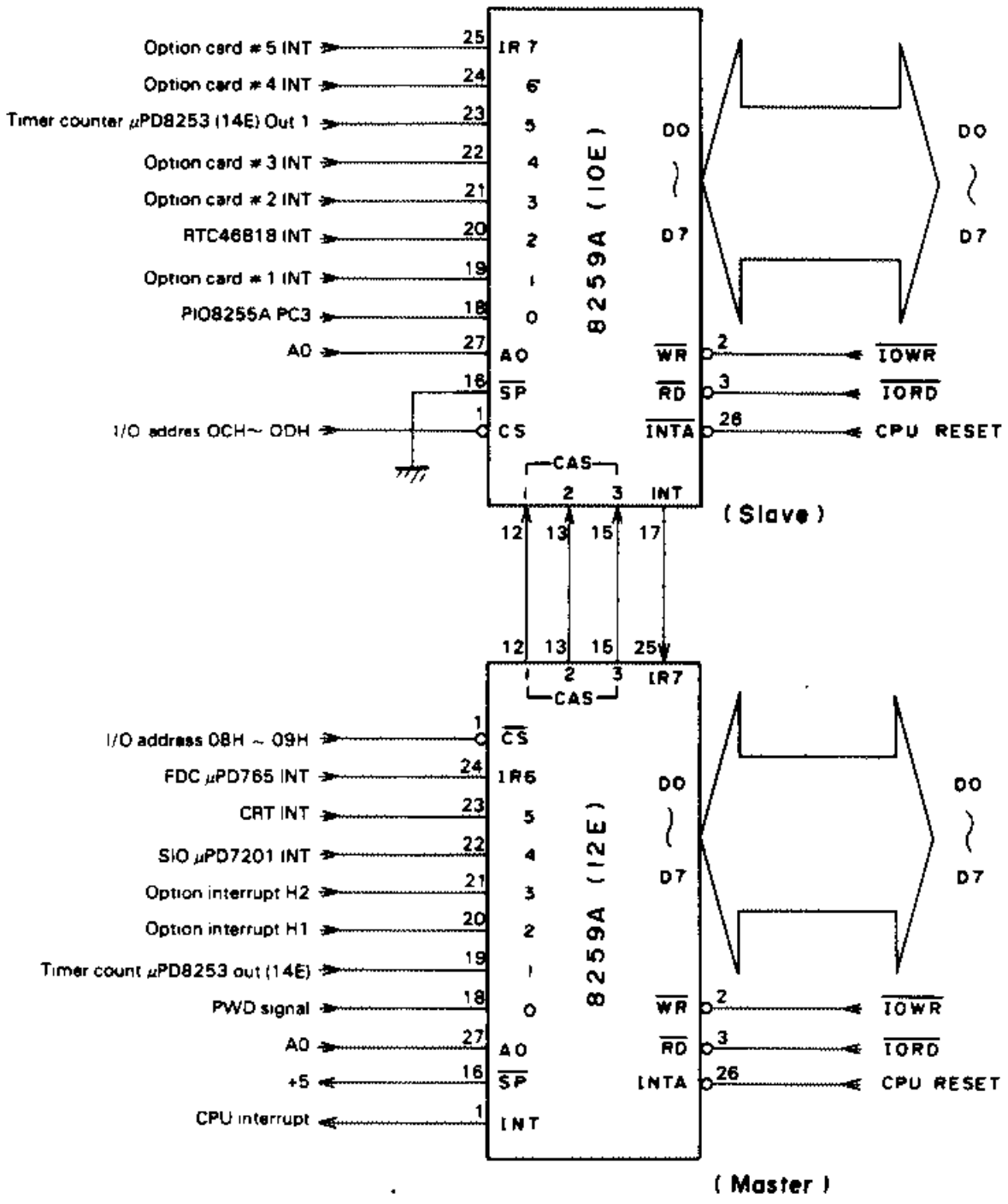
(2) Difference between INT(H) and INT(L) (Interrupt request signals)

Although there are three types of interrupt request signals (INT(H) 1, INT(H) 2, and INT(L)) for each option connector, INT(H) 1 and INT(H) 2 are common to all of the connectors. Therefore, only one card which utilizes INT(H) 1 or 2 can be used at any given time. However, since INT(L) is assigned to the various connectors individually, it can be used with several cards simultaneously. Connection of the INT(H) and INT(L) interrupts on the main board is shown below.



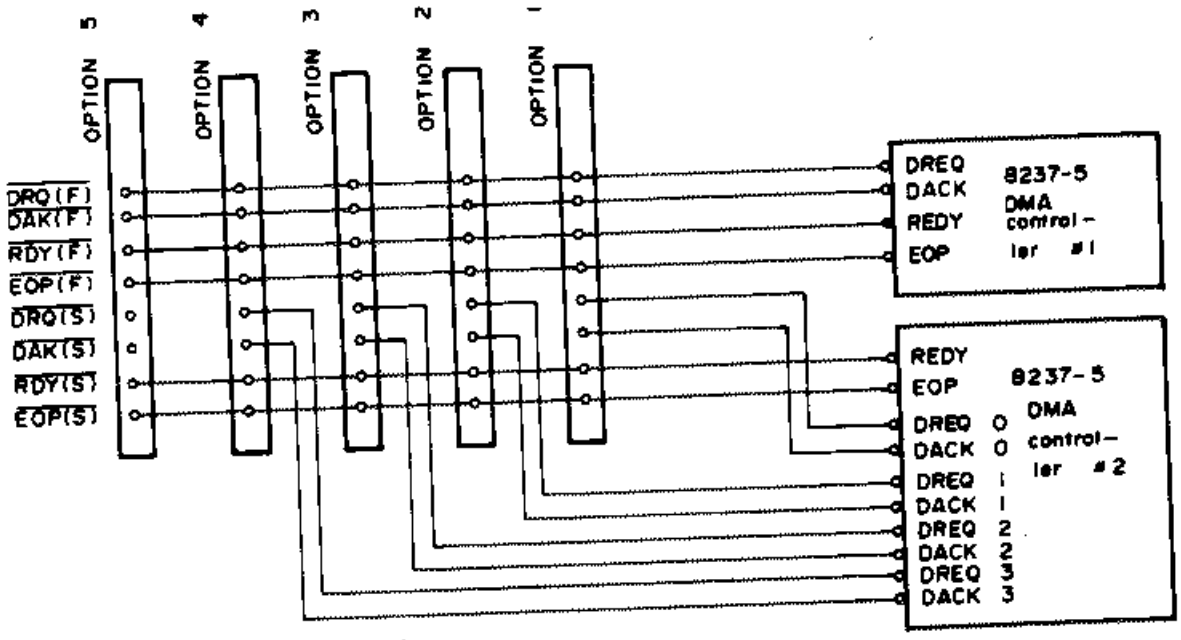
| Connection | | Relative address | Interrupt cause | |
|---|---|---|---|---|
| Master | IR0 | 0000 | Power down detection interrupt | High-order |
| | IR1 | 0004 | Software timer # 1 interrupt | |
| | IR2 | 0008 | External (option) interrupt INTF 1 | |
| | IR3 | 000C | External (option) interrupt INTF 2 | |
| | IR4 | 0010 | Keyboard/RS-232C interrupt | |
| | IR5 | 0014 | CRT/light pen interrupt | |
| | IR6 | 001B | Floppy controller interrupt | |
| | | | | Priority |
| Slave | IR0 | 0020 | Printer interrupt | |
| | IR1 | 0024 | External (option) interrupt # 1 | |
| | IR2 | 0028 | Calendar clock interrupt | |
| | IR3 | 002C | External (option) interrupt # 2 | |
| | IR4 | 0030 | External (option) interrupt # 3 | |
| | IR5 | 0034 | Software timer # 2 interrupt | |
| | IR6 | 0038 | External (option) interrupt # 4 | |
| | IR7 | 003C | External (option) interrupt # 5 | Low-order |

Interrupt addresses


Option card # 5 INT
Option card # 4 INT
Timer counter μPD8253 (14E) Out 1
Option card # 3 INT
Option card # 2 INT
RTC46818 INT
Option card # 1 INT
PIO8255A PC3
A0
I/O addres OCH~ ODH
25
24
23
22
21
20
19
18
27
16
1
IR 7
6
5
4
3
2
1
0
A0
SP
CS
8259A (10E)
DO
D7
WR
RD
INTA
2
3
26
IOWR
IORD
CPU RESET
CAS
1
2
3
INT
(Slave)
12
13
15
17
12
13
15
25
IR7
I/O address 08H ~ 09H
FDC μPD765 INT
CRT INT
SIO μPD7201 INT
Option interrupt H2
Option interrupt H1
Timer count μPD8253 out (14E)
PWD signal
A0
+5
CPU interrupt
1
24
23
22
21
20
19
18
27
16
1
CS
IR6
5
4
3
2
1
0
A0
SP
INT
8259A (12E)
DO
D7
WR
RD
INTA
2
3
26
IOWR
IORD
CPU RESET
(Master)

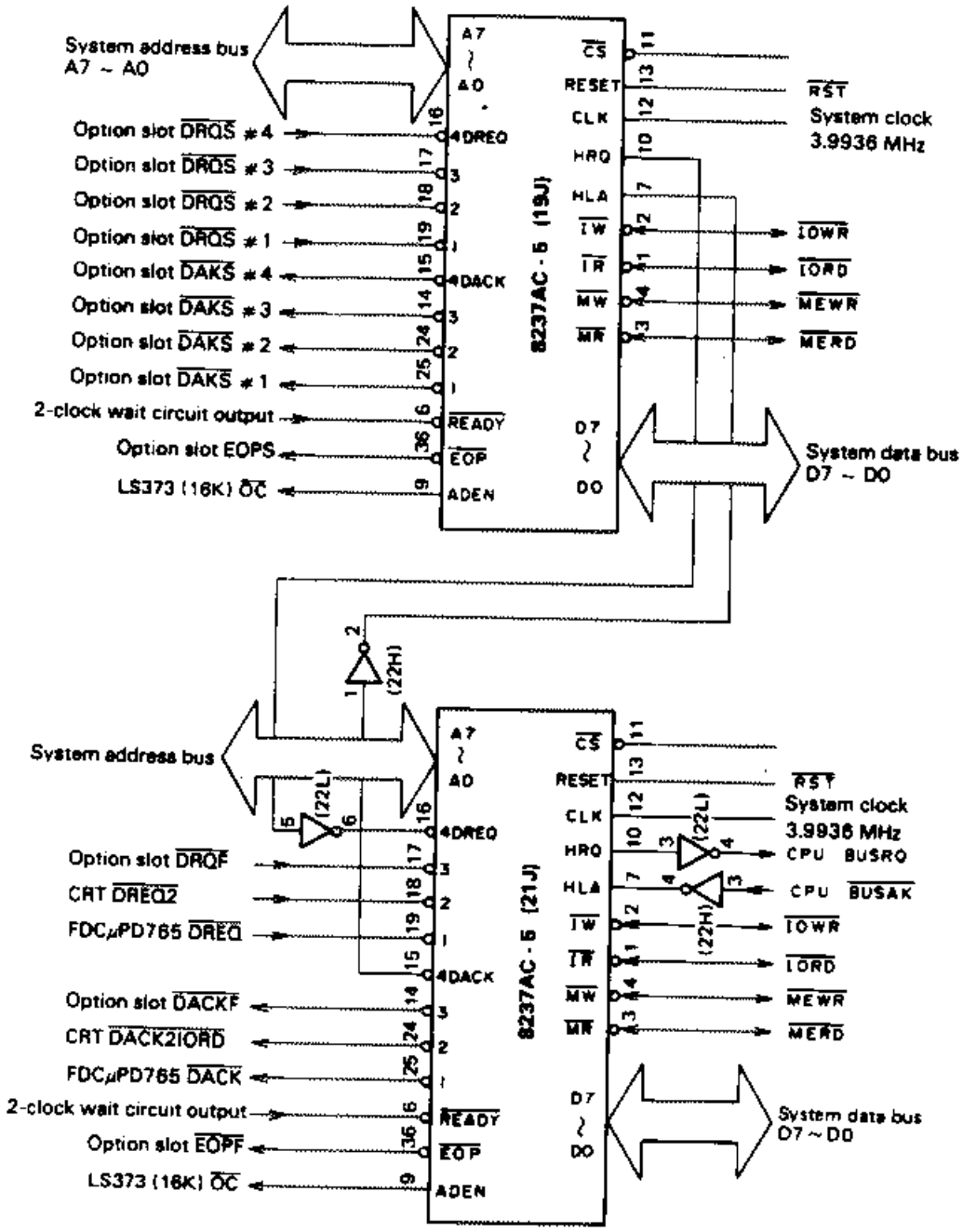
(3) Difference between $\overline{DRQ(F)}$ and $\overline{DRQ(S)}$

There are also two types of DMA request signals for each option connector, $\overline{DRQ(F)}$ and $\overline{DRQ(S)}$. $\overline{DRQ(F)}$ is common to all of the connectors, while $\overline{DRQ(S)}$ is assigned individually. However, $\overline{DRQ(S)}$ and $\overline{DAK(S)}$ are not connected to option connector 5.
Also, $\overline{RDY(F)}$ and $\overline{EOP(F)}$ corresponding to $\overline{DRQ(F)}$ and $\overline{DRQ(S)}$ are common to all of the connectors, as are $\overline{RDY(S)}$ and $\overline{EOP(S)}$.
This is because all the $\overline{DRQ(S)}$ signals use the same DMA controller. Finally, $\overline{DAK(S)}$ is individually assigned to all of the connectors in the same manner as $\overline{DRQ(S)}$.
These relationships are shown in the figure below.



| Channel | | Connection | |
|---|---|---|---|
| Master | 1 | Floppy disk | High |
| | 2 | Monitor | |
| | 3 | Option slots (One of OP # 1 through OP # 5) | |
| | | | Priority |
| Slave | 1 | Option slots (OP # 1) | |
| | 2 | Option slots (OP # 2) | |
| | 3 | Option slots (OP # 3) | |
| | 4 | Option slots (OP # 4) | Low |

DMA request level




DMA.controller μPD8237

(4) Difference between $\overline{\text{BSAK}}$ and $\overline{\text{DAK}}$

Both of these signals are active during DMA operation, but whereas $\overline{\text{BSAK}}$ is active during all DMA operations (i.e., the signal is output even when the CPU is stopped), $\overline{\text{DAK}}$($\overline{\text{DAK(F)}}$ or $\overline{\text{DAK(S)}}$) becomes active only when the corresponding $\overline{\text{DRQ}}$ is accepted and that DMA is operating. For this reason, it is recommended that these two signal types be used as follows.

a. $\overline{\text{BSAK}}$ should be ANDed upon I/O port address decoding and the I/O port non-selected when it is LOW. (This is because the address bus contains a memory address when $\overline{\text{BSAK}}$ is LOW.)

b. Use $\overline{\text{DAK}}$ for chip selection of the I/O port outputting the corresponding $\overline{\text{DRQ}}$.

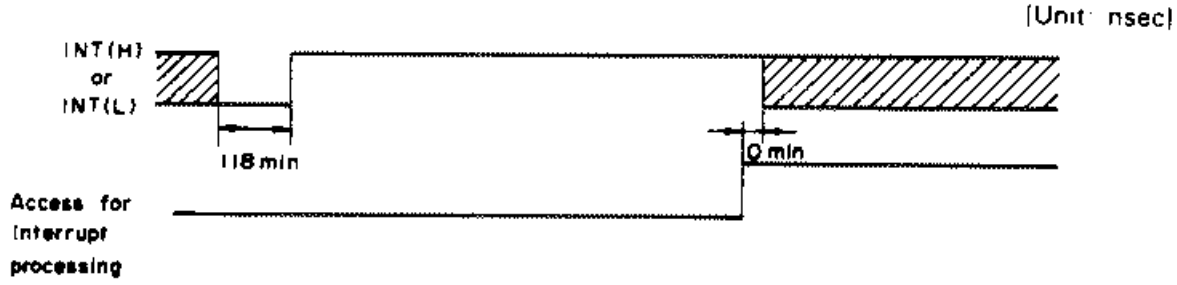
It is particularly important that $\overline{\text{BSAK}}$ is used as described, since incorrect operation will result (regardless of whether the DMA is used) if this processing is not performed.

(5) External memory select

$\overline{\text{MEMX}}$ is required when the option card includes memory. This signal becomes LOW when bit 3 in the memory bank register is 1 and neither P-ROM, C-MOS RAM, nor the common area are selected. Thus, programming considerations are necessary when external memory (on the option card) is to be used. In other words, when external memory is to be selected, bit 3 in the memory bank register must be set to 1 and bits 7 - 4 (the internal memory bank) must be set to 0 so that memory on the main board is not selected. Note must also be taken of the fact that the resident RAM area cannot be placed on external memory.

(6) Interrupt processing

Interrupts from the option slots are controlled by the INT(H) or INT(L) signals. An 8259A is used as the interrupt controller in the main system, and the INT signals are connected directly to the IR terminal of this 8259A. When the INT signal goes from LOW to HIGH, it must be kept HIGH from its rising edge until the $\overline{\text{INTA}}$ from the CPU has been accepted by the 8259A; however, since the $\overline{\text{INTA}}$ signal is not output to the option connector, the INT signal must also be kept HIGH until interrupt processing is started for that device. Finally, since a rising edge is necessary, be sure to observe the rules concerning the duration of the LOW level for the INT signal. These considerations are outlined in the figure below.

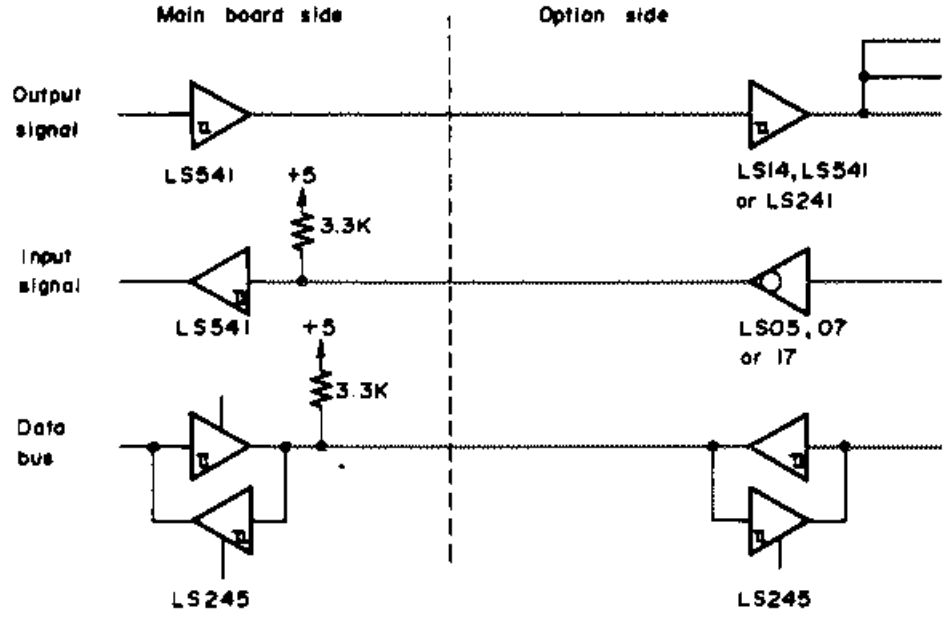


(7) Notes concerning inclusion of options in the OS

When option cards are prepared, some additional circuit must be provided to make it possible for the OS to determine whether previously reserved options are present, and to allow it to automatically control interrupt tables and so forth. The OS must use the following sequence to determine whether the various options are connected to the option connectors.
First, data is output to the ports designated for each option (with a different port for each option); depending on the option, the content of the data may also be designated. If the applicable option is connected, an interrupt is generated, causing INT(H) or INT(L) to go HIGH. In the case of an INT(L) interrupt, the main system is able to determine the slot to which the card is connected from the interruption address, which differs according to slot number. If the option card is not connected, the OS recognizes the fact because no interrupt is generated.
Therefore, a circuit must be provided so that an interrupt is applied when data is written into one of the port addresses assigned to options controlled by the OS, and to clear the interrupt when that same port is read out.

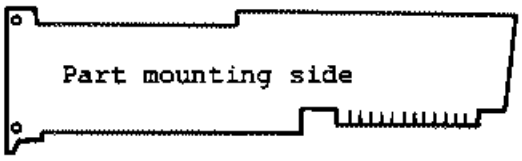
(8) I/O signal interface

All input signals fed to the main board from the option side are pulled up by 3.3K ohm resistors. These signals (other than bidirectional data bus signals) are received by the 74LS541, and therefore should be controlled by an open collector circuit. The 74LS541 is also used for driving output signals (other than data bus signals) which are fed to the option side from the main board.
The option side should be provided with a one-stage buffer for connection of multiple options.
I/O switching for the data bus must be controlled by the 74LS245 bidirectional bus buffer on the main board, as well as on the option side. This is to prevent data conflicts.
Signal lines which are not used must be left open.
The recommended I/O interface circuit is shown below:

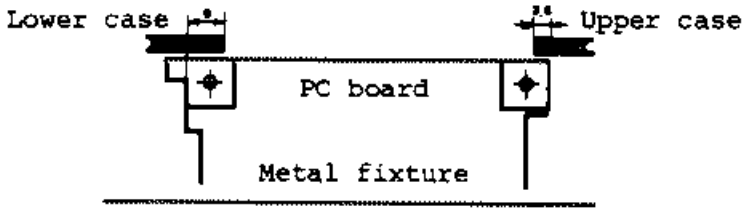


## 2.8. Mounting of parts

° Parts should be mounted only on the part mounting side of PC board (the side at the front when the slot connector is located right below) taking care to set the height of part to within 15 mm from the PC board surface, and not to make contact between the part and PC board surface or between parts.




° All parts, except for the external interface connector, should be mounted inside the PC board contour.
When mounting the external interface connector, refer to the following drawing as the connector position and size are restricted by the case cover.

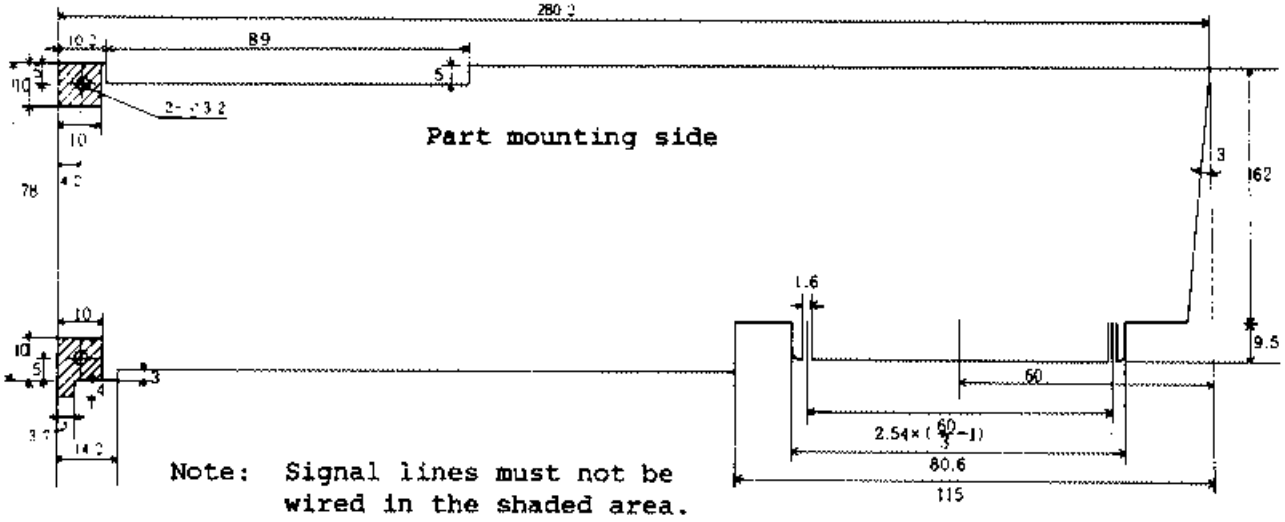



° Wiring should be as short as possible on the PC board, and be fixed as required.

° Lead wires (lead wires of IC resistor, etc.) on the soldered side (rear side of part mounting side) should be 1 - 2 mm high from the PC board surface and arranged so as not to make a shortcircuit with the other lead wires.

## 2.9. Outer Dimensions of Option Card

Unit: mm




Note: Signal lines must not be wired in the shaded area.

# CHAPTER 3 Q10MF - MULTIFONT ROM CARD -

## 3.1. General

The Q10MF is a character generator ROM card of 14 x 17 dots provided with six 128-bit mask ROMs, and is mountable on the option slot of QX-10. The characters mounted on this card are supported by the EPSON Multifont CP/M. The multifont characters mounted on Q10MF include the information for proportional printing, enabling proportional printing by choice.

## 3.2. Hardware

### 3.2.1 General

a. The character generator ROM card is controlled by the 8-bit slave CPU8039, and the control program is contained in PROM2716.
The following three kinds of ROMs are mounted on the character generator ROM card.

| RON location | | Multifont ROM card |
|---|---|---|
| #1 | 1A | KA10 (M12020A) |
| #2 | 2A | M12030CA |
| #3 | 1B | M12031CA |
| #4 | 2B | M12032CA |
| #5 | 3A | M12033CA |
| #6 | 3B | M12034CA |
| #7 | 1C | |
| #8 | 2C | |

Table 3-1

(ROM in use: HITACHI HN43128)

* The above ROM includes fonts of 512 characters each.

Three flags (IBF, OBF and ERR) are provided for data transfer with the main system, and the font codes and patterns are transferred by way of handshaking.
(For details, refer to the Software section.)

b. The printed circuit board of the multifont character generator ROM card is the same and is discriminated by the mounted mask ROM and jumper switch setting. Jumper switch setting and I/O address are as shown below.

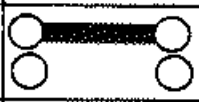
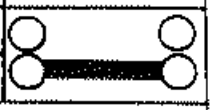
| | I/O address | | Jumper J2 | | Jumper J1 |
|---|---|---|---|---|---|
| Multifont ROM card (Q10MF) | FC | FD |  | A B |  |
| | R | | Pattern data | | |
| | W | | Pattern code | | |
| | | R | STATUS | | |
| | | W | INTERRUPT | | |

Table 3-2

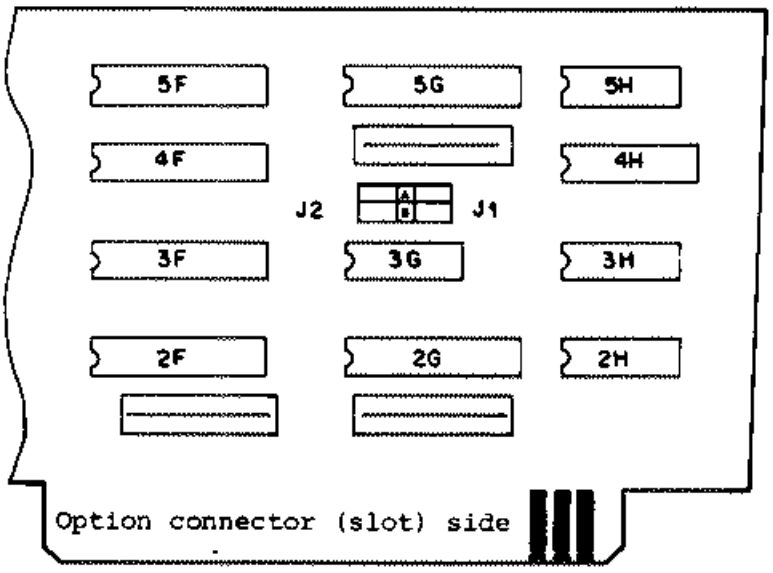



Fig. 3-1

### 3.2.2 Block diagram

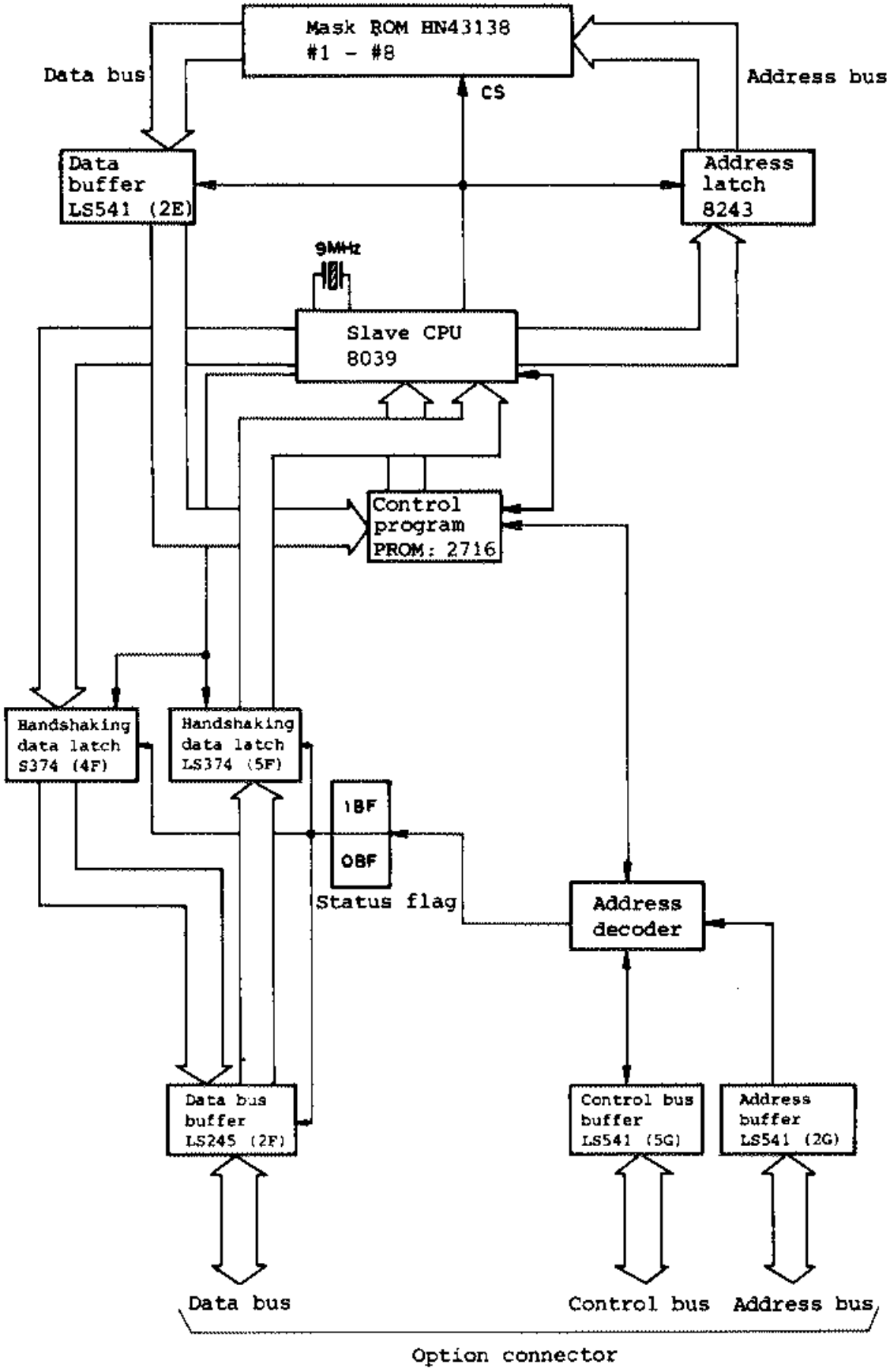



Fig. 3-2

### 3.2.3 Data flow

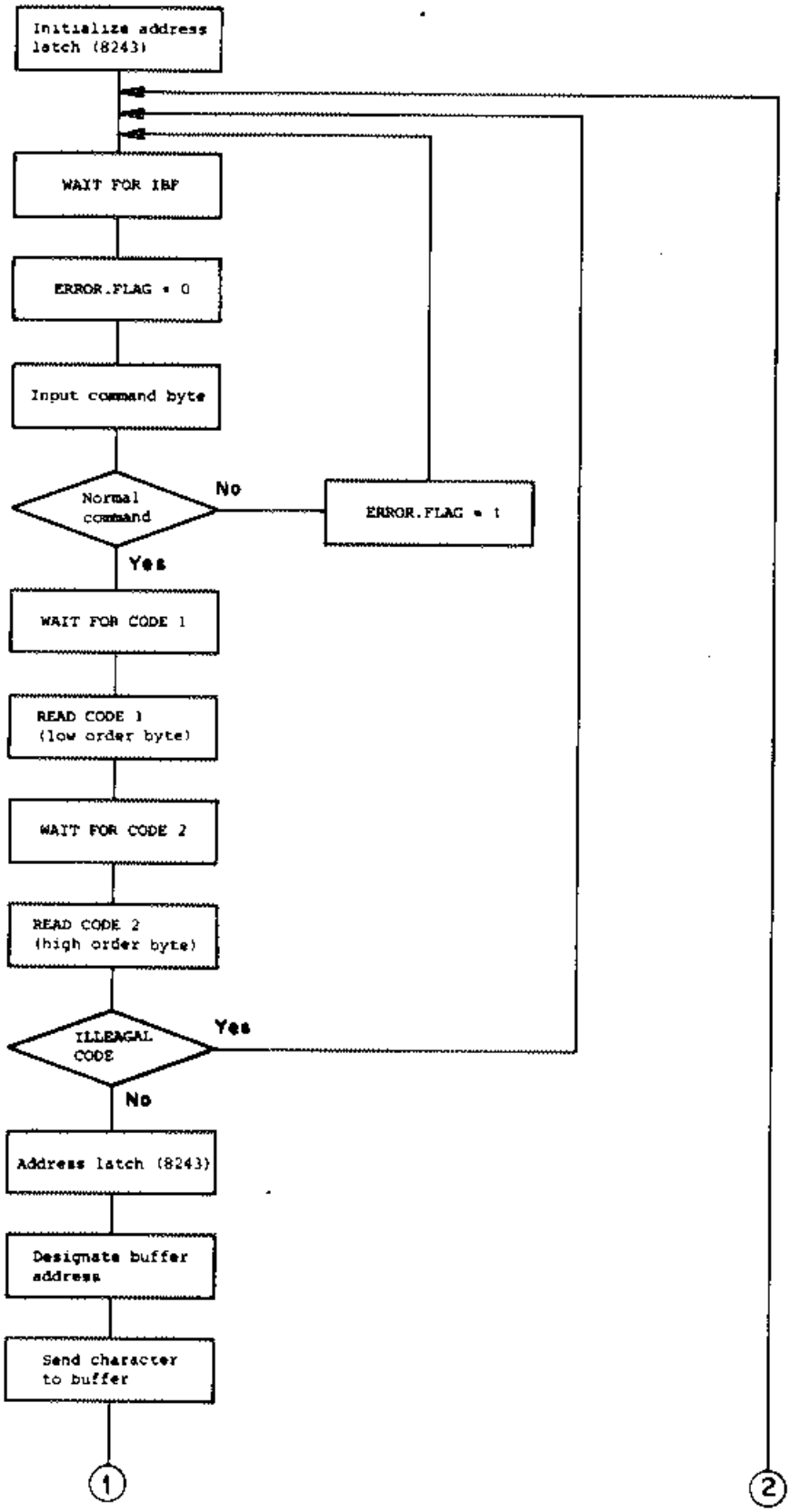
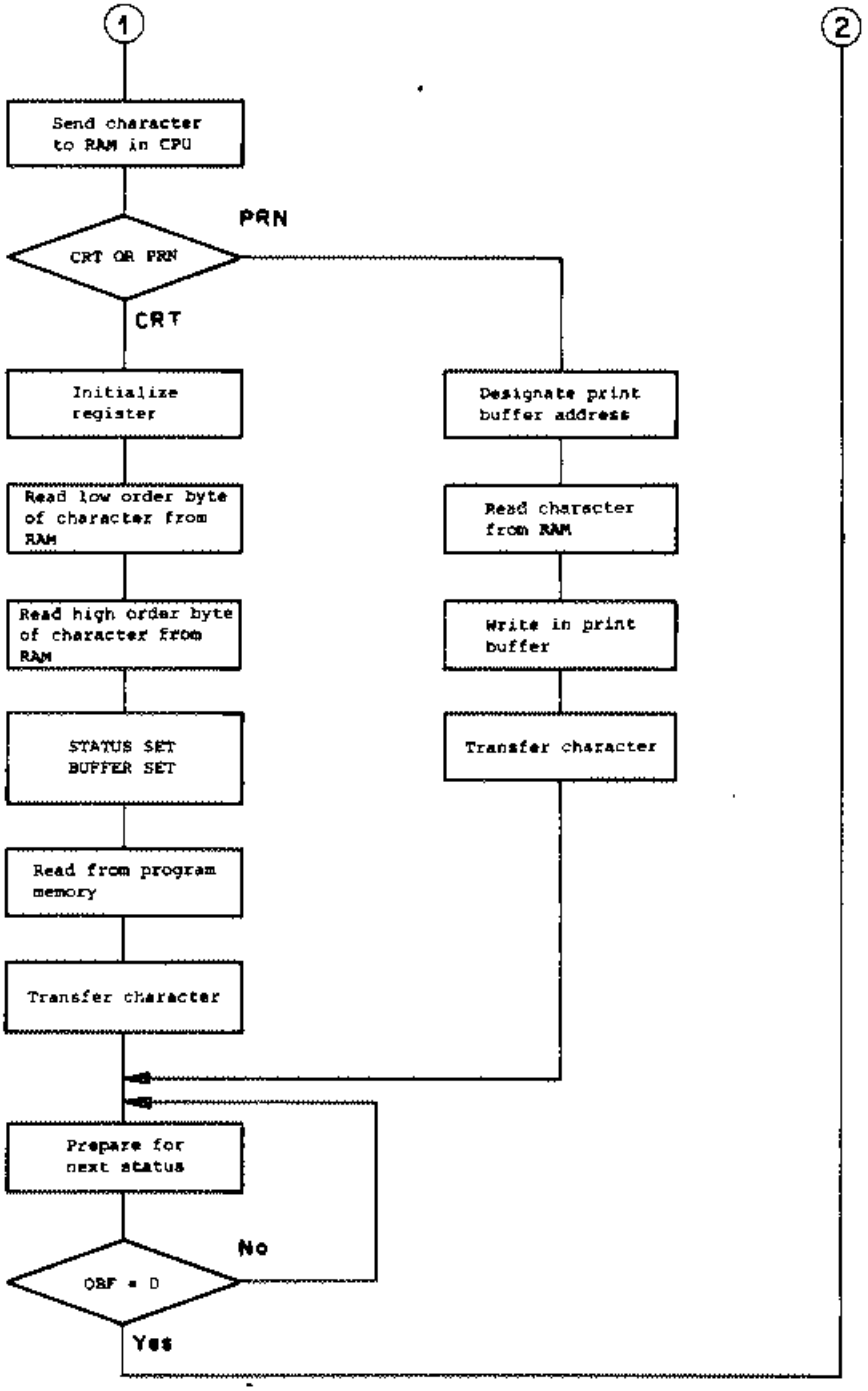



Fig. 3-3


1
2
Send character to RAM in CPU
CRT OR PRN
PRN
CRT
Initialize register
Read low order byte of character from RAM
Read high order byte of character from RAM
STATUS SET
BUFFER SET
Read from program memory
Transfer character
Designate print buffer address
Read character from RAM
Write in print buffer
Transfer character
Prepare for next status
OBF = 0
No
Yes

## 3.3. Software

Two commands, status port and data port are input to the Q10MF option card.

(1) Status port (FDH: Set by the jumper wires.)

A. When this port is read, the following status can be read.

| IBF | X | X | X | X | X | ERR | OBF |
|---|---|---|---|---|---|---|---|

IBF
- 0: Character pattern not readable
- 1: Character pattern readable

ERR
- 0: Normal
- 1: Error

OBF
- 0: Character code writable
- 1: Character code not writable

B. When data (contents are optional) is written into this port, the hardware interrupt is effected in INT (L).
As this interrupt signal line is assigned to separate interrupt addresses for each option slot, the slot in which the Q10MF is inserted can be discriminated.
To reset this interrupt, read the status port.

(2) Data port (FCH: Set by the jumper wires.)

A. Data to be written in this port consists of the following three bytes.

Command byte: A command to specify use of the pattern read from the character generator for CRT or printer.

| 1 | MODE | 0 | 0 | 0 | 0 | 0 | bit |
|---|---|---|---|---|---|---|---|

MODE 0: Pattern mode for printer
1: Pattern mode for CRT

bit 0: Pattern for CRT (1) For NON-DMA
1: Pattern for CRT (2) For DMA

Character code byte: Sends the high order and low order codes of the character code in that order, following the command byte. However, the character code is in a range of 0000H - 0DFFH, and a code out of this range will be error.

| Low order byte of character code |
|---|

| High order byte of character code |
|---|

To write the above three bytes into the option card, they must be written one by one while confirming that the "OBF" bit becomes 0 in the status port. When the Q10MF option card receives and becomes ready for reading the character pattern, INT (L) is interrupted.
(To reset this interrupt, read the status post.)

B. Character pattern is read from the data port.

Status byte: Before the character pattern, the data indicating the status information of that character pattern is read.

| VALID | MODE | 0 0 | UP | RIGHT | LEFT | DOWN |
|---|---|---|---|---|---|---|

VALID
0: Character code is invalid.
1: Character code is valid.

MODE
0: Pattern for printer
1: Pattern for CRT

| | | |
|---|---|---|
| UP | Extension in the up direction | No (0) Yes (1) |
| RIGHT | Extension in the right direction | No (0) Yes (1) |
| LEFT | Extension in the left direction | No (0) Yes (1) |
| DOWN | Extension in the down direction | No (0) Yes (1) |

Character pattern: Pattern information differs as follows for CRT and printer.

## Pattern for Printer

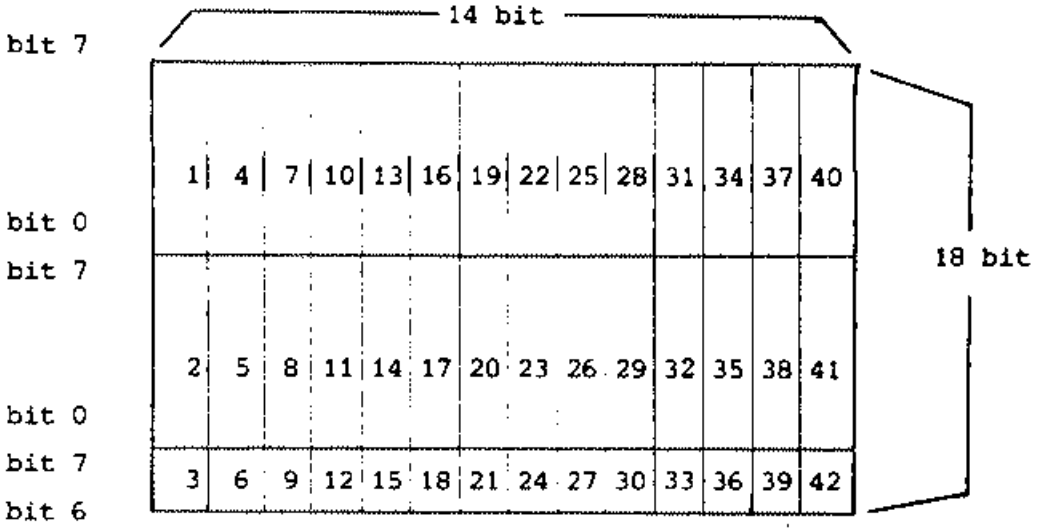



Fig. 3-4

## Pattern for CRT (1)

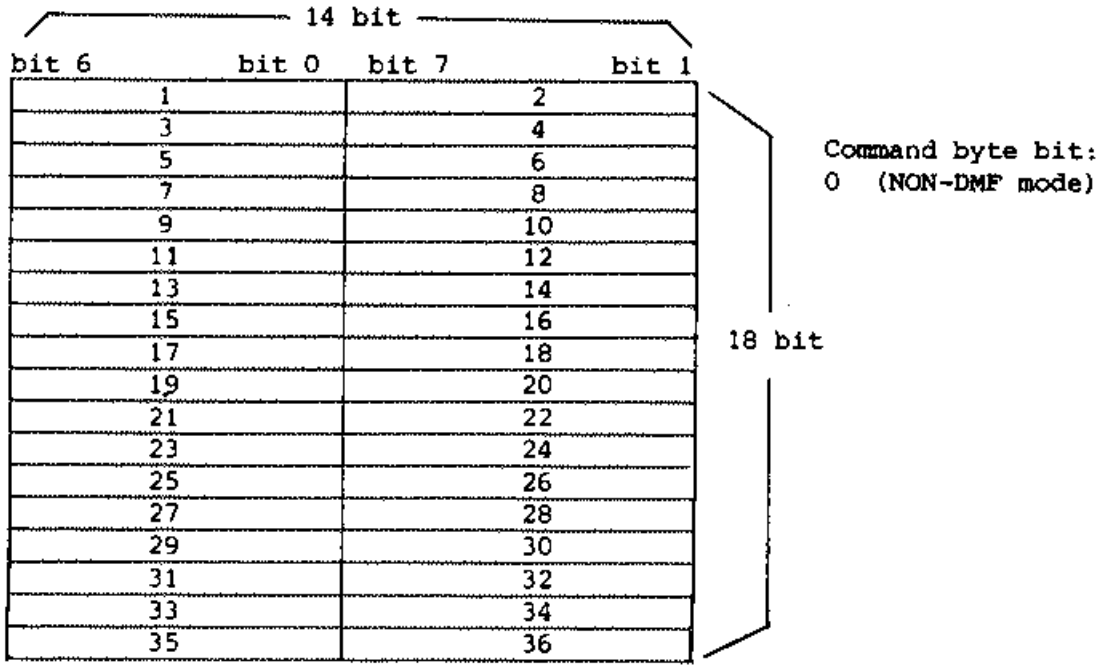



Fig. 3-5

## Pattern for CRT (2)

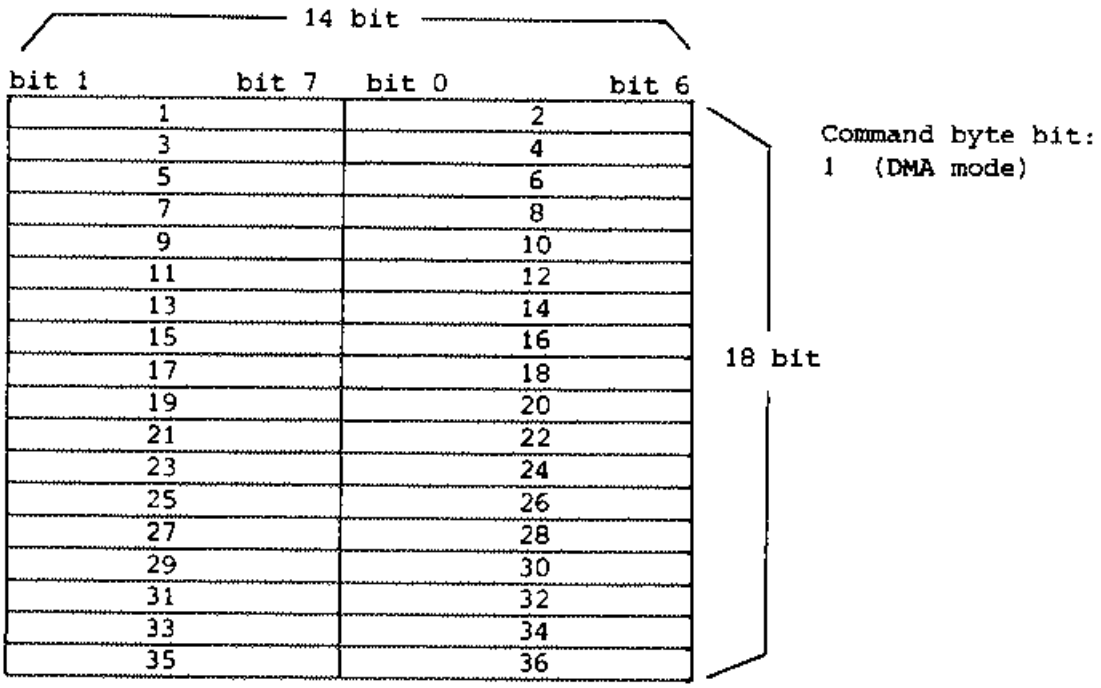
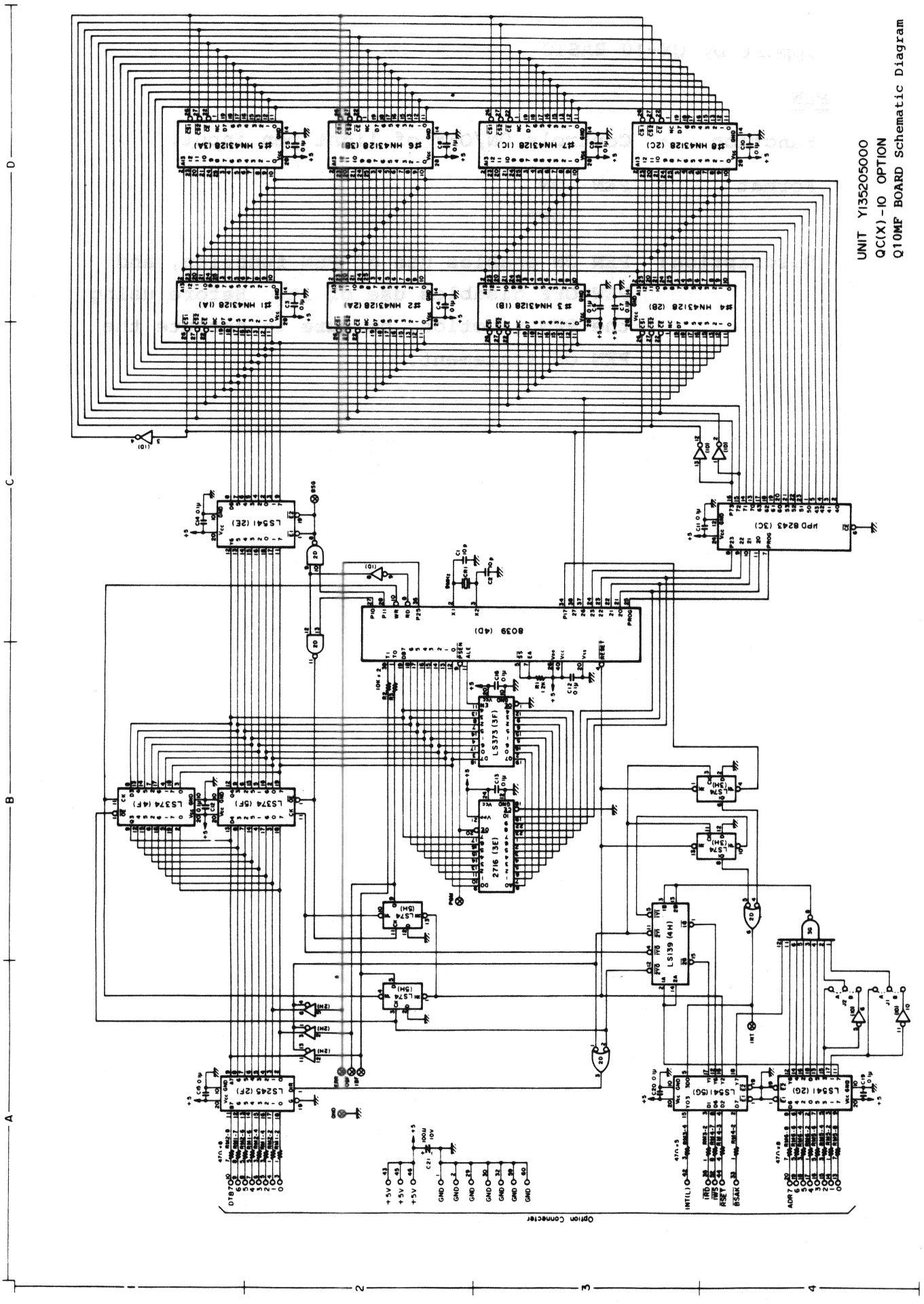



Fig. 3-6

To read these patterns, the bytes must be read one by one each time IBF becomes 1 while monitoring the IBF bit in the status port.


UNIT Y135205000
QC(X)-10 OPTION
Q10MF BOARD Schematic Diagram
#1 HN43128 (1A)
#2 HN43128 (2A)
#3 HN43128 (1B)
#4 HN43128 (2B)
#5 HN43128 (3A)
#6 HN43128 (3B)
#7 HN43128 (1C)
#8 HN43128 (2C)
LS541 (2E)
LS374 (4F)
LS374 (5F)
LS245 (2F)
8039 (4D)
LS373 (3F)
2716 (3E)
LS139 (4H)
LS541 (5G)
LS541 (2G)
μPD 8243 (3C)
Option Connecter

# CHAPTER 4 Q10RS - RS-232C INTERFACE CARD -

## 4.1. General

The Q10RS is an option card for RS232C interface and is used to support asynchronous and synchronous (SDLC.BY-SYNC) communication. The transfer speed can be set by the software, and is usable up to 19200 BPS in asynchronous mode. In this option card, the address can be changed by the jumper wires. Up to two cards at a time can be mounted on the option slot. As the Q10RS can support the 2-channel RS232C port, up to five channels can be mounted together with the standard RS232C port.

| | | |
|---|---|---|
| Cables: | For modem | #523 |
| | For Null modem | #524 |
| | Branched cable | #525 |

## 4.2. Hardware

### 4.2.1. General

The Q10RS uses the μPD7201 as a serial controller, which supports asynchronous and synchronous communication. The counter timer μPD8253-5 is also provided to supply transmission and reception clocks for the μPD7201. The driver/receiver of RS-232C employs 75188/75189, and the supply voltage is ±12 V.
The μPD7201 has two transmission and reception channels A and B, which support up to two channels of RS-232C. The ID check circuit is also provided to check if the Q10RS card is mounted. Interface with CPU permits polling or interrupt.

## 4.2.2 Block diagram

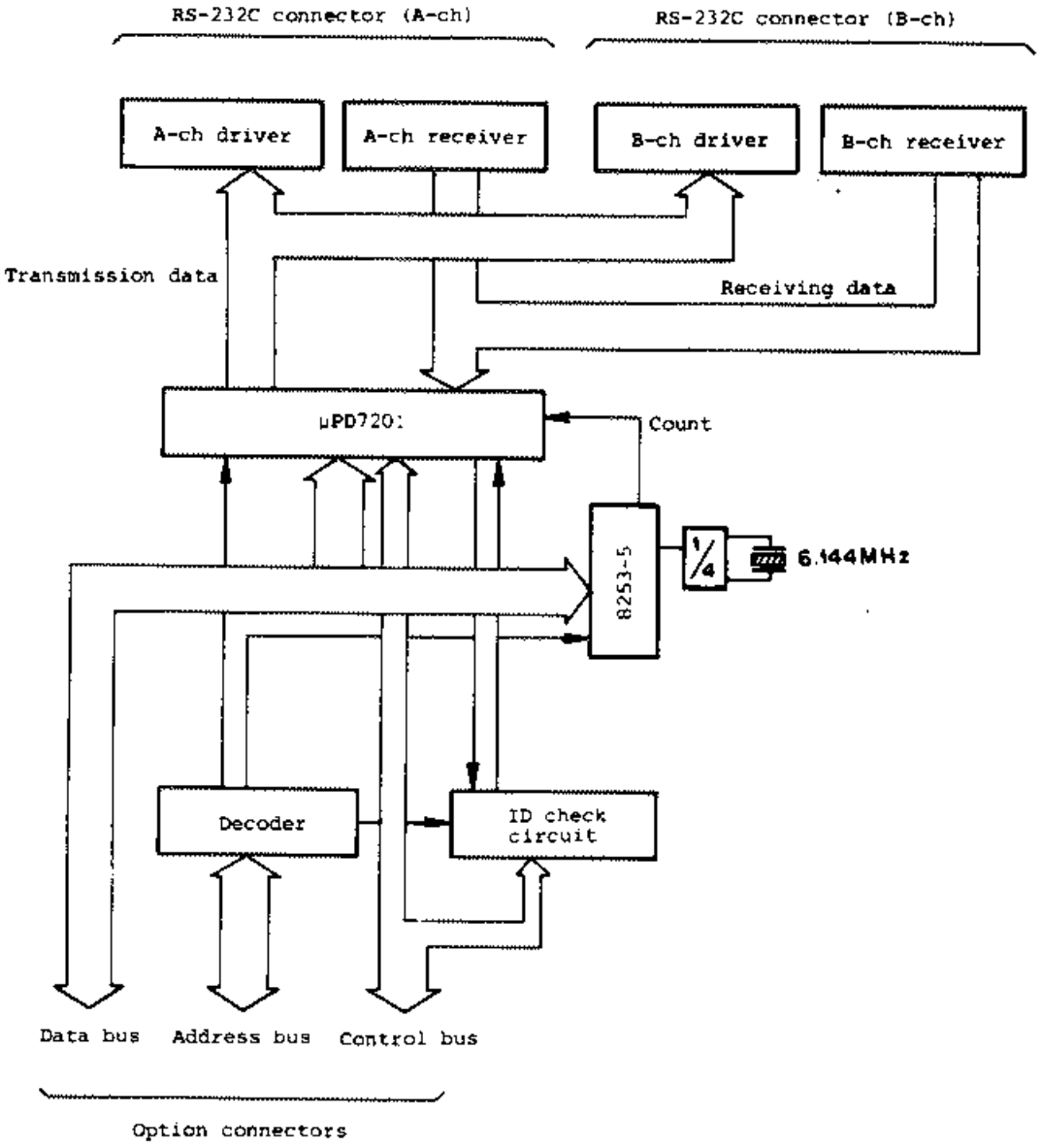



Fig. 4-1

### 4.2.3 RS-232C connectors

| Pin No. | Signal name | Channel | Function | Remarks |
|---|---|---|---|---|
| 1 | AA (FG) | —— | Safety ground | |
| 2 | BA (TXD) | A-ch | Transmission data | 7201 |
| 3 | BB (RXD) | A-ch | Receiving data | 7201 |
| 4 | CA (RTS) | A-ch | Transmission request | 7201 |
| 5 | CB (CTS) | A-ch | Transmission enable | 7201 |
| 6 | CC (DSR) | A-ch | Data connection finished | Read in LS367. |
| 7 | AB (SG) | —— | Ground for signal | |
| 8 | CF (DCD) | A-ch | Carrier detection | 7201 |
| 9 | | —— | | |
| 10 | | —— | | |
| 11 | REV. | A-ch | | Same as CD. Not provided in RS-232C specifications. |
| 12 | SCF (DCD) | B-ch | Secondary carrier detection | 7201 |
| 13 | SCB (CTS) | B-ch | Secondary transmission enable | 7201 |
| 14 | SBA (TXD) | B-ch | Secondary transmission data | 7201 |
| 15 | DB (TXC) | A-ch | Transmission clock | 7201 |
| 16 | SBB (RXD) | B-ch | Secondary receiving data | 7201 |
| 17 | DD (RXC) | A-ch | Receiving clock | 7201 |
| 18 | DSRB | B-ch | Data connection finished | Read in LS367. (Assigned by EPSON.) |
| 19 | SCA (RTS) | B-ch | Secondary transmission request | 7201 |
| 20 | CD (DTR) | A-ch | Data terminal ready | 7201 |

| | | | | |
|---|---|---|---|---|
| 21 | | —— | | |
| 22 | CE (RING IND) | Common | Call display | Read in LS367. |
| 23 | CH (DATA RATE) | Common | Transfer speed selection | Changed over with the dip switch. |
| 24 | DA (TXC) | | Transmission clock | Output to modem. |
| 25 | DTR B | B-ch | | 7201 (Assigned by EPSON.) |

Table 4-1 Locations of Q10RS connectors

The Q10RS option card includes up to the secondary channel (B-channel) of EIA RS-232C.
At these two channels can be independently controlled, two channels of RS-232C can be used by using a two-branched cable (#525), for example.
However, since secondary DTR and DSR are not defined in the RS-232C specifications, a complete two-channel system cannot be made as it were. So, DTR and DSR are assigned to pins 25 and 18 so that independent two channels of RS-232C can be used.

### 4.2.4 Setting of jumper wires

#### (1) Setting the interface signals

| | Signal name | ON | OFF | Set at delivery |
|---|---|---|---|---|
| J1 | SCB (Secondary CTS) | Pulled up | Not pulled up | ON |
| J2 | SCF (Secondary CD) | Pulled up | Not pulled up | ON |
| J3 | CF (DCD) | Pulled up | Not pulled up | ON |
| J4 | CC (DSR) | Pulled up | Not pulled up | ON |
| J5 | CB (CTS) | Pulled up | Not pulled up | ON |

Table 4-2

#### (2) Setting communication modes

| | Signal name | Asynchronous (set at delivery) | Synchronous | |
|---|---|---|---|---|
| | | | External clock used | Internal clock used |
| J6-A | External transmission clock | OFF | ON | OFF |
| J6-B | Internal transmission clock | ON | OFF | ON |
| J7-A | Internal receiving clock | ON | OFF | OFF |
| J7-B | External receiving clock | OFF | ON | ON |

Table 4-3

## (3) Address map (Option connectors)

| J8-A | J8-B | |
|---|---|---|
| ON | OFF | Mapping addresses at 00A4 (H) - 00AF (H). (Set at delivery.) |
| OFF | ON | Mapping addresses at 00C4 (H) - 00CF (H). |

Table 4-3

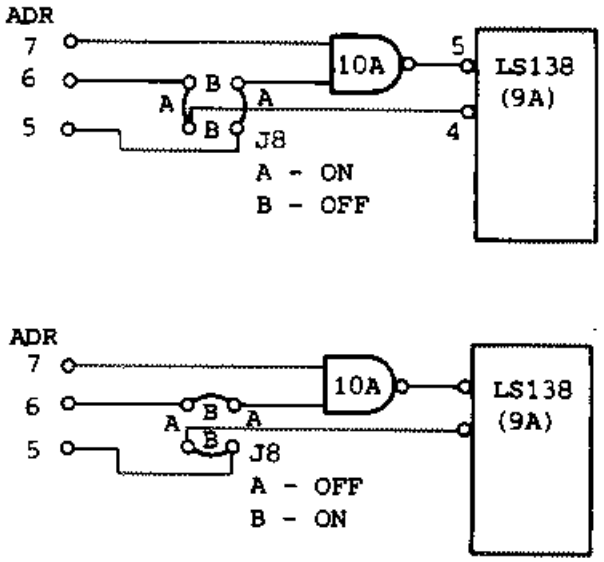



Fig. 4-2

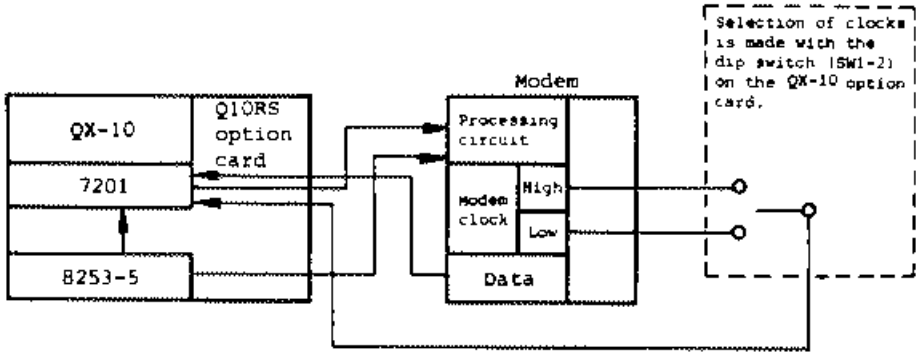
(4) Selecting transfer speeds (Modem clock)

| | ON | OFF | Set at delivery |
|---|---|---|---|
| SW1-1 | Meaningless | | ON |
| SW1-2 | Setting the channel to high level | Setting the channel to low level | ON |
| SW1-3 | Not used | | ON |
| SW1-4 | | | ON |

Table 4-4

When two Q10RS option cards are used in the option slot, setting of JB should be made different.

Reference:




There are two synchronous systems: one is to transmit a clock from the Q10RS option card (using the internal clock) and the other is to receive a clock from the modem (using the external clock). The asynchronous system does not perform transmission and reception of the external clock. The difference between the signals of A and B channels is shown together with pin numbers in the table below. As seen from the table, the pin of TXC.RXC (transmission clock·Reception clock) does not exist in B-channel.

This indicates that the modem (external) clock cannot be used. Therefore, when using the clock from the modem, use the A-channel.
The jumper wires and dip switch should be set to accordingly.

RS-232C interface connectors

| Pin No. | Signal name | Color |
|---|---|---|
| 1 | CG | Shield |
| 2 | TXD (A) | Orange/Red |
| 3 | RXD (A) | Orange/Black |
| 4 | RTS (A) | Gray/Red |
| 5 | CTS (A) | Gray/Black |
| 6 | DSR (A) | White/Red |
| 7 | SG | White/Black |
| 8 | CD (A) | Yellow/Red |
| 12 | CD (B) | Yellow/Black |
| 13 | CTS (B) | Pink/Red |
| 14 | TXD (B) | Pink/Black |
| 15 | TXC | Orange/Red |
| 16 | RXD (B) | Orange/Black |
| 17 | RXC | Gray/Red |
| 18 | DSR (B) | Gray/Black |
| 19 | RTS (B) | White/Red |
| 20 | DTR (A) | White/Black |
| 22 | RING IND. | Yellow/Red |
| 23 | RATE SEL | Yellow/Black |
| 24 | TXC | Pink/Red |
| 25 | DTR (B) | Pink/Black |

Table 4-5

A-channel connectors

| Pin No. | Signal name | Color |
|---|---|---|
| 1 | CG | Shield |
| 2 | TXD (A) | Orange/Red |
| 3 | RXD (A) | Orange/Black |
| 4 | RTS (A) | Gray/Red |
| 5 | CTS (A) | Gray/Black |
| 6 | DSR (A) | White/Red |
| 7 | SG | White/Black |
| 8 | CD (A) | Yellow/Red |
| 11 | DTR (A) | White/Black |
| 15 | TXC | Orange/Red |
| 17 | RXC | Gray/Red |
| 20 | DTR (A) | White/Black |
| 22 | RING IND. | Yellow/Red |
| 23 | RATE SEL | Yellow/Black |
| 24 | TXC | Pink/Red |

B-channel connectors

| Pin No. | Signal name | Color |
|---|---|---|
| 1 | CG | Shield |
| 2 | TXD (B) | Pink/Black |
| 3 | RXD (B) | Orange/Black |
| 4 | RTS (B) | White/Red |
| 5 | CTS (B) | Pink/Red |
| 6 | DSR (B) | Gray/Black |
| 7 | SG | White/Black |
| 8 | CD (B) | Yellow/Black |
| 11 | DTR (B) | Pink/Black |
| 20 | DTR (B) | Pink/Black |

## 4.3. Software

### 4.3.1 I/O MAP of Q10RS

I/O ports assigned for options are available in 80 (H) - FF (H). Among them, A4 (H) - AF and C4 (H) - CF (H) are assigned to Q10RS. This permits mounting of up to two cards at a time on the option slot by changing setting of the jumper wire (J8).
The I/O map is as shown below.

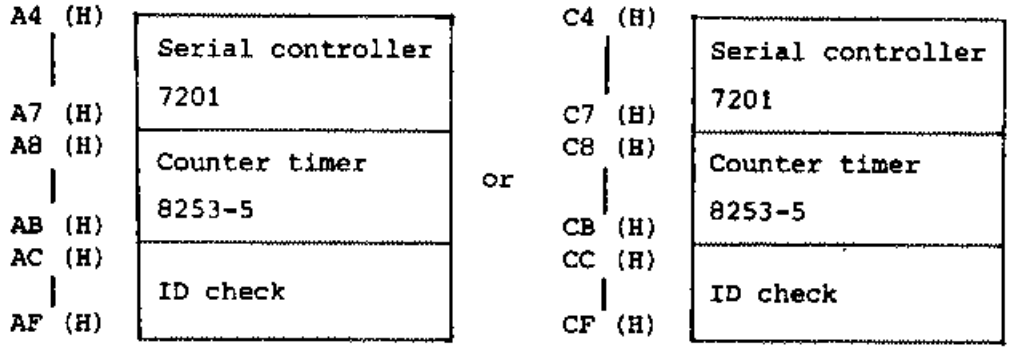



Fig. 4-6

### 4.3.2 ID check method

This is the method of checking whether or not the Q10RS option card exists on the option slot, and identifying the slot on which the Q10RS is mounted.

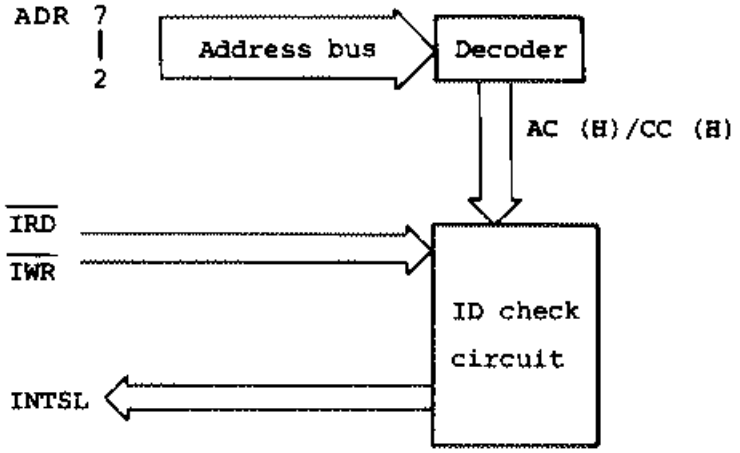


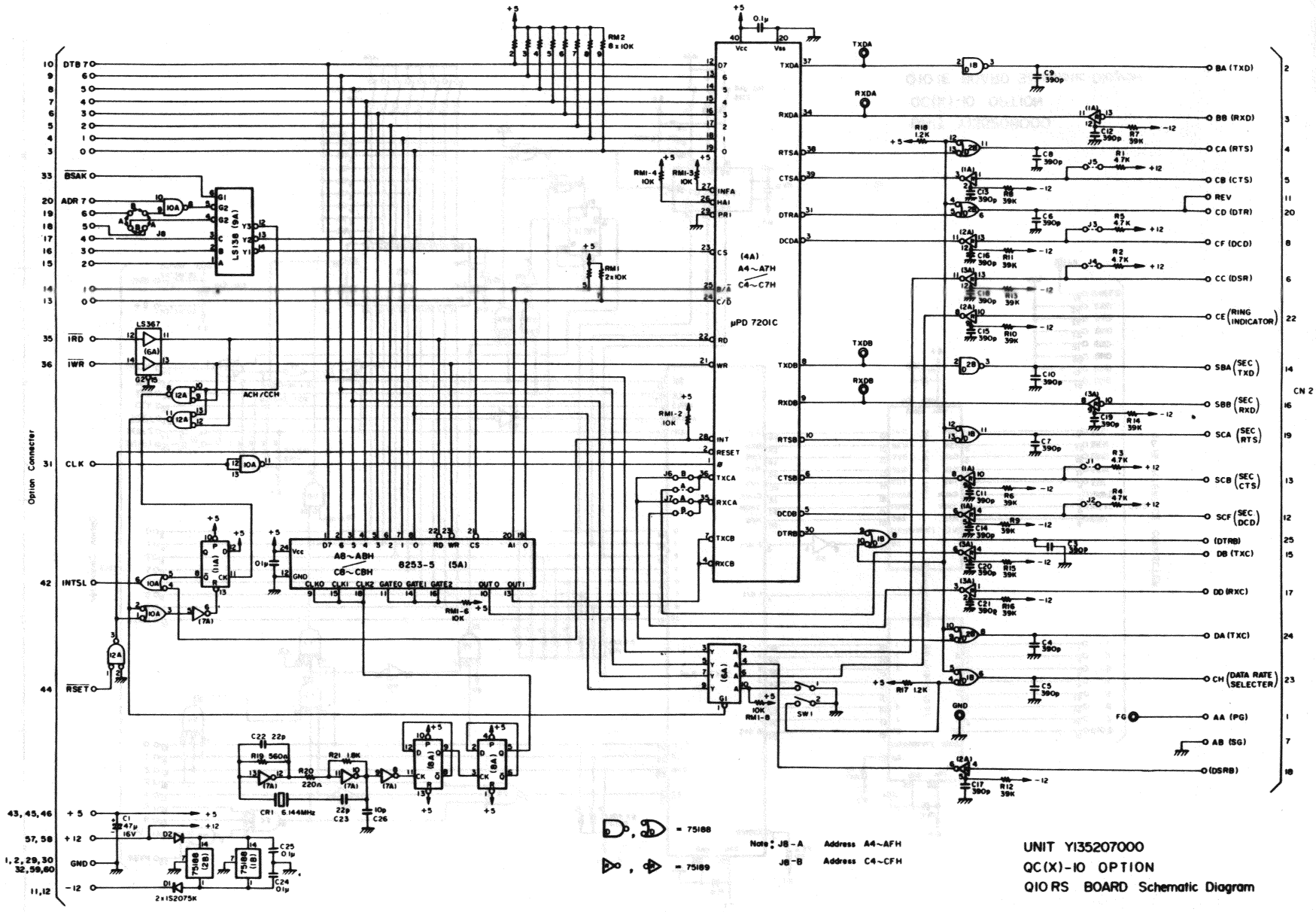

Fig. 4-7

Write optional data in AC (H) (any one of AC (H) - AF (H)) or CC (H) (any one of CC (H) - CF (H)). If the Q10RS option card has been mounted, the address corresponding to that slot number is interrupted. Existence of the card is indicated by it. The interrupt request is reset by reading AC (H) or CC (H) by the interrupt routine.

The contents of AC (H) and CC (H) are as follows.

| DSR Ach | DSR Bch | RINGER | Always high | DIP SW |
|---|---|---|---|---|
| D7 | D6 | D5 | D4 D3 D2 D1 | D0 |

With respect to DSR and RINGER, the bit becomes 0 when the RS-232C level is ON.
(As the Q10RS option board uses 75188/75189 as driver/receiver, the level is ±15 V.)
The bit becomes 0 when the dip switch is ON.
The dip switch is connected to D0. The purpose of using the dip switch is to ascertain whether the Q10RS option card is asynchronously or synchronously set, and to start the support program accordingly.


A
B
C
D
Option Connecter
RS-232C INTERFACE CONNECTER
CN 2
DTB 7
BSAK
ADR 7
IRD
IWR
CLK
INTSL
RSET
ACH/CCH
μPD 7201C
8253-5 (5A)
A8~ABH
C8~CBH
RM1
RM2 8×10K
RMI-2 10K
RMI-3 10K
RMI-4 10K
RMI-6 10K
RMI-8 10K
R17 1.2K
R18 1.2K
SW1
TXDA
RXDA
RTSA
CTSA
DTRA
DCDA
TXDB
RXDB
RTSB
CTSB
DCDB
DTRB
BA (TXD)
BB (RXD)
CA (RTS)
CB (CTS)
REV
CD (DTR)
CF (DCD)
CC (DSR)
CE (RING INDICATOR)
SBA (SEC TXD)
SBB (SEC RXD)
SCA (SEC RTS)
SCB (SEC CTS)
SCF (SEC DCD)
(DTRB)
DB (TXC)
DD (RXC)
DA (TXC)
CH (DATA RATE SELECTER)
AA (PG)
AB (SG)
(DSRB)
FG
GND
43, 45, 46
57, 58
1, 2, 29, 30 32, 59, 60
11, 12
2×1S2075K
= 75188
= 75189
Note: J8-A Address A4~AFH
J8-B Address C4~CFH
UNIT Y135207000
QC(X)-10 OPTION
QIORS BOARD Schematic Diagram

# CHAPTER 5 Q10IE - IEEE-488 INTERFACE CARD -

## 5.1. General

The Q10IE option card is the interface card which is mounted on the option slot of QX-10 and enables connection of QX-10 to the IEEE-488 bus system. This option card is provided with the following functions defined in IEEE-488.

(1) All functions of source handshaking
(2) All functions of acceptor handshaking
(3) All functions of talker and extended talker
(4) All functions of listener and extended listener
(5) All functions of service request
(6) All functions of remote/local
(7) Parallel pole 1 (composed by remote messages) and parallel pole 2 (composed by local messages)
(8) All functions of device clearing
(9) All functions of device triggering
(10) All functions of controller

These functions are enabled by the program for the μPD7210 GPIB-IFC (General Purpose Interface Bus-Interface Controller) on the option card.

## 5.2. Specifications

(1) Total cable length : 20 m max.

(2) Cable length between units : 5 m max.

(3) Maximum number of units to be connected: 15

(4) Transfer system : 3-wire handshaking

(5) Data transfer : 8-bit parallel

(6) Signal logic : Negative

True : L level (0.8 V max.)

False: H level (2.0 V min.)

## 5.3. IEEE-488

### 5.3.1 IEEE-488 bus configuration

The IEEE-488 standard is a general purpose interface system bus which enables easy construction of an automated system by making parallel connection of plural sets of measuring instruments, peripheral equipments, etc. and standardizing remote control and data transfer.
This interface bus consists of 16 signal lines. The Connectors defined in the IEEE-488 are mounted in each component unit and used for connection between these units via cables. Up to 15 sets of units can be connected on the same bus. Data transfer between the units is based on the 3-wire handshaking system performed by three transfer control lines. This enables assured data transfer even between units with different transfer speeds.

16 signal lines of the interface bus are:

| | | |
|---|---|---|
| Data bus ..... | 8 | (DI01 ~ DI08) |
| Transfer control bus ..... | 3 | (DAV, NRFD and NDAC) |
| Administration bus ..... | 5 | (IFC, ANT, SRQ, REN and EOI) |

Fig. 5-2 shows the basic timing of IEEE-488.
When the IFC (Interface Clear) is sent from the controller, all the units on the IEEE-488 are initialized.
When the ATN (Attention) line then goes to low, the system is set to the mode of sending commands from the controller.

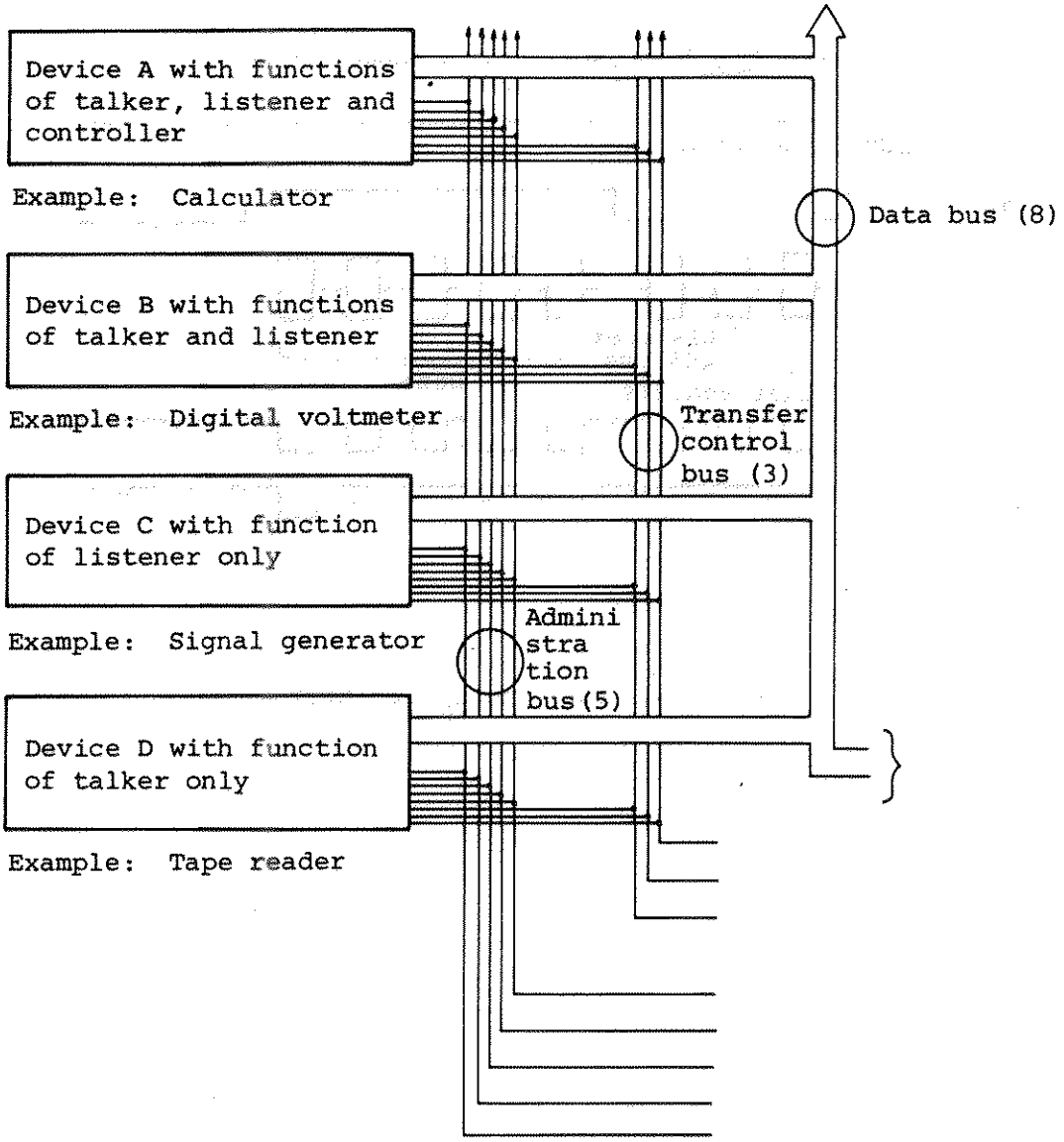



Fig. 5-1

Fig. 5-1 Functions and structure of interface

After resetting all the listeners by UNL (Unlisten), designate the addresses of talker and listener. Then, set the ATN line high. Then, data transfer is started from the talker to the listener. The DAV (Data Valid) indicates that when a command or data is transmitted, the information is effective at low level.

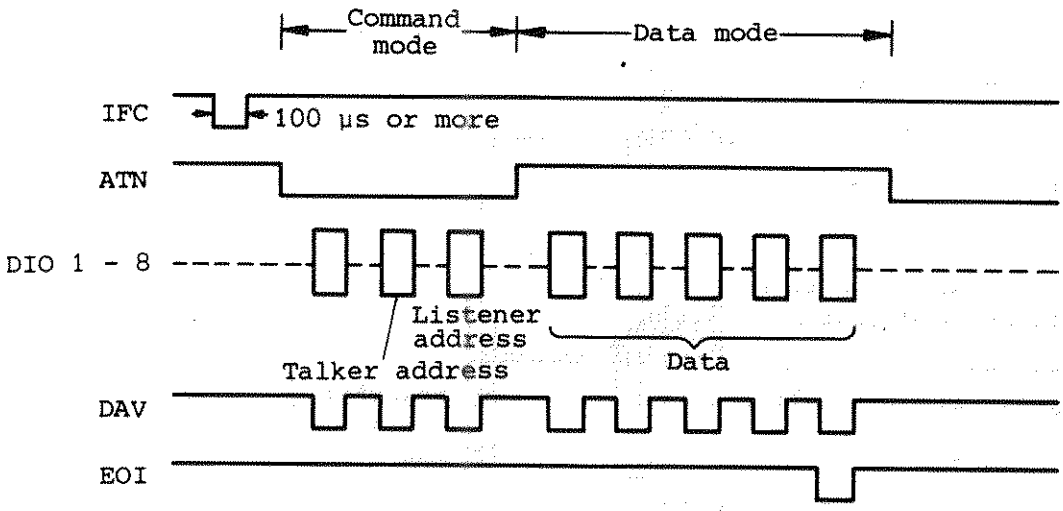



Fig. 5-2 Basic timing of GPIB

### 5.3.2 IEEE-488 handshaking

Handshaking is performed with three control signals shown below. As the talker makes data transfer by checking the state of the listener, data transfer can be securely made even with equipment of low data transfer speed.

NRFD (Not Ready For Data): Reception ready signla
NDAC (Not Data Accepted) : Reception end signal
DAV (Data Valid) : Signal indicating data validity

The timing for handshaking is shown below.

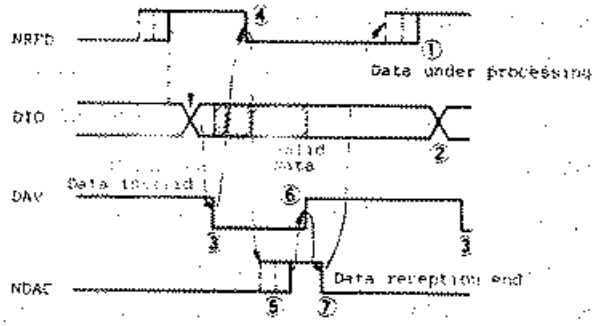



Fig. 5-3 Timing for handshaking

Description of timing for handshaking

(1) Listener is waiting for data.
(2) Transmission data is output to the talker data line.
(3) Check NRFD of the talker (when NRFD is "H", set DAV to "L" and make the data valid.)
(4) Read the data when DAV of the listener is "L". (Set NRFD to "L" and set the state of data under processing. After completion of data input, the listener sets NDAC to "H".)
(5) After receiving the data, the listener sets NDAC to "H".
(6) The talker sets DAV to "H" and informs the listener of invalid data bus.
(7) The listener sets NDAC to "L" when DAV is "H", and goes to handshaking in the state of not yet receiving the data.

## 5.4. Hardware

### 5.4.1 Setting conditions of interface PC board

(1) Setting the interrupt level (Jumper wires J1, J2 and J3)

The QX-10 uses two interrupt controllers (μPD8259) enabling handling of 15 kinds of external interrupt. The priority level (interrupt level) of 15 steps is given to each interrupt. When an interrupt occurs, the priority level is compared with that of the program under execution and whether or not the interrupt is accepted is determined.
The priority level for the built-in options is available in options (#1) - (#7), as shown below. The interrupt level for these options is different according to setting of the jumper wires on the PC board or the option mounting position on the option slot. Therefore, when the option is accepted, setting of the jumper wire or the option mounting position on the option slot is determined considering frequency of use, data transfer speed, etc.
The following table shows the relationship between the option slots and priority level.

Interrupt Level (Priority Level)

| Level | | Cause of interrupt |
|---|---|---|
| High | 1 | Detection of power shut off |
| | 2 | Soft timer |
| | 3 | Option (#1) |
| | 4 | Option (#2) |
| | 5 | Keyboard/RS-232C |
| | 6 | Monitor/Light pen |
| Pri-ority | 7 | Floppy controller |
| | 8 | Printer |
| | 9 | Option (#3) |
| | 10 | Calendar clock |
| | 11 | Option (#4) |
| | 12 | Option (#5) |
| | 13 | Soft timer (#2) |
| | 14 | Option (#6) |
| Low | 15 | Option (#7) |

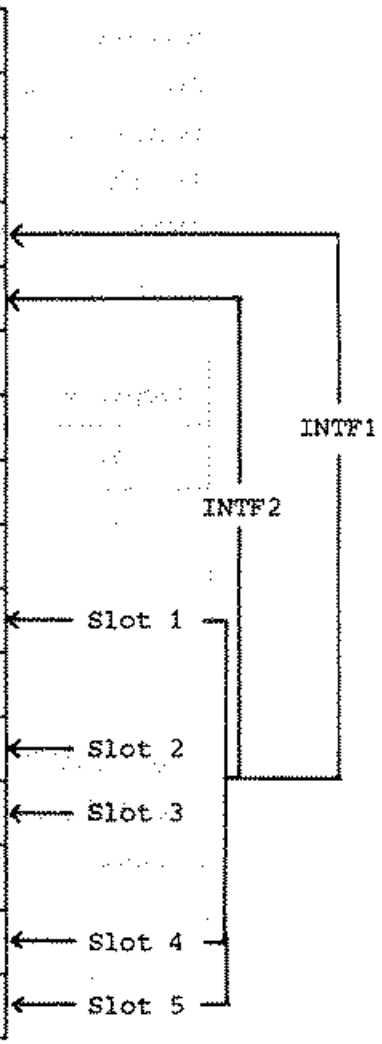



Table 5-1

Usually, for the interrupt from the option, the interrupt level for options (#3) - (#7) is assigned. However, it is possible to make the priority level for options higher, irrespective of their mounting positions on the slot.
In this option PC board, as shown in Table 5-2, INTF1 or INTF2 interrupt is enabled by selecting with the jumper wires.

| Jumper wire | Meaning | Setting at delivery |
|---|---|---|
| J1 | INTF1 (External interrupt #1) | OFF |
| J2 | INTF2 (External interrupt #2) | OFF |
| J3 | INTSL (Option slot interrupt) | ON |

Table 5-2 Meaning of jumper wires

When INTF1 or INTF2 is not selected, as shown in the table, the interrupt level (options (#3) - (#7)) changes according to the slot position.

(2) Setting the dip switches (Dip switches 1 and 2)

Dip switch 1

This switch is used to set the address of self node (my address) in the IEEE-488 system.
By reading the I/O address 90H, the state can be read according to the following table.

| Dip SW No. | Data bus to be read | Setting at delivery |
|---|---|---|
| 1 | D7 | OFF |
| 2 | D6 | OFF |
| 3 | D5 | OFF |
| 4 | D4 | OFF |
| 5 | D3 | OFF |
| 6 | D2 | OFF |
| 7 | D1 | OFF |
| 8 | D0 | OFF |

Table 5-3

* ON of the dip switch corresponds to "0" and OFF "1", respectively.

Dip switch 2

This switch is opened for the user.
By reading the address 91H, the state can be read according to the following table.

| Dip SW No. | Data bus to be read | Setting at delivery |
|---|---|---|
| 1 | Not used | OFF |
| 2 | D2 | OFF |
| 3 | D1 | OFF |
| 4 | D0 | OFF |
| —— | D3 - D7 are indefinite. | OFF |

Table 5-4

## 5.4.2 Locations of connector signals

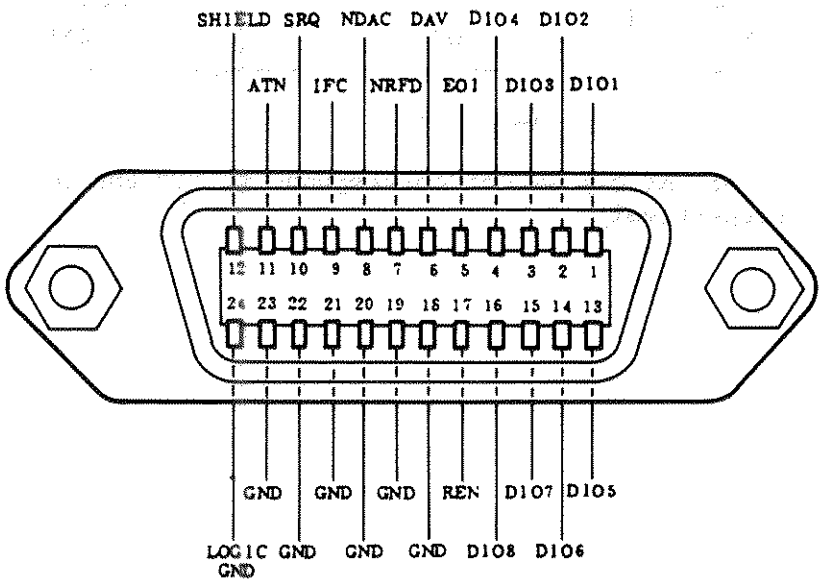



Fig. 5-4

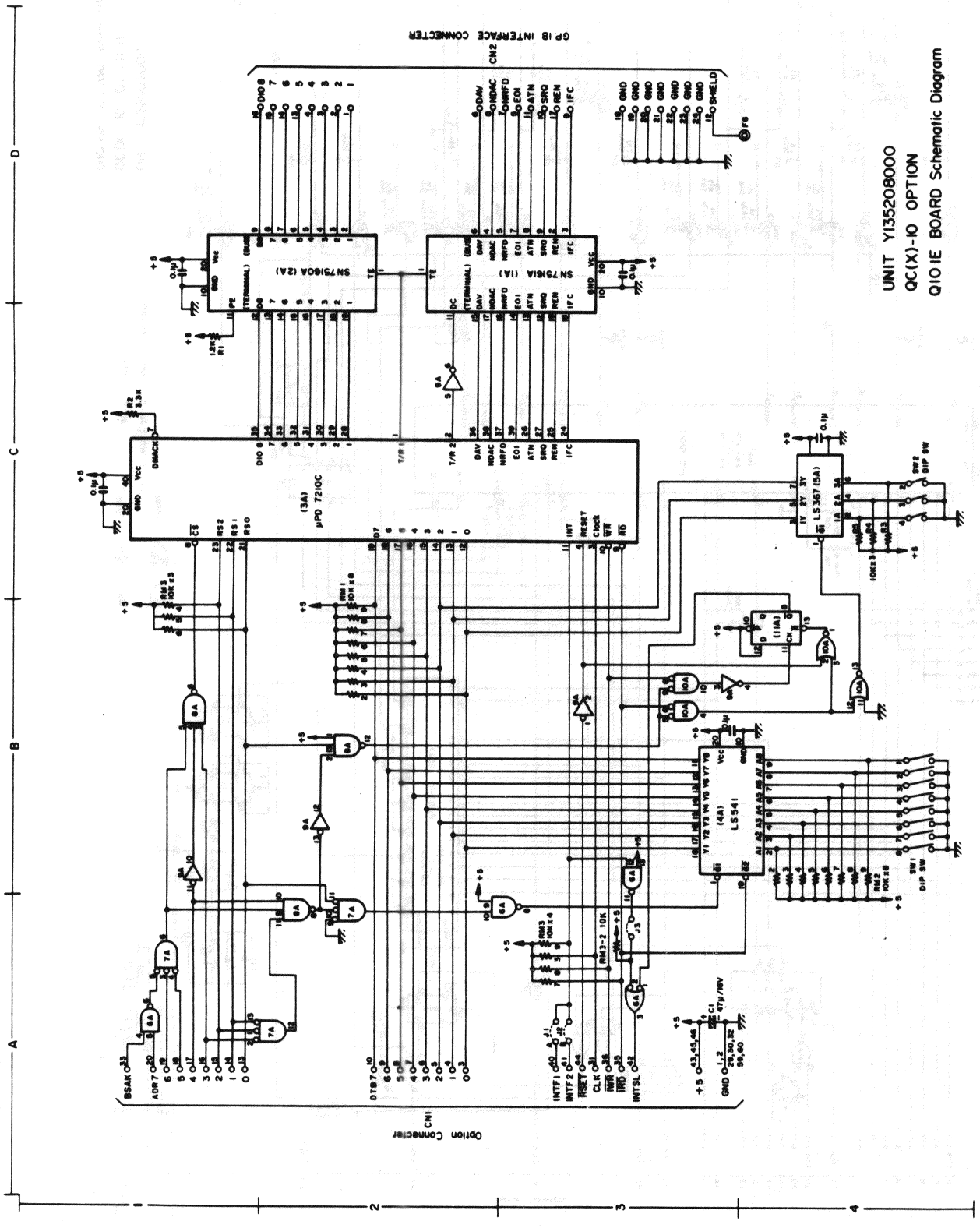
| Signal pin No. | Function | Signal name | Direction | Meaning |
|---|---|---|---|---|
| 1 | Data line | DIO1 | Input/output | 8-bit parallel data bus |
| 2 | Data line | DIO2 | Input/output | 8-bit parallel data bus |
| 3 | Data line | DIO3 | Input/output | 8-bit parallel data bus |
| 4 | Data line | DIO4 | Input/output | 8-bit parallel data bus |
| 5 | Control line | EOI | ** (Output) | Indicates the data end signal output from the talker or the parallel pole execute signal output from the controller. |
| 6 | Handshaking | DAV | (Input/output) | Talker/controller data check signal (H: Invalid, L: Valid) |
| 7 | Handshaking | NRFD | Output | Data wait signal (H: Receivable, L: Under data processing) |
| 8 | Handshaking | NDAC | Output | Data reception end (H: Reception end) |
| 9 | Control line | IFC | * Output | Interface clear (Output signal from the controller) |
| 10 | Control line | SRQ | (Input/output) | Control call signal from talker/listener |
| 11 | Control line | ATN | * Output | Data line mode designation (Data/command ... H: Data) |
| 12 | —— | SHIELD | —— | Interface cable shielding |
| 13 | Data line | DIO5 | Input/output | 8-bit parallel data bus |
| 14 | Data line | DIO6 | Input/output | 8-bit parallel data bus |
| 15 | Data line | DIO7 | Input/output | 8-bit parallel data bus |
| 16 | Data line | DIO8 | Input/output | 8-bit parallel data bus |

| Signal pin No. | Function | Signal name | Direction | Meaning |
|---|---|---|---|---|
| 17 | Control line | REN | * Output | Remote/local control |
| 18 | —— | GND6 | —— | Ground |
| 19 | —— | GND7 | —— | Ground |
| 20 | —— | GND8 | —— | Ground |
| 21 | —— | GND9 | —— | Ground |
| 22 | —— | GND10 | —— | Ground |
| 23 | —— | GND11 | —— | Ground |
| 24 | —— | GND (L) | —— | Ground |

Table 5-5

* Output lines from the controller

** Output line from the talker


GP IB INTERFACE CONNECTER
CN2
SN75160A (2A)
SN75161A (1A)
μPD 7210C
(3A)
LS367 (5A)
LS541
(4A)
Option Connector
CN1
UNIT Y135208000
QC(X)-10 OPTION
Q10 IE BOARD Schematic Diagram

# CHAPTER 6 Q10AD - A/D-D/A CONVERTER INTERFACE -

## 6.1. General

The Q10AD includes both an A/D converter and a D/A converter on one card, which is mounted in one of the option slots of the QX-10. Both of these devices can be used independently with the QX-10's software. The features of this card are described below.

(a) A/D converter

1) The A/D converter is equipped with 8 analog input channels, any one of which can be selected by command for input to the A/D converter.

2) Analog input signals in the range from -12 V to +12 V can be converted to digital data.

3) The maximum rate at which analog input signals can be sampled is 23.8 kHz; therefore, digital data can be obtained for analog signals with frequencies of up to 11.9 kHz.

4) Analog input signals are converted to 8-bit digital values in one of two selectable formats: offset binary or straight binary (described later).

(b) D/A converter

This converter outputs analog signals whose voltage varies according to the 8-bit digital data supplied from the QX-10 as follows:

Unipolar output: 0 V $\pm$10 mV to +5.1 V $\pm$10 mV
(Voltage changes by 20 mV for each change in the LSB of the digital value.)

Bipolar output : -5.1 V $\pm$10 mV to +5.1 V $\pm$10 mV
(Voltage changes by 40 mV for each change in the LSB of the digital value.)

## 6.2. I/O Map

The I/O map of the Q10AD changes according to the settings of jumpers J5A and J5B. At the time of shipment from the factory, jumper J5A is connected.
If jumper J5B is connected, "4" is added to all addresses indicated when jumper J5A is connected. Note that this will result in overlap with the I/O map for the Q10RS (RS-232C interface).
The I/O map is as indicated in the table below when jumper J5A is connected. Addresses indicated in parentheses apply when J5B is connected.

| Address | Writes (OUT instruction) | Reads (IN instruction) |
|---|---|---|
| A0H (A4H) | Selects one of the analog channels for A/D conversion. Channels are selected by outputting the number of the desired channel to the data bus. The channel numbers are 0 to 7 (AIN0 - 7). | Inhibited. |
| A1H (A5H) | Executing an OUT instruction to this address starts A/D conversion. It does not matter what value is on the data bus. | Reads 8-bit data resulting from A/D conversion into the CPU. |
| A2H (A6H) | Writes digital values for D/A conversion. Writing data to this address latches the data and outputs the corresponding analog voltage to AOUT. | Inhibited. |
| A3H (A7H) | When the Q10AD is mounted in one of the option slots, a write to this address activates INTSL to generate an interrupt. | Reading this address inactivates INTSL (for acknowledgement). During A/D conversion, the D0 value on the data bus can be monitored to identify completion of A/D conversion (when D0 = 1). |

## 6.3. A/D Converter

### (a) A/D conversion procedures

A flow chart of A/D conversion procedures is shown in Fig. 6-1. These procedures are described below. (In the examples, it is assumed that jumper J5A is connected.)

1) Channel select

This step select one of the 8 analog input channels for A/D conversion. These 8 channels are designated AIN0 to AIN7, and the procedure for selecting one of these is to write the corresponding number to I/O address A0H. Once a channel has been selected, that channel is held until another channel selection is made; therfore, the channel selection need only be made once if only a certain channel is to be used. Further, channel AIN0 is selected by default upon reset.

Example: Selecting AIN3

```
LD A, 03H     ; LOAD CHANNEL NUMBER INTO A
OUT (0A0H), A; CHANNEL SELECT
```

2) Acquisition time (4 μs wait)

The sample holding circuit of the A/D converter is such that Max. 4 μs is required for the holding level of the output voltage to catch up when the input level changes from one sample to the next.

3) Start A/D conversion

A/D conversion is started by executing a Z-80 OUT instruction to write any data to I/O address 0A1H.

4) Detecting completion of A/D conversion

Completion of A/D conversion is detected either by interrupt or by monitoring the status of data bus bit D0.

i. Detection by interrupt

Depending on the jumper settings, the following interrupts become active when conversion is completed.

| Jumper J3 | Jumper J4A | Jumper J4B | Interrupt activated |
|---|---|---|---|
| o | x | x | INTSL |
| x | o | x | INTF1 |
| x | x | o | INTF2 |
| x | x | x | None |

o: Jumper connected.
x: Jumper not connected.

Note: Do not connect more than one of these jumpers at a time.

ii. Detection by status

The status of conversion can be determined by reading I/O address 0A3H and checking the value of data bus bit D0.

D0 = 0: Conversion being performed.
D0 = 1: Conversion completed.

5) Read 8-bit data

The 8-bit digital value resulting from conversion of the analog input voltage can be determined by reading address 0A1H. The conversion format is determined by the setting of jumper J2 as follows:

i. Jumper J2 connected (offset binary format)

Bipolar analog input to A/D converter IC BA9101 is possible in the range from -2.55 V to +2.55 V. The digital value returned for -2.55 V is 00H, and that returned for +2.55 V is 0FFH. The LSB of the digital value output changes for each 20 mV shift in the analog input voltage.

ii. Jumper J2 disconnected (straight binary)

In this case, unipolar analog input to A/D converter IC BA9101 is possible in the range from 0 V to +5.1 V. The digital value returned for 0 V is 00H, and that returned for +5.1 V is 0FFH. The LSB of the digital value output changes with each 20 mV shift in the analog input voltage.

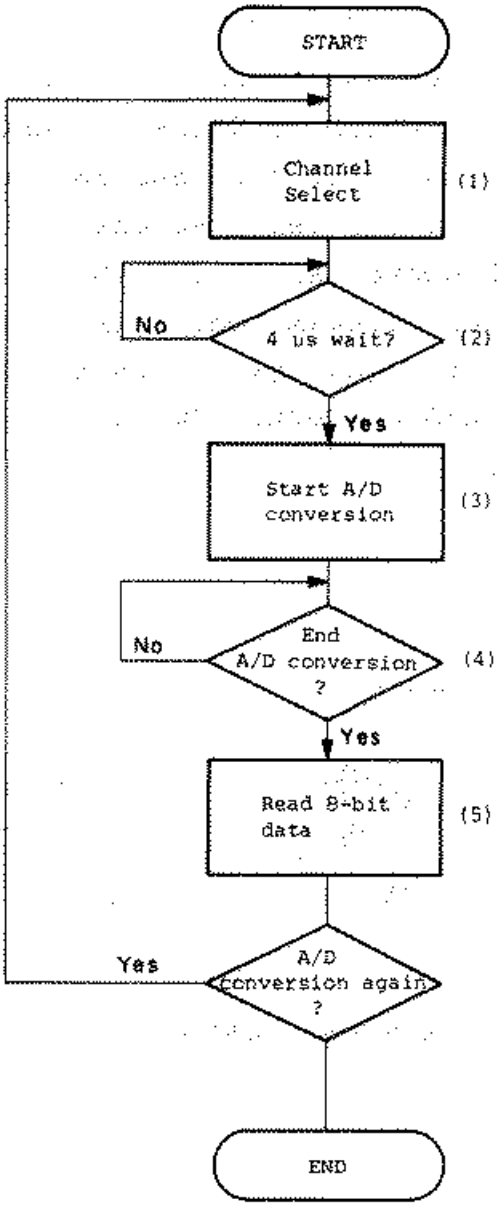



Fig. 6-1 Flow chart of A/D conversion

(b) Analog input channels AIN0 to AIN7

There are eight analog input channels, numbered AIN0 to AIN7, each of which is paired to GND. The settings of two DIP switches (SW1 and SW2) determine whether the input from the selected channel is fed directly to the A/D converter IC (BA9101) or to an operational amplifier (TL084A) which is used as a buffer to control the signal gain. In the latter case, input to the A/D converter IC is from the operational amplifier.
(See Fig. 6-2.)

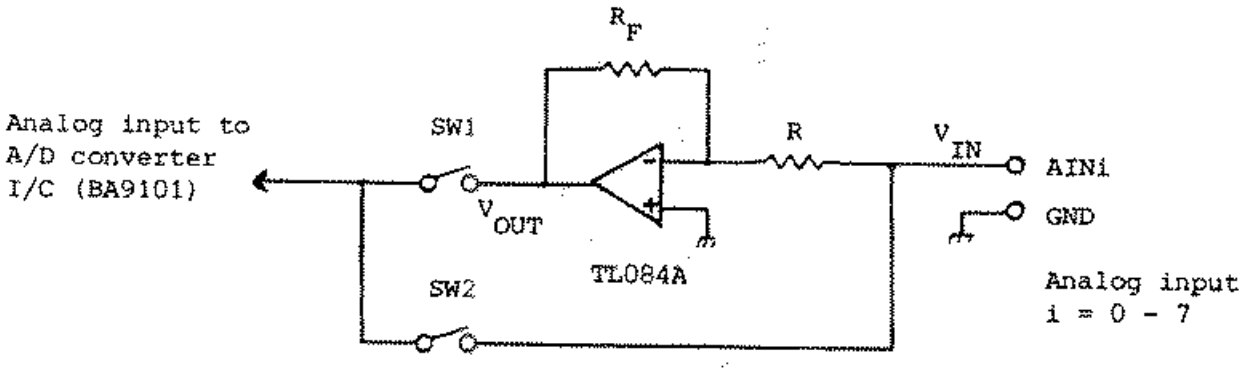



Fig. 6-2 Analog signal input stage

One or the other of these modes is selected as follows:

Mode 1: In this mode, SW1 is OFF and SW2 is ON, and the input signal voltage from channel AINi is fed directly to the A/D converter.

Mode 2: In this mode, SW1 is ON and SW2 is OFF, and the input gain from channel AINi is converted by operational amplifier TL0894A for input to the A/D converter.

When mode 2 is selected, the relationship between signal voltage $V_{IN}$ and output voltage $V_{OUT}$ after gain conversion is as indicated by the following expression.

$$V_{OUT} = - \frac{Rf}{R} V_{IN}$$

Thus, although the rated range of input voltages for the A/D converter IC (BA9101) is limited to 0 V to 5.1 V for direct binary conversion (or to -2.55 V to +2.55 V for binary offset conversion), selection of appropriate resistances makes it possible to increase the range to -12 V to +12 V by reducing the gain of the analog input signal. (The power supply voltage of the operational amplifier is +12 V.) In this case, it is necessary to note that the signal polarity is reversed and the amount of error increases as input levels approach 12 V.
Resistors R (R1 to R8) and Rf (R9 to R16) are not installed at the time of shipment from the factory, and must be installed by the user. See the schematic diagram for correspondence between the various channels and the resistors used for R and $R_f$.

The values used for R and $R_f$ are primarily determined by the input offset current and the rated load of the operational amplifier.
The resistance of R should be in the range from 100 ohms to 10 kohms, and that of $R_f$ should be in the range from 1 kohm to 1000 kohms.

Note: Do not set both DIP switches to ON simultaneously.

Correspondence between the bit numbers of the DIP switches and the analog input channels (AIN0 to AIN7) is shown in Table 6-1.
These bit numbers are printed on the circuit board.
These switches make it possible to determine the input mode for each channel independently.

| Analog input channel | SW1 bit number | SW2 bit number |
|---|---|---|
| 0 | 8 | 8 |
| 1 | 7 | 7 |
| 2 | 6 | 6 |
| 3 | 5 | 5 |
| 4 | 4 | 4 |
| 5 | 3 | 3 |
| 6 | 2 | 2 |
| 7 | 1 | 1 |

Table 6-1 Analog input channels and corresponding DIP switch bit numbers

(c) Internal reference voltage adjustment for A/D converter IC BA9101

The output voltage of A/D converter IC BA9101's internal reference voltage generator is adjusted by changing the setting of potentiometer VR3. Changing this setting adjusts the rate at which the least significant bit of the digital output data changes for shifts in the level of the analog voltage input to the A/D converter IC. See Fig. 6-3.

(d) Offset adjustment

Offset for the input voltage is adjusted by changing the setting of potentiometer VR2. See Fig. 6-4.

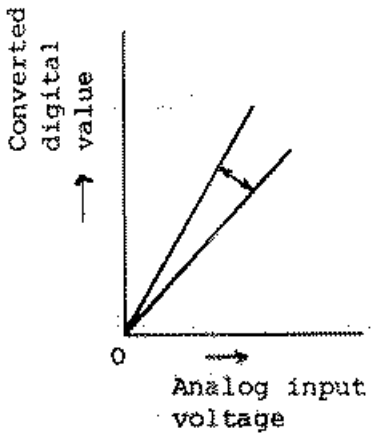



Fig. 6-3

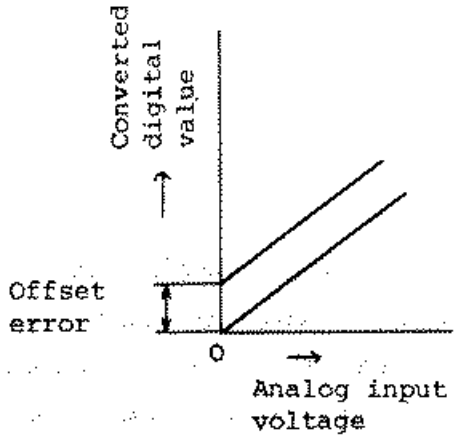



Fig. 6-4

(e) A/D conversion timing (A/D converter IC BA9101)

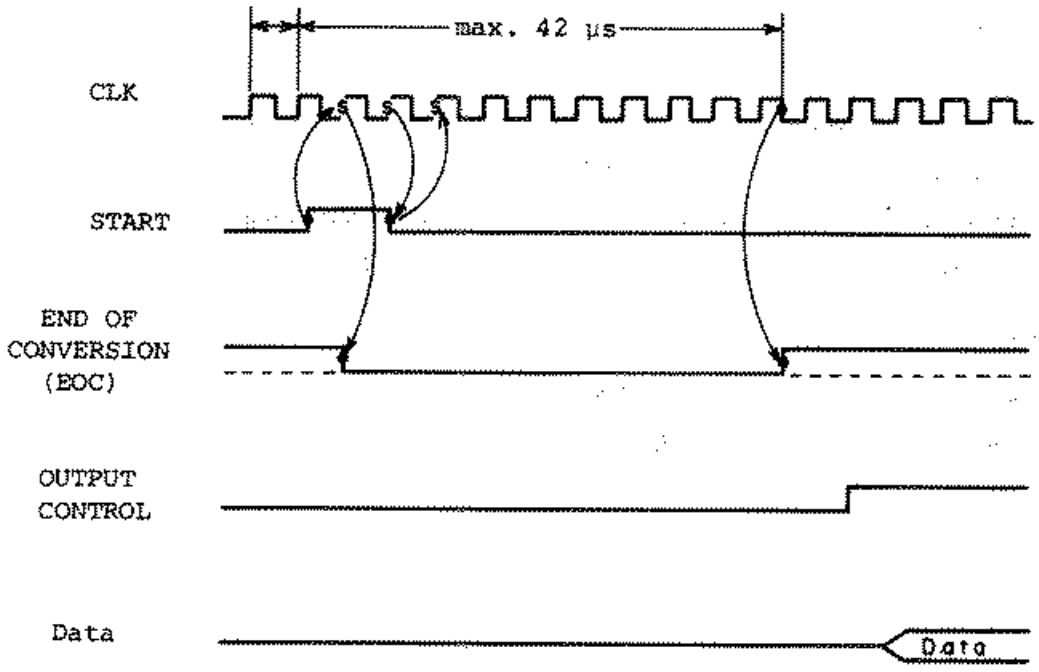



Fig. 6-5 A/D conversion timing chart

Conversion begins when EOC becomes "L" at the rising edge of the first CLK pulse after START becomes "H". EOC becomes "H" again (indicating that conversion has been completed) at the rising edge of the eighth CLK pulse after START drops back to "L". After the end of conversion, data is assured for a maximum of 220 ns after OUTPUT CONTROL rises.

(f) Sampling rate

As is indicated by the timing chart in (e) above, a maximum of 42 μs is required for one A/D conversion operation.

Sampling rate = 1/42 μs ≒ 23.8 kHz

Therefore, A/D conversion is possible for signals with frequencies up to 11.9 kHz even under the worst possible conditions.

(g) A/D converter linearity error

Although the LSB of the digital value produced by the A/D converter changes for each 20 mV change in the analog input voltage, it does not change at an accurate rate for variation in the analog input voltage within a certain range (which varies according to unit). Therefore, the digital values resulting from conversion do not precisely correspond to the analog input voltage. The maximum extent of this error is ±1 LSB.

(h) Procedure for adjusting the A/D converter

As shown in Table 6-2, the A/D converter should be adjusted so that digital values of 0, 1 and 254 are obtained for analog input voltages of 0 V, 20 mV and 5.08 V, respectively (during straight binary conversion). For offset binary conversion, adjust so that digital values of 0, 1 and 254 are obtained for analog voltages of -2.55 V, -2.53 V, respectively.

| Type conversion | Analog input corresponding to 0 | Analog input corresponding to 1 | Analog input corresponding to 254 |
|---|---|---|---|
| Straight binary | 0 V | 20 mV | 5.08 V |
| Offset binary | -2.55 V | -2.53 V | +2.53 V |

Table 6-2

Although the analog-digital characteristic can be adjusted based only on the two digital values 0 and 255, a line including error such as that indicated by B in Fig. 6-6 may result during straight binary conversion, even though the line indicated by A is ideal; therefore, the two point method is not recommended. The same applies to offset binary adjustment.

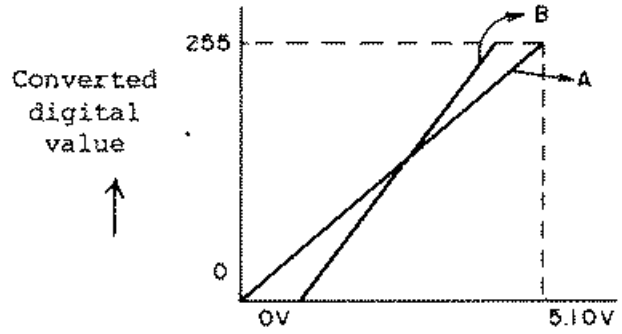



Fig. 6-6

## 6.4. D/A Converter

(a) Data is latched by outputting an 8-bit digital value to I/O address 0A2H (when jumper J5A is connected), then the corresponding analog voltage is output from AOUT. Whether the voltage output is bipolar or unipolar is determined by the setting of jumper J1A. Table 6-3 shows analog output voltages corresponding to digital values for both output formats.

| Output format | Setting of J1A/B | Analog output for 00H | Analog output for 0FFH | Change in voltage for each change in LSB |
|---|---|---|---|---|
| Unipolar | A connected | 0 V ±1.0 mV | +5.1 V ±10 mV | 20 mV |
| Bipolar | B connected | -5.1 V ±10 mV | +5.1 V ±10 mV | 40 mV |

Table 6-3

Note: Jumper J1 A and B must not both be connected at the same time.

(b) Potentiometer VR1

VR1 controls the internal reference voltage of the D/A converter; this potentiometer is adjusted to bring the analog voltages resulting from D/A conversion into the ranges shown in Table 6-3.

(c) D/A converter error

When VR1 has been adjusted so that output voltages are in the ranges indicated in Table 6-3, analog output error will be less than the amount of change in voltage indicated for each change in the LSB of the digital value.

(d) Load

The maximum load which may be connected to the output terminal is 500 ohms.

## 6.5. Jumpers

Jumpers included on the option card are J1A, J1B, J2, J3, J4A, J4B and J5.

(a) J1A and J1B

These jumper determine whether the analog output resulting from D/A conversion is bipolar or unipolar. (See 6.4. "D/A Converter".)

(b) J2

This jumper sets the A/D converter for either bipolar or unipolar analog input. (See 5) "Reading data" in section 6.3. "A/D Converter".)

(c) J3, J4A and J4B

The settings of these jumpers determine which interrupt becomes active upon completion of A/D conversion. (See 4) "Detecting completion of A/D conversion" in section 6-3. "A/D Converter".)

(d) At the time of shipment from the factory, jumpers J1A, J2, J3 and J5A are connected.

## 6.6. DIP Switches

Two DIP switches, SW1 and SW2, are mounted on the option card. Turning the bits of these switches ON or OFF determines whether analog input from each of the 8 channels is input directly to the BA9101, or is buffered for input by operational amplifier TL084A. (See (b) of section 6.3. "A/D Converter".)
At the time of shipment from the factory, all bits of SW1 are set to OFF and all bits of SW2 are set to ON.

## 6.7. Potentiometers

Three potentiometers, VR1, VR2 and VR3, are mounted on the option card.

(a) VR1

This potentiometer controls the D/A converter's internal reference voltage.

(b) VR2

This potentiometer adjusts the A/D converter offset.

(c) VR3

This potentiometer controls the A/D converter's internal reference voltage.

* At the time of shipment from the factory, VR1 is adjusted so that unipolar characteristics are as shown in Table 6-3.

## 6.8. Resistors

Resistors R1 to R16 determine the gain of the operational amplifier. These resistors are not installed at the factory, and must be installed by the user.

## 6.9. Connector Pin Assignments

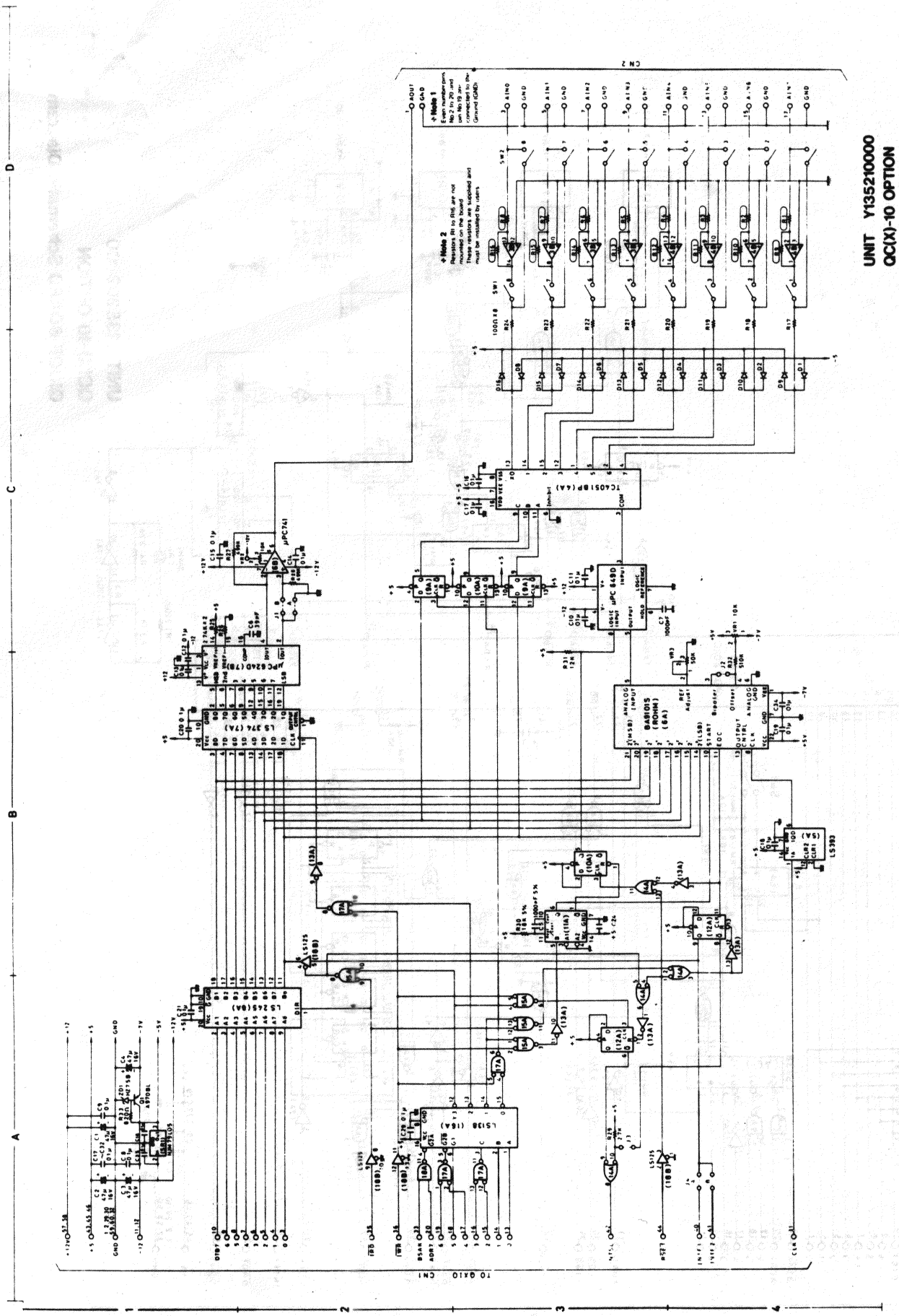
Pin numbers and signal names for the interface connector to the QX-10 are as shown in the table below.

| Pin No. | Signal name | Function | Pin No. | Signal name | Function |
|---|---|---|---|---|---|
| 1 | GND | GND | 20 | AD7 | Address bus 7 |
| 2 | GND | GND | 29 | GND | GND |
| 3 | D0 | Data bus 0 | 30 | GND | GND |
| 4 | D1 | Data bus 1 | 31 | CLK | Clock |
| 5 | D2 | Data bus 2 | 32 | GND | GND |
| 6 | D3 | Data bus 3 | 33 | $\overline{\text{BSAK}}$ | Bus acknowledge |
| 7 | D4 | Data bus 4 | 34 | $\overline{\text{IRD}}$ | I/O read |
| 8 | D5 | Data bus 5 | 35 | $\overline{\text{IWR}}$ | I/O write |
| 9 | D6 | Data bus 6 | 40 | INTF1 | INTF1 |
| 10 | D7 | Data bus 7 | 41 | INTF2 | INTF2 |
| 13 | AD0 | Address bus 0 | 42 | INTSL | INTSL |
| 14 | AD1 | Address bus 1 | 43 | +5 V | +5 V |
| 15 | AD2 | Address bus 2 | 44 | $\overline{\text{RESET}}$ | Reset signal |
| 16 | AD3 | Address bus 3 | 45 | +5 V | +5 V |
| 17 | AD4 | Address bus 4 | 46 | +5 V | +5 V |
| 18 | AD5 | Address bus 5 | 59 | GND | GND |
| 19 | AD6 | Address bus 6 | 60 | GND | GND |

## 6.10. External Interface

Pin numbers and corresponding signals for the analog output (AOUT) and analog input (AIN0 to AIN7) connector are as shown in the table below.

| Pin No. | Signal | Function |
|---|---|---|
| 1 | AOUT | Analog signal output after D/A conversion |
| 2 | GND | Ground |
| 3 | AIN0 | Analog input channel 0 |
| 4 | GND | Ground |
| 5 | AIN1 | Analog input channel 1 |
| 6 | GND | Ground |
| 7 | AIN2 | Analog input channel 2 |
| 8 | GND | Ground |
| 9 | AIN3 | Analog input channel 3 |
| 10 | GND | Ground |
| 11 | AIN4 | Analog input channel 4 |
| 12 | GND | Ground |
| 13 | AIN5 | Analog input channel 5 |
| 14 | GND | Ground |
| 15 | AIN6 | Analog input channel 6 |
| 16 | GND | Ground |
| 17 | AIN7 | Analog input channel 7 |
| 18 | GND | Ground |
| 19 | GND | Ground |
| 20 | GND | Ground |



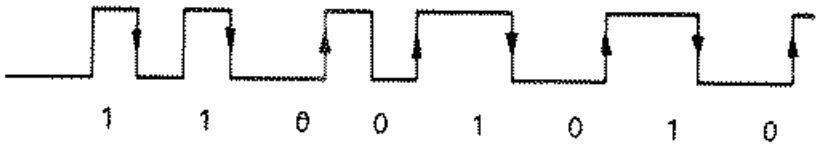
UNIT Y135210000
QC(X)-10 OPTION
Q10AD BOARD Schematic Diagram

# CHAPTER 7 Q10OF - OPTICAL FIBER INTERFACE -

## 7.1. General

The Q10OF is the interface card which is to be mounted on the option slot of QX-10 and used for connection with external devices via the optical fiber cable.
As a communication system, BYSYNC and SDLC are selectable. The transmission speed is 500 kbps (fixed). The coding system employs Manchester coding.

Manchester coding system



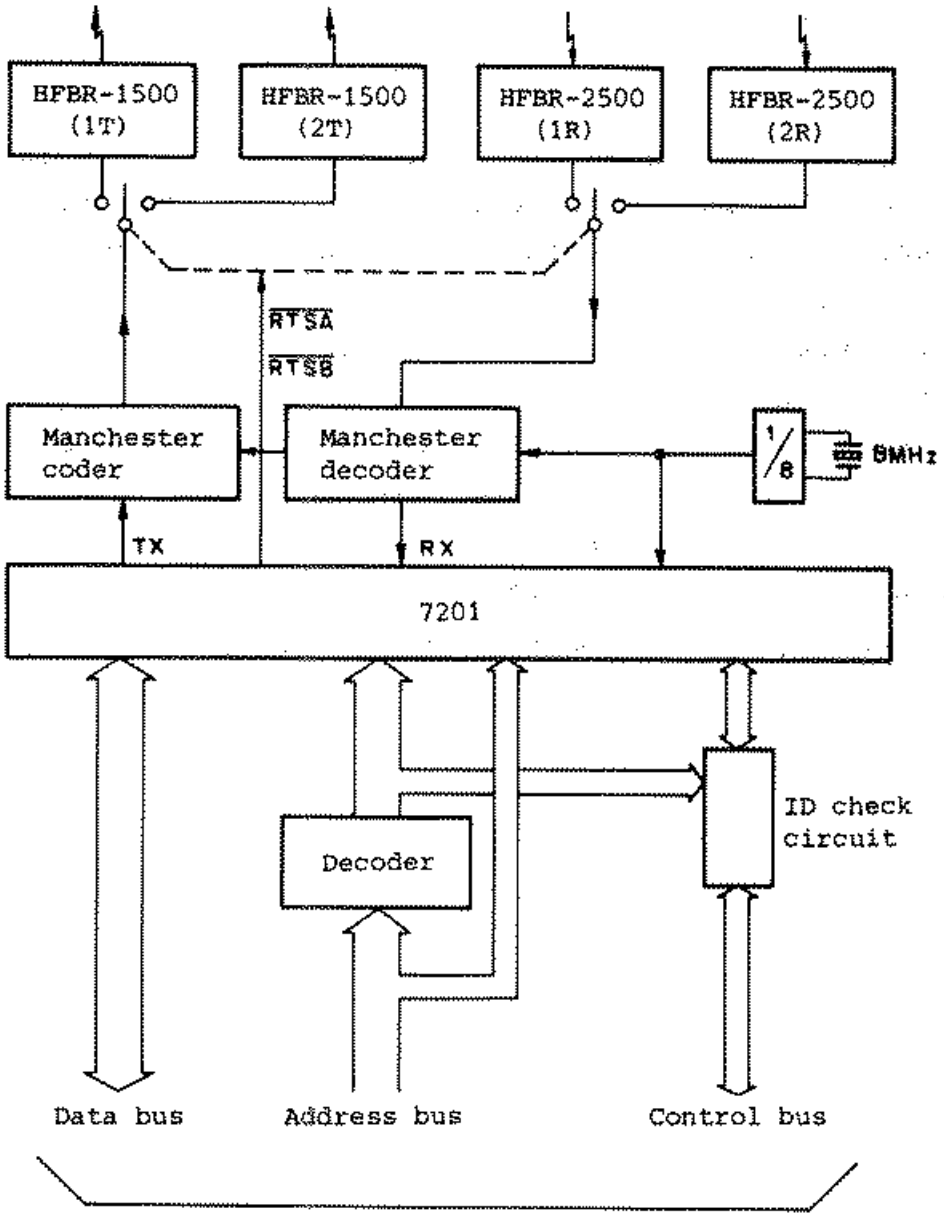

DMA is used for data transfer between µPD7201 and QX-10 main unit.

## 7.2. Hardware

### 7.2.1 General

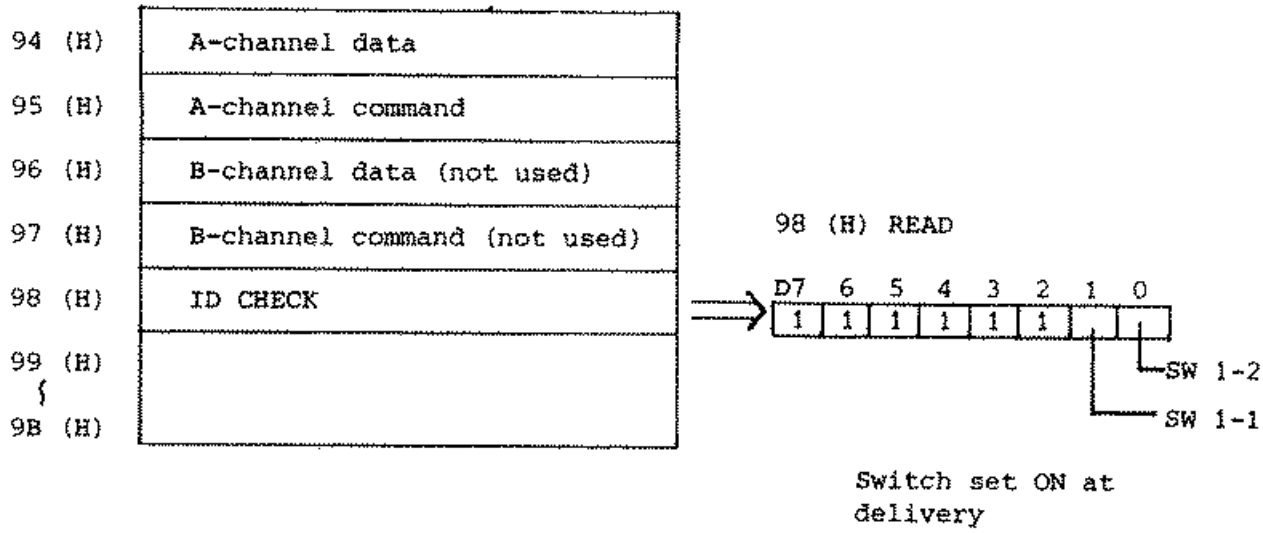
The Q10OF is the interface circuit which uses μPD7201 as a serial controller and optical fiber as a transmission media.
μPD7201 has two serial channels (A and B). From these two channels, only the A-channel is used. Two fiber channels are connected for the A-channel, which are selected by the software.
The transfer rate is fixed to 500 kbps. Manchester coding system is used for signal coding.
DMA is used for data transfer between μPD7201 and QX-10. So, the Q10OF option card cannot be inserted into the option slot #5. The circuit (ID CHECK circuit) is also provided to inform the CPU whether or not the Q10OF option card is mounted on the option slot.

## 7.2.2 Block diagram




Note #1 ~ 4

### 7.2.3 I/O map



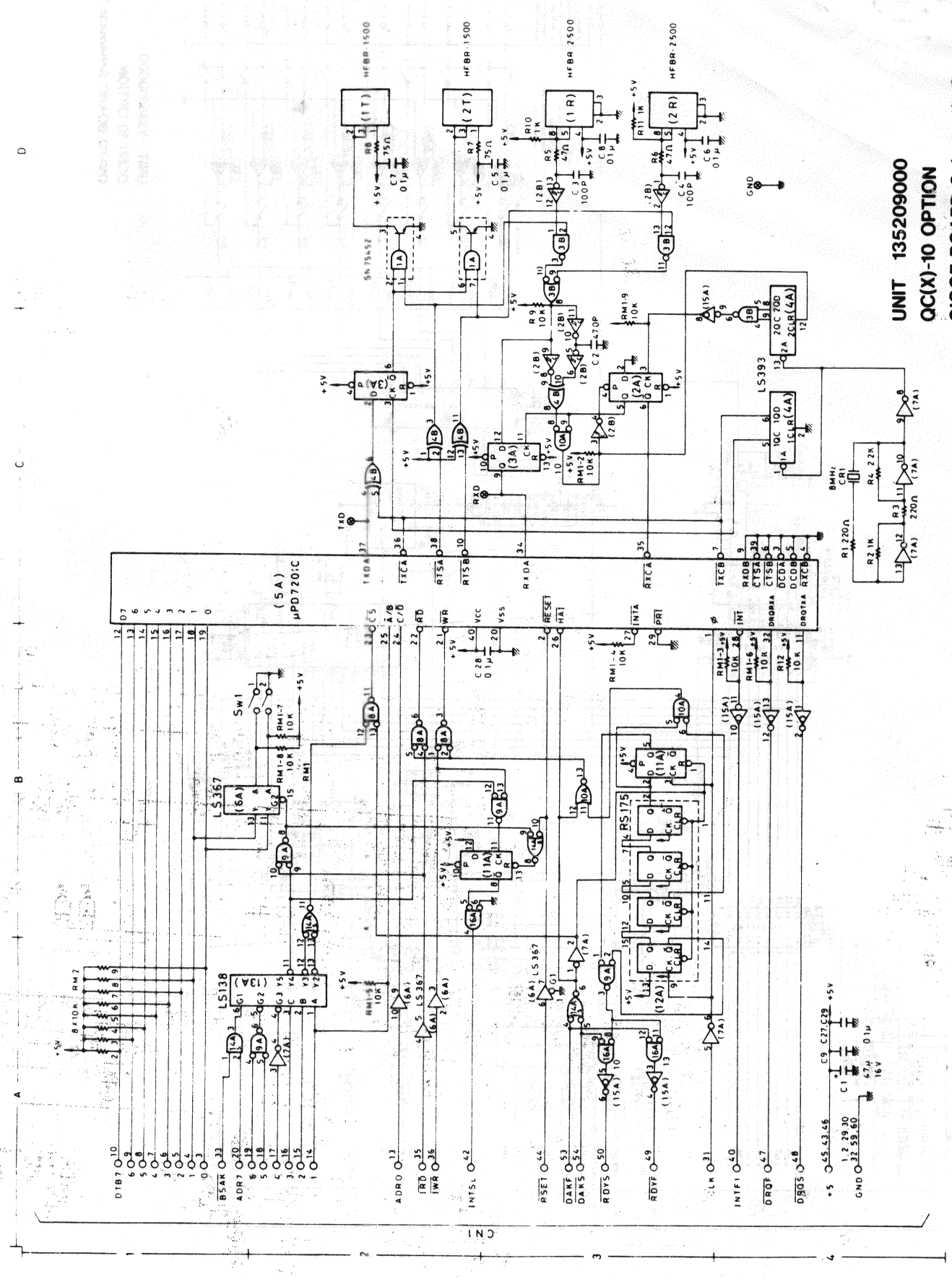

Switch set ON at delivery

### 7.2.4 Interface with QX-10

Interrupt for ID CHECK: INT (L)
Interrupt for 7201 : INT (H)1
RX: DRQ (F) ↔ DMA: DACK (F)
TX: DRQ (S) ↔ DMA: DACK (S)

### 7.2.5 Optical fiber transmitter/receiver and cable

Transmitter : HP HFBR-1500 (x 2)
Receiver : HP HFBR-2500 (x 2)
Optical fiber cable set: HP HFBR-3504 (x 2: Standard accessory)



**UNIT 135209000**
**QC(X)-10 OPTION**
**QIOOF BOARD Schematic Diagram**

# CHAPTER 8 Q10CMS - COLOR MONITOR SUBBOARD -

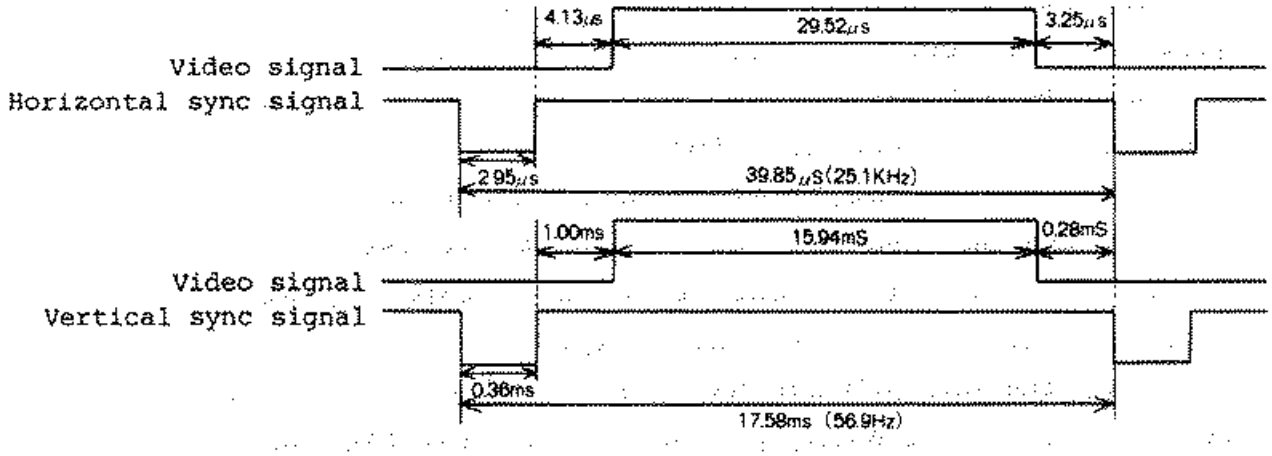
## 8.1 General

This sub board is mounted on the main board via connectors CN9 and CN10 provided on the main board (Q10 SYM board), and used as an interface board for connection with a high resolution color monitor.
With this board, it is possible to draw a picture in picsell units and display 640 dots x 400 dots x 7 colors in specified color on the color monitor.
The output connector from QX-10 to the color monitor is the same CN4 as that at use of green monitor.
Connector CN5 on the rear panel can be used without modification for the light pen input.
When this sub board is mounted, pin definition of CN4 is different from that when the green monitor sub board (Q10 GMS or Q10 GGS board) is mounted, and it is not possible to display on the green monitor.

## 8.2 Specifications

| | | |
|---|---|---|
| Output signal | : | RGB separate output |
| | | Video signal: TTL level positive polarity |
| | | Horizontal sync signal: TTL level negative polarity |
| | | Vertical sync signal: TTL level negative polarity |
| Scanning frequency: | | Horizontal: 25.1 kHz |
| | | Vertical : 56.9 Hz |
| Resolution | : | Horizontal: 640 dots |
| | | Vertical : 400 lines |

Signal timing:




NRZ signal of video signal DOT CLOCK 21.679 MHz, TTL level

Fig. 8-1

## 8.3 Block diagram

The block diagram of Q10 CMS board is shown in Fig. 8-2.
GDC μPD7220 is used as a display controller as in the green monitor sub board (Q10 GMS or Q10 GGS).
The GDC μPD7220 assigns I/O addresses 2CH - 2DH and 38H - 3BH as I/O channels for the CPU.
The video memory has three color planes based on control by the GDC μPD7220, each of which is used as memories for R, G and B. This reserves a large capacity without applying load to the CPU memory space.
Further, the GDC μPD7220 has the calculating function for plotting or drawing pictures, enabling high speed processing.

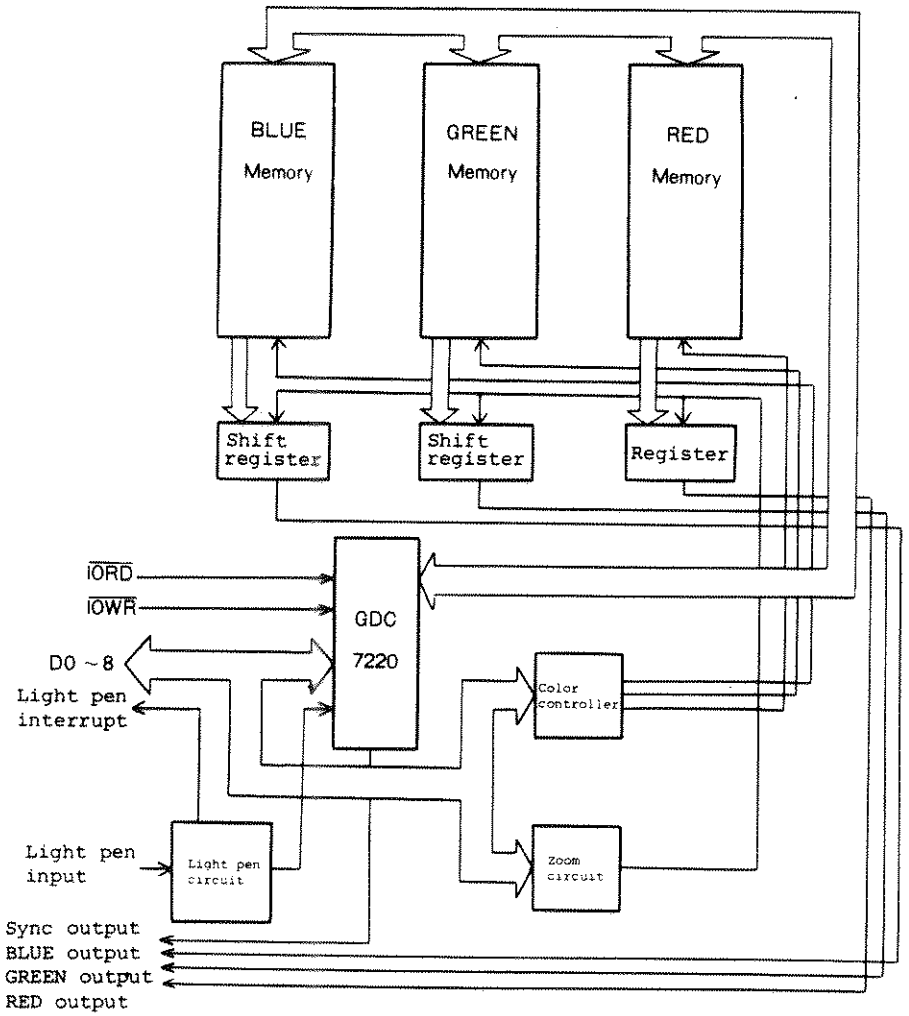



Fig. 8-2 Q10 CMS board block diagram

## 8.4 Configuration of video memory

The video memory exists in three planes for each color of R, G and B. One data consists of 16 bits. The memory of each color is 16K x 16 bits when the 16 kbit dynamic RAM is used, and 64 x 16 bits when the 64 kbit dynamic RAM is used.

Neutral tints can be expressed by writing the same capacity for more than two memory planes. In this case, memory banking is necessary for each color plane. Switching of these banks is performed by the color control register mapped in the I/O address 2DH. Corresponding memory planes will be connected to the GDC μPD7220: blue if the contents of 2DH are 01H, green if 02H, and red if 04H.

However, when more than two of these low order three bits are set to 1, two or more memory planes will be selected causing contention for the bus. Therefore, when two or more memory planes are selected, they must be selected one by one.

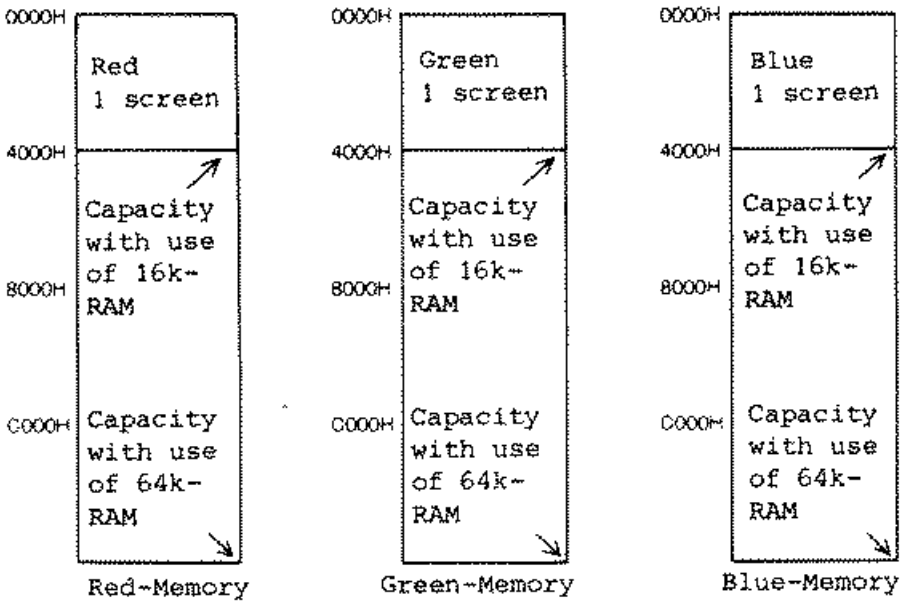



Fig. 8-3 Video memory map

The relationship between the memory address and raster is as shown in Fig. 8-4.

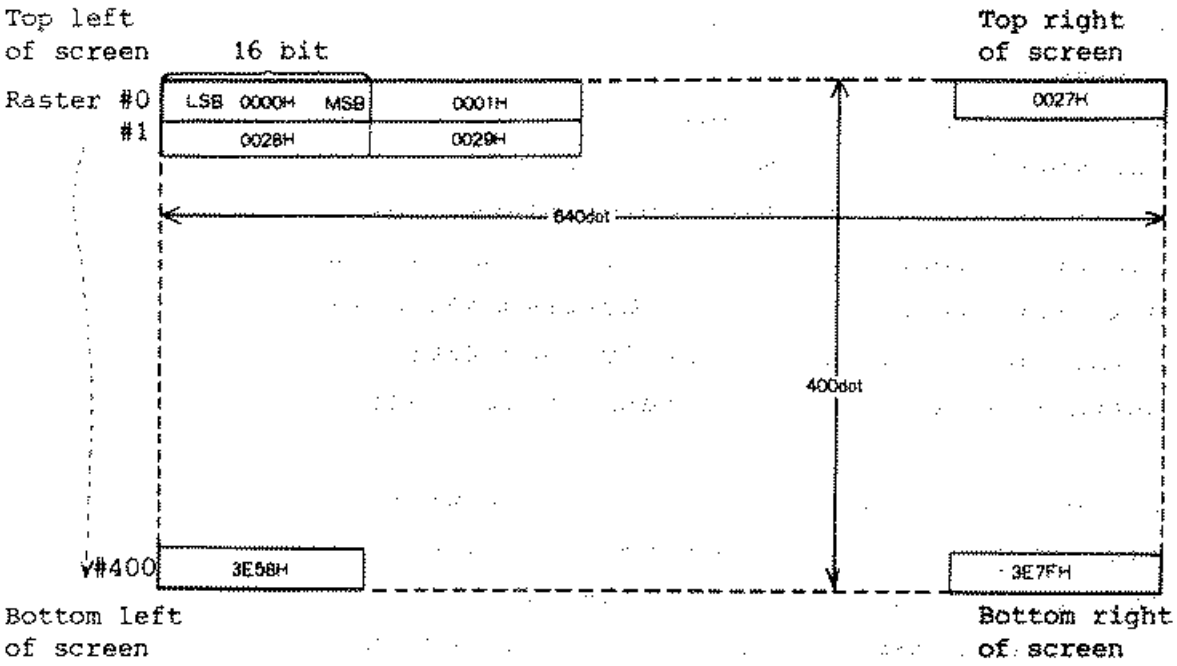



Fig. 8-4 Memory address and raster
(at non-zoom, start address = 0000H)

## 8.5 Sync signal

Horizontal and vertical sync signals are generated from the GDC μPD7220. The scanning frequency is set by the SYNC command for GDC. In the case of QX-10, the type of monitor sub board is discriminated by reading the data of I/O port 2CH in IPL at switching power on, and the scanning frequencies for green monitor and color monitor are set by the software.
As shown in Fig. 8-5, the D-type flip-flop is used in the sync signal output circuit so that the output polarity of sync signal can be selected for each monitor to be used by changing the jumper wires.

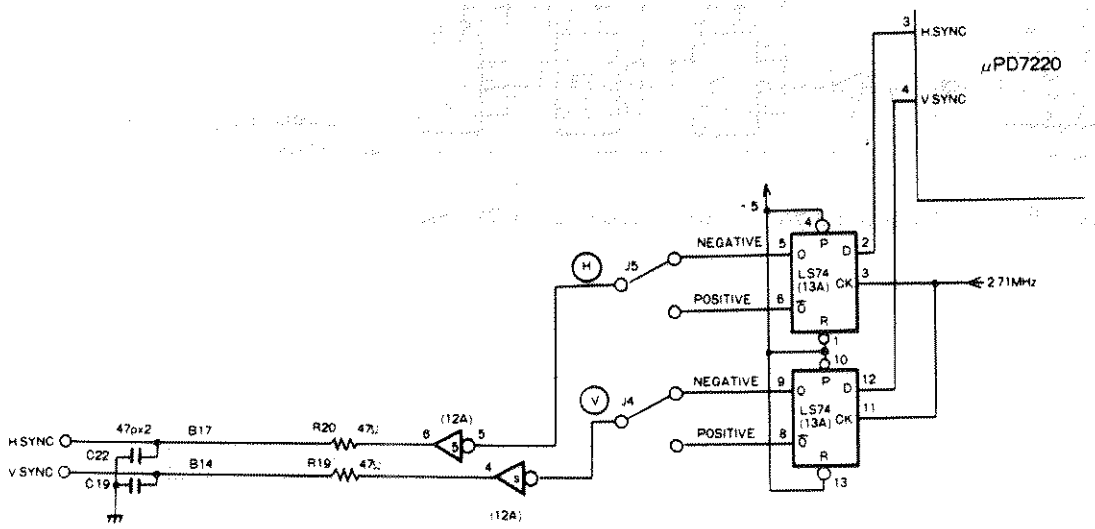



Fig. 8-5 Horizontal/vertical sync signal output circuit

## 8.6 Clock supply circuit

Fig. 8-6 shows the clock supply circuit on the Q10 CMS board. At the 2CCLK terminal of GDC μPD7220, the original oscillation frequency 21.679 MHz of the oscillation module (CR1) is divided into eight by three flip-flops assigned to the 2-divider and supplied as a clock of 2.71 MHz.

The original oscillation frequency 21.679 is used as a dot clock of video signal, enabling drawing of pictures at the high speed of 0.046 μsec/dot.

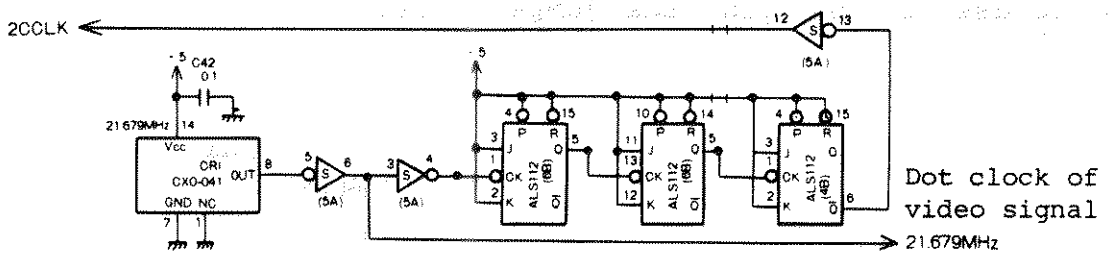



Fig. 8-6 Video signal dot clock 21.679 MHz

## 8.7 Video memory interface circuit

### 8.7.1 $\overline{RAS}/\overline{CAS}$ signal supply circuit

This color monitor sub board uses a 16K-bit or 64K-bit dynamic RAM for memory planes for each color of red, green and blue. $\overline{RAS}$ and $\overline{CAS}$ signals required by this dynamic RAM are supplied by the circuit shown in Fig. 8-7.

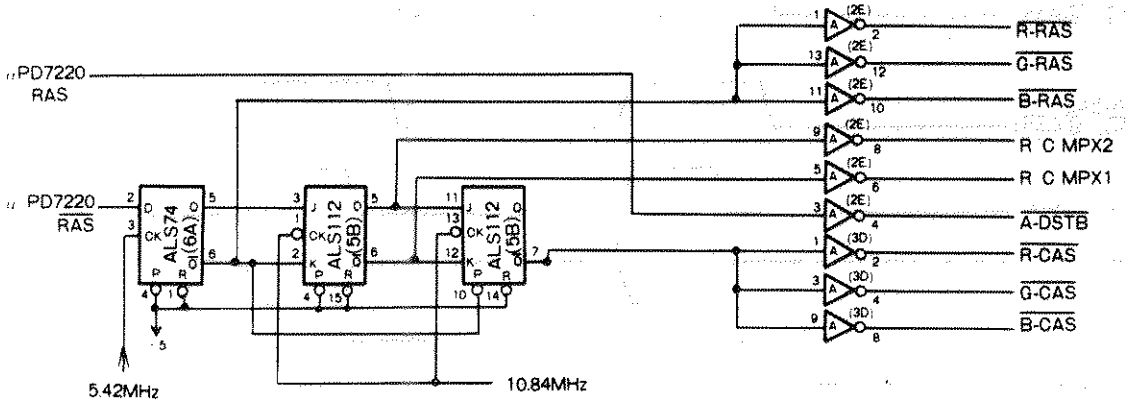



Fig. 8-7 $\overline{RAS}/\overline{CAS}$ signal supply circuit

The $\overline{RAS}$ signal for the color plane is supplied to the $\overline{RAS}$ signal terminal (pin 6) of GDC μPD7220 after being delayed 1/4 clock of 2CCLK (0.092 μsec) by the D-type flip-flop ALS74 (6A) which has 5.42 MHz as a clock. The $\overline{CAS}$ signal is supplied after being delayed more 1/4 clock (0.37 μsec) against the $\overline{RAS}$ signal.
In addition, this circuit also supplies the multiplex signal and $\overline{ADSTB}$ signal for the address multiplexer ALS573 (4C and 5C) for the video memory.
Fig. 8-8 shows the timing chart of these signals.

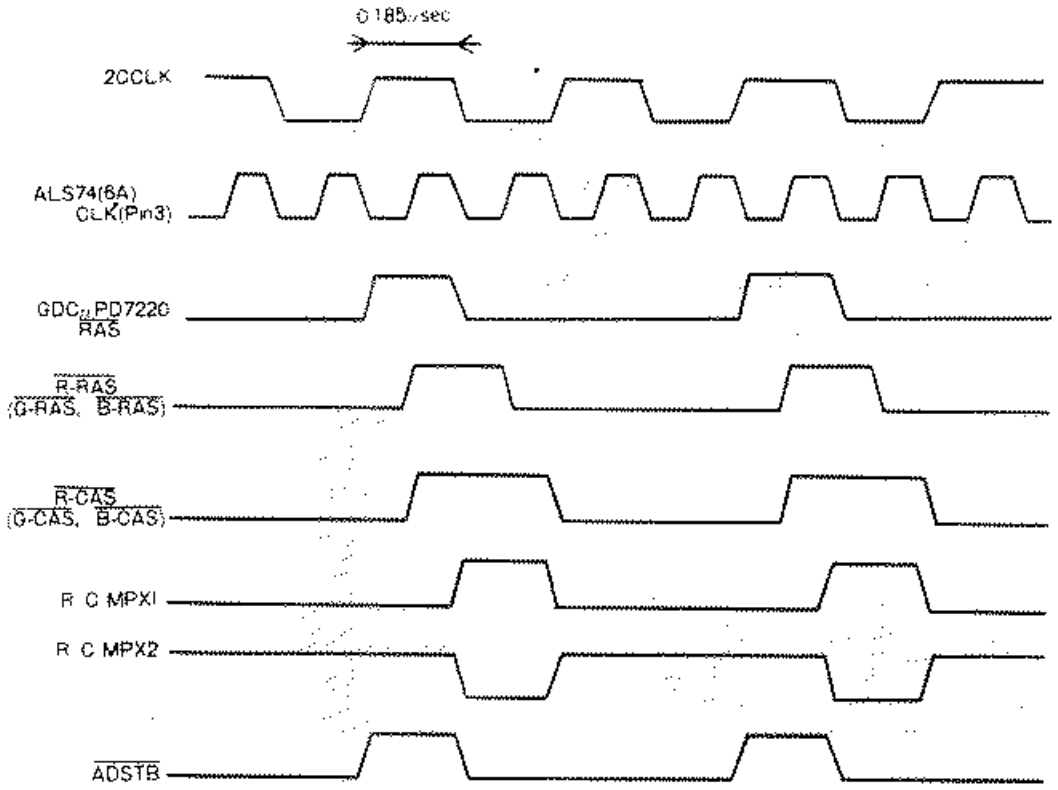



Fig. 8-8 $\overline{\text{RAS}}/\overline{\text{CAS}}$ signal timing

### 8.7.2 Video data read circuit

At the picture drawing (R/M/W) cycle of GDC μPD7220, the video memory contents are read by the GDC μPD7220. Fig. 8-9 shows the video data read circuit. Fig. 8-10 shows the read timing.

As the $\overline{\text{DBIN}}$ signal of the GDC μPD7220 becomes low level when the video data is read, and the inputs to one end of each NAND gate of IC 3E become high level.

The inputs to the other end of these NAND gates are memory plane select signals, only one of which is set to high level.

Then, as the output of the NAND gate whose two inputs are high level becomes low level, the G2 terminal of the 3-state buffer LS541 on the output data bus of any one of the memory planes selected becomes low active.

On the other hand, data bus DB3 is connected to the G1 terminal of this 3-state buffer LS541.

DB3 becomes 0 when the READ command is executed. So, the G1 terminal becomes low level, too, the data of LS541 is output, and the GDC μPD7220 is enabled to read the video memory.

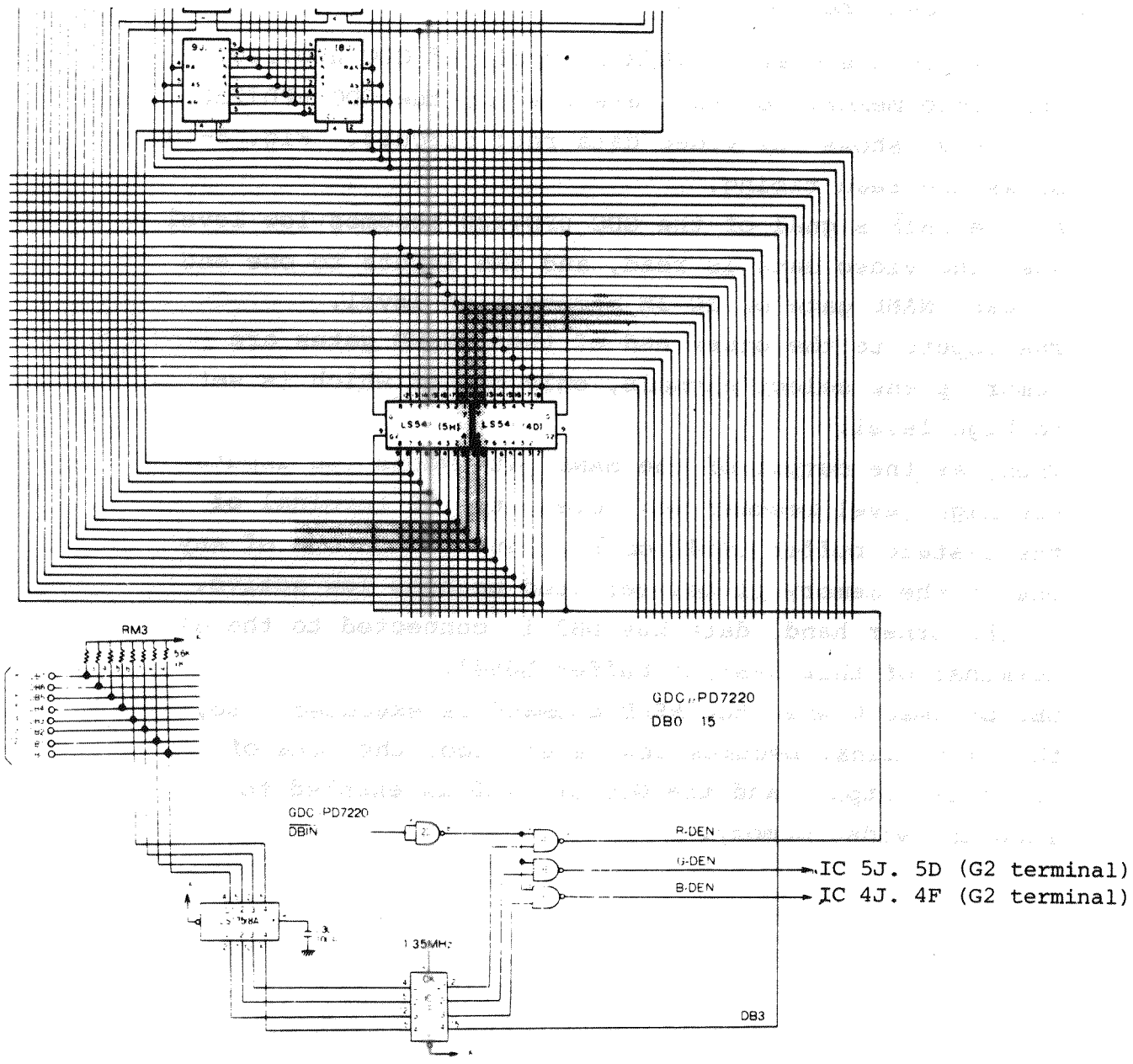



Fig. 8-9 Video data read circuit

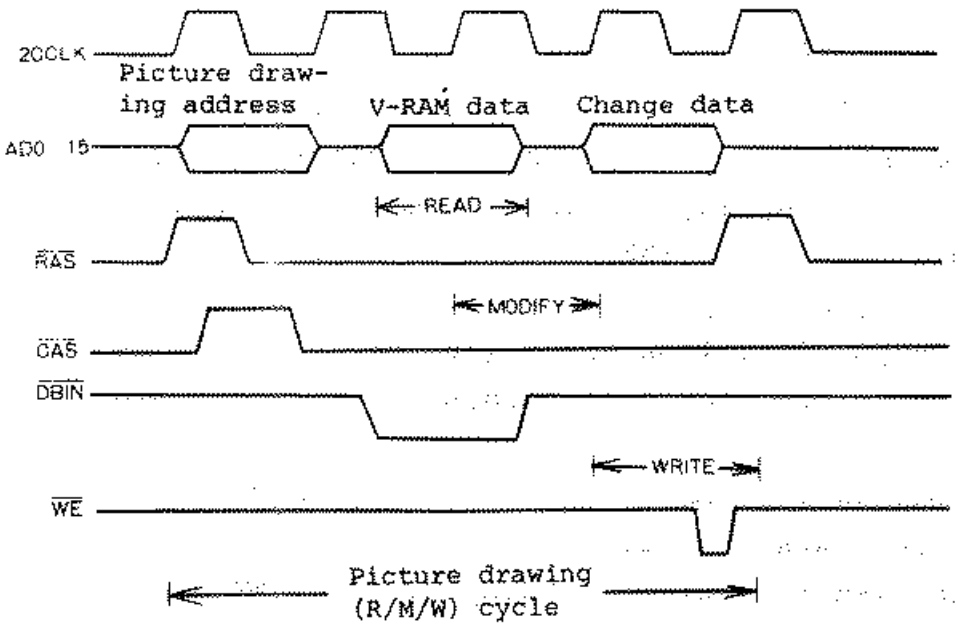



Fig. 8-10 Picture drawing (R/M/W) cycle

### 8.7.3 Video data write circuit

As shown in Fig. 8-10, the timing of writing data in the video memory is delayed by 2.25 clocks of 2CCLK from the trailing edge of $\overline{DBIN}$ signal. The circuit to supply this write ($\overline{WE}$) signal is shown in Fig. 8-11. The $\overline{DBIN}$ signal output from the GDC μPD7220 is coupled to the D-type flip-flop LS175 (1B) having 2CCLK as a clock, where the signal is delayed by 2 clocks of 2CCLK.

The output is applied to the next stage J-K flip ALS112 (3B), where it is further delayed by 1/4 clock of 2CCLK, and the output is supplied as a $\overline{WE}$ signal.

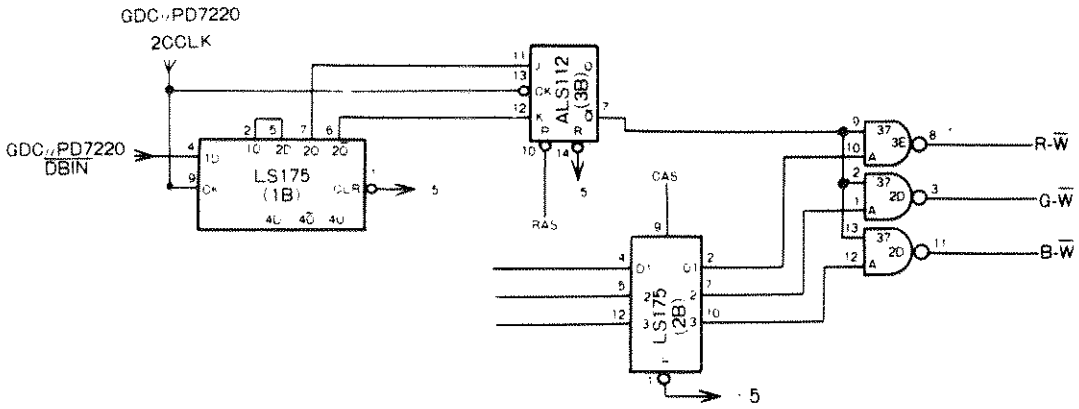



Fig. 8-11 Video data write circuit

## 8.8 Video data output circuit

When a display address is supplied to the video memory during the display cycle of the GDC μPD7220, the display data is output from the video memory onto the address data bus line.

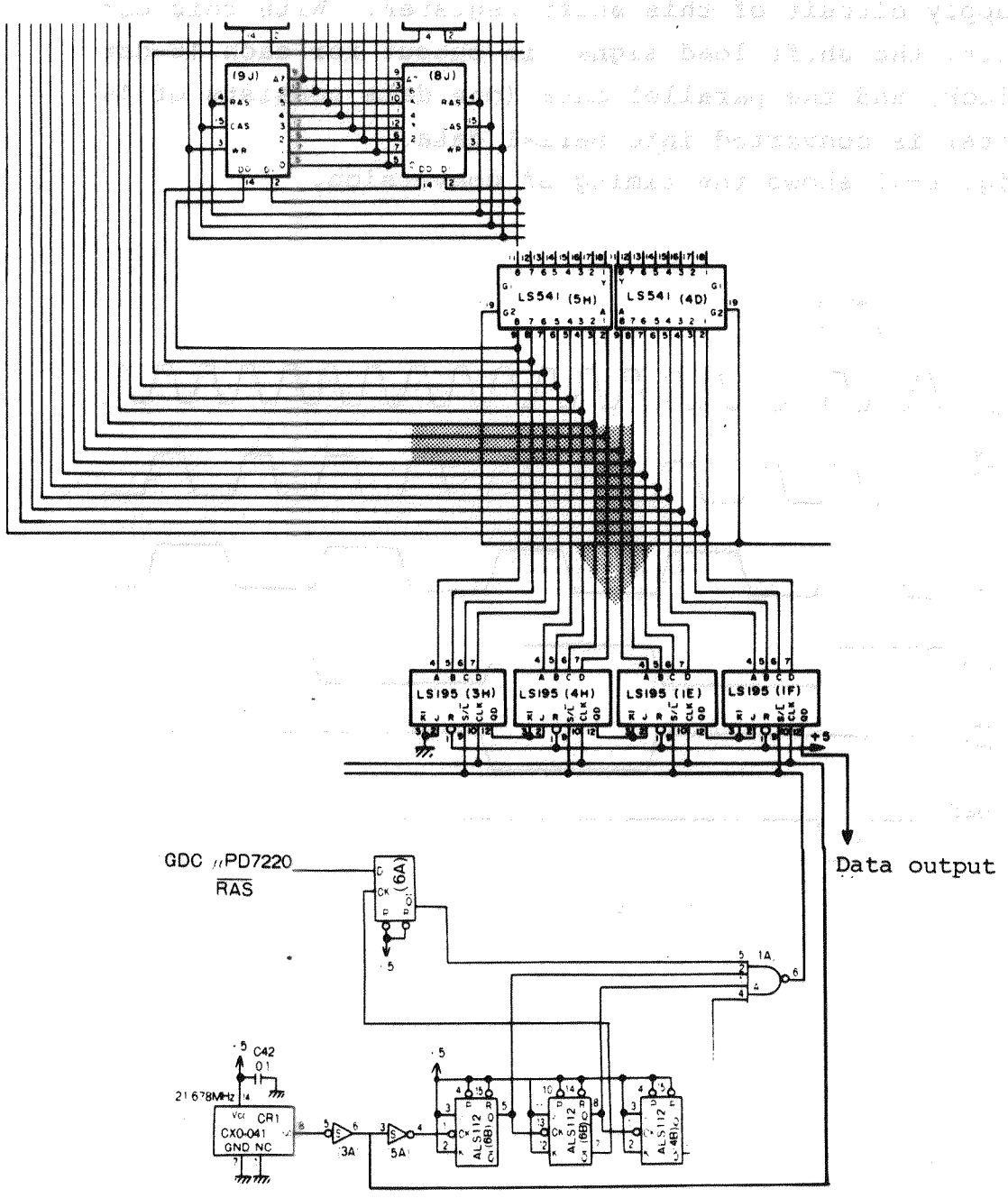



Fig. 8-12 Shift load signal supply circuit

For displaying these parallel data on the CRT, it is necessary to convert them into serial data. The shift register LS195 is inserted onto the address data bus line to make parallel-to-serial conversion of the video data.

The circuit shown in Fig. 8-12 is the shift load signal supply circuit of this shift register. With this circuit, the shift load signal is output for each 16-dot clock, and the parallel data (one data consists of 16 bits) is converted into serial data.

Fig. 8-13 shows the timing of conversion.

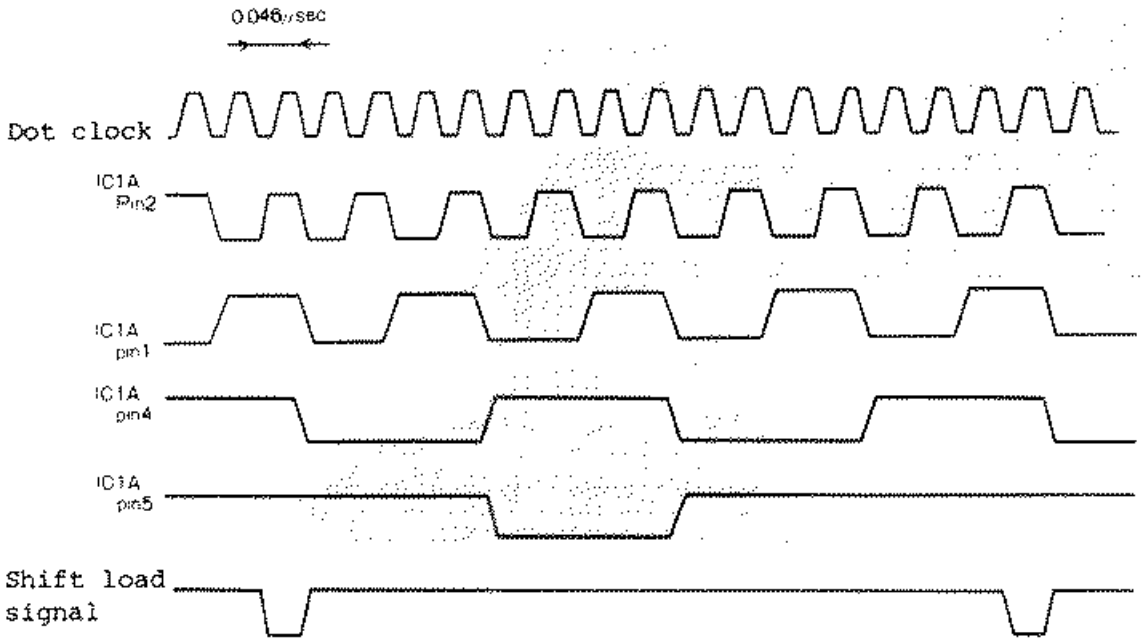



Fig. 8-13

## 8.9 Video signal conversion circuit

The video data output from the shift register of each memory plane is applied to the D-type flip-flop ALS574 (3A).

The ALS574 (3A) uses 21.679 MHz as a clock, which provides a dot clock of video data. On the other hand, the signal indicating the blanking period is generated from the $\overline{\text{BLANK}}$ signal terminal of the GDC μPD7220. As shown in Fig. 8-14, this $\overline{\text{BLANK}}$ signal is ANDed with the data of each memory plane, disabling display during the blanking period.

The video data is finally transmitted via the transistor (2SC1384) driven with +5 V and output to the color monitor as an NRZ (Non-Return to Zero) signal of TTL level.

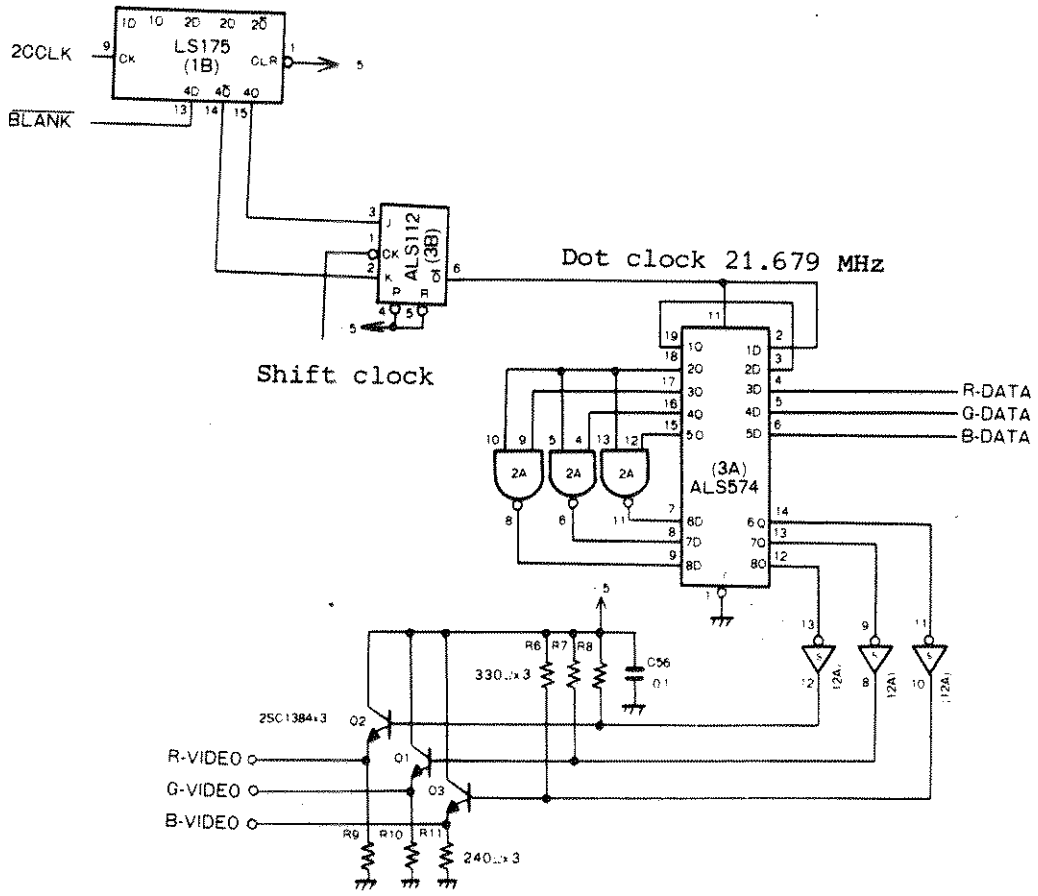



Fig. 8-14

# CHAPTER 9 Q10LP - LIGHT PEN -

## 9.1. General

The Q10 LP light pen is used, as shown in Fig. 9-1, to detect the light from the fluorescent element by touching the light receiving unit at the light pen tip and converting it into an electric signal. The photo signal converted into an electric signal is amplified in the light pen and then converted to the TTL level (negative logic) on the basis of a certain threshold level, and output as an address signal when the light pen detects the light on the CRT screen.

The light pen is provided with a photoelectric switch which is actuated by pressing the light receiving unit of the light pen tip onto the CRT screen. The switch output is output to the QX-10 as a light pen interrupt signal.

The light pen is connected to the DIN connector (5B type) on the rear panel of the main unit, and supported by EPSON Japanese BASIC and EPSON Multifonts BASIC.

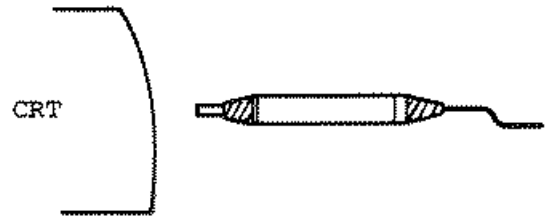



Fig. 9-1

## 9.2. Specifications

### 9.2.1 Electrical specifications

| | | | |
|---|---|---|---|
| 1. | Signal output | : | TTL (negative logic) |
| 2. | Switch output | : | TTL (negative logic) |
| 3. | Response speed | : | 400 ns - 800 ns |
| 4. | Optics | : | 5L7 |
| 5. | Resolution | : | 3 mm in diameter |
| 6. | Supply voltage | : | +5 V (50 mA) |
| 7. | Switch stroke | : | 1.2 mm $\pm$0.2 mm |
| 8. | Switch pressure | : | 100 g $\pm$30 g |
| 9. | Wavelength range | : | 420 - 980 mm |

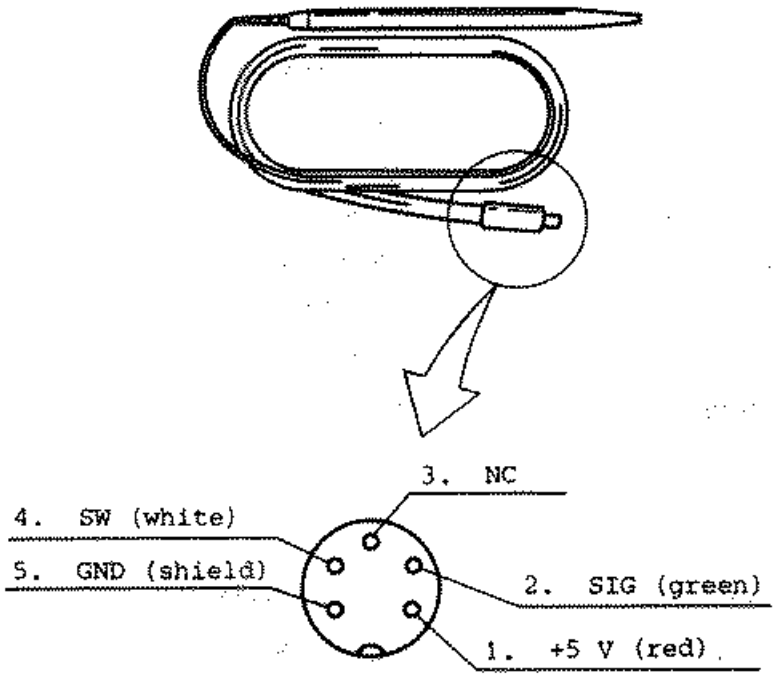
### 9.2.2 Environmental conditions

| | | | |
|---|---|---|---|
| 1. | Temperature | : | Operational: 0 - +55°C |
| | | | Storage : -10 - +75°C |
| 2. | Humidity | : | 0 - 95% (no dew) |

### 9.2.3 Dimensions and weight

| | | | |
|---|---|---|---|
| 1. | Dimensions | : | 12ø x 140 mm |
| 2. | Weight | : | 40 g |
| 3. | Cable length | : | 1500 mm |

### 9.2.4 Connector specifications




(TOP VIEW)

Fig. 9-2

## 9.3. Structure

### 9.3.1 Names of each part

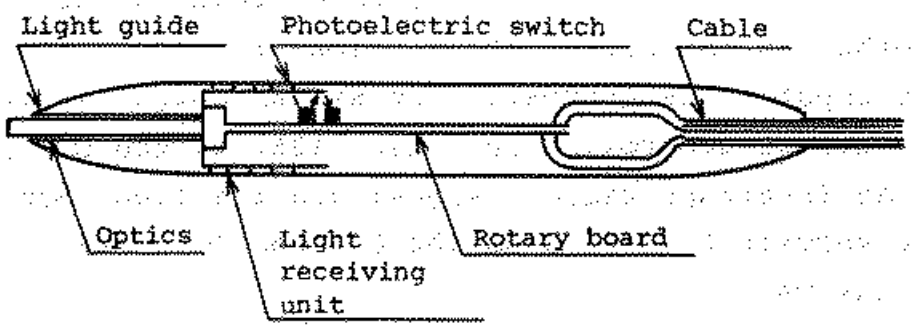



Fig. 9-3 (a)

### 9.3.2 Photoelectric switch

The photoelectric switch utilizes optical reflection as shown in Fig. 9-3 (b). An LED and phototransistor are combined to make a contactless switch.

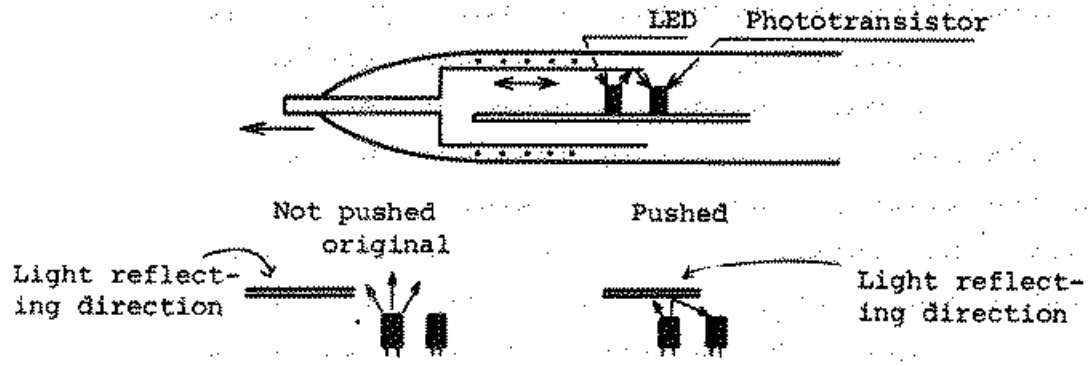



Fig. 9-3 (b) Photoelectric switch structure

## 9.4. Light Pen Sequence

The light pen has two outputs: one is the output of the switch (photoelectric switch actuated by pushing force), and the other is the signal (SIG) output responsive to the light input. The photoelectric switch output is sent to the interrupt controller μPD8259A (12E) on the Q10 SYM board as an interrupt request signal via the light pen interrupt service flip-flop on the Q10 GMS (Q10 CMS) board in the QX-10.

The SIG output is applied to the light pen input terminal of the graphic display controller μPD7220 and used to latch the address when the light pen detects the light on the CRT screen. It is also used to raise the light pen status flag in the GDC.

The photoelectric switch output is also turned on when the light pen is pushed against anything other than the CRT screen. Therefore, the light pen interrupt service routine needs to be executed after checking the light pen status flag in the GDC.

Fig. 9-4 is the flow chart showing the light pen sequence. As stated above, when the light pen is used, the interrupt processing is executed. If the light pen is continuously pushed against the screen, the interrupt occurs continuously disabling other processing. Therefore, the light pen interrupt mask must be set immediately after the light pen address is read.

The light pen interrupt level is as shown in Table 5-1. The above should be particularly noted, as the interrupt levels of floppy disk, printer, calendar clock option and software timer 2 are lower than that of the light pen.

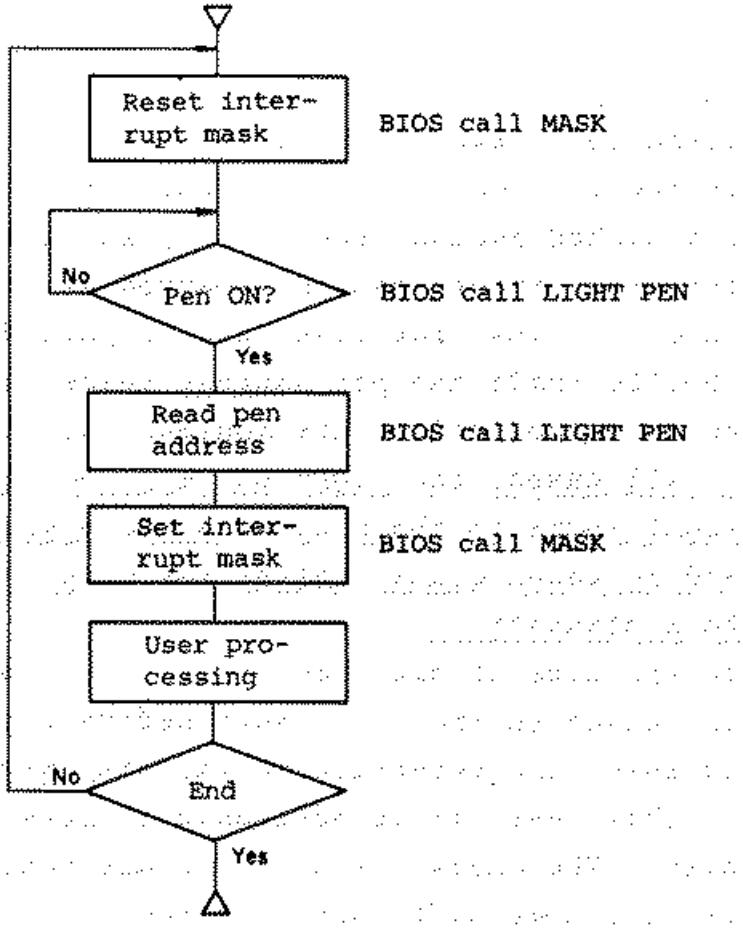



Fig. 9-4 Light pen sequence

## 9.5. Precautions on Using Light Pen

9.5.1. The display is divided into 400 dots in the vertical direction. Even a slight displacement (particularly in the vertical direction) while the light pen is being pushed against the display surface results in incorrect input, causing lowered sensitivity. (Because, when the light pen is pushed once, the μPD7220 reads the pen address twice and does not make an interrupt unless the address coincides.)
In all cases, the light pen must be applied at a right angle to the display surface and pushed gently and released quickly after the display picture comes to a standstill.
In the case of green monitor, if the brightness in increased to the level just before the back raster is seen, the detection sensitivity may be lowered. In this case, it is advisable to make highlight display. The character with low dot density (e.g., "1") is sometimes difficult to detect. In this case, use an inverted character for a selector or color the back screen.

9.5.2. The light pen detects some colors easily and some with difficulty. Generally, the detection sensitivity becomes lower in the order of blue, green and red. The light pen detection sensitivity is particularly low against red. Thus, detecting the part displayed red with the light pen should be avoided.
The light pen detects the color mixed with red, e.g., purple, normally.

9.5.3. An interrupt occurs continuously as long as the light receiving unit at the tip of the light pen is being pushed, and all other processings are suspended during this period. Therefore, avoid pushing the light receiving unit of the light pen unnecessarily.

## 9.6. Software

Support by QX-10 HP CP/M (BIOS entry address F657M)

LIGHT PEN

Functions : (1) Check if the light pen is pushed.
(2) Read the light pen input data.

Input parameters: C:2 in (1) above
C:3 in (2) above

Results : In (1) above

A:0 The light pen is not pushed.

A:0FFH The light pen is pushed and data is input.

In (2) above

A:0 No data

A: Other than 0 Data is input.

BC: Position in the horizontal direction

0 - 79 (green CRT used non-MFBASIC, non-MF mode)

0 - 39 (green CRT used non-MFBASIC, MF mode MFBASIC width 80 mode MFBASIC width 40 mode) (Color CRT used)

DE: Position in the vertical direction

0 - 24 (green CRT used non-MFBASIC, non-MF mode)

0 - 399 (green CRT used non-MFBASIC, MF mode MFBASIC width 80 mode MFBASIC width 40 mode) (Color CRT used)

Zflag:0 Error

A:1 Parameter error

Others: Destruction

PEN

Function : Provides the data input from the light pen.

Format : PEN ( < function > )

Description: PEN function provides information about the current state of the light pen. < Function > takes the value of 0 - 4 and has the following functions.

PEN (0): Trigger sense
Indicates whether the light pen is pushed after PEN (0) function is last read. True (-1) is returned if the light pen is pushed, false (0) if not. Note that this information indicates whether or not the light pen has been pushed, not whether or not it is now being pushed. When PEN (0) function is once read, it is reset. As the coordinates used by PEN (1) - PEN (4) are also read when PEN (0) function returns a true value, it must be confirmed before PEN (1) - PEN (4) are used that PEN (0) function returns a true value.

PEN (1): Returns the horizontal coordinates when the light pen is pushed as graphic coordinates. The value of 0 - 624 is returned. As the light pen resolution is 16 dots in the horizontal direction, the value is returned skipping 16 numbers.

PEN (2): Returns the vertical coordinates when the light pen is pushed as graphic coordinates. The value of 0 - 400 is returned.

PEN (3): Returns the horizontal coordinates when the light pen is pushed as character coordinates. In the 40-digit mode, the value of 1 - 40 is returned. In the 80-digit mode, the value of 1 - 80 is returned. As the light pen resolution is two characters in the horizontal direction, the value is returned skipping two numbers.

PEN (4): Returns the vertical coordinates when the light pen is pushed as character coordinates. The value of 1 - 20 is returned.

Before using the PEN function, be sure to execute the ON statement to permit input of the light pen.
If not, "Illegal function call" error occurs. When the light pen is not used, it is better to execute the OFF statement to disable hardware interrupt of the light pen.

Support by QX-10 BASIC

PEN

Function : Controls ON/OFF of light pen input.

Format : PEN ON
OFF

Description: PEN ON enables use of PEN function, and PEN OFF disables use of it. Before using the PEN function, be sure to execute the PEN ON statement.