JADE
Computer Products

THE BIG Z
REVISION C

2 MHz OR 4 MHz SWITCHABLE Z-80 CPU WITH ON-BOARD SERIAL I/O PORT

INTRODUCTION

The **JADE BIG Z** Z80 Microprocessor CPU board is a very stable and powerful CPU, designed for the S-100 bus and in reasonable conformity with the proposed IEEE S-100 Bus Standard.

The **Big Z** CPU provides on-board EPROM and on-board serial communications via an RS232C standard interface which supports transmit and receive data and one standard handshake line.

The **Big Z** CPU board has been manufactured to the most exacting specifications, using the highest quality material and components conservatively rated for long life. As such, it may be expected to give you many thousands of hours of useful active service.

If you have purchased the **Big Z** as an assembled and tested unit, you should know that it has passed rigorous tests, running in a real-time disk-based environment and executing the most complicated programs we can devise. Before it goes out the door, every assembled and tested **Big Z** must prove itself to our picky engineering personnel.

Although any component can fail, most ICs die in their infancy, and the burn-in time each **Big Z** receives insures that we catch practically all of these infant mortalities.

If you have purchased the **Big Z** as a kit, we strongly urge you to read this manual in its entirety before attempting to construct the board. Although there are about as many ways of assembling a board as the tenth power of the components on it, if you will follow the assembly instructions step-by-step, construction will be easier for you and much more pleasurable for both of us.

FEATURES

On-board 2708/2716/2732 EPROM can be addressed to any 1K, 2K, or 4K boundary. * Power-on jump directly to the on-board EPROM. * Optional wait state for on-board EPROM. * On-board EPROM may be used in shadow mode (accessed only after power-on or reset). * Allows full 64K RAM memory to be used. * On-board 8251 USART for synchronous or asynchronous RS232 operation. * Independent crystal-controlled baud rate generator provides all standard baud rates from 110 to 9600. * Switch-selectable 2 or 4 MHz operation. * Optional M1 wait states can be generated. * Automatic MWRT generation if a front panel is not used, automatically disabled if a front panel is connected. * DMA capability. * Latched data output bus provides additional data hold time for reliable operation with all device types. * Straight-through address and data paths provide improved read access times for I/O and memory devices. * On-board serial port switch-selectable to any pair of I/O port locations from 00 through FE hex. * Reverse channel capability on USART allows use with buffered peripherals or devices with "not ready" indication. * Front panel data cable interface. * Fully buffered S-100 interface. * Separate voltage regulators (no diodes) assure a clean, stable power supply. * Intelligent, clean layout of PC board. * Reflow soldered, plated, and fully masked PC board. * Gold-plated S-100 bus connector is Imsai standard. * Complete 1K monitor software listing included in manual. * Fully warranted by **JADE**, one of the largest microcomputer product suppliers in the world.

FUNCTIONAL DESCRIPTION

Figure 1-1 is a block diagram describing the functional blocks contained on the **JADE Big Z** CPU. The following sections describe each of the blocks in Figure 1-1.

Z80 CPU

At the heart of the Big Z is the powerful Z80 microprocessor which provides the major control signals required to read and write to memory and I/O ports. Also generated by the Z80 are a 16-bit address bus and an 8-bit bidirectional data bus.

OSCILLATOR

The oscillator is a crystal-controlled circuit which generates Phi1 and Phi2 clock signals for the S-100 bus, the Clock* S-100 signal, and the internal system clock. Also involved with this circuitry are the Reset and Power-on Clear signals.

STATUS AND CONTROL BUFFERS

The status and control buffers provide the drive for the various S-100 bus status and control signals. During a DMA operation (when BUSAK is high on the Z80 chip), or during maintenance functions, the status and control buffers are tri-stated, allowing a DMA device to control the bus as a temporary bus master.

ADDRESS BUFFER

The address buffer is a 16-bit tri-state buffer which drives the 16-bit address to the S-100 bus. It also is tri-stated during DMA operations or maintenance functions.

DATA OUT BUFFER

The data out buffer is an 8-bit tri-state buffer which drives the 8 data out signals to the S-100 bus. Data is gated out to the S-100 bus only during memory write or I/O output cycles. The data out buffer is tri-stated during DMA operations or maintenance functions.

DATA IN BUFFER

The S-100 data in bus is provided to the Z80 during read memory or I/O input bus cycles by the data in buffers. These buffers are disabled during write memory or I/O output cycles, and for DMA operations. They may also be disabled by the following conditions;

RUN and SS (Single Step) low (false) at pins 71 and 21 of the S-100 bus.

On-board EPROM selected during a memory read operation.

USART selected during an I/O operation.

Power-on jump enabled and Power-On Latch (2 sections of U10) is set.

MEMORY DECODE AND CONTROL

The memory decode and control circuitry decodes the high-order address bits from the internal address bus and selects the EPROM. This block also generates the signals required to disable the data in buffers and interacts with the Shadow option circuitry to phantom out the EPROM.

EPROM

The on-board EPROM can be either a 1K (2708-type), 2K (2716 or TMS2716 type), or 4K (2732-type) EPROM. The EPROM may be switch selected for any 1K, 2K, or 4K boundary, depending on the type of EPROM installed.

I/O ADDRESS DECODE AND CONTROL

The I/O address decode and control circuitry decodes the lower 8 bits of the internal address bus to determine which ports are being accessed during I/O instructions. This block also interacts with the EPROM select circuitry and the circuitry which disables the data in buffers.

SERIAL I/O

The serial I/O provides synchronous and asynchronous communications via RS232C level interfaces. Included in this block is the crystal-controlled oscillator and baud rate generator for the 8251 USART.

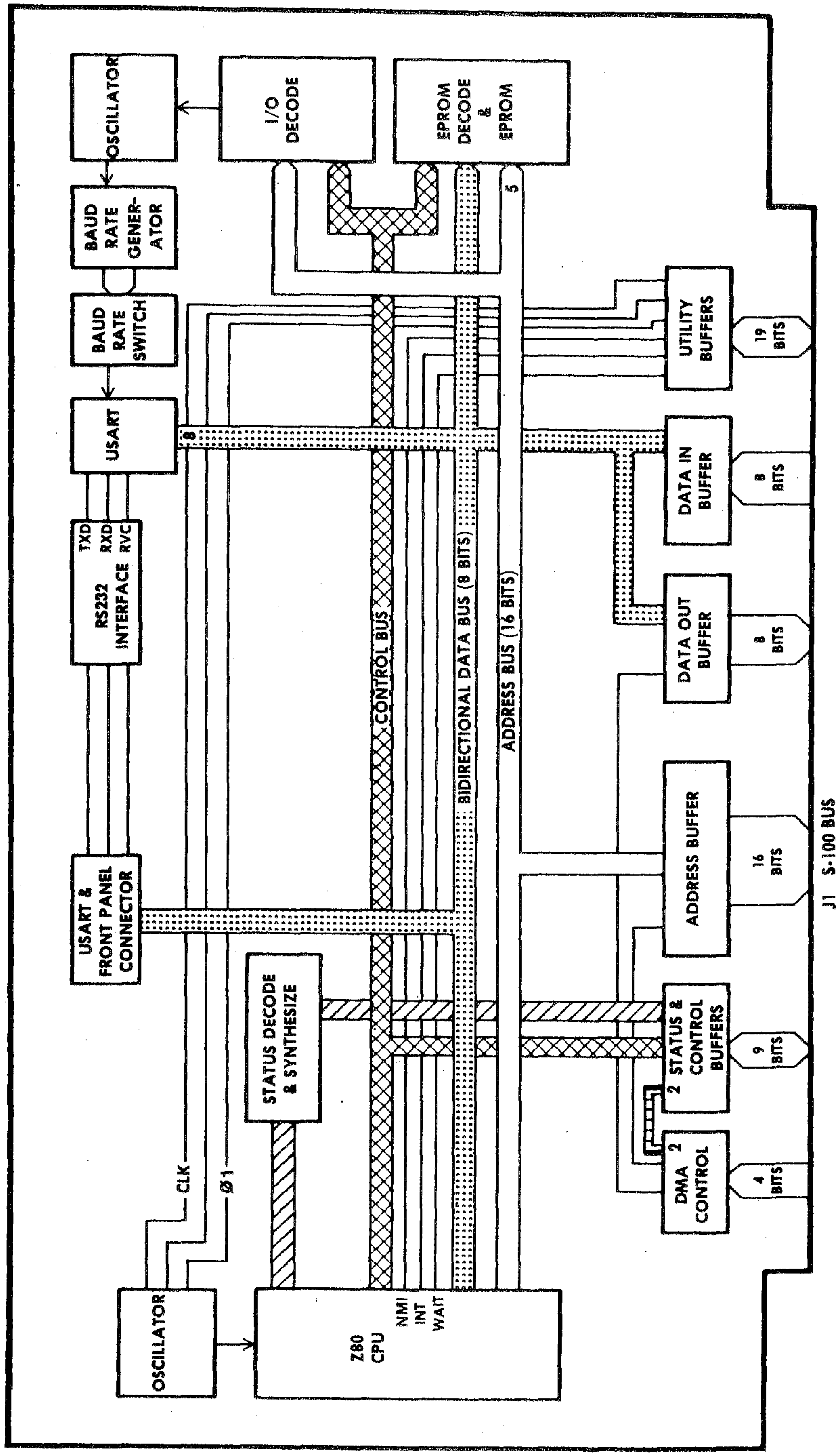
OSCILLATOR
I/O DECODE
EPROM DECODE & EPROM
5
BAUD RATE GENERATOR
BAUD RATE SWITCH
UTILITY BUFFERS
19 BITS
USART
8
DATA IN BUFFER
8 BITS
TXD
RXD
RVC
RS232 INTERFACE
CONTROL BUS
BIDIRECTIONAL DATA BUS (8 BITS)
ADDRESS BUS (16 BITS)
DATA OUT BUFFER
8 BITS
ADDRESS BUFFER
16 BITS
J1 S-100 BUS
USART & FRONT PANEL CONNECTOR
STATUS DECODE & SYNTHESIZE
STATUS & CONTROL BUFFERS
9 BITS
2
DMA CONTROL
4 BITS
CLK
Ø1
OSCILLATOR
Z80 CPU
NMI
INT
WAIT

Figure 1.1

TECHNICAL DESCRIPTION

S-100 INTERFACE

Address Bus

The internal address bus is driven to the S-100 bus by tri-state buffers U25, U36, and a portion of U35. These buffers (8T97, 8097, or 74367 ICs) are tri-stated during DMA operations or maintenance functions. This is accomplished via one of the inverter sections of U18, which is driven by the ADDSB* signal on pin 22 of the S-100 bus. Normally, the input to the inverter is held high by a pullup resistor on pin 1 of U18, which forces a low output from the inverter on pin 2. This low level signal is routed to the enable pins on the address buffers.

When ADDSB* goes true (low), the output on pin 23 of the inverter U18 goes high, disabling the address buffers.

Data In Bus

The internal bidirectional data bus is driven from the S-100 bus by tri-state buffers U38 and a portion of U29. These buffers are enabled only during read memory or I/O input cycles. They are also disabled by the following conditions:

1. SSWDSB* is low (true) at pin 53 of the S-100 bus. This signal is one of the inputs to NAND gate U22, along with sWO*. It is normally held high (false) by pullup resistor pack U31.

2. RUN or SS on pins 71 and 21 respectively of the S-100 bus is low (false). These signals are held normally high by pullup resistors in resistor pack U31. They are inputs to NOR gate U8. This NOR output is NORed with the NAND of SSWDSB* and sWO* by another section of U8, and this signal is applied to pin 3 of the 3-input NAND gate U4, where it is NANDed with the signals discussed below.

3. On-board EPROM is selected during a memory read operation. The signal EPS*, which is the output from pin 6 of AND gate U7 is applied to pin 4 of NAND gate U4.

4. On-board USART selected during an I/O operation (either input or output cycle). The DCS* signal, generated as the output of OR gate U14 at pin 8, is applied to pin 5 of NAND gate U4, whose output drives the tri-state input of data in buffers U38 and U29.

5. Power-on Jump is enabled and the Power-On Latch (2 sections of U10) is set.

Data Out Bus

The internal data bus is provided to the S-100 DO (data out) bus for memory write or I/O output cycles by tri-state buffers U37 and a portion of U25. The DODSB* signal on pin 23 of the S-100 bus will disable these buffers when it goes low (true). It is provided to the tri-state control inputs of the buffers via inverter U18. The input to inverter U18 on pin 13 is held normally high by pullup resistor R1, forcing the output of the inverter to be low, thereby enabling the buffers. When DODSB* goes true (low), the pullup resistor is overcome and the tri-state inputs of the buffers go high, disabling (tri-stating) these buffers.

The input to the data out buffers are provided by latches U27 and U26. Data is passed through the latches by the high level of Phi2 clock. The falling edge of Phi2 clock disables the latches.

A true (low) signal at DODSB* will tri-state the data out bus for DMA or maintenance functions.

Status Signals

The primary status signals sM1, sOUT, sINP, sMEMR, and sWO* are provided to the S-100 bus via tri-state buffer U39. U39 is tri-stated by STADSB*, on pin 18 of the S-100 bus, going low (true). Normally, a pullup resistor holds the input to inverter U30 on pin 1 high, forcing the output of inverter U30 on pin 2 low, enabling the buffer at U39. When STADSB* goes true (low), the output of the inverter goes high, tri-stating the U39 buffer.

sM1 on pin 44 of the S-100 bus is provided by the CPU through buffer U39 and inverter U30. It is derived from the Z80's M1* signal, on pin 27 of the CPU. This signal is applied to pin 9 of inverter U30. The output of U30, pin 8, will be high when the Z80 M1* signal is true (low). The output of U30 is applied to input pin 14 of buffer U39 and is transferred to the S-100 bus from output pin 13 of buffer U39, provided that U39 is not tri-stated by a true (low) signal on STADSB*

sM1 signals that the processor is fetching an instruction op code; therefore, it signals an opcode fetch cycle.

sOUT on pin 45 of the S-100 bus is provided by the CPU through buffer U39, AND gate U41, and inverters U18 and U30. It is derived from the Z80 WR* and IORQ* signals. These outputs from the Z80, on pins 22 and 20 respectively, are inverted by U18 and U30. The outputs of these inverters, on pins 8 and 10 respectively of U18 nd U30, will be high when WR* and IORQ* are true (low). If both of these outputs are high—meaning that WR* and IORQ* are true—the output of AND gate U41, on pin 11, will also be high. This signal is output to pin 12 of U39 and is transferred to the S-100 bus from U39 output pin 11, provided U39 is not tri-stated by STADSB* being true (low).

sOUT signals an output to an I/O port; therefore, it may be referred to as an I/O output cycle signal.

sINP on pin 46 of the S-100 bus is provided by the CPU through buffer U39, latch U40, AND gate U41, and inverter U30. It is derived from the Z80's RD* and IORQ* signals. These outputs from the Z80, on pins 21 and 20 respectively, are applied to U30 inverter pins 3 and 11. The outputs of the inverter, on pins 4 and 10 respectively, are applied to AND gate U41 on input pins 10 and 9. When the outputs of inverter U30 are high (Z80 RD* and IORQ* signals are low (true)), the output of AND gate U41, on pin 8, will be high. This signal is applied to the input of U40 latch on pin 7. Now, when PSYNC is high, the signal is clocked through U40, being output on pin 9, and is applied to buffer U39 input pin 10. The signal is transferred through the buffer, output on pin 9, to S-100 bus pin 46, provided U39 is not tri-stated by STADSB* being true (low).

sINP signals an input from an I/O port; therefore, it may be referred to as an I/O input cycle signal.

sMEMR on pin 47 of the S-100 bus is provided by the CPU through buffer U39, latch U40, AND gate U41, and inverters U18 and U30. It is derived from the Z80's RD* and MRQ* signals. These outputs from the Z80, on pins 21 and 19 respectively, are applied to inverters U30 and U18, on input pins 3 and 3 respectively. The output of these inverters, on pins 4 and 4 respectively, will be high when the Z80 signals RD* and MRQ* are true (low). The outputs of the inverters are applied to input pins 5 and 4 of AND gate U41. When both of these inputs are high, the output of U41, on pin 6, will be high. This output is applied to input pin 6 of U40. Now, when PSYNC is high, the signal is clocked through the latch and is output on pin 10 of U40. This output is applied to input pin 6 of buffer U39. It passes through the buffer, is output on pin 7, and is applied to S-100 pin 47, provided that STADSB* is not active (low).

sMEMR signals a read from memory; therefore, it may be referred to as a memory read cycle signal.

*sWO** on pin 97 of the S-100 bus is provided by the CPU through buffer U39, latch U40, NAND gate U22, and inverter U18, together with inverter U30 and AND gate U41. It is derived from the Z80's RD* and INTA* signals, where INTA* is derived—itself—from the Z80 signals M1* and IORQ*.

Z80 signal RD*, on pin 21 of the CPU, is applied to input pin 2 of NAND gate U22. The other input pin is driven by the output of inverter U30, pin 6. The input to this inverter is the output of AND gate U41. U41 ANDs IORQ with M1. These signals are provided from the Z80's IORQ* and M1* signals on pins 20 and 27 respectively of the CPU.

When RD* is false (high) and IORQ* and M1* are both false (also high), the output of NAND gate U22, pin 3, will go low. This low is applied to latch U40 on pin 3 and is clocked through the latch by PSYNC, being output on U40 pin 15. This output is applied to U39 buffer input pin 4, is transferred through the buffer to pin 5, and output to S-100 bus pin 97 as sWO*. Note that the following conditions must be met for sWO* to be true: the processor is not in a read cycle (RD* is false—high), and neither is it in an Interrupt Acknowledge cycle (IORQ* ANDed with M1* is false).

sWO* signals that the processor is not in a data input cycle. It is used as an early indication that a write operation will take place.

Other Status Signals

The IEEE-defined status signal sXTRQ* is not supported by the Big Z CPU. This signal is used to request a 16-bit wide input or output, and gangs the DO and DI buses together to form a single 16-bit bidirectional data bus. Since the Big Z is not a 16-bit processor, this signal protocol is not implemented.

sINTA on pin 96 of the S-100 bus is provided by the CPU through buffer U6, AND gate U41, and inverter U30. It is derived from the Z80's IORQ* and M1* signals. These outputs from the Z80, on pins 20 and 21 respectively, are inverted by inverter U30. The signals are applied to input pins 11 and 9 of U30, and output on pins 10 and 8, respectively, as inverted signals. They are then applied to input pins 1 and 2 of AND gate U41 When the Z80 IORQ* and M1* are both true (low), the outputs of both inverters will be high. These high signals, applied to AND gate U41, result in a high being output on pin 3 of U41. This is applied to buffer U6 input pin 4, transferred through the buffer, output on pin 4, and applied to S-100 bus pin 96 as sINTA, provided that CCDSB* is false (high).

sINTA signals that the processor is acknowledging an interrupt request from a peripheral device; therefore, it may be referred to as an interrupt acknowledge signal.

sHLTA on pin 48 of the S-100 bus is provided by the CPU through buffer U17 and inverter U18. It is derived from the Z80's HLTA* signal on pin 18 of the CPU. HLTA* is applied to pin 5 of inverter U18, where it is inverted and output on pin 6 as HLTA. HLTA is applied to buffer U17, input pin 6, is transferred through the buffer, and output on pin 7, where it is applied to S-100 bus pin 48. Buffer U17 is always enabled, since the tri-state inputs are grounded.

Control Signals—Output

There are five control signals defined by IEEE as control outputs. These are: pSYNC, pSTVAL*, pDBIN, pWR* and pHLDA.

*pSTVAL** is not implemented on the Big Z CPU. This is defined as a signal which, in conjunction with pSYNC, indicates that stable address and status information may be sampled from the bus in the current cycle. For Big Z applications, it is redundant and is therefore not implemented.

pSYNC is generated by one-shot U5, which is clocked by the Z80 signals IORQ*, RFS* and MRQ*. pSYNC is transferred to pin 76 of the S-100 bus through buffer U6, which may be tri-stated by the signal CCDSB*.

Z80 RFSH* is applied directly to pin 4 of NAND gate U10, where is is NANDed with MRQ. MRQ is derived from the Z80 MRQ* through inverter U18. MRQ*, on pin 19 of the CPU, is applied to U18 pin 3, inverted, and output on pin 4 as MRQ. MRQ is applied to input pin 5 of NAND gate U10. When the Z80 signal MRQ* is true (low), and RFSH* is false (high), both inputs of the NAND gate U10 will be high, resulting in a low output from pin 6. This output is NANDed by gate U4 with IORQ* from the Z80 pin 20. The output of U4 at pin 12 is applied to one-shot U5. The multivibrator clocks out, with its timeout period being determined by C24, a 100 picofarad capacitor, and R2, a 2.7K ohm resistor. The timeout, with these values, is approximately 270 nanoseconds. The output of the U5 multivibrator, on pin 6, is applied to U6 buffer input pin 10. It is transferred through U6 to output pin 9, and from there to the S-100 bus pin 76 as pSYNC.

pSYNC is only high during the first part of a memory or I/O cycle due to the effect of multivibrator U5. It is used to indicate the start of a new bus cycle, and is provided for those S-100 devices that look at status information during this time as per 8080 device conventions.

pDBIN on pin 78 of the S-100 bus is provided by the CPU through buffer U6 as an OR of Z80 signals RD* and IORQ* being—either of them—true. Z80 signal RD*, on pin 21 of the CPU, is inverted by inverter U30. The output of U30 on pin 4 is applied to input pin 1 of OR gate U14. The other input to this OR gate, pin 2, is derived from the output of AND gate U41, which ANDs together IORQ* and M1* both true to generate INTA (Interrupt Acknowledge). Either INTA or RD* true will generate a high output from OR gate U14, pin 3. This is applied to U6 buffer input pin 6, transferred through the buffer to output pin 7, and drives S-100 bus pin 78 (pDBIN), provided that the buffer is not tri-stated by a true condition of CCDSB*.

pDBIN signals that the processor is in a data input cycle, either I/O or memory read; therefore, it is a generalized read strobe gating data from an addressed bus slave onto the data in bus.

*pWR** on pin 77 of the S-100 bus is provided by the CPU through buffer U6 as a slightly delayed WR* signal from the Z80 CPU. Z80 signal WR*, on pin 22 of the CPU, is applied to inverter U18. The output of U18 on pin 8 is applied to both inputs of OR gate U8 on pins 5 and 6. The output of this OR gate on pin 4 is applied to buffer U6 input pin 2, is transferred through the buffer to output pin 3, where it is driven to S-100 bus pin 77, provided that buffer U6 is not tri-stated by CCDSB* being true.

pWR* signals that the processor is in a data output cycle, either I/O or memory; therefore, it is a generalized write strobe that writes data from the bus into an addressed bus slave.

pHLDA on pin 26 of the S-100 bus is provided by the CPU through buffer U17. It is simply an inverted Z80 BUSAK*. BUSAK* from the Z80, on pin 23, is applied to inverter U15 pin 5. The output of this inverter is applied to buffer U17 input pin 10, is transferred through the buffer, exits on pin 9, and is then applied to S-100 bus pin 26. When BUSAK* is true (low) on the Z80, pHLDA will be high on the S-100 bus.

pHLDA is the hold acknowledge signal that indicates to the highest priority device that is requesting a hold that the CPU is relinquishing control of the bus. When a device requests a hold and is acknowledged by the CPU, the Z80 tri-states its own data and address busses and generates BUSAK* true, which is passed to the S-100 bus as pHLDA. This signal is always passed onto the bus, since the tri-state inputs of buffer U17 are grounded and the buffer is always enabled.

Control Signals—Input

There are six control input lines defined by IEEE. These are: RDY, XRDY, INT*, NMI*, HOLD*, and SIXTN*.

*SUXTN** is not implemented on the Big Z CPU. SIXTN* is a 16-bit acknowledge signal indicating that a requested 16-bit data transfer is possible. Since the Big Z is an 8-bit oriented CPU, this signal is not required.

RDY is provided to the CPU from S-100 bus pin 72. This is a general ready line, and is specified as an open collector line. It is input to the CPU card from S-100 connector pin 72 and is routed to AND gate U7 where it is ANDed with XRDY. A pullup resistor on resistor pack U32 holds pin 2 of AND gate U7 normally high.

XRDY is provided to the CPU from S-100 bus pin 72. This is a special ready line commonly used by front panel devices to stop and single-step the processor. The IEEE does not specify it is an open collector line.

therefore it should not be used by other cards on the bus else a bus conflict may be created. XRDY is also routed to AND gate U7. A pullup resistor on resistor pack U31 holds pin 1 of AND gate U7 normally high.

A low on either input of U7 will result in a low output from pin 3. In other words, when either XRDY or RDY go false (low), the output of U7 will go low. The output of U7 (pin 3) is applied to input pin 12 of AND gate U7, where it is ANDed with the output of the wait-state generator U20, which is normally low unless a wait state is being generated. The output of U7, pin 11, is applied to the Z80 WAIT* input on pin 24 of the CPU. Therefore, a wait state is generated to the Z80 by either the wait state generator U20, or by XRDY or RDY being pulled low (going false) on the S-100 bus.

*INT** and *NMI** are input directly to the corresponding pins on the Z80 (pins 16 and 17, respectively), through input buffer U17. The tri-state inputs of U17 are grounded; therefore, the buffer is always enabled and these signals pass unimpeded through the buffer to the Z80 CPU.

These two lines are used to request service from the CPU. The INT* line may be masked by a Disable Interrupt command to the CPU, but the NMI* line is non-maskable and will always be responded to by the Z80. Both lines should be asserted as a level, rather than a pulse, and should be held true until the interrupt is acknowledged.

*HOLD** is input to the CPU from S-100 bus pin 74, through buffer U17. The output of U17, pin 3, is routed directly to the BUSRQ* line on the Z80 CPU on pin 25. Buffer U17 is never tri-stated, since its tri-state inputs are grounded; therefore, the CPU will always respond to HOLD*.

HOLD* is specified as an open collector line and signals that a bus device is requesting the Z80 to relinquish the bus for a DMA operation.

HOLD*, NMI*, and INT* are held normally high byu resistor pack U31 on the inputs of buffer U17.

Non-IEEE Control Lines

*RFSH** is provided to the S-100 bus as the non-inverted RFSH* signal of the Z80 CPU. Z80 RFSH* on pin 28 of the CPU is routed to input pin 12 of buffer U6. It is transferred through the buffer, exits on pin 11, and is routed to S-100 bus pin 66. This signal is generated as a service to dynamic memory cards that utilize the Z80 RFSH* signal.

MRQ is provided to the S-100 bus as the inverted MRQ* signal of the Z80 CPU. Z80 MRQ*, on pin 19 of the CPU, is inverted by U18, and is applied to input pin 12 of buffer U17 as MRQ. It is transferred through the buffer, exits on output pin 11, and is routed to S-100 bus pin 65. This signal is generated as a service to memory and other cards that require the MRQ signal.

Both of the above signals utilize S-100 pins that have not been defined by the IEEE S-100 Standards Committee; therefore, there should be no conflict with IEEE S-100 standard cards.

pWAIT is provided to the S-100 bus as the inverted WAIT* signal going into pin 24 of the Z80 CPU. It is buffered by inverter U18, and is generated as a service to those cards that may require it. It, also, uses an IEEE undefined S-100 pin, pin 27.

DMA Control Lines

The primary DMA control lines utilized by the Big Z CPU card are: DODSB*, ADDSB*, STDSB*, and CCDSB*.

*DODSB** comes into the Big Z CPU via pin 23 of the S-100 bus. It is routed through inverter U18, and is applied to the tri-state inputs of U37 and that portion of U25 which is concerned with the Data Out bus. The input side of inverter U18 is held normally high by pullup resistor R1. When DODSB* becomes true (low), the output of inverter U18 becomes high, disabling the data out buffers.

*ADDSB** comes into the Big Z CPU via pin 22 of the S-100 bus. It is routed through inverter U18 (pins 1 and 2), and is applied to the tri-state inputs of U36, U35, and that portion of U25 which is concerned with the Address bus. The input side of inverter U18 is held normally high by a pullup resistor in resistor pack U31. When ADDSB* goes true (low), the output of inverter U18 will go high, disabling the address bus buffers

*STADSB** comes into the Big Z CPU via pin 18 of the S-100 bus. It is routed through inverter U30, and is applied to the tri-state inputs of U39. The input side of inverter U30 is held normally high by a pullup resistor in resistor pack U28. When STDSB* becomes true (low), the output of inverter U15 goes high and disables buffer U6, tri-stating pSYNC, pDBIN, sINTA, and pWR*

The DMA arbitration lines DMA0* through DMA7* are not implemented on the Big Z CPU.

SYSTEM UTILITIES

System Power Lines

1. A positive 8 volt DC supply is assumed on S-100 pins 1 and 51. This supply is routed to voltage regulator VR4 where it is regulated to the plus 5 volts required by the chips on the board. A 1.5 microfarad tantalum capacitor is located on the input side of VR4, and a 0.1 microfarad ceramic capacitor is located at various places on the board, serving to bypass transients and helping to keep the plus 5 volt supply steady.

2. A negative 16 volt supply is assumed on S-100 bus pin 52. This supply is routed to voltage regulators VR1 and VR2, where it is regulated to the minus 12 volts and minus 5 volts required by the chips on the board. A

1.5 microfarad tantalum capacitor is located on both sides of both regulators, which serve to keep the voltage supply steady.

3. A positive 16 volt supply is assumed on S-100 bus pin 2. This supply is routed to VR3 where it is regulated to the plus 12 volts required by the chips on the board. In common with VR4, a 1.5 microfarad tantalum cap is located on the input side of VR3, and a 0.1 microfarad cap is located on the output side.

4. Ground lines are assumed on pins 50 and 100 of the S-100 bus. The Big Z CPU does not implement the ground lines on pins 20, 53, and 70 specified by the IEEE S-100 standard.

System Clock

The system clock, referred to on-board the Big Z CPU as Phi2, is generated by the Big Z oscillator section and is output to the S-100 bus on pin 24 through buffer U29.

Phi1 is also generated by the Big Z oscillator section and is output to the S-100 bus on pin 25 through buffer U29. **CAUTION:** Phi1 conflicts with the IEEE pSTVAL* signal line. In an IEEE system, this line must be cut. It is provided as a service to those cards that may require it. If no cards in your system require the Phi1 clock line, we suggest that this line should be cut.

The primary system clock is the Phi2 clock, which provides the control timing for all bus cycles.

CLOCK is derived from the Big Z oscillator section and is routed to the S-100 bus on pin 49, through buffer U29. It is a 2 MHz signal, regardless of the optional switch settings which select an internal 2 or 4 MHz clock. IEEE specifies a 2 MHz clock signal on this pin.

System Reset Functions

*RESET**. When RESET*, coming into the Big Z CPU from S-100 bus pin 75, goes low (true), U11 provides a RESET* signal to the Z80 CPU, and to the Power-On Latch. This signal is also provided to the S-100 bus as POC* (Power-On Clear*) on S-100 pin 99. RESET* and POC* are held low for approximately 470 milliseconds due to the time it takes to recharge C22, a 100 microfarad electrolytic capacitor, through R3, a 4.7K ohm resistor. This meets the IEEE specification of a minimum active period of 10 milliseconds for POC*

Memory Write Strobe

MWRT is provided to the S-100 bus on pin 68 via buffer U6. It is derived from the Z80 signals MRQ* and WR* true (active low on pins 19 and 22 of the Z80 chip), ANDed together by AND gate U17. When WR* and MRQ* on the Z80 are true, both inputs to AND gate U7 will be high, since the Z80 signals are inverted by inverter U18.

The generation of MWRT is inhibited when a front panel is connected to the system, and the front panel is allowed to generate its own MWRT signal.

Special Caution

*SSWDSB** is provided to the Big Z CPU on S-100 bus pin 53. This signal is used as a sense-switch disable line on Imsai and other front panels. It is in direct conflict with IEEE S-100 standards, which define pin 53 as a ground line. If the Big Z CPU card is to be used with an IEEE S-100 system, or in an IEEE-standard motherboard, such as the JADE ISO-BUS, this line must be cut between pin 12 of NAND gate U22 and pin 53 of the S-100 bus. Since it is held normally high by the pullup resistor in resistor pack U31, cutting this line will not affect the normal operation of the CPU—it will merely allow it to run.

This concludes the Technical Description of the Big Z/S-100 interface. The following sections are a Technical Description of the EPROM interface, the USART interface, and the Oscillator sections of the board.

EPROM INTERFACE

The EPROM interface circuitry is comprised of DM8131 comparator U34, switch module U33, NAND gates U10, U22, and U4, inverter U15, and AND gate U7.

The comparator at U34 monitors the state of address lines A10 through A15 (depending on which EPROM you have selected) on the internal address bus. It compares the state of these lines to the settings of switch module U33. If a particular switch (1 through 7) of U33 is closed, the switch-side inputs to comparator U34 are grounded (low). If the switches are open, the switch-side inputs to comparator U34 are pulled high by pullup resistors in resistor pack U32.

When a state of equality exists between the switch settings and the current state of A10 through A15, the equal compare output at pin 9 of U34 will go low. This signal is always inverted by inverter U15; therefore, when the comparator finds equality, the output of U15 will be high. Conversely, when there is inequality, the output of U15 will be low.

The output of U15 is applied to input pin 9 of NAND gate U22, where it is NANDed with the output of AND gate U41, pin 6, defined as MEMRD (memory read). When equality is true (high at this point) and MEMRD is true, the output of NAND gate U22, pin 8, will be low; but if either MEMRD or equality is false (low), the output of U22 will be high.

NAND gates comprising two sections of U10 are connected as a flipflop whose SET input is at pin 13, and whose RESET input is at pin 9. This cross-connected set of NAND gates is referred to as the Power-On Jump/Reset Latch (hereafter referred to as the POJ Latch).

The RESET* signal, connected to RESET* pin 26 of the Z80 CPU, is connected to the SET input of the POJ latch through switch 8 of switch module U23. When this switch is closed, a negative pulse from the RESET* line will set the latch. The SET input of the POJ latch is held normally high by a pullup resistor in resistor pack U28.

Consider a power-on sequence: the state of comparator U34 may be indeterminate, but we know that RESET* will be low (true); therefore, a low pulse will be applied to pin 13 of U10. This results in a high output which is routed to pin 10, forcing pin 8 to go low. Now we have two lows on the inputs of 13 and 12 at U10, so the output on pin 11 will definitely be high. This circles around, like a dog chasing its own tail, reinforcing its own state and tending to keep the flipflop set. This high output is also applied to NAND gate U22 via input pin 5.

Since the first instruction the Z80 will execute is a memory read, MEMRD will also soon go high. This forces the output of NAND gate U22, pin 6, low. This low is applied to AND gate U7, which results in a low being output on pin 6, and the EPROM is selected (EPS* becomes true). Now the Z80 will begin reading its instructions from the EPROM. This state of affairs will continue until the EPROM jumps outside its own range.

EPS* can only be generated by one of the following conditions: The POJ latch is set, or there is a state of equality on the comparator and MEMRD is true. The first condition is met during reset; the second condition is met when we are doing memory reads in the address range selected by the switches on U33.

EPS* is applied to pin 4 of NAND gate U4. If EPS* is true (low), the output of U4 at pin 6 must be high; therefore, the data in buffers are disabled, and we can only read from the EPROM.

By the same token, if we are *not* reading from the EPROM, EPS* will be false (high). If we are reading from the USART, DCS* will be true (low), and again the output of U4 will go high, disabling the data in buffers. If EPS* is false (high), and DCS* is also false (high), there is yet another condition that can tri-state the data in buffers: SSWDSB* is true (low) at pin 53 of the S-100 bus (remember, we told you to cut it when the Big Z was used in a system where pin 53 is always grounded), or either RUN or SS is low (false) at pins 71 and 21 of the S-100 bus.

How does the EPROM get selected in the Shadow Mode? Simple. The address switches on U33 don't necessarily have anything to do with it. When the CPU is reset, the RESET* line at pin 13 of U10 will go low, forcing the output high and setting the POJ latch. The first instruction executed by the Z80 will be a read (op code fetch), so pin 4 of U22 goes high along with pin 5 (the SET condition of flipflop U10). This outputs a low to pin 5 of U7. The other side of this AND gate is held high by the pullup resistor R14, and since the J-K link is cut, it must remain high, irrespective of the state of the output of U22 pin 8, because there is nothing to pull it low. Therefore, a lot on pin 5 of U7 ANDed with a high on pin four must result in a low being output from pin 6, which is—you guessed it—the EPS* signal. Since the address bus of the Z80 will be at zero, and we no longer care about the state of A10-A15, the Z80 must begin executing instructions from the EPROM.

Now, when MEMRD is true and we have an equality from the comparator, the POJ latch is reset and the EPROM is deselected, never to be heard from again and vanishing into thin air like a Hindu fakir. Why? Because the only thing that will *set* the POJ latch again is another reset or power-on condition. *Voila!* We are Shadowed.

Note that the Z80 can do memory *writes* to anywhere in memory, and all I/O operations, and even reads from memory as long as the address range from which it is reading is different from that selected by the switches of U33.

This circuitry is subtle, and not immediately apparent—but trust us, it works. A little pencil-and-paper doodling with logic equations will prove it to even the most stubborn doubter.

USART INTERFACE

The USART interface circuitry is comprised of comparator U24, switch module U23, pullup resistor pack U32, the baud rate generator and its associated crystal, OR gate U14, inverter U15, NOR gate U8, the USART itself (an 8251), and the RS232 level shifters at U12 and U9.

The lower portion of the internal address bus is monitored by the comparator U24 on lines A2-A7. The current state of the address bus is compared to the switch settings on U23 switches 1 through 6. As with the EPROM select circuitry, the switch-side inputs to the comparator can be either low or high—high if the switch is open by courtesy of resistor pack U32, or low by virtue of the fact that when a switch is closed it is grounded.

When equality is found, pin 9 of the comparator will go low. This signal is applied to pin 9 of OR gate U14, where it is ORed with the output of OR gate U14, pin 11. U14's section whose output is on pin 11 ORs A1 with IORQ*. DCS* is generated by an IORQ* true (low) or A1 low, ORed with equality from comparator U24. The output of U14 pin 8 is also applied to U4 pin 5 as DCS* to disable the data in buffers.

Tx and Rx clocks are provided to the USART via the MC14411 baud rate generator, whose internal timing is determined by Y2 crystal. A 16-times maximum baud rate (9600 baud or 153.6 KHz) is provided by NOR gate U8. One input, pin 8, is grounded; the other is routed in from the baud rate generator U2 pin 18.

The Tx data output from the 8251 USART is sent to pin 2 of U12, an MC1488 RS232 level shifter, where it is output from pin 3 as a level that swings between plus and minus 12 volts.

Similarly, the Rx data input to the USART is sent from RS232 level shifter U9 to pin 3 of the USART, as is the Reverse Channel signal. Reverse Channel can be used as a "busy" or "not ready" indicator.

RxD, TxD and RVC are available at the front panel and USART connector U19 at pins 16, 12, and 14 respectively.

CAUTION: If you are using a front panel board connected to U19, make *sure* that it does not make contact with the USART side (pins 9-16). Failure to observe this caution can result in damaged front panel boards and damaged RS232 level shifters. Watch those Imsai front panels!

OSCILLATOR SECTION

The oscillator section of the Big Z CPU consists of the following components:

A. Main Oscillator Circuit

This consists of crystal Y1, a 4 MHz crystal; inverter U21 (2 sections), capacitors C23, 26 and 27 (0.001 microfarad caps); R10 and R11; and section 1 of U11, a 7474 flipflop. Pin 4 of U21 produces a 4 MHz square wave as the result of the action of the crystal, capacitors, resistors and inverters in the circuit. Flipflop U11 is connected as a divide-by-two circuit. Its Q output, on pin 5, is presented to pin 4 of buffer U29, where is is buffered out to pin 49 of the S-100 bus as CLOCK*. Its Q* output, on pin 6, reaches around to its D input, forming the divide-by-two, and is also presented to switch S1 as a 2 MHz signal.

Switch 1 chooses between the 4 MHz signal available from pin 4 of U21, or the 2 MHz signal available as the Q* of U11.

B. Secondary Oscillator Circuit

This circuit consists of switch 1, and sections of inverters U15, U21, and U30. The center point of the single-pole double-throw switch S1 receives either a 2 MHz square wave or a 4 MHz square wave, depending on its position. This is fed through inverter U21 (pins 5 and 6) to the Z80 Phi clock input on the CPU pin 6. It is also fed to input pin 13 of inverter U30, exits via pin 12, and is applied to input pin 2 of buffer U29. It passes through buffer U29 which is always enabled by virtue of the fact that its tri-state inputs are grounded, exits at pin 3, and is transmitted to the S-100 bus, pin 24, as the Phi2 clock.

The center point of switch S1 is additionally fed to pin 9 of inverter U21, where it is delayed by the gate-time of U21, exits via pin 8, and is routed to input pin 13 of inverter U30 through an RC network consisting of C25, a 100 picofarad capacitor, and R12, a 6.8K ohm resistor. This RC network delays the signal by approximately 680 nanoseconds. At inverter U30, the signal is again slightly delayed by the inverter's gate time, exits on pin 10, and is routed to input pin 10 of buffer U29. It passes through the buffer, exits via pin 9, and is transmitted to the S-100 bus on pin 25 as Phi1 clock.

CAUTION:
Phi1 clock is provided as a convenience only, and is in direct conflict with the IEEE specification of pin 25 as pSTAVAL*. On IEEE S-100 systems, this clock should be eliminated by cutting the trace between U29 pin 9 and S-100 bus pin 25.

For those cards or systems that require the Phi1 clock signal, this circuitry provides a very good approximation of the actions of an 8080-style 8224 clock driver.

This concludes the Technical Description of the Big Z CPU.

THE BIG Z OPTIONS

OPTION 1—ON-BOARD EPROM

You should have installed the following components: an 8-position switch module at U33, a 24-pin socket at U13, a 16-pin socket at U34, and an 8131 IC at U34.

For a 2708-type EPROM

1. Set switch 7 on U33 to OFF.
2. Set switch 8 on U33 to ON.
3. Select EPROM address from Table A-1 and set the switches on U33 accordingly.

For a TMS 2716-type (TI three-voltage EPROM):

1. Install a jumper from A to C.
2. Install a jumper from D to B.
3. Cut the etch from B to C.
4. Set switches 1 and 7 on U33 to ON.
5. Set switch 8 on U33 to OFF.
6. Select EPROM address from Table A-2 and set the switches on U33 accordingly.

For an Intel-type 2716 (single plus 5 volt only)

1. Cut the etch from L to E.
2. Cut the etch from F to M.
3. Install a jumper from D to M.
4. Install a jumper from C to B.
5. Install a jumper from I to A.
6. Install a jumper from plus 5 volts to E.
7. Set switches 1 and 7 on U33 to ON.
8. Set switch 8 on U33 to ~~ON~~. OFF
9. Select EPROM address from Table A-2 and set the switches on U33 accordingly.

For an Intel 2732/TMS 2732 (4K) EPROM:

1. Cut the etch from L to E.
2. Cut the etch from F to M.
3. Cut the etch from G to H.
4. Install a jumper from D to M.
5. Install a jumper from G to B.
5. Install a jumper from C to B.
6. Install a jumper from G to E.
7. Install a jumper from H to I.
8. Set switch 1, 2 and 7 on U33 to ON.
9. Set switch 8 of U33 to OFF.
10. Select EPROM address from Table A-3 and set the switches on U33 accordingly.

OPTION 2—M1 WAIT STATE

1. Set switch 7 of U23 to OFF.
2. Install a jumper from R to F.
3. Change USART option to Option 7.

OPTION 3—1K x 8 Masked ROM (VECTOR GRAPHIC MONITOR)

1. Install a jumper from I to A.
2. Set switch 1 on U33 to OFF.
3. Set switch 8 on U33 to ON.
4. Select EPROM address from Table A-1 and set switches on U33 accordingly.

OPTION 4—NO EPROM AND NO POWER-ON JUMP

1. Set switch 7 and 8 on U23 to OFF.

OPTION 5— POWER-ON JUMP

1. Set switch 8 on U23 to ON .

NOTE: an EPROM *must* be on the board to use the Power-On Jump Option. The Big Z CPU will not perform an off-board Power-On Jump.

OPTION 6—EPROM WAIT STATE (4MHz)

1. Set switch 7 on U23 to ON.

NOTE: An EPROM *must* be on the board to use this option.

OPTION 7—USART OPTION

You should have installed the following components: an 8-position switch module at U23, a 22 megohm resistor at R6, a 1.8432 MHz crystal at Y2, a 24-pin socket at U2, a 28-pin socket at U3, a 16-pin socket at U24, an 8131 IC at U24, an 8251 IC at U3, a MC14411 IC at U2, an MC1488/75188 IC at U12, a MC1489/75189 IC at U9, the plus and minus 12 volt regulators at VR3 and VR2 respectively, and an 8-position switch module at U1.

1. Set ONE switch on U1 to the desired baud rate. Note that only ONE switch may be on at any given time. The baud rate is silk-screened next to U1 on the board. All switches other than the one selected must be set OFF.
2. Select the desired I/O port address from Table A-4 and set the switches on U23 accordingly.

OPTION 8—SHADOW EPROM

1. Cut the etch from J to K.
2. Install EPROM as shown in Option 1.
3. Enable the Power-On Jump as shown in Option 5.

This option is normally used to perform a system boot function. When the system is powered up or reset is activated, the power-on/reset latch formed by U10 is on and the processor will run code from the EPROM. The processor will continue running from the EPROM until a jump occurs to the address range selected by the switches on U33. Note that the program in the EPROM should be assembled to run in an address range OTHER than the one which is selected by the switch positions on U33.

When the jump to the selected U33 address range is detected, the EPROM will no longer be accessed, and will be transparent to the system. The program in the EPROM may be assembled to run in any address range as long as that address range is different from the range selected by the switches on U33. The EPROM is accessed for all memory read operations until a memory read is detected that generates an address in the range selected by the switches on U33. At this time, normal memory reads may take place because the power-on/reset latch will be cleared, and normal addressing is restored. I/O instructions and memory writes will execute normally while the power-on/reset latch is set, but all memory reads will address the EPROM.

*OPTION 9—MRQ**

Please note that the Memory Request Strobe MREQ, as supplied to the S-100 bus by the Big Z CPU card is a *positive true* signal. This does not conform with many memory card requirements. If your memory cards require an MRQ* signal, you can invert MRQ by using one of the spare gates on the board. To do this, tie pins 9 and 10 of U4 high by installing a jumper between these pins and pin 14 (5 volts) of U4. Cut the etch that runs between pin 11 of U17 and pin 65 of the S-100 bus. Install a jumper from pin 11 of U17 to pin 11 of U4. Install a jumper from the output of U4, pin 8, to S-100 bus pin 65. This will give you an inverted MRQ signal. Although the timing of this signal will be slightly delayed, the delay is negligible and should meet the requirements of most any memory board.

BOARD ASSEMBLY INSTRUCTIONS

The **JADE BIG Z** CPU board is intended for those people who have had some prior experience with kit building and digital electronics. If you do not fall into this category, it is highly recommended that you find an experienced person to help you with the assembly and checkout of the board.

Although there is nothing sacred in the suggested steps that follow, if you will follow them step-by-step you should find your task much easier. We suggest that you start at a time when you will be able to complete the board. It will help to mark the boxes as you complete each step.

☐ 1. Make sure you have the tools you will need to asemble this kit. For this board you will need the following: a soldering iron (20 watts maximum), *Rosin Core* solder (preferably 63/37), diagonal cutters, a small magnifying glass, a screwdriver, and a lead former or a pair of needle-nose pliers.

☐ 2. Check the parts received against the parts list. Take special care to correctly identify look-alike parts; i.e., resistors, capacitors and diodes. If anything is missing from your kit, please call **JADE's** Customer Service Department and report the shortage immediately.

☐ 3. Read the section of this manual titled "Construction and Soldering Tips." If you have trouble identifying any of the parts, the section titled "Parts Identification" should help you. Do this *now* before you proceed any further.

CAUTION

USE EYE PROTECTION WHILE SOLDERING OR CUTTING WIRE

☐ 4. Install 14-pin sockets at U4, U5, U7, U8, U9, U10, U11, U12, U14, U15, U18, U20, U21, U22, U30, and U41. Do *not* solder them in yet.

☐ 5. Install 16-pin sockets at U6, U17, U24, U25, U26, U27, U28, U29, U31, U32, U34, U35, U36, U37, U38, U39, and U40. Do *not* solder them in yet.

☐ 6. Install 24-pin sockets at U2 and U13. Do *not* solder them in yet.

☐ 7. Install 28-pin socket at U3. Do *not* solder it in yet.

☐ 8. Install 40-pin socket at U16. Do *not* solder it in yet.

☐ 9. A handy trick to help you construct your board is to insert all the above sockets into the board first, then place the flat styrofoam cover you received with your kit box firmly against the top of the board. Turn it over, holding the flat styrofoam piece tightly against the board. The IC sockets should not be on the bottom. Press the board down, forcing the sockets into the styrofoam. Now solder alternating corner pins of the IC sockets to hold them in place temporarily (pins 8 and 16 on a 16-pin socket, for instance.)

Now turn the board over and very carefully inspect it to determine that all the IC sockets are down flat against the board. If you find any that aren't down flat, melt the solder joints at the corners of the IC socket and press it down against the board.

When you have determined that all the IC sockets are down firmly on the board, turn the board back over and solder all the pins. Make sure that all the pins are sticking through the board. IC sockets are very difficult to remove once they are soldered onto a board. For soldering hints, turn to Appendix B of this manual.

☐ 10. Install 1.5 ufd capacitors at C16 through C21. (NOTE that there are *two* C17s on the board. This is to allow you a choice between using dip tantalum caps and radial electrolytics. Dip tantalums are much preferable and are the type shipped with the Big Z kits as supplied by **JADE**. Install C17 according to the type of capacitor you are using.)

☐ 11. Install 0.1 ufd capacitors at C1 through C15.

☐ 12. Install the three DIP switches at U1, U23, and U33. Do not place these DIP switches in sockets— they are liable to fall out under use.

☐ 13. Install a 100 microfarad electrolytic capacitor at C22.

☐ 14. Install a 100 picofarad capacitor at C24 and C25.

☐ 15. Install a 0.001 ufd capacitor at C23, C26, and C27.

☐ 16. Install a 330 ohm resistor (orange, orange, brown) at R5.

☐ 17. Install the 1K ohm resistors (brown, black, red) at R4, R10, and R11.

☐ 18. Install a 2.7K ohm resistor (red, violet, red) at R2.

☐ 19. Install the 4.7K ohm resistors (yellow, violet, red) at R1, R3, R7, R8, R9, R13 and R14.

☐ 20. Install the 6.8K ohm resistors (blue, gray, red), at R12.

☐ 21. Install the 22 megohm resistor (red, red, blue) at R6.

☐ 22. Install a 4 MHz crystal at Y1.

☐ 23. Install a 1.8432 MHz crystal at Y2.

☐ 24. Install the voltage regulators. The 7805/LM340T5 regulator is installed at VR4. This is the plus 5 volt regulator and should be used with a heat sink. If you have a good heat sink compound, we suggest you use it at this regulator only. Use it sparingly, as too much is worse than none at all. Now install the 7912/LM320T12 regulator (minus 12 volts) at VR2. Install the 7905/LM320T5 (minus 5 volts) regulator at VR1. Install the 7812/LM340T12 (plus 12 volts) regulator at VR3. Button them down with the screws and nuts supplied. Place the screw through the solder side of the board, with the nut next to the regulator.

☐ 25. Check all your solder joints carefully. Inspect the board for cold solder joints or solder bridges, as per the instructions in Appendix B.

☐ 26. **BEFORE INSTALLING ANY ICs**—place the board in your computer and check all the voltages to make sure that you do not have any power supply shorts on the board. The output voltages from all the regulators can be measured on the pin facing toward the top of the board (away from the S-100 connector). Be careful not to let your probes short the voltage regulator pins together, since this can destroy a voltage regulator very neatly—and quickly. If all of the voltages are up to par (plus or minus about half a volt or so), continue to step 27; otherwise, check the board again for shorts. Find that short before you install any ICs, and correct it.

☐ 27. Install all ICs and resistor packs in the locations shown on the Assembly Drawing.

☐ 28. Install whatever options you have chosen from the Options list.

☐ 29. Install a single-pole double-throw switch at T-U-V. If a switch has not been included in your kit, solder in the wire-wrap pins in its place. The center to top hole (T to U) selects a 2 MHz clock. The center to bottom hole (U to V) selects a 4 MHz clock. Regardless of the switch setting, the CLOCK* signal on pin 49 of the S-100 bus will be 2 MHz, as per IEEE specifications.

☐ 30. You should now be on the air. If you have trouble, go to the "Troubleshooting Tips" section of this manual for checkout procedures. If you don't—happy computing!

CHECKOUT PROCEDURES AND TROUBLESHOOTING TIPS

Before plugging the board into the sytem, do the following:

1. Carefully inspect the board for solder shorts or damaged components.

2. Insure that all ICs are out of their sockets at this point.

3. Install all options that are to be used in your system. Be especially careful when installing EPROM options, because your EPROM may be permanently damaged by improper jumper configurations. Five-volt-only EPROMS can be destroyed by the minus 5 and plus 12 volts supplied to the EPROM socket if the etches are not properly cut. Ohm them out before installing the EPROM, or check the voltages at the proper socket pins.

Some confusion can exist for parts labeled 2716. Texas Instrument parts use plus 12 and minus five volts, while others (such as Intel), are five-volt-only types. The Texas Instrument TMS2516 is a five-volt-only part that is identical to the Intel 2716.

4. Plug the processor board into the bus with power OFF, being careful to line up pins 50 and 100 with the ground pins on the bus. If the board should somehow inadvertently become reversed in the S-100 connector, extensive damage could result when power is applied. In most mainframes, it is physically impossible to insert the card backwards—but some

people have managed to do it. It never hurts to make sure, and we'd rather insult your intelligence by telling you about it than see you destroy your CPU card.

5. It is highly recommended that the plus five volt supply be monitored while applying power for the first time. Shut the system down *immediately* if the supply does not read five volts (plus or minus something really reasonable). Monitor the other voltages as well before attempting to run the processor in the system.

6. Next, install all the ICs in their sockets according to the parts list or the assembly drawing. Make certain that pin one of all ICs are down, facing the S-100 bus connector on the board. There is no exception to this rule—*all* ICs face the bottom of the board. If you are not sure where pin 1 is on an IC, refer to the parts identification section of this manual.

7. Carefully turn the power on. Check for any discoloration in the parts and touch each IC gingerly. If it is *very* hot, chances are that you have inserted it backwards. Remove it, throw it away, and install a new part. The old one might work, but it is bound to fail in the near future, and according to Murphy's Law, which states that darn near anything can happen bad, it will fail exactly when you are most depending on it, like in a 14-hour sort or something. (Editor's Note: JADE's corollary to Murphy's Law states that "Murphy was an *optimist!*")

If you have a front panel, single-step the board to see if the first few instructions are fetched properly. In case of problems, carefully check all options installations and switch settings, since this is the most common cause of difficulty with this board.

Please note that not all front panel boards will work with the **Big Z** CPU card. Since the Big Z was designed to conform as much as possible with the proposed IEEE S-100 standard, it does not provide mirrored I/O addressing. Mirrored I/O addressing is an old Imsai/80890 convention in which the I/O address is mirrored (carried by both the upper and lower halves of the address bus). With the advent of the Z80 CPU, it became possible to perform block I/O instructions. The Z80 uses the upper half of the address bus to provide a byte count to its peripherals during these block move I/O instructions, and the use of mirrored I/O addressing effectively precludes this entire class of very useful instruction from the Z80's reportoire.

Some board designers (heaven only knows why) decode the upper half of the address bus for an I/O address. Why? We've never been able to figure it out. Among these that we know about are the Vector Graphic Flashwriters and I/O cards, Imsai front panel boards, Imsai I/O boards, the MECA tape system, Computime clock and calculator boards, and others.

Although the IEEE does not specifically forbid this practice, it is strongly discouraged. The designers of the Big Z CPU have elected not to implement mirrored I/O addressing. If you have cards which use this addressing scheme, we suggest that they be modified **to decode the *lower* half of the address bus (A0-A7) rather than the upper half.**

One of the most common problems we have encountered with our customers using the Big Z is caused by the EPROM not being properly accessed after a power-on or reset. If the EPROM you are using has a paper label over the window, do not assume that it is a 2708 or other EPROM. Carefully lift the label to see if a transparent window is present on the device. If no window is present, it is a masked ROM or PROM. ROMs and PROMs that have pinouts similar to the 2708 or 2716 will work on the Big Z provided that you insure that pins 18, 19, 20 and 21 of the device are supplied with the same voltages as in the circuit in which they were originally used.

Instructions are included in the Options section for interfacing a Vector Graphics Monitor ROM. Note that the ROM, PROM or EPROM that is the starting point of the system monitor or bootstrap loader must be located on the Big Z CPU board in order to use the power-on jump feature. Devices that form the remainder of the system monitor may reside on other boards in the system, but the starting point of the monitor *must* by on the processor board.

Tarbell disk controllers that use an on-board cold-start loader ROM will not work with the Big Z. JADE has available several monitor ROMs that include the Tarbell disk interface cold-start loader routines. The on-board ROM on the Tarbell controller must be disabled.

To continue the checkout procedure:

8. If the voltages you have monitored during steps 5 and 7 have not been up to par, either the regulators are defective (most unlikely), or a short circuit exists somewhere on the board. Power down and check for solder bridges.

9. Check Z80 pin 6 for a 2 or 4 MHz square wave. If this is not present, you have trouble in the Oscillator section of the board. Check the ICs. Check the capacitors and resistors for proper values. Check for solder bridges or shorts.

10. Halt the CPU. Hold the reset button down and look at the following pins of the Z80 with a voltmeter or preferably a logic probe or oscilloscope:

pin 26 (RESET*) should be LOW.
pins 1-5 and 30-40 (A0-A15) should be HIGH.
pins 7-10 and 12-15 (D0-D7) should be HIGH.

Now release the RESET button. Look at the following pins on the Z80:

pin 26 (RESET*) should be HIGH.
pin 25 (BUSRQ*) should be HIGH.

pin 24 (WAIT*) should be LOW.
pin 18 (HLTA*) should be HIGH.
pin 27 (M1*) should be LOW.
pin 16 (INT*) should be HIGH.
pin 17 (NMI*) should be HIGH.
pin 23 (BUSAK*) should be HIGH.
A0-A15 should be LOW.

11. Install a monitor EPROM. Hit reset. Examine pin 9 of comparator U34. You should see a low-going pulse as the EPROM is selected. If pin 9 remains high, you have probably addressed your switches incorrectly. Check them out against the proper settings on the applicable Table A section for your type of EPROM. If pin 9 remains low, either there is something wrong with the address lines of the internal address bus, or the comparator is defective, or U10 is defective. Make sure you have the pullup resistor packs and pullup resistors properly installed.

12. With an EPROM installed, check pin 9 of comparator U24 to determine if the USART is being addressed correctly. Follow the same logic as in step 11 above.

13. Check your monitor program against the sample monitor program included with this manual. You may have a software problem. The most common software problem we have encountered centers around incorrect initialization of the 8251 USART.

PROGRAMMING THE USART

A simple program that uses the USART as output is included with this manual. Note that the RS232C interface from the USART is contained on the same DIP connector as the front panel signals. When connecting a front panel, be careful to insure that the RS232 levels do not go to any circuitry on the front panel through the DIP connector cable. This could render the USART unusable, as well as damage components on the front panel board. The DIP cable will have to be split at the DIP connector if a front panel is used in conjunction with the RS232 interface. A cable from pins 1 through 8 will go to the front panel. A cable from pins 9 through 16 will go to the RS232 connector or plug.

The USART appears as two consecutive port I/O addresses to the processor. U24 decodes a group of four consecutive addresses and the two lower addresses of this group of four are enabled by A1 going low at pin 12 of U14. The upper two addresses may be enabled to talk to the USART by cutting the etch on the solder side of the board at U14, pin 12.

An ODD address (i.e., A0 is 1 or high) selects the USART command/status register and an EVEN address (i.e., A0 is 0 or low) selects the USART data register. After a power-on or reset, the USART must be programmed (initialized) for use by outputting a mode word, followed by a command word. The format for the mode word is as follows:

Bit 0 0
Bit 1 1
Bits 2 & 3:
00 means 5 bits per character.
10 means 6 bits per character.
01 means 7 bits per character.
11 means 8 bits per character (most usual configuration)
Bit 4—0 means parity disabled, 1 means parity enabled.
Bit 5—0 means odd parity selected, 1 means even parity selected.
Bits 6 & 7:
00 is an invalid, illegal combination.
01 means one and one-half stop bits.
10 means one stop bit (most usual configuration).
11 means 2 stop bits (usually used at 300 baud or less).

After writing the mode word, a slight delay is needed before writing the command word. This word can be sent to the USART after a LD A instruction, which will provide the necessary delay, and is required anyway. The command word is written to control the transmit or receive function of the USART. The functional format for the command word is as follows:

Initiate Transmit is 33 hex.
Initiate Receive is 36 hex.
Reset is 40 hex (same as a power-on condition).
Initiate both transmit and receive is 37 hex.

The mode and command words are only written *once* after a power-on or reset is performed. The command word may be written each time the function is to change or be selected. Note that this is not necessary when the command word sent to the USART is 37 hex—both transmit and receive are enabled.

The status register of the USART is obtained from inputting the command register. The format of the status register is as follows:

Bit 0. When this bit is high, it means that the Transmitter Buffer is empty and the USART is ready for another data character. This bit is reset by outputting a character to the USART's data register.

Bit 1. When this bit is high it means that a character has been received and assembled by the USART (data is available). This bit is reset when the character is input from the data register of the USART.

Bit 2. When this bit is high, it means that the transmitter is enabled and the USART is in its Transmit Mode.

Bit 3. When this bit is high, it means that the USART has detected a parity error in the character it has just received, or transmitted.

Bit 4. When this bit is high, it signals an Overrun Error. This means that the received data was not input from the USART by the CPU soon enough to allow the USART to properly receive and assemble the next character.

Bit 5. When this bit is high, it signifies a Framing Error. A framing error means that an improper stop bit was detected at the end of the character. This condition can be caused by transmitting the wrong number of data bits or by the wrong baud rate being selected.

Bit 6 is not used, and its condition is meaningless.

Bit 7. When this bit is high, it means Reverse Channel. This is used for a "buffer full" or "not ready" indication from peripheral devices. It can be active high or low, depending on the device. A TTL-level signal may be used at the RS232 interface is an RS232 signal is not available.

The following software example sets the mode word to select 8 bits per character, no parity, and 1 stop bit. The system should have been powered-on or reset just prior to executing this program. The command word that is output next selects the transmit and receive mode. The status is read and bit 0 is tested to see if the USART is ready for a character. If this bit is high, then a 55 hex (ASCII "U") is output as a character. The program then loops, testing the status, and transmits a continuous string of "U's". If the transmit data is viewed with an oscilloscope, it appears as a square wave with the low or high portions equal to the bit time or baud rate. The reciprocal of the baud rate will give the bit time in seconds. For example, 1/600 baud equals 1.667 milliseconds (0.001667 seconds).

```
                         'USART SOFTWARE EXAMPLE'
ADDR   CODE        STMT SOURCE STATEMENT

                   0002 ;
                   0003          PSECT     ABS
>0100              0004          ORG       0100H
                   0005 ;
                   0006 ;        define symbols used
                   0007 ;
>0011              0008 SSTAT    EQU       11H
>0010              0009 SDATA    EQU       10H
>0001              0010 TXRDY    EQU       01H
                   0011 ;
                   0012 ;
0100   3E4E        0013 PGM:     LD        A,4EH    ;mode word
0102   D311        0014          OUT       (SSTAT),A
                   0015 ;out to USART command port
0104   3E37        0016          LD        A,37H    ;command word
                   0017 ;enables both transmit and receive
                   0018 ;modes
0106   D311        0019          OUT       (SSTAT),A
>0108              0020 LOOP:
0108   DB11        0021          IN        A,(SSTAT)
                   0022 ;input from USART status port
010A   E601        0023          AND       TXRDY
                   0024 ;test for transmitter buffer ready
010C   28FA        0025          JR        Z,LOOP-$         ;loop until it's empt
010E   3E55        0026          LD        A,55H    ;ASCII "U"
0110   D310        0027          OUT       (SDATA),A
                   0028 ;transmit the character
0112   18F4        0029          JR        LOOP-$   ;return and do it again
                   0030          END
```

EPROM TABLES

Table A-1
2704/2708 EPROM Address Select (U33)

Address Range	SW1 A15	SW2 A14	SW3 A13	SW4 A12	SW5 A11	SW6 A10
0000—03FFX	X	X	X	X	X	X
0400—07FFX	X	X	X	X	X	
0800—0BFFX	X	X	X	X		X
0C00—0FFFX	X	X	X	X		
1000—13FF	X	X	X		X	X
1400—17FF	X	X	X		X	
1800—1BFF	X	X	X			X
1C00—1FFF	X	X	X			
2000—23FF	X	X		X	X	X
2400—27FF	X	X		X	X	
2800—2BFF	X	X		X		X
2C00—2FFF	X	X		X		
3000—33FF	X	X			X	X
3400—37FF	X	X			X	
3800—3BFF	X	X				X
3C00—3FFF	X	X				
4000—43FF	X		X	X	X	X
4400—47FF	X		X	X	X	
4800—4BFF	X		X	X		X
4C00—4FFF	X		X	X		
5000—53FF	X		X		X	X
5400—57FF	X		X		X	
5800—5BFF	X		X			X
5C00—5FFF	X		X			
6000—63FF	X			X	X	X
6400—67FF	X			X	X	
6800—6BFF	X			X		X
6C00—6FFF	X			X		
7000—73FF	X				X	X
7400—77FF	X				X	
7800—7BFF	X					X
7C00—7FFF	X					
8000—83FF		X	X	X	X	X
8400—87FF		X	X	X	X	
8800—8BFF		X	X	X		X
8C00—8FFF		X	X	X		
9000—93FF		X	X		X	X
9400—97FF		X	X		X	
9800—9BFF		X	X			X
9C00—9FFF		X	X			
A000—A3FF		X		X	X	X
A400—A7FF		X		X	X	
A800—ABFF		X		X		X
AC00—AFFF		X		X		

Table A-1 (continued)
2704/2708 EPROM Address Select (U33)

Address Range	SW1 A15	SW2 A14	SW3 A13	SW4 A12	SW5 A11	SW6 A10
B000—B3FF		X			X	X
B400—B7FF		X			X	
B800—BBFF		X				X
BC00—BFFF		X				
C000—C3FF			X	X	X	X
C400—C7FF			X	X	X	
C800—CBFF			X	X		X
CC00—CFFF			X	X		
D000—D3FF			X		X	X
D400—D7FF			X		X	
D800—DBFF			X			X
DC00—DFFF			X			
E000—E3FF				X	X	X
E400—E7FF				X	X	
E800—EBFF				X		X
EC00—EFFF				X		
F000—F3FF					X	X
F400—F7FF					X	
F800—FBFF						X
FC00—FFFF						

Table A-2
2716/2516 EPROM Address Select (U33)

Address Range	SW1 A15	SW2 A14	SW3 A13	SW4 A12	SW5 A11
0000—07FF	X	X	X	X	X
0800—0FFF	X	X	X	X	
1000—17FF	X	X	X		X
1800—1FFF	X	X	X		
2000—27FF	X	X		X	X
2800—2FFF	X	X		X	
3000—37FF	X	X			X
3800—3FFF	X	X			
4000—47FF	X		X	X	X
4800—4FFF	X		X	X	
5000—57FF	X		X		X
5800—5FFF	X		X		
6000—67FF	X			X	X
6800—6FFF	X			X	
7000—77FF	X				X
7800—7FFF	X				
8000—87FF		X	X	X	X

Table A-2 (continued)

2716/2516 EPROM Address Select (U33)

Address Range	SW1 A15	SW2 A14	SW3 A13	SW4 A12	SW5 A11
8800—8FFF		X	X	X	
9000—97FF		X	X		X
9800—9FFF		X	X		
A000—A7FF		X		X	X
A800—AFFF		X		X	
B000—B7FF		X			X
B800—BFFF		X			
C000—C7FF			X	X	X
C800—CFFF			X	X	
D000—D7FF			X		X
D800—DFFF			X		
E000—E7FF				X	X
E800—EFFF				X	
F000—F7FF					X
F800—FFFF					

Table A-3

2732 EPROM Address Select (U33)

Address Range	SW1 A15	SW2 A14	SW3 A13	SW4 A12
0000—0FFF	X	X	X	X
1000—1FFF	X	X	X	
2000—2FFF	X	X		X
3000—3FFF	X	X		
4000—4FFF	X		X	X
5000—5FFF	X		X	
6000—6FFF	X			X
7000—7FFF	X			
8000—8FFF		X	X	X
9000—9FFF		X	X	
A000—AFFF		X		X
B000—BFFF		X		
C000—CFFF			X	X
D000—DFFF			X	
E000—EFFF				X
F000—FFFF				

Table A-4

USART Address Select (U23)

Address Range	SW1 A7	SW2 A6	SW3 A5	SW4 A4	SW5 A3	SW6 A2
00—01	X	X	X	X	X	X
04—05	X	X	X	X	X	
08—09	X	X	X	X		X
0C—0D	X	X	X	X		
10—11	X	X	X		X	X
14—15	X	X	X		X	
18—19	X	X	X			X
1C—1D	X	X	X			
20—21	X	X		X	X	X
24—25	X	X		X	X	
28—29	X	X		X		X
2C—2D	X	X		X		

Table A-4 (continued)

USART Address Select (U23)

Address Range	SW1 A7	SW2 A6	SW3 A5	SW4 A4	SW5 A3	SW6 A6
30—31	X	X			X	X
34—35	X	X			X	
38—39	X	X				X
3C—3D	X	X				
40—41	X		X	X	X	X
44—45	X		X	X	X	
48—49	X		X	X		X
4C—4D	X		X	X		
50—51	X		X		X	X
54—55	X		X		X	
58—59	X		X			X
5C—5D	X		X			
60—61	X			X	X	X
64—65	X			X	X	
68—69	X			X		X
6C—6D	X			X		
70—71	X				X	X
74—75	X				X	
78—79	X					X
7C—7D	X					
80—81		X	X	X	X	X
84—85		X	X	X	X	
88—89		X	X	X		X
8C—8D		X	X	X		
90—91		X	X		X	X
94—95		X	X		X	
98—99		X	X			X
9C—9D		X	X			
A0—A1		X		X	X	X
A4—A5		X		X	X	
A8—A9		X		X		X
AC—AD		X		X		
B0—B1		X			X	X
B4—B5		X			X	
B8—B9		X				X
BC—BD		X				
C0—C1			X	X	X	X
C4—C5			X	X	X	
C8—C9			X	X		X
CC—CD			X	X		
D0—D1			X		X	X
D4—D5			X		X	
D8—D9			X			X
DC—DD			X			
E0—E1				X	X	X
E4—E5				X	X	
E8—E9				X		X
EC—ED				X		
F0—F1					X	X
F4—F5					X	
F8—F9						X
FC—FD						

IEEE S-100 PINOUT
and
SIGNAL DEFINITIONS

The following S-100 pinout is as stated in the IEEE Preliminary Specifications, and is subject to revision.

1.	+8V	Average maximum must be less than 11 Volts.
2.	+16V	Average maximum must be less than 21.5 Volts.
3.	XRDY	Active high. One of two bus ready signals [see also pin 72].
4.	VI0*	Vectored Interrupt Line 0, active low, open collector.
5.	VI1*	[see pin 4 above for this and the following:]
6.	VI2*	
7.	VI3*	
8.	VI4*	
9.	VI5*	
10.	VI6*	
11.	VI7*	
12.	NMI*	Non-maskable Interrupt, active low, open collector.
13.	PWRFAIL*	Active low bus power failure signal.
14.	DMA3*	
15.	A18	Extended Address Bit 18
16.	A16	Extended Address Bit 16
17.	A17	Extended Address Bit 17
18.	SDSB*	Active low, open collector. Used to disable the 8 status signal lines.
19.	CDSB*	Active low, open collector. Used to disable the 5 control output signals.
20.	GND	Ground, common with pins 50 and 100. [Formerly defined as memory protect.]
21.	NDEF	Not defined. Throughout this definition of the S-100 pinout, NDEF may be used by a manufacturer, but any pin so used must be fully specified.
22.	ADSB*	Active low, open collector. Used to disable the 16 address lines.
23.	DODSB*	Active low, open collector. Used to disable the 8 data output lines.
24.	Phi Clk	Phase 1 clock which provides the master timing for the bus.
25.	pSTVAL*	Status valid strobe, active low. In conjunction with pSYNC, this signal indicates that stable

		address and status signals are present on the bus.
26.	pHLDA	Active high. Hold acknowledge signal.
27.	RFU	Reserved for future use.
28.	RFU	See above.
29.	A5	Address Bit 5
30.	A4	Address Bit 4
31.	A3	Address Bit 3
32.	A15	Address Bit 15
33.	A12	Address Bit 12
34.	A9	Address Bit 9
35.	DO1	Data Out Bit 1, bidirectional data bit 1
36.	DO0	Data Out Bit 0, bidirectional data bit 0
37.	A10	Address Bit 10
38.	DO4	Data Out Bit 4, bidirectional data bit 4
39.	DO5	Data Out Bit 5, bidirectional data bit 5
40.	DO6	Data Out Bit 6, bidirectional data bit 6
41.	DI2	Data In Bit 2, bidirectional data bit 10
42.	DI3	Data In Bit 3, bidirectional data bit 11
43.	DI7	Data In Bit 7, bidirectional data bit 15
44.	sM1	Status signal indicating that the current machine cycle is an op code fetch cycle.
45.	sOUT	Status signal indicating that the current machine cycle is an I/O output cycle.
46.	sINP	Status signal indicating that the current machine cycle is an I/O input cycle.
47.	sMEMR	Status signal indicating that the current machine cycle is a memory read cycle, and is not an INTA instruction fetch cycle.
48.	sHLTA	Status signal indicating that a HALT instruction is being executed.
49.	CLOCK	A 2 MHz [+/- 0.5%], 40-60% duty cycle clock which is not required to be synchronous with any other bus signal.
50.	GND	Common with pin 100.
51.	+8V	Common with pin 1.
52.	-16V	
53.	GND	Common with pin 100. [Formerly Sense Switch Disable*. All CPU cards used in the IEEE S-100 bus which have the SSWDSB* line connected must have this pin cut. The signal may be connected through the front panel connector cable.]
54.	SLAVE CLR*	This is a signal used to reset bus slaves. It must be active with POC* and may also be generated by external means.
55.	DMA0*	Active low, open collector DMA request line.
56.	DMA1*	See above.
57.	DMA2*	See above.
58.	sXTRQ*	An active low status signal which requests 16-bit bus slaves to assert SIXTN*
59.	A19	Extended Address Bit 19
60.	SIXTN*	An active low status signal asserted by 16-bit bus slaves in response to sXTRQ*.
61.	A20	Extended Address Bit 20.
62.	A21	Extended Address Bit 21.
63.	A22	Extended Address Bit 22.

64.	A23	Extended Address Bit 23.
65.	NDEF	Not defined.
66.	NDEF	Not defined.
67.	PHANTOM*	Active low, open collector.
68.	MWRT	pWR^sOUT*, follows pWR* within 30 ns.
69.	RFU	Reserved for future use.
70.	GND	Common with pin 100. [Formerly memory unprotect.]
71.	RFU	
72.	RDY	Active high, open collector [see comments for pin 3].
73.	INT*	Active low, open collector, principal interrupt request signal.
74.	HOLD*	Active low, open collector, used in conjunction with pHLDA to coordinate DMA operations.
75.	RESET*	Active low, open collector, master reset signal.
76.	pSYNC	Control signal identifying the beginning of a new bus cycle.
77.	pWR*	Active low control signal that identifies the presence of valid data on the DO bus.
78.	pDBIN	Control signal requesting data on the DI bus.
79.	A0	Address Bit 0.
80.	A1	Address Bit 1.
81.	A2	Address Bit 2.
82.	A6	Address Bit 6.
83.	A7	Address Bit 7.
84.	A8	Address Bit 8.
85.	A13	Address Bit 13.
86.	A14	Address Bit 14.
87.	A11	Address Bit 11.
88.	DO2	Data Out Bit 2, bidirectional data bit 2.
89.	DO3	Data Out Bit 3, bidirectional data bit 3.
90.	DO7	Data Out Bit 7, bidirectional data bit 7.
91.	DI4	Data In Bit 4, bidirectional data bit 12.
92.	DI5	Data In Bit 5, bidirectional data bit 13.
93.	DI6	Data In Bit 6, bidirectional data bit 14.
94.	DI1	Data In Bit 1, bidirectional data bit 9.
95.	DI0	Data In Bit 0, bidirectional data bit 8.
96.	sINTA	Status signal identifying a bus input cycle that follows an accepted interrupt request on INT*.
97.	sWO*	Active low status signal identifying a bus cycle which transfers data from a bus master to a bus slave.
98.	ERROR*	Active low, open collector status signal which identifies an error condition during the present bus cycle.
99.	POC*	Power-on clear signal for all bus devices. This signal, when asserted, must remain low for at least 10 milliseconds.
100.	GND	System ground line.

```
ADDR   CODE         STMT SOURCE STATEMENT

                         ;****************************************************************
                         ;****************************************************************
                         ;***       BIG Z MONITOR (1K VERSION 2.0)  9/10/79  AB
                         ;****************************************************************
                         ;          ASSUMPTIONS
                         ;          SERIAL PORT ON BIGZ IS SET TO 10 AND 11 HEX
                         ;          TARBELL TAPE USING STANDARD TARBELL PORTS
                         ;          OR KC STANDARD VIA JADE SERIAL/PARALLEL CARD
                         ;                  SET TO PORTS 01 & 81 HEX
                         ;          NO MEMORY SIZE IS ASSUMED
                         ;
                         ;CONDITIONAL ASSEMBLY PARAMETERS
                         ;          define values of true/false
>FFFF                    TRUE       EQU     0FFFFH
>0000                    FALSE      EQU     0
                         ;
                         ;          set conditional assembly values
>0000                    TARBEL EQU         FALSE
>FFFF                    KCTAPE     EQU     TRUE
                         ;
                         ;SYSTEM EQUATES
                         ;
                                    PSECT   ABS
>E000                    MON        ORG     0E000H
                         ;
>0000                    TAPE       EQU     0
>0080                    TAPST      EQU     80H
>0011                    KBDST      EQU     11H
>0010                    KBDDT      EQU     10H
>0002                    KBDIN      EQU     02H
>0001                    KBDOT      EQU     01H
>00FC                    WAIT       EQU     0FCH
>00FA                    SECT       EQU     0FAH
>00F8                    DCOM       EQU     0F8H
>00FB                    DDATA      EQU     0FBH
>00F8                    DSTAT      EQU     0F8H
>007D                    SBOOT      EQU     007DH
>006E                    TARBL      EQU     6EH
                         ;
                         ;
E000   C321E0                       JP      INIT
E003   C370E0                       JP      EXEC
E006   C390E3                       JP      CONIN
E009   C385E3                       JP      CONOUT
E00C   C325E3                       JP      HEXIN
E00F   C359E3                       JP      HEXOUT
E012   C354E3                       JP      DHXOT
E015   C370E3                       JP      CRLF
E018   C37DE3                       JP      SPACE
E01B   C32BE2                       JP      TREAD
E01E   C395E2                       JP      TWRIT
E021   0601                 INIT    LD      B,1
E023   3E4E                         LD      A,4EH
E025   D311                         OUT     (KBDST),A
E027   3E37                         LD      A,37H
E029   D311                         OUT     (KBDST),A
E02B   21FFFF                       LD      HL,0FFFFH
E02E   23                   FTOP:   INC     HL
```

```
      'BIG Z MONITOR 2.0.A/B'          SD SYSTEMS Z80 ASSEMBLER PAGE 0002
ADDR  CODE       STMT SOURCE STATEMENT

E02F  7E         0060           LD      A,(HL)
E030  2F         0061           CPL
E031  77         0062           LD      (HL),A
E032  BE         0063           CP      (HL)
E033  2F         0064           CPL
E034  77         0065           LD      (HL),A
E035  2004       0066           JR      NZ,FTOP1-$
E037  0600       0067           LD      B,0
E039  18F3       0068           JR      FTOP-$
E03B  78         0069 FTOP1:    LD      A,B
E03C  B7         0070           OR      A
E03D  20EF       0071           JR      NZ,FTOP-$
E03F  2B         0072           DEC     HL
E040  2B         0073           DEC     HL
E041  F9         0074           LD      SP,HL
E042  E5         0075           PUSH    HL
E043  FDE1       0076           POP     IY
                 0077 ;2 CR/LF's
E045  CD70E3     0078           CALL    CRLF
E048  CD70E3     0079           CALL    CRLF
E04B  2163E0     0080 FTOP2     LD      HL,MSG1
E04E  7E         0081 INIT1:    LD      A, (HL)
E04F  CD85E3     0082           CALL    CONOUT
E052  23         0083           INC     HL
E053  FE03       0084           CP      03H
E055  20F7       0085           JR      NZ,INIT1-$
E057  CD70E3     0086           CALL    CRLF
E05A  210100     0087           LD      HL,1
E05D  39         0088           ADD     HL,SP
E05E  CD54E3     0089           CALL    DHXOT
E061  182D       0090           JR      EXEC-$
                 0091           IF      TARBEL
                 0092 MSG1:     DEFM    'JADE COMPUTER SYSTEMS BIG Z MONITOR 2.0B'
                 0093           ENDIF
                 0094           IF      KCTAPE
E063  4A414445   0095 MSG1:     DEFM    'JADE COMPUTER SYSTEMS BIG Z MONITOR 2.0A'
      20434F4D
      50555445
      52205359
      5354454D
      53204249
      47205A20
      4D4F4E49
      544F5220
      322E4F41
                 0096           ENDIF
E08B  0D0A0D0A   0097           DEFB    0DH,0AH,0DH,0AH
E08F  03         0098           DEFB    03H
E090  FDF9       0099 EXEC:     LD      SP,IY
                 0100           IF      TARBEL
                 0101           SUB     A
                 0102           OUT     (TARBL),A
                 0103           ENDIF
E092  CD70E3     0104 EXEC3:    CALL    CRLF
E095  3E23       0105           LD      A,'#'
E097  CD85E3     0106           CALL    CONOUT
E09A  CD7DE3     0107           CALL    SPACE
E09D  CD90E3     0108 EXEC4:    CALL    CONIN
```

```
ADDR   CODE      STMT SOURCE STATEMENT

E0A0   FE21      0109             CP      21H
E0A2   FA9DE0    0110             JP      M,EXEC4
E0A5   FE41      0111             CP      'A'
E0A7   284A      0112             JR      Z,ALTER-$
E0A9   FE44      0113             CP      'D'
E0AB   2871      0114             JR      Z,DUMP-$
E0AD   FE47      0115             CP      'G'
E0AF   283E      0116             JR      Z,GO-$
E0B1   FE43      0117             CP      'C'
E0B3   CAB8E1    0118             JP      Z,COPY
E0B6   FE54      0119             CP      'T'
E0B8   CACDE1    0120             JP      Z,TEST
E0BB   FE46      0121             CP      'F'
E0BD   CAA0E1    0122             JP      Z,FILL
E0C0   FE4D      0123             CP      'M'
E0C2   CA3CE1    0124             JP      Z,MAP
E0C5   FE4C      0125             CP      'L'
E0C7   CA72E1    0126             JP      Z,LOAD
E0CA   FE53      0127             CP      'S'
E0CC   CA8CE2    0128             JP      Z,TSAVE
E0CF   FE52      0129             CP      'R'
E0D1   CA17E2    0130             JP      Z,TLOAD
E0D4   FE56      0131             CP      'V'
E0D6   CADEE2    0132             JP      Z,VERIFY
E0D9   FE58      0133             CP      'X'
E0DB   CACBE2    0134             JP      Z,STRM
                 0135             IF      KCTAPE
E0DE   FE59      0136             CP      'Y'
E0E0   CA68E2    0137             JP      Z,TUNE
                 0138             ENDIF
E0E3   FE42      0139             CP      'B'
E0E5   CAB5E3    0140             JP      Z,BOOT
E0E8   FE45      0141             CP      'E'
E0EA   CA00F0    0142             JP      Z,0F000H
                 0143 ;           the above is a jump to the Versafloppy BIOS ROM
E0ED   18A3      0144             JR      EXEC3-$
E0EF   CD22E3    0145 GO:         CALL    SPHIN
E0F2   E9        0146             JP      (HL)
E0F3   CD22E3    0147 ALTER:      CALL    SPHIN
E0F6   CD70E3    0148 ALT1:       CALL    CRLF
E0F9   CD54E3    0149             CALL    DHXOT
E0FC   CD7DE3    0150             CALL    SPACE
E0FF   7E        0151             LD      A,(HL)
E100   CD59E3    0152             CALL    HEXOUT
E103   E5        0153             PUSH    HL
E104   CD22E3    0154             CALL    SPHIN
E107   5D        0155             LD      E,L
E108   E1        0156             POP     HL
E109   FE0D      0157             CP      0DH
E10B   CA1BE1    0158             JP      Z,ALT3
E10E   FE2F      0159             CP      '/'
E110   CA90E0    0160             JP      Z,EXEC
E113   FE2E      0161             CP      '.'
E115   2001      0162             JR      NZ,ALT2-$
E117   73        0163             LD      (HL),E
E118   23        0164 ALT2:       INC     HL
E119   18DB      0165             JR      ALT1-$
E11B   2B        0166 ALT3:       DEC     HL
```

```
ADDR  CODE      STMT SOURCE STATEMENT

E11C  18D8      0167         JR      ALT1-$
E11E  CD16E3    0168 DUMP:   CALL    DHXIN
E121  CD70E3    0169 DUMP1:  CALL    CRLF
E124  CD54E3    0170         CALL    DHXOT
E127  0610      0171         LD      B,16
E129  CD7DE3    0172 DUMP2:  CALL    SPACE
E12C  7E        0173         LD      A,(HL)
E12D  CD59E3    0174         CALL    HEXOUT
E130  CD06E3    0175         CALL    CMPDH
E133  DA90E0    0176         JP      C,EXEC
E136  23        0177         INC     HL
E137  05        0178         DEC     B
E138  20EF      0179         JR      NZ,DUMP2-$
E13A  18E5      0180         JR      DUMP1-$
E13C  0601      0181 MAP:    LD      B,1
E13E  210000    0182         LD      HL,0
E141  7E        0183 MAP1    LD      A,(HL)
E142  2F        0184         CPL
E143  77        0185         LD      (HL),A
E144  BE        0186         CP      (HL)
E145  2F        0187         CPL
E146  77        0188         LD      (HL),A
E147  3E00      0189         LD      A,0
E149  2801      0190         JR      Z,MAP2-$
E14B  3C        0191         INC     A
E14C  B8        0192 MAP2:   CP      B
E14D  47        0193         LD      B,A
E14E  2811      0194         JR      Z,MAP4-$
E150  2B        0195         DEC     HL
E151  B7        0196         OR      A
E152  2004      0197         JR      NZ,MAP3-$
E154  23        0198         INC     HL
E155  CD70E3    0199         CALL    CRLF
E158  CD54E3    0200 MAP3:   CALL    DHXOT
E15B  CD7DE3    0201         CALL    SPACE
E15E  2801      0202         JR      Z,MAP4-$
E160  23        0203         INC     HL
E161  23        0204 MAP4:   INC     HL
E162  7D        0205         LD      A,L
E163  B4        0206         OR      H
E164  20DB      0207         JR      NZ,MAP1-$
E166  78        0208         LD      A,B
E167  B7        0209         OR      A
E168  C290E0    0210         JP      NZ,EXEC
E16B  2B        0211         DEC     HL
E16C  CD54E3    0212         CALL    DHXOT
E16F  C390E0    0213         JP      EXEC
E172  CD7DE3    0214 LOAD:   CALL    SPACE
E175  CD8EE1    0215 LOAD0:  CALL    LHXIN
E178  20FB      0216         JR      NZ,LOAD0-$
E17A  CD8EE1    0217 LOAD1:  CALL    LHXIN
E17D  FE20      0218         CP      ' '
E17F  20F4      0219         JR      NZ,LOAD0-$
E181  EB        0220         EX      DE,HL
E182  CD8EE1    0221 LOAD2:  CALL    LHXIN
E185  F5        0222         PUSH    AF
E186  7D        0223         LD      A,L
E187  12        0224         LD      (DE),A
```

```
ADDR  CODE      STMT SOURCE STATEMENT

E188  13        0225         INC   DE
E189  F1        0226         POP   AF
E18A  20F6      0227         JR    NZ,LOAD2-$
E18C  18EC      0228         JR    LOAD1-$
E18E  CD25E3    0229 LHXIN:  CALL  HEXIN
E191  FE0A      0230         CP    0AH
E193  28F9      0231         JR    Z,LHXIN-$
E195  B7        0232         OR    A
E196  28F6      0233         JR    Z,LHXIN-$
E198  FE23      0234         CP    '#'
E19A  CA90E0    0235         JP    Z,EXEC
E19D  FE0D      0236         CP    0DH
E19F  C9        0237         RET
E1A0  CD16E3    0238 FILL:   CALL  DHXIN
E1A3  D60D      0239         SUB   0DH
E1A5  2806      0240         JR    Z,FILL0-$
E1A7  E5        0241         PUSH  HL
E1A8  CD25E3    0242         CALL  HEXIN
E1AB  7D        0243         LD    A,L
E1AC  E1        0244         POP   HL
E1AD  2B        0245 FILL0:  DEC   HL
E1AE  23        0246 FILL1:  INC   HL
E1AF  77        0247         LD    (HL),A
E1B0  CD06E3    0248         CALL  CMPDH
E1B3  30F9      0249         JR    NC,FILL1-$
E1B5  C390E0    0250         JP    EXEC
E1B8  CD45E3    0251 COPY:   CALL  TRPIN
E1BB  CDC1E1    0252         CALL  COPY0
E1BE  C390E0    0253         JP    EXEC
E1C1  1B        0254 COPY0:  DEC   DE
E1C2  0B        0255         DEC   BC
E1C3  13        0256 COPY1:  INC   DE
E1C4  03        0257         INC   BC
E1C5  12        0258         LD    (DE),A
E1C6  0A        0259         LD    A,(BC)
E1C7  CD06E3    0260         CALL  CMPDH
E1CA  30F7      0261         JR    NC,COPY1-$
E1CC  C9        0262         RET
E1CD  CD16E3    0263 TEST:   CALL  DHXIN
E1D0  13        0264         INC   DE        ;add 1 to ending address
E1D1  E5        0265         PUSH  HL
E1D2  DDE1      0266         POP   IX        ;save starting address
E1D4  0E00      0267         LD    C,256     ;total number of passes
E1D6  0600      0268         LD    B,0       ;starting pattern
E1D8  DDE5      0269 TEST0:  PUSH  IX
E1DA  E1        0270         POP   HL        ;get preserved start address
E1DB  7D        0271 TEST1:  LD    A,L
E1DC  AC        0272         XOR   H
E1DD  A8        0273         XOR   B
E1DE  77        0274         LD    (HL),A
E1DF  23        0275         INC   HL
E1E0  7C        0276         LD    A,H
E1E1  BA        0277         CP    D
E1E2  20F7      0278         JR    NZ,TEST1-$
E1E4  DDE5      0279         PUSH  IX
E1E6  E1        0280         POP   HL        ;fetch start address for read test
E1E7  7D        0281 TEST2:  LD    A,L
E1E8  AC        0282         XOR   H
```

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ADDR  CODE      STMT SOURCE STATEMENT

E1E9  A8        0283            XOR     B
E1EA  BE        0284            CP      (HL)
E1EB  C4FFE1    0285            CALL    NZ,ERRO ;found an error, exit
E1EE  23        0286            INC     HL
E1EF  7C        0287            LD      A,H
E1F0  BA        0288            CP      D
E1F1  20F4      0289            JR      NZ,TEST2-$
E1F3  04        0290            INC     B
E1F4  3E50      0291            LD      A,'P'
E1F6  CD85E3    0292            CALL    CONOUT
E1F9  0D        0293            DEC     C
E1FA  20DC      0294            JR      NZ,TEST0-$
E1FC  C390E0    0295            JP      EXEC
E1FF  F5        0296 ERRO:      PUSH    AF
E200  E5        0297            PUSH    HL
E201  CD54E3    0298            CALL    DHXOT
E204  CD7DE3    0299            CALL    SPACE
E207  78        0300            LD      A,B
E208  CD59E3    0301            CALL    HEXOUT
E20B  CD7DE3    0302            CALL    SPACE
E20E  F1        0303            POP     AF
E20F  CD59E3    0304            CALL    HEXOUT
E212  CD70E3    0305            CALL    CRLF
E215  E1        0306            POP     HL
E216  C9        0307            RET
                0308 ;
                0309 ;
                0310            IF      KCTAPE
E217  CD16E3    0311 TLOAD:     CALL    DHXIN
E21A  CD2BE2    0312            CALL    TREAD
E21D  CA90E0    0313            JP      Z,EXEC
E220  CD7DE3    0314            CALL    SPACE
E223  3E23      0315            LD      A,'#'
E225  CD85E3    0316            CALL    CONOUT
E228  C390E0    0317            JP      EXEC
E22B  3EB0      0318 TREAD:     LD      A,0B0H
E22D  D380      0319            OUT     (TAPST),A
E22F  0604      0320 TRDA:      LD      B,4
E231  CD5FE2    0321 TRDB:      CALL    CIN
E234  FEFF      0322            CP      0FFH
E236  20F7      0323            JR      NZ,TRDA-$
E238  0B        0324            DEC     BC
E239  20F6      0325            JR      NZ,TRDB-$
E23B  CD5FE2    0326 TRDC:      CALL    CIN
E23E  FEFF      0327            CP      0FFH
E240  28ED      0328            JR      Z,TRDA-$
E242  FEE6      0329            CP      0E6H
E244  20E9      0330            JR      NZ,TRDA-$
E246  0600      0331            LD      B,0
E248  3E24      0332            LD      A,'$'
E24A  CD85E3    0333            CALL    CONOUT
E24D  2B        0334            DEC     HL
E24E  23        0335 TRD1:      INC     HL
E24F  CD5FE2    0336            CALL    CIN
E252  77        0337            LD      (HL),A
E253  80        0338            ADD     A,B
E254  47        0339            LD      B,A
E255  CD06E3    0340            CALL    CMPDH
```

```
ADDR   CODE      STMT SOURCE STATEMENT

E258   30F4      0341             JR      NC,TRD1-$
E25A   CD5FE2    0342             CALL    CIN
E25D   B8        0343             CP      B
E25E   C9        0344             RET
E25F   DB80      0345 CIN:        IN      A,(TAPST)
E261   E601      0346             AND     01H
E263   28FA      0347             JR      Z,CIN-$
E265   DB00      0348             IN      A,(TAPE)
E267   C9        0349             RET
E268   CD7DE3    0350 TUNE:       CALL    SPACE
E26B   3EB0      0351             LD      A,0B0H
E26D   D380      0352             OUT     (TAPST),A
E26F   CD70E3    0353 TUN0:       CALL    CRLF
E272   2620      0354             LD      H,32
>E274            0355 TUN1:
E274   CD5FE2    0356 TUN2:       CALL    CIN
E277   FEFF      0357             CP      0FFH
E279   28F9      0358             JR      Z,TUN2-$
E27B   2E2B      0359             LD      L,'+'
E27D   FEE6      0360             CP      0E6H
E27F   2802      0361             JR      Z,TUN3-$
E281   2E3F      0362             LD      L,'?'
E283   7D        0363 TUN3:       LD      A,L
E284   CD85E3    0364             CALL    CONOUT
E287   25        0365             DEC     H
E288   20EA      0366             JR      NZ,TUN1-$
E28A   18E3      0367             JR      TUN0-$
E28C   CD16E3    0368 TSAVE:      CALL    DHXIN
E28F   CD95E2    0369             CALL    TWRIT
E292   C390E0    0370             JP      EXEC
E295   3EB0      0371 TWRIT:      LD      A,0B0H
E297   D380      0372             OUT     (TAPST),A
E299   0610      0373             LD      B,16
E29B   3EFF      0374 TWRT0:      LD      A,0FFH
E29D   CDC0E2    0375             CALL    COUT
E2A0   05        0376             DEC     B
E2A1   20F8      0377             JR      NZ,TWRT0-$
E2A3   3EE6      0378             LD      A,0E6H
E2A5   CDC0E2    0379             CALL    COUT
E2A8   2B        0380             DEC     HL
E2A9   0600      0381             LD      B,0
E2AB   23        0382 TWRT1:      INC     HL
E2AC   7E        0383             LD      A,(HL)
E2AD   CDC0E2    0384             CALL    COUT
E2B0   80        0385             ADD     A,B
E2B1   47        0386             LD      B,A
E2B2   CD06E3    0387             CALL    CMPDH
E2B5   30F4      0388             JR      NC,TWRT1-$
E2B7   78        0389             LD      A,B
E2B8   CDC0E2    0390             CALL    COUT
E2BB   CDC0E2    0391             CALL    COUT
E2BE   1800      0392             JR      COUT-$
E2C0   F5        0393 COUT:       PUSH    AF
E2C1   DB80      0394             IN      A,(TAPST)
E2C3   E680      0395             AND     80H
E2C5   28FA      0396             JR      Z,COUT+1-$
E2C7   F1        0397             POP     AF
E2C8   D300      0398             OUT     (TAPE),A
```

```
ADDR   CODE      STMT SOURCE STATEMENT

E2CA   C9        0399          RET
E2CB   CD7DE3    0400 STRM:    CALL    SPACE
E2CE   3EB0      0401          LD      A,0B0H
E2D0   D380      0402          OUT     (TAPST),A
E2D2   3EFF      0403 STRM1:   LD      A,0FFH
E2D4   CDC0E2    0404          CALL    COUT
E2D7   3EE6      0405          LD      A,0E6H
E2D9   CDC0E2    0406          CALL    COUT
E2DC   18F4      0407          JR      STRM1-$
                 0408          ENDIF
                 0409 ;
                 0410          IF      TARBEL
                 0411 TLOAD    CALL    DHXIN
                 0412          CALL    TREAD
                 0413          JP      Z,EXEC
                 0414          LD      A,'*'
                 0415          CALL    CONOUT
                 0416          JP      EXEC
                 0417 TREAD    LD      A,1
                 0418          OUT     (TARBL),A
                 0419          PUSH    HL
                 0420          LD      HL,20000
                 0421          CALL    DELAY
                 0422          POP     HL
                 0423          LD      B,0
                 0424          LD      A,11H
                 0425          OUT     (TARBL),A
                 0426          DEC     HL
                 0427 TRD1     INC     HL
                 0428          CALL    CIN
                 0429          LD      (HL),A
                 0430          ADD     A,B
                 0431          LD      B,A
                 0432          CALL    CMPDH
                 0433          JR      NC,TRD1-$
                 0434          CALL    CIN
                 0435          CP      B
                 0436          PUSH    AF
                 0437          SUB     A
                 0438          OUT     (TARBL),A
                 0439          POP     AF
                 0440          RET
                 0441 CIN      IN      A,(TARBL)
                 0442          AND     10H
                 0443          JR      NZ,CIN-$
                 0444          IN      A,(TARBL+1)
                 0445          RET
                 0446 TSAVE    CALL    DHXIN
                 0447          CALL    TWRIT
                 0448          JP      EXEC
                 0449 TWRIT    LD      A,2
                 0450          OUT     (TARBL),A
                 0451          PUSH    HL
                 0452          LD      HL,0FFFFH
                 0453          CALL    DELAY
                 0454          POP     HL
                 0455          SUB     A
                 0456          LD      B,A
```

```
ADDR   CODE        STMT SOURCE STATEMENT

                                 CALL    COUT
                                 LD      A,0E6H
                                 CALL    COUT
                                 DEC     HL
                        TWRT1    INC     HL
                                 LD      A,(HL)
                                 CALL    COUT
                                 ADD     A,B
                                 LD      B,A
                                 CALL    CMPDH
                                 JR      NC,TWRT1-$
                                 LD      A,B
                                 CALL    COUT
                                 CALL    COUT
                                 CALL    COUT
                                 SUB     A
                                 OUT     (TARBL),A
                                 RET
                        COUT     PUSH    AF
                                 IN      A,(TARBL)
                                 AND     20H
                                 JR      NZ,COUT+1-$
                                 POP     AF
                                 OUT     (TARBL+1),A
                                 RET
                        STRM     CALL    SPACE
                                 LD      A,2
                                 OUT     (TARBL),A
                        STRM1    LD      A,0E6H
                                 CALL    COUT
                                 JR      STRM1-$
                        DELAY    EX      (SP),HL
                                 EX      (SP),HL
                                 DEC     HL
                                 LD      A,L
                                 OR      H
                                 JR      NZ,DELAY-$
                                 RET
                                 ENDIF
                        ;
E2DE   CD45E3           VERIFY:  CALL    TRPIN
E2E1   EB                        EX      DE,HL
E2E2   2B                        DEC     HL
E2E3   0B                        DEC     BC
E2E4   23               VRFY1:   INC     HL
E2E5   03                        INC     BC
E2E6   02                        LD      (BC),A
E2E7   BE                        CP      (HL)
E2E8   2814                      JR      Z,VRFY2-$
E2EA   CD70E3                    CALL    CRLF
E2ED   CD54E3                    CALL    DHXOT
E2F0   CD7DE3                    CALL    SPACE
E2F3   7E                        LD      A,(HL)
E2F4   CD59E3                    CALL    HEXOUT
E2F7   CD7DE3                    CALL    SPACE
E2FA   02                        LD      (BC),A
E2FB   CD59E3                    CALL    HEXOUT
E2FE   CD06E3           VRFY2:   CALL    CMPDH
```

```
ADDR  CODE      STMT SOURCE STATEMENT

E301  30E1      0515          JR    NC,VRFY1-$
E303  C390E0    0516          JP    EXEC
E306  F5        0517 CMPDH:   PUSH  AF
E307  7A        0518          LD    A,D
E308  BC        0519          CP    H
E309  2007      0520          JR    NZ,CMP1-$
E30B  7B        0521          LD    A,E
E30C  BD        0522          CP    L
E30D  2003      0523          JR    NZ,CMP1-$
E30F  F1        0524          POP   AF
E310  37        0525          SCF
E311  C9        0526          RET
E312  F1        0527 CMP1:    POP   AF
E313  37        0528          SCF
E314  3F        0529          CCF
E315  C9        0530          RET
E316  CD22E3    0531 DHXIN:   CALL  SPHIN
E319  E5        0532          PUSH  HL
E31A  FE0D      0533          CP    0DH
E31C  C425E3    0534          CALL  NZ,HEXIN
E31F  EB        0535          EX    DE,HL
E320  E1        0536          POP   HL
E321  C9        0537          RET
E322  CD7DE3    0538 SPHIN:   CALL  SPACE
E325  210000    0539 HEXIN:   LD    HL,0
E328  CD90E3    0540 HXIN1:   CALL  CONIN
E32B  FE30      0541          CP    '0'
E32D  F8        0542          RET   M
E32E  FE47      0543          CP    'F'+1
E330  F0        0544          RET   P
E331  FE3A      0545          CP    '9'+1
E333  FA3BE3    0546          JP    M,HXIN2
E336  FE41      0547          CP    'A'
E338  F8        0548          RET   M
E339  CE09      0549          ADC   A,9
E33B  E60F      0550 HXIN2:   AND   0FH
E33D  29        0551          ADD   HL,HL
E33E  29        0552          ADD   HL,HL
E33F  29        0553          ADD   HL,HL
E340  29        0554          ADD   HL,HL
E341  B5        0555          OR    L
E342  6F        0556          LD    L,A
E343  18E3      0557          JR    HXIN1-$
E345  CD22E3    0558 TRPIN:   CALL  SPHIN
E348  EB        0559          EX    DE,HL
E349  CD25E3    0560          CALL  HEXIN
E34C  E5        0561          PUSH  HL
E34D  CD25E3    0562          CALL  HEXIN
E350  E5        0563          PUSH  HL
E351  C1        0564          POP   BC
E352  E1        0565          POP   HL
E353  C9        0566          RET
E354  7C        0567 DHXOT:   LD    A,H
E355  CD59E3    0568          CALL  HEXOUT
E358  7D        0569          LD    A,L
E359  F5        0570 HEXOUT:  PUSH  AF
E35A  0F        0571          RRCA
E35B  0F        0572          RRCA
```

```
ADDR  CODE      STMT SOURCE STATEMENT

E35C  0F                       RRCA
E35D  0F                       RRCA
E35E  CD62E3                   CALL    HXOT1
E361  F1                       POP     AF
E362  E60F           HXOT1:    AND     0FH
E364  C630                     ADD     A,30H
E366  FE3A                     CP      '9'+1
E368  FA85E3                   JP      M,CONOUT
E36B  C607                     ADD     A,7
E36D  C385E3                   JP      CONOUT
E370  F5             CRLF:     PUSH    AF
E371  3E0D                     LD      A,0DH
E373  CD85E3                   CALL    CONOUT
E376  3E0A                     LD      A,0AH
E378  CD85E3                   CALL    CONOUT
E37B  F1                       POP     AF
E37C  C9                       RET
E37D  F5             SPACE:    PUSH    AF
E37E  3E20                     LD      A,20H
E380  CD85E3                   CALL    CONOUT
E383  F1                       POP     AF
E384  C9                       RET
E385  F5             CONOUT:   PUSH    AF
E386  DB11                     IN      A,(KBDST)
E388  E601                     AND     KBDOT
E38A  28FA                     JR      Z,CONOUT+1-$
E38C  F1                       POP     AF
E38D  D310                     OUT     (KBDDT),A
E38F  C9                       RET
E390  DB11           CONIN:    IN      A,(KBDST)
E392  E602                     AND     KBDIN
E394  28FA                     JR      Z,CONIN-$
E396  DB10                     IN      A,(KBDDT)
E398  E67F                     AND     7FH
E39A  FE61                     CP      61H
E39C  3806                     JR      C,ECHO-$
E39E  FE7C                     CP      7CH
E3A0  3002                     JR      NC,ECHO-$
E3A2  D620                     SUB     20H
E3A4  FE18           ECHO:     CP      18H
E3A6  CA90E0                   JP      Z,EXEC
E3A9  18DA                     JR      CONOUT-$
E3AB  7E             PTXT:     LD      A,(HL)
E3AC  FE03                     CP      03H
E3AE  C8                       RET     Z
E3AF  CD85E3                   CALL    CONOUT
E3B2  23                       INC     HL
E3B3  18F6                     JR      PTXT-$
E3B5  DBFC           BOOT      IN      A,(WAIT)
E3B7  AF                       XOR     A
E3B8  6F                       LD      L,A
E3B9  67                       LD      H,A
E3BA  3C                       INC     A
E3BB  D3FA                     OUT     (SECT),A
E3BD  3E8C                     LD      A,8CH
E3BF  D3F8                     OUT     (DCOM),A
E3C1  DBFC           RLOOP     IN      A,(WAIT)
E3C3  B7                       OR      A
```

```
ADDR  CODE      STMT SOURCE STATEMENT

E3C4  F2CEE3    0631             JP      P,RDONE
E3C7  DBFB      0632             IN      A,(DDATA)
E3C9  77        0633             LD      (HL),A
E3CA  23        0634             INC     HL
E3CB  C3C1E3    0635             JP      RLOOP
E3CE  DBF8      0636 RDONE       IN      A,(DSTAT)
E3D0  B7        0637             OR      A
E3D1  CA7D00    0638             JP      Z,SBOOT
E3D4  76        0639             HALT
                0640 ;
                0641             END
```

ADDR   CODE   STMT SOURCE STATEMENT

ALT1	E0F6	ALT2	E118	ALT3	E11B	ALTER	E0F3		
BOOT	E3B5	CIN	E25F	CMP1	E312	CMPDH	E306		
CONIN	E390	CONOUT	E385	COPY	E1B8	COPYO	E1C1		
COPY1	E1C3	COUT	E2C0	CRLF	E370	DCOM	00F8		
DDATA	00FB	DHXIN	E316	DHXOT	E354	DSTAT	00F8		
DUMP	E11E	DUMP1	E121	DUMP2	E129	ECHO	E3A4		
ERRO	E1FF	EXEC	E090	EXEC3	E092	EXEC4	E09D		
FALSE	0000	FILL	E1A0	FILLO	E1AD	FILL1	E1AE		
FTOP	E02E	FTOP1	E03B	FTOP2	E04B	GO	E0EF		
HEXIN	E325	HEXOUT	E359	HXIN1	E328	HXIN2	E33B		
HXOT1	E362	INIT	E021	INIT1	E04E	KBDDT	0010		
KBDIN	0002	KBDOT	0001	KBDST	0011	KCTAPE	FFFF		
LHXIN	E18E	LOAD	E172	LOADO	E175	LOAD1	E17A		
LOAD2	E182	MAP	E13C	MAP1	E141	MAP2	E14C		
MAP3	E158	MAP4	E161	MON	0000	MSG1	E063		
PTXT	E3AB	RDONE	E3CE	RLOOP	E3C1	SBOOT	007D		
SECT	00FA	SPACE	E37D	SPHIN	E322	STRM	E2CB		
STRM1	E2D2	TAPE	0000	TAPST	0080	TARBEL	0000		
TARBL	006E	TEST	E1CD	TESTO	E1D8	TEST1	E1DB		
TEST2	E1E7	TLOAD	E217	TRD1	E24E	TRDA	E22F		
TRDB	E231	TRDC	E23B	TREAD	E22B	TRPIN	E345		
TRUE	FFFF	TSAVE	E28C	TUNO	E26F	TUN1	E274		
TUN2	E274	TUN3	E283	TUNE	E268	TWRIT	E295		
TWRTO	E29B	TWRT1	E2AB	VERIFY	E2DE	VRFY1	E2E4		
VRFY2	E2FE	WAIT	00FC						

```
CROSS REFERENCE LISTING
SYMBOL VALUE  TYPE   STMT   STATEMENT REFERENCES
------ -----  ----   ----   --------------------

ALT1   E0F6          0148   0167 0165
ALT2   E118          0164   0162
ALT3   E11B          0166   0158
ALTER  E0F3          0147   0112
BOOT   E3B5          0621   0140
CIN    E25F          0345   0356 0347 0342 0336 0326 0321
CMP1   E312          0527   0523 0520
CMPDH  E306          0517   0514 0387 0340 0260 0248 0175
CONIN  E390          0602   0604 0540 0108 0044
CONOUT E385          0595   0618 0614 0598 0592 0587 0585 0582 0580 0364 0333
+                           0316 0292 0106 0082 0045
COPY   E1B8          0251   0118
COPY0  E1C1          0254   0252
COPY1  E1C3          0256   0261
COUT   E2C0          0393   0406 0404 0396 0392 0391 0390 0384 0379 0375
CRLF   E370          0583   0506 0353 0305 0129 0169 0148 0104 0086 0079 0078
+                           0049
DCOM   00F8          0035   0628
DDATA  00FB          0036   0632
DHXIN  E316          0531   0368 0311 0263 0238 0168
DHXOT  E354          0567   0507 0298 0212 0200 0170 0149 0089 0048
DSTAT  00F8          0037   0636
DUMP   E11E          0168   0114
DUMP1  E121          0169   0180
DUMP2  E129          0172   0179
ECHO   E3A4          0612   0610 0608
ERRO   E1FF          0296   0285
EXEC   E090          0099   0613 0516 0370 0317 0313 0295 0253 0250 0235 0213
+                           0210 0176 0160 0090 0043
EXEC3  E092          0104   0144
EXEC4  E09D          0108   0110
FALSE  0000          0016   0019
FILL   E1A0          0238   0122
FILL0  E1AD          0245   0240
FILL1  E1AE          0246   0249
FTOP   E02E          0059   0071 0068
FTOP1  E03B          0069   0066
FTOP2  E04B          0080
GO     E0EF          0145   0116
HEXIN  E325          0539   0562 0560 0534 0242 0229 0046
HEXOUT E359          0570   0568 0513 0510 0304 0301 0174 0152 0047
HXIN1  E328          0540   0557
HXIN2  E33B          0550   0546
HXOT1  E362          0577   0575
INIT   E021          0053   0042
INIT1  E04E          0081   0085
KBDDT  0010          0030   0605 0600
KBDIN  0002          0031   0603
KBDOT  0001          0032   0597
KBDST  0011          0029   0602 0596 0057 0055
KCTAPE FFFF          0020   0310 0135 0094
LHXIN  E18E          0229   0233 0231 0221 0217 0215
LOAD   E172          0214   0126
LOAD0  E175          0215   0219 0216
```

```
ADDR    CODE       STMT SOURCE STATEMENT

LOAD1   E17A        0217   0228
LOAD2   E182        0221   0227
MAP     E13C        0181   0124
MAP1    E141        0183   0207
MAP2    E14C        0192   0190
MAP3    E158        0200   0197
MAP4    E161        0204   0202 0194
MON     0000        0025
MSG1    E063        0095   0080
PTXT    E3AB        0615   0620
RDONE   E3CE        0636   0631
RLOOP   E3C1        0627   0635
SBOOT   007D        0038   0638
SECT    00FA        0034   0626
SPACE   E37D        0590   0538 0511 0508 0400 0350 0314 0302 0299 0214 0201
+                          0172 0150 0107 0050
SPHIN   E322        0538   0558 0531 0154 0147 0145
STRM    E2CB        0400   0134
STRM1   E2D2        0403   0407
TAPE    0000        0027   0378 0348
TAPST   0080        0028   0402 0394 0372 0352 0345 0319
TARBEL  0000        0019   0410 0100 0091
TARBL   006E        0039
TEST    E1CD        0263   0120
TEST0   E1D8        0269   0294
TEST1   E1DB        0271   0278
TEST2   E1E7        0281   0289
TLOAD   E217        0311   0130
TRD1    E24E        0335   0341
TRDA    E22F        0320   0330 0328 0323
TRDB    E231        0321   0325
TRDC    E23B        0326
TREAD   E22B        0318   0312 0051
TRPIN   E345        0558   0497 0251
TRUE    FFFF        0015   0020
TSAVE   E28C        0368   0128
TUN0    E26F        0353   0367
TUN1    E274        0355   0366
TUN2    E274        0356   0358
TUN3    E283        0363   0361
TUNE    E268        0350   0137
TWRIT   E295        0371   0369 0052
TWRT0   E29B        0374   0377
TWRT1   E2AB        0382   0388
VERIFY  E2DE        0497   0132
VRFY1   E2E4        0501   0515
VRFY2   E2FE        0514   0505
WAIT    00FC        0033   0629 0621
ERRORS=0000
```

APPENDIX B

CONSTRUCTION AND SOLDERING TIPS

Choose a well-lighted work space with enough room to place your tools, parts, and instructions where they will be easy to reach. If you have two light sources that can be adjusted, this will help eliminate shadows which interfere with seeing your work.

Familiarize yourself with all of the general operations to be performed. It might even help to do a dry run of sorts, getting everything together and following the procedures.

The tools you will need for each individual kit will be listed in the assembly instructions. A basic set would include: a low wattage soldering iron (20 watts or less—remember, you're working with microcomputers, not building bridges)—and with a 650-degree tip if you can get one; a holder which will keep you from accidentally touching the hot tip; a pair of wire cutters (also called dykes or side cutters, preferably beveled so that you can cut close to the board); a pair of needle-nose pliers; a damp sponge or a moistened cloth to use to wipe the soldering iron's tip; a magnifying glass to examine details, and a lead former to bend leads. The latter is available at most electronics parts houses in an inexpensive plastic version, or you can make your own out of wood. If you're into building lots of electronic kits, they're worth their weight in gold.

Arrange your tools in order of their frequency of use and orient them so they're easy to reach. Make sure that they are clean and in good working order.

Keep your work area clean and uncluttered.

Make sure that your chair is set at a proper height and is comfortable for your work station.

Try to keep food and drink away from your area. Always strive for neatness and uniformity. This means removing bits and pieces of scrap wire and solder blobs, as you work, so they don't become buried in your board and short something out. Inevitably, according to Murphy, they will sneak underneath IC sockets and if there's a place that's hardest to get to to fix, that's *exactly* where they'll lodge.

Soldering can cause several different kinds of problems in kit building. Heat can damage the PC board and the components, especially diodes and transistors, or create unwanted electrical connections. Most problems can be eliminated by using the right soldering iron (and the right solder—*rosin* core, *not* acid core), and by developing an efficient technique.

Parts are inserted on the component (front) side of the board. Soldering is done on the back side. This is always a rule, unless you are specifically directed otherwise in the assembly instructions.

If you plan on building many kits (and one memory board can be many kits), spend the few extra dollars to buy yourself a quality temperature-controlled soldering station. Spending the $30 can save you from ruining a $200 kit.

Use only **Rosin Core** solder when constructing electronic kits. Never, never, not **ever** use acid core—that's only for pipes and sheet metal. A solder with a high ratio of tin to lead is important, too. 60/40 is good—but 63/37 is better, and the difference will amaze you. If you can't get 63/37 at your local electronics parts house, JADE carries it, along with most of the other accessories you might need.

Make sure you have a well-tinned tip. A tip is well tinned when it has a thin film of solder coating on the surface of the iron. Oxide and resin build up as you work with it and the bright shiny look will disappear. That's what the wet sponge or moistened cloth is for. The iron should be wiped clean about every ten connections or so to get rid of that oxide and resin. Copper-tinned iron are fairly good, but gold-coated tips are much better.

Some DON'Ts: DON'T have any unnecessary items at your work station. DON'T use worn or damaged tools. NEVER solder equipment that is plugged in. DON'T pull on a solder joint to see if it's good. NEVER flip excess solder from the tip of your iron—use the sponge or cloth. NEVER put solder on your iron and then transfer it to a cold joint.

Heat both the component wire and the solder pad with the tip of the iron until it looks wet or liquid. Then touch the solder to the junction between the iron, the pad, and the wire. When the solder melts and flows onto the connection, quickly remove the iron's tip. Allow the joint to cool without moving any of the components. A good joint will be smooth and bright. A bad one will be a dull lead-looking glob of solder.

Avoid using too much solder! From our experience at repairing customer's boards, this is the sin most often committed. If little drops of solder appear on the opposite side of the board, you're either using too much solder or too much heat. Be extremely careful when you solder adjacent pads because the heat may cause the solder to flow between them, making a solder "bridge". Bridges are only good for crossing rivers—they don't belong on electronic boards. They make an unwanted electrical connection.

If you do find a bridge, the best way to remove it is to clean your iron on the dampened sponge or cloth and then touch the bridge with the clean hot tip until it wets and sticks to the tip. Then get rid of it.

Excess wire can be removed with diagonal cutters. WAIT until the joint has cooled. Beware of flying pieces of wire. **Always use eye protection when soldering or cutting wire!**

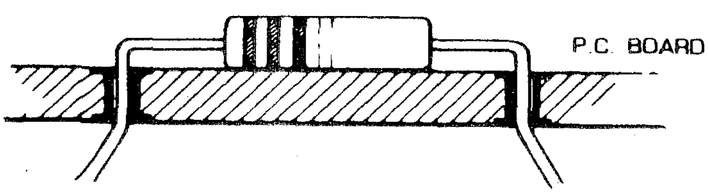
After you're all done, use Freon solvent to remove the flux. Flux is that brown stuff that gets on the board near your soldering joints, and it is formed of burned resin. Not only does it *look* bad (preventing your wonderful soldering job from looking all bright and shiny and seeing the light of day), it can cause electrical headaches as well, especially in higher-frequency circuits. Not only this, but it makes it much more difficult to find bridges and shorting flakes of solder, since the rosin hides the solder under an effective coverup. Leave coverups to the politicians—clean your board.

JADE technical support people have found that a board works about like it looks. If it's been put together with care and good workmanship, it will work just fine. In life, you only get out of it what you put into it, and it works the same with electronic kits.

COMPONENT INSTALLATION

Install all components in their proper location, and if polarity is important, observe the proper markings. The component should be installed flush with the circuit board, unless a clearance is specifically called for in the assembly instructions. This clearance is usually required for hot components that might burn or discolor the printed circuit board.

The lead should have a discernable length extending straight from the body of the component before beginning the bend. The component body shall not be damaged nor the body-to-lead seal be damaged by the forming operation. The component should be centered between the bends, although this is not a requirement. Where feasible, all forming should be done so that the part number is visible when installed in the printed circuit board.



Soldering techniques probably are the hardest to master of any electronic assembly technique. If you have never soldered at all, it is probably best that you practice on some old scrap printed circuit board available at most electronic parts houses and surplus shops.

For electronic assembly, always use rosin core solder, not acid core solder. Acid core solder will corrode, and it's impossible to stop the corrosion once it's begun. It will eventually ruin the printed circuit board.

A soldering iron of small wattage (preferably 27 to 40 watts absolute maximum), should be used. Always keep the tip clean and free from dross (oxidized solder) by wiping on a moistened sponge or folded up Kleenex (moistened). Use small solder with a 60/40 ratio (60% tin and 40% lead).

When ready to solder a joint, apply heat to the joint first, then apply the solder to the opposite side of the joint from the iron. (See Figure B-1). Then remove the solder and finally the soldering iron. A good solder joint has an even flow of solder over the entire joint. A good joint will have a bright glistening look. A bad solder joint, commonly called a "cold" solder joint, will have a dull appearance. Also, do not move the part or the lead while the solder is cooling or a cold or fractured solder joint will result (see Figure B-2a-c).

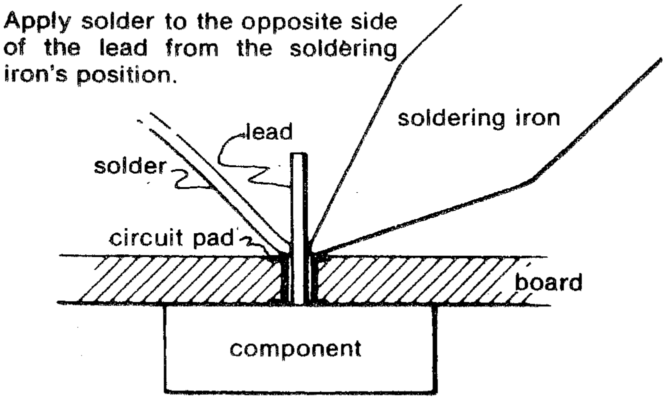


Figure B-1 Illustrates proper soldering techniques

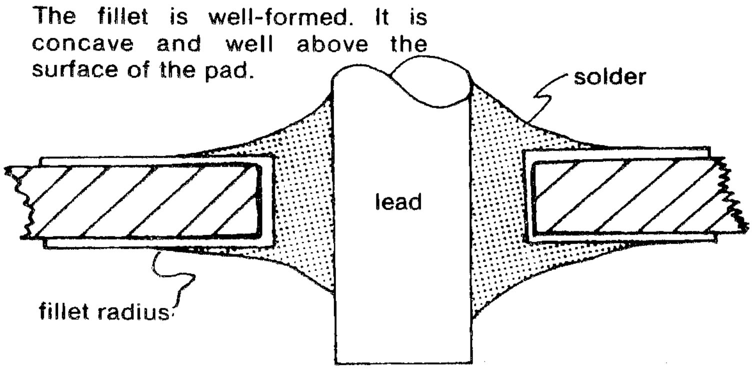


Figure B-2 (a) Illustrates an Optimum Solder Joint

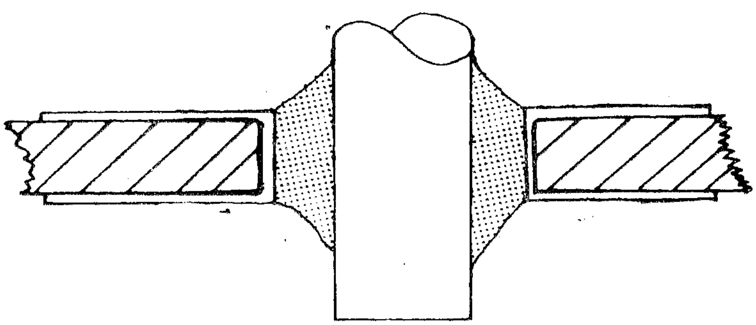


Figure B-2 (b) Illustrates the minumin solder acceptable

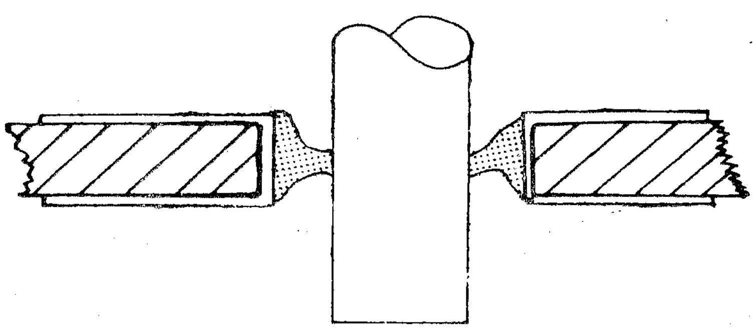
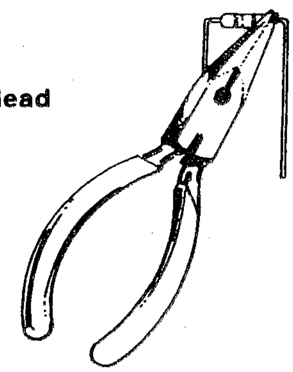


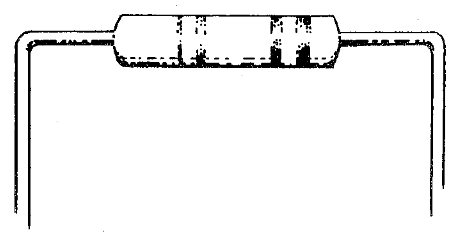
Figure B-2 (c) Illustrates insufficient solder.

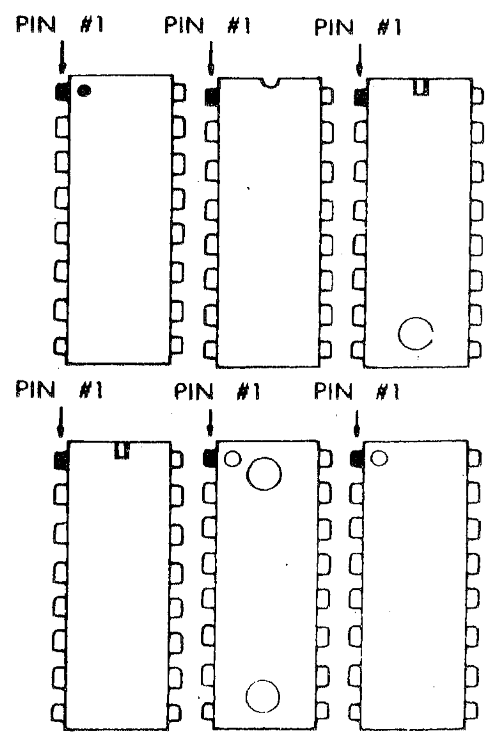
Lead Forming

Lead forming is performed by grasping the body of the part with the fingers of one hand. With the other hand holding long-nose pliers, grasp the lead near the body with the taper of the pliers defining the length of lead from the body of the part to the lead. Bend the lead with the opposite hand to form the bend as in Figure B-3.

Figure B-3 Illustrates lead forming techniques.







PARTS LIST FOR JADE BIG Z CPU - REVISION C BOARD

Item No	Qty/ Assy	Jade Part No.	Description
1	1	CPU-30200D	Manual, Big Z Revision C
2	1	CPU-30200B	PC Board, Big Z Revision C, 2/4 MHz
3	1	ICM-Z80A	Microprocessor IC, Z80A, 4MHz - U16
4	1	ICS-8251	USART, 8251 - U3
5	1	ICS-MC14411	Baud Rate Generator, MC14411 - U2
6	9	ICT-N8T97	Hex TS Buffer, 8T97/74367/8097/74LS367 - U6,17,25,29,35-39
7	2	ICM-DM8131N	6-Bit Comparator, DM8131 - U24, 34
8	3	ICT-7475	Quad Latch, 7475/74LS75 - U40, 26, 27
9	2	ICT-7474	Dual D Flipflop, 7474/74LS74 - U11, 20
10	1	ICT-74121	One-shot, 74121/74LS121 - U5
11	1	ICT-7432	Quad 2-input OR, 7432/74LS32 - U14
12	2	ICT-7400	Quad 2-input NAND, 7400/74LS00 - U10, 22
13	2	ICT-7408	Quad 2-input AND, 7408/74LS08 - U7, 41
14	1	ICT-7410	Triple 3-input NAND, 7410/74LS10 - U4
15	1	ICT-7402	Quad 2-input NOR, 7402/74LS02 - U8
16	4	ICT-7404	Hex Inverter, 7404/74LS04 - U15, 18, 21, 30
17	1	ICT-1488	RS232 Driver, MC1488/75188 - U12
18	1	ICT-1489	RS232 Receiver, MC1489/75189 - U9
19	1	ICL-LM7805	+5V Regulator, LM340T5/7805 - VR4
20	1	ICL-LM7812	+12V Regulator, LM340T12/7812 - VR3
21	1	ICL-LM7905	-5V Regulator, LM320T5/7905 - VR1
22	1	ICL-LM7912	-12V Regulator, LM320T12/7912 - VR2
23	1	CRY-040	Crystal, 4.0000 MHz - Y1
24	1	CRY-018L	Crystal, 1.8432 MHz - Y2
25	1	SKL-4001	Socket, 40-pin low profile
26	1	SKL-2801	Socket, 28-pin low profile
27	2	SKL-2401	Socket, 24-pin low profile
28	18	SKL-1601	Socket, 16-pin low profile
29	16	SKL-1401	Socket, 14-pin low profile
30	3	SWD-108	DIP Switch, 8-position - U1, 23, 33
31	1	SWX-101	Switch, SPDT, low profile, T-U-V switch
32	3	RCD-16154.7K	Resistor Pack, 15-resistor, 16-pin 4.7K pullups - U28, 31, 32
33	7	RCQ-4.70K	Resistor, 4.7K ¼-watt - R1, 3, 7, 8, 9, 13, 14
34	1	RCQ-330.0	Resistor, 330 ohm, ¼watt - R5
35	3	RCQ-1.0K	Resistor, 1K, ¼-watt - R4, 10, 11
36	1	RCQ-2.70K	Resistor, 2.7K ¼ watt - R2
37	1	RCQ-22.0M	Resistor, 22 Meg, ¼-watt - R6
38	1	RCQ-6.80K	Resistor, 6.8K, ¼ watt - R12
39	15	CAD-104P500	Capacitor, disk ceramic, 0.1uf - C1-15
40	1	CAA-101M639	Capacitor, 100uf axial electrolytic/50-100uf - C22
41	3	CAD-102P500	Capacitor, disk ceramic, 0.001uf - C23, 26, 27
42	2	CAD-101P500	Capacitor, 100pf mica - C24, C25
43	6	CAT-15P250	Capacitor, tantalum, 1.5uf/1.5-3.3uf - C16-21
44	1	HDH-36100	Heat Sink, AHM, TO-220 style (use at VR4)
45	4	- - - -	Screws, 6-32 x ½"
46	4	- - - -	Nuts, Hex, #6
47	4	- - - -	Washers, Lock, #6
			Last U Number = U41
			Last R Number = R14
			Last C Number = C27
			Last Y Number = Y2
			Last V Number = VR4

JADE COMPUTER PRODUCTS

ENGINEERING PRODUCT-IMPROVEMENT BULLETIN - CPU-30201

BIG Z CPU CARD - ECN 1Ø1 2 December, 1980

Problem: Erratic reset operation.

Symptoms: The CPU fails to reset reliably when the reset line is pulled low, although it will reset properly on power-on.

Cause: Excessive time constant on RC network on input to IC U21, pin 1 (reset buffer). The time constant of the power-on/reset network is approximately 0.5 seconds (470 milliseconds). This delay is required for operation with front-panel type systems, but it is lengthy for turnkey systems using an on-board EPROM monitor. The specification for the Z80 CPU is a minimum of 4 clock cycles.

Cure: Remove C22, a 100 microfarad electrolytic capacitor, and install a 1 to 10 microfarad tantalum capacitor in its place. The lower value capacitor may cause the board to fail to reset when doing a power-on without striking the reset switch on the mainframe. If this is experienced, the value of C22 should be increased, up to 22 microfarads. The optimum value may be found for each particular system by experimentation.

JADE COMPUTER PRODUCTS

ENGINEERING PRODUCT-IMPROVEMENT BULLETIN - CPU-30201

BIG Z CPU CARD - ECN 1Ø2 | 2 December, 1980

Problem: Timing Problems Associated with Status Signal Delay.

Symptoms: The CPU card fails to operate with some dynamic memory cards at 4 MHz, and operates erratically with some disk controller cards at all operating clock rates.

Cause: In an attempt to make the BIG Z CPU as versatile as possible, it was designed to operate with a front panel board of the Imsai type. This requires latching the status signals sWO*, sMEMR and sINP. This latching is done by IC U40, a 7475/74LS75 IC, clocked by the signal pSYNCH. The manual fails to mention that this takes the CPU board out of IEEE timing specification.

Cure: Remove IC U40 and install a 16-pin dip header with jumpers installed between pins 2/16, 3/15, 6/10 and 7/9. This removes the latch and does not introduce a pSYNCH delay for these signals.

Inter-card Compatibility:

The above modification must be done to allow the BIG Z CPU to operate with an S.D. Systems Expandoram II at either 2 or 4 MHz. It must be done to ensure reliable operation with the JADE Double D Disk Controller, and other types of disk controller cards (not required for any S.D. Systems disk controller or for the Expandoram I when operated at 2 MHz.

JADE COMPUTER PRODUCTS

ENGINEERING PRODUCT-IMPROVEMENT BULLETIN - CPU-30201

BIG Z CPU CARD - ECN 1Ø3 2 December, 1980
Revision C level, manufacturing level 5 and above

Problem: Owner's manual errata

Checkout Procedures & Troubleshooting Tips - page 14.

In paragraph 10, step 1, it is stated that pins 1-5 and 30-40 as well as the data pins on the Z80 should show high during reset. In actuality, they are tri-stated, and the more sophisticated logic probes, as well as oscilloscopes, will show them as somewhere in the indeterminate range.

In step 2, it is stated (incorrectly) that pin 24 of the Z80 should be low. In reality, it should be high unless you have selected the EPROM wait state option or installed the M1 wait state option, in which case it will be high with low-going pulses. In the same step it is stated that pin 27 (M1*) of the Z80 should be low. In reality, it will be high with low-going pulses. The above instructions were intended for those people with primitive logic probes, and they are correct as stated; however, the manual should be changed to reflect a more accurate state of affairs for those people who have oscilloscopes or newer types of logic probes.

EPROM Tables - pages 17 & 18

Although it is not specifically stated in the manual, the purpose of the Xes is to indicate a switch CLOSED position, or ON position. A properly installed switch will have its 1 position facing the S100 bus. The tables are correct if the switch positions marked X are closed.

NOTE however, the function of switch positions 6, 7 and 8. These switches are for the purpose of making the EPROM slot as versatile as possible. Switch 8 routes Address Line A10 to one input to the comparator 8131 at U34, as well as one side of switch U33, position 7. If switches 7 and 8 are both closed, the effect is to ground A10, preventing it from ever going high. This is neither very effective, nor particularly good for the Z80 CPU chip. If you are wanting to compare A10 to a zero condition, turn switch position 8 ON, turn switch position 7 OFF (removing the ground from A10), and turn switch position 6 ON, grounding the B-side input to the comparator and forcing a comparison to a ZERO state. Conversely, if you want to compare A10 to a high or 1 state, turn switch 8 ON, turn switch 7 OFF and turn switch 6 OFF. The pullup resistor will then pull the B-side comparator input corresponding to A10 high, forcing a comparison equal when A10 goes to a high or 1 state. To ignore the state of A10, turn switch 8 OFF, and turn switches 7 and 6 both ON. Refer to the schematics for an understanding of this.

Monitor Listing - The monitor program listing has been upgraded to remove a few bugs in the original. A new revised listing is available for $15 from JADE.

Schematic - despite customer calls to the contrary, there are only 2 minor errors in the schematic diagram. Error 1: the arrow on the data-out buffers U25 and U37 is shown pointing the wrong way--picky, picky. Error 2: (this

one should cause problems only to those engineering types who attempt to do things from the schematic rather than following the written instructions. On page 2 of the schematic, the labels are reversed on the jumper leading from +12V to pin 19 of the EPROM slot. The +12V side is labeled M, where it should properly be labeled F, and likewise, the EPROM side of the jumper is labeled F where it should correctly be labeled M. All instructions for installing the different types of EPROMS as listed in the OPTIONS section of the manual are correct. Follow the instructions.

Options Section - pages 10 and 11

a) 2708-type EPROM - all instructions are correct.
b) 2716 TI (tri-voltage) type EPROM:
   Step 4, which reads "Set switches 1 and 7 on U33 to ON" applies to revision A and B level boards only--for a C-level revision step 4 should read: "Set switches 6 and 7 on U33 to ON."
c) 2716 single-voltage EPROM:
   Step 7, which reads "Set switches 1 and 7 on U33 to ON" applies to revision A and B level boards only--for a C-level revision board, step 7 should read "Set switches 6 and 7 on U33 to ON."
   Step 8, which reads "Set switch 8 on U33 to ON" should read "Set switch 8 on U33 to OFF. (typographic error.)
d) 2732-type EPROM:
   Step 8, which reads "Set switch 1, 2 and 7 on U33 to ON" applies to revision A and B level boards only--for a C level revision board, step 8 should read: "Set switches 5, 6 and 7 on U33 to ON.
e) Under Option 2--M1 Wait State Option, there is a printer's error in step 2.
   Step 2 should read: "Install a jumper from R to P (not F). Delete step 3.
f) Disregard Option 3 entirely--this ROM is no longer available.

A very careful review of the manual by the JADE Engineering Staff has determined that these are the only existing errors in the Big Z CPU Manual. Future printings should incorporate these changes.

JADE COMPUTER PRODUCTS

ENGINEERING PRODUCT-IMPROVEMENT BULLETIN - CPU-30201 2 December, 1980

BIG Z CPU CARD - ECN 1Ø4

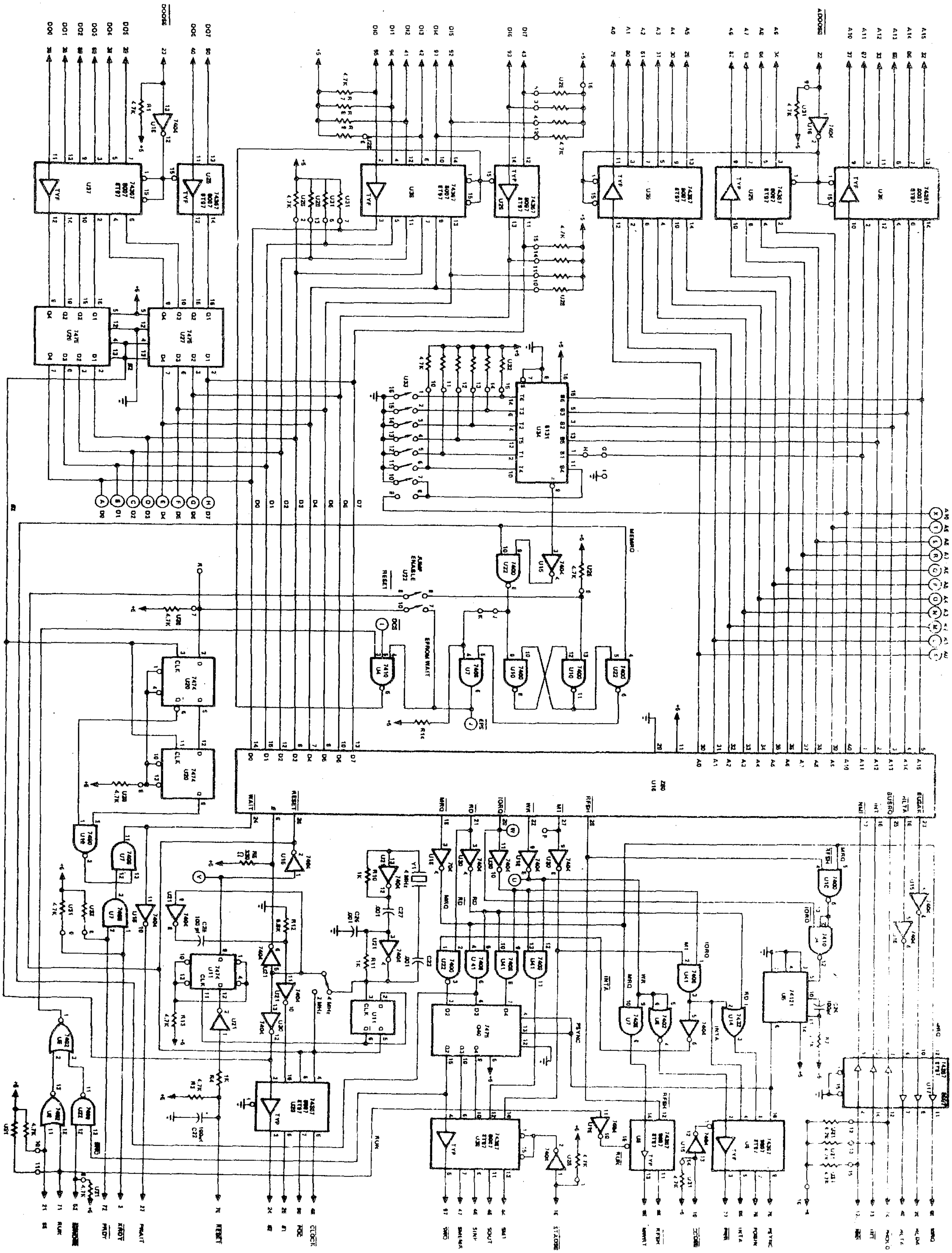
Problem: The CPU will not respond through the serial port at 4 MHz, although it operates reliably at 2 MHz.

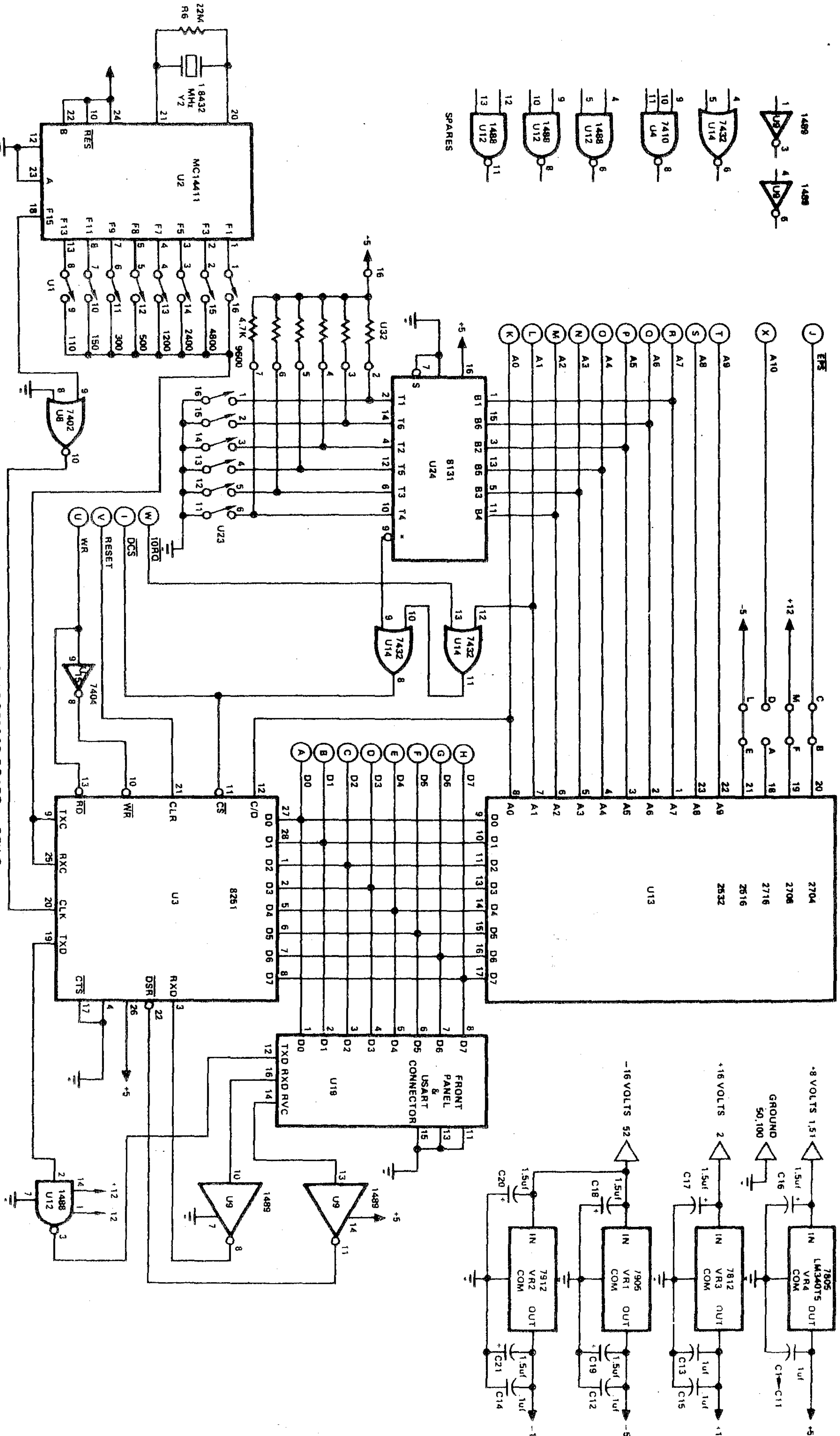
Symptoms: The serial port throws garbage on the screen, or it fails to operate entirely.

Cause: Installation of incorrect USART chip (8251)
We have encountered problems, primarily with customers who have purchased bare boards but with some kit customers as well, with the USART installed at U3. If the USART is not specifically rated to operate at 4 MHz, it usually won't. This holds especially true for some particular brands of 8251 USART. Also, we have seen earlier types of 8251 USART, purchased on the surplus market, installed. The earlier 8251s were very unreliable, especially at higher clock rates, and some brands of 8251s of the newer version are very erratic at high clock rates.

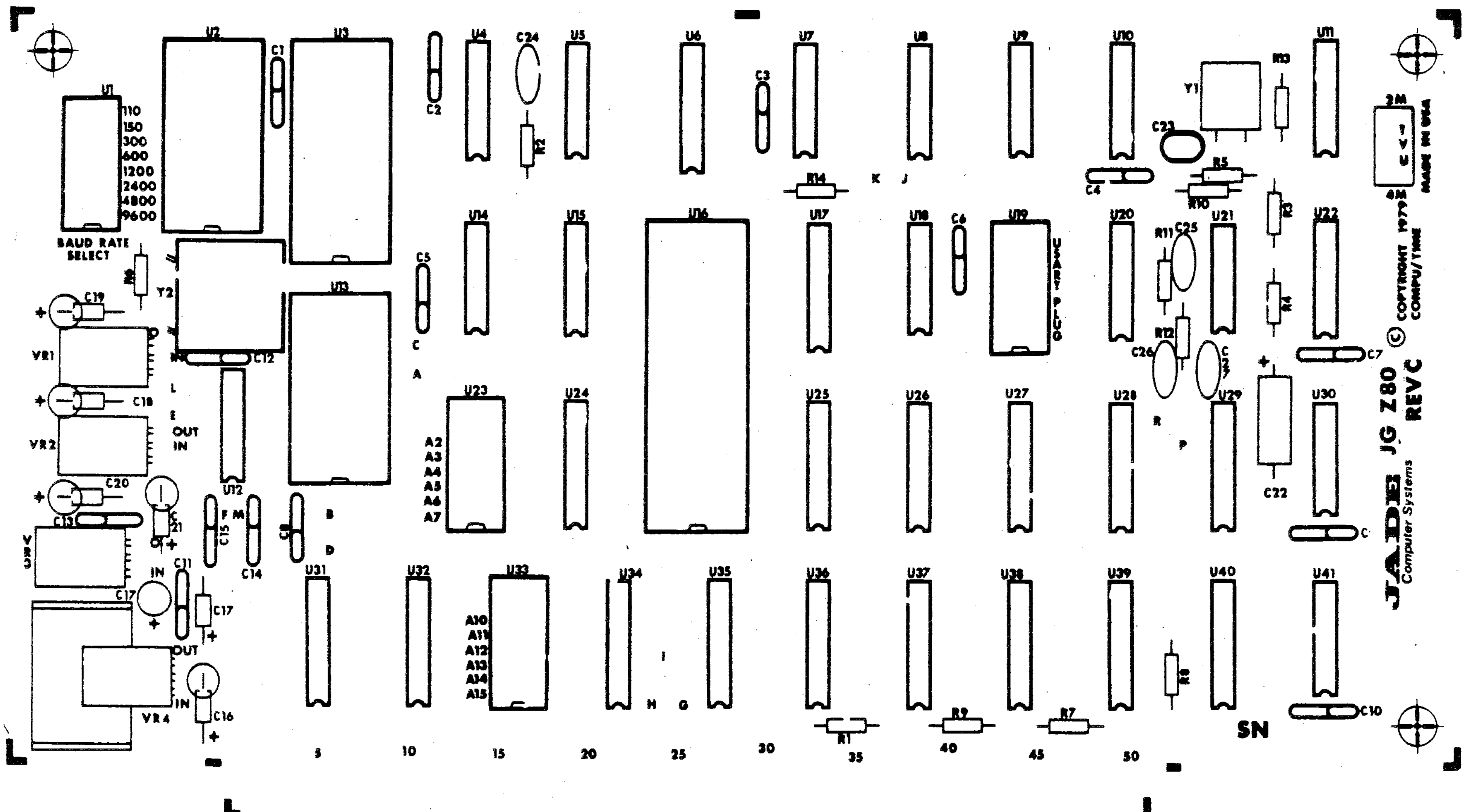
Cure: Install a B-type USART, specifically rated at 4 MHz operation.

Alternate: Install ECN 1Ø5 (USART Wait State).
(The above solution is not the preferable one!)





BIG Z Z80 MICROPROCESSOR BOARD — REV C
PAGE 2 OF 2



PARTS PLACEMENT DIAGRAM