JADE

Computer Products

Serial Parallel Interrupt Controller

4901 West Rosecrans Ave., Hawthorne, Ca. 90250 213-973-7707

SPIO BOARD

PRODUCT SPECIFICATION & USERS MANUAL

INTRODUCTION

The JADE SPIO Serial/Parallel/Interrupt Controller board is an IEEE S-100 standard multi-user communications board designed around the Zilog Z80 peripheral chip line. It features two Z80-SIO Serial I/O controllers, up to four Z80-CTC Counter/Timer chips, and a Z80-PIO Parallel I/O controller chip.

The JADE SPIO board conforms to IEEE S-100 standards, and follows the JADE design concept: providing the most features possible on a single board through density of integration; providing maximum flexibility at minimum cost; featuring low power consumption in relationship to the working throughput capacity of the board.

The SPIO board has been manufactured to the most exacting specifications, using the highest quality material and components conservatively rated for long life. As such, it may be expected to give the user many thousands of hours of useful active service.

If you have purchased the SPIO board as an assembled and tested unit, you should know that it has passed rigorous tests, running in a real-time disk-based environment. Before it goes out the door, every assembled and tested SPIO board must prove itself to our engineering personnel.

Although any component can fail, most ICs die in their infancy, and the burn-in time each SPIO board receives insures that we catch practically all of these infant mortalities.

If you have purchased the SPIO board as a kit, we strongly urge you to read this manual in its entirety before attempting to construct the board. Although there are many ways of assembling a board, if you will follow the assembly directions step-by-step, construction will be easier for you.

The JADE SPIO board is designed to take advantage of multi-user operating systems such as Digital Research MP/M and Phase One Systems OASIS. Due to its inclusion of the Zilog peripheral chips, it is specifically oriented toward an interrupt-driven multi-user, multi-tasking asynchronous operating system.

A microcomputer used in standard systems is primarily I/O bound--that is, it spends a good percentage of its time waiting for some external event to occur, such as a key being pressed at the keyboard. Even on a relatively fast tape interface such as the Tarbell, for instance, a Z80 running at 2 MHz can be processing thousands of instructions between one request for a byte of output and the next. It is easy to see, therefore, that the throughput of the computer (which is an expression of its ability to do work), is severly limited.

Interrupt-driven systems allow the computer to proceed with the execution of its programs. When some peripheral device (a CRT terminal, printer, disk drive, etc.) requires service, it generates an interrupt. The CPU then acknowledges this interrupt, saves its current system state by storing all registers and the current PC location and executes the peripheral's interrupt service routine. When it has accomplished this and the peripheral's request has been satisfied, it returns to the previous task until the same or another peripheral needs service again.

The Z80 and other Zilog-designed CPUs, such as the new Z8000, have the capability to take full advantage of this interrupt scheme. Operating in Interrupt Mode 2, the Z80 can, in effect, very effectively emulate a much larger mainframe machine. Additionally, all Zilog support chips (Z80-CTC, -SIO, -PIO, etc.) have the built-in ability to generate the required interrupt vectors. Under Mode 2, the CPU maintains a table of interrupt vectors in memory--locations which point to the addresses of various peripheral service routines. Upon acknowledgement of the interrupt, the CPU pushes the program counter onto the current stack, then (in effect) calls the service routine pointed to by the contents of the vector address provided by the peripheral chip.

Additionally, all Zilog peripheral chips have a built-in priority scheme, using a daisy-chain structure, which is implemented on the JADE SPIO board. Multiple SPIO boards can be connected into the system, since the Zilog Interrupt Enable In and Interrupt Enable Out signals (IEI/IEO) can be interconnected among many boards. When using multiple boards under the daisy-chain interrupt scheme, it is advisable to connect them in a carry lookahead circuit, or use a wait-state extender.

The JADE SPIO board can be used as a data concentrator, communicating with IBM, DEC or Data General types of mainframe computers via a very fast serial line. The Z80-SIO can be programmed to operate in synchronous, asynchronous or bisynchronous (IBM) modes, and it also supports HDLC/SDLC protocol. All modem control lines have been brought to the outside world through on-board RS232C standard channels, fully bidirectional, and including all handshaking lines.

The Z80-PIO provides two channels of bidirectional 8-bit data flow in a bit-parallel/byte-serial fashion, and each channel is provided with two handshaking lines. As above, these lines are fully buffered to the outside world.

The Z80-CTCs allow the user to provide interval timers, real-time clocks, programmable baud-rate generators for the SIOs, and to monitor the S-100 Interrupt Vector lines to provide a vector to the CPU on the occurrence of an interrupt.

Although the Zilog peripheral chips are quite complex internally--especially the SIOs--and must be programmed, their progamming is relatively easy, and their very complexity provides an enormous range of flexibility in use.

THEORY OF OPERATION 3.0

3.1 Interface to IEEE-standard S-100 Bus (refer to sheet 1 of the schematic)

Interface to the S-100 bus is accomplished as follows:

Data In 0-7 are received from the S-100 bus by bus receiver 4P, a 74LS244 octal non-inverting bus receiver providing Schmidt-trigger inputs. It is tri-stated when the board is not selected by an I/O write operation. The enable line for the bus receiver is provided by the output pin 6 of IC 2H, a 7410 three-input NAND gate.

Data Out 0-7 are transmitted from the internal bidirectional 8-bit board data bus through bus transmitter 4R, a 74LS244 octal non-inverting bus buffer/driver. It is tri-stated when the board is not selected by a read operation. The enable line for the bus output buffer is provided by output pin 8 of IC 4H, a 7410 three-input NAND gate.

Address Lines 0-4 are brought onto the board via bus receiver 4J, a 74LS244 non-inverting bus buffer with Schmidt-trigger inputs. 4J is always enabled, since its enable pin is grounded. A0 and A1 are routed from the outputs of 4J to all CTCs, SIOs and the PIO. A2, A3, and A4 are inputs to IC 4H, a 74LS138 octal demultiplexer circuit. If a full 32-port contiguous address space for the board is not desired, A4 can be re-routed to comparator 4L by wiring point Y to point FF.

Address Lines 5-15 are brought onto the board and input to 8131 comparators 4L and 4M. A5-A7 are hard-wired, whereas A8-A15 form a full 64K I/O address space for advanced processors such as the Z8000.

Vectored Interrupt Lines 0-7 (IEEE specified as pins 4, 5, 6, 7, 8, 9, 10, and 11 respectively on the S100 bus) are brought to the Clock/Trigger inputs of CTCs 0 and 1 at IC locations 3A and 3D. These inputs are pulled up by a 4.7K pullup SIP resistor pack SIP2. Thus, these lines are being constantly monitored by CTCs 0 and 1. When the lines are pulled low the associated CTC (presuming it is programmed with a count of 1 and interrupts are enabled for the particular channel in question), will generate an interrupt request and, upon acknowledgement, will provide an independent vector address (lower 8 bits) to the CPU, under Z80 Mode 2 Interrupt schema.

sM1 on S100 bus pin 44 is input to IC 4F, an inverting bus receiver (74LS240). The output of this inverter, on pin 5, is routed to all Z80 support chips as M1*, and to IC 1N pin 10, a 7408 negative OR gate, which is used to generate a special PIO reset signal.

pWR* on S100 bus pin 77 is input to IC 4F pin 4. IC 4F is a 74LS240 inverting buffer. PWR is routed from pin 16 of IC 4F to pin 3 of IC 2H.

sOUT on S100 bus pin 45 is input to pin 15 of IC 4J, a 74LS244 non-inverting buffer. It is output from pin 5 and is routed to pin 5 of IC 2H and pin 6 of IC 1H.

pDBIN on S100 bus pin 78 is input to pin 13 of IC 4J, a 74LS244 non-inverting buffer. It is output from pin 7 and is routed to pin 10 of IC 2H.

sINP on S100 bus pin 46 is input to pin 11 of IC 4J, a 74LS244 non-inverting buffer. It is output from pin 9 and routed to pin 9 of IC 2H and pin 5 of IC 1H.

IC 24, a 7410, is used to decode an I/O read or write. The first section receives PWR and sOUT and BOARD SELECTED to form DATA OUT ENABLE* which enables data bus output buffer 4P. The second section receives pDBIN and sINP and BOARD SELECTED to form DATA IN ENABLE* which is used to enable data bus input buffer 4R. Additionally, this signal is also routed to all Z80 peripheral chips as the signal RD*.

IEEE-standard S100 signal SLAVE CLEAR* on bus pin 54, POC* on bus pin 99, and RESET* on bus pin 75 are brought to points P, R, and N respectively. From any of these three points, they are jumpered to point S and thence to pin 6 of IC 1R, a 74LS244 non-inverting buffer. The output of this buffer, on pin 14, is used as the board RESET* signal. The input to the inverter is tied to pullup resistor R10, a 4.7K resistor. The internal board RESET* signal is also input to pin 9 of IC 1N, a 7408 negative-input OR gate, where it is ORed with board signal M1* to provide a special PIO RESET* signal.

PHI CLOCK on S100 bus pin 24 is input to pin 8 of IC 1R, a 74LS244 non-inverting buffer, and is output on pin 12 as the internal board phi clock. This clock signal is routed to all Z80 peripheral chips and is used to synchronize these peripheral chips to the Z80 CPU host controller. (see Note 1 below)

SIXTEEN BIT REQUEST and SIXTEEN BIT ACKNOWLEDGE (IEEE S-100 standard signals SXTNRQ* on bus pin 58 and SXTN* on bus pin 60 respectively) are implemented by this board in anticipation of future expansion revisions. SXTNRQ* is input to pin 6 of IC 4F, an inverting buffer (74LS240). This input is normally pulled high by SIP2, a 4.7K pullup resistor. The output, on pin 14 of IC 4F is input to one side of an AND gate at IC 1F. The other input to this gate is the signal BOARD SELECTED. The output of AND gate 1F, on pin 8, is routed to pin 5 of IC 2F, a 7438 open-collector NAND gate. The other input to this NAND gate is either ground (jumper position B) or a pullup resistor R7 (4.7K) when jumper position A is selected. Jumper position B will **disable** any possible Sixteen Bit Acknowledge, and jumper position A will **enable** Sixteen Bit Acknowledge when (a) Sixteen Bit Request is asserted AND (b) the board is selected. Jumper position B is the normal position for this board revision level.

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INT* on S100 bus pin 73, and **NMI*** (Non-Maskable Interrupt) on S100 pin 12 are outputs from the SPIO board. The internal interrupt signal generated by any Z80 peripheral support chip is wire-ORed and brought to inverting buffer 4F (74LS240, pin 2). The output of this buffer, on pin 18, is then NANDed by IC 2F with a high from pullup resistor SIP1 if jumper H is not installed, or with a low by grounding pin 10 if jumper H is installed. The output of this NAND gate, on pin 8, is brought to point V. Point B is pulled toward 5V by SIP1 pullup resistor. Point V can be jumpered to go out on S100 pin 73 (INT*) by jumpering V, or to S100 bus pin 12 (NMI*) by jumpering U. It is strongly suggested that the user should select the V jumper rather than the U jumper, and make full use of the Z80 Mode 2 Interrupt structure.

POWER INPUTS to the board are as follows:

S100 pins 1 and 51 (+8V) are routed to VR1, an LM323 TO3-style regulator. It is bypassed by C5 on the bus side, and by C4 on the board side.

S100 pin 2 (+16V) is routed to VR3, a 340T12 +12V regulator in the TO-220 style. It is bypassed by C8 on the bus side and by C9 on the board side. The +12V DC is routed to all RS232 level shifter ICs on the board.

S100 pin 52 (-16V) is routed to VR2, a 320T12 -12V regulator in the TO-220 style. It is bypassed by C6 on the bus side and by C7 on the board side. THe -12V DC is routed to all RS232 level shifter ICs on the board.

GROUND is provided by S100 pins 50, 100, 20, 70, and 53. **CAUTION.** Under some non-IEEE standard S100 protocols, pin 53 is Sense Switch Disable signal. Grounding this pin can halt the operation of some CPU boards. Additionally, pins 20 and 70 were defined in some systems as Memory Protect and Memory Unprotect respectively. Grounding these pins can interfere with some memory boards. For non-IEEE standard operation, these pins can be cut away from ground on the SPIO board.

This completes the description of the SPIO/S100 bus interface circuitry.

Note 1:

If the CPU board you are using is not IEEE S-100 standard, and S100 pin 24 does not carry the same clock signal as is routed to the Z80, you may have to cut the line between pin 8 of IC 1R and S100 pin 24 and route IC 1R pin 8 to the proper in-phase clock signal. SD Systems boards invert the Z80 clock signal before putting it out onto the S-100 bus on pin 24. At 2.5 MHz (using an SBC100), this will not make a difference; however, with an SBC200 CPU, the clock phase may have to be altered for more reliable operation. All alterations should, of course, be made on the CPU board to bring it up to IEEE S-100 standards.

BOARD ADDRESSING (refer to sheet 1 of the schematic)

Board Addressing is performed by ICs 4L, 4M, and 4H, in conjunction with I/O read decoder and I/O write decoder 2H.

Address Lines A0 and A1 are brought from the bus through bus buffer 4J, and are then routed to all Z80 peripheral chips. A2-A4 are routed to IC 4H, an octal demultiplexer, where they are decoded to form chip select lines 0-7. The enables to IC 4H are as follows: G1 is tied through pullup resistor R21. G2A* is enabled by the equal output of IC 4L which has compared A5-A7 (or A5-A9 for 64K I/O space addressing) with the settings of switch 4K. G2B* is enabled by the equal output of IC 4M, which has compared A10-A15 with the settings of switch 4N, or by ground if jumper W is installed.

For normal 256-port addressing, jumpers BB, DD, and W should be installed. For 64K I/O addressing, install CC, EE, W, KK, LL, AA, HH, JJ, and Z.

NOTE:

With switches 4K and 4N in the ON position, the address bit being compared is being compared to a zero (low) level. With the switch in the OFF position, the comparison is to a high level, since pullup SIPs 3 and 4 are used to pull the comparison inputs to a high level. Closing the switch grounds the comparison inputs. Therefore, to compare to an address bit with a zero level, turn the switch that corresponds to this particulsar address bit to the ON position. On the other hand, turn the switch OFF to compare to a high address bit.

CTCs 0 & 1 (CTC BANK 1) (refer to sheet 1 of the schematic)

Chip Select 0 is routed to select CTC 0 at IC position 3A; therefore, CTC 0 will occupy the first 4 port locations of the I/O map. Similarly, Chip Select 1 is routed to CTC 1 at IC location 3D; therefore, CTC 1 will occupy the second group of 4 I/O port locations.

CTCs 0 & 1 are intended to monitor the 8 vectored interrupt lines of the IEEE S-100 standard bus. Their CLK/TRG* inputs are tied to S100 pins 4 through 11, with the CLK/TRG* input to CTC 0 channel 0 monitoring Vector Interrupt Line 0, CTC 0 channel 1 monitoring Vector Interrupt Line 1, etc. These lines are pulled high by SIP 2 resistor pack.

Assuming the CTCs channels have their interrupts enabled and have been programmed with a count of 1, any signal that pulls one of the S100 Vectored Interrupt lines low will generate an interrupt from the CTC channel to which it is connected. If the Z80 interrupts are enabled and the CPU is in interrupt mode 2, on the receipt of an Interrupt Acknowledge sequence from the CPU, the interrupting CTC will provide a vector on the bus. The counter will also automatically be reset to a count of 1, rearming the CTC channel for the next occurrence of an interrupt on the V1 lines.

CTC 0 occupies the highest priority on the internal board interrupt daisy chain. CTC 1 occupies the second highest priority slot. The ZC/TO outputs of CTCs 0 & 1 are not connected, since CTC Bank 1 was designed as an interrupt vector monitor and/or programmable interval timers, using interrupts to signal a Zero Count/Timeout condition.

CTCs 2 & 3 (CTC BANK 2) (refer to sheet 2 of the schematic)

CTC2 and CTC3, selected by Chip Select 2 and 3 respectively, occupy the third and fourth bank of port locations on the board. These chips may be used to provide programmable baud rates for the SIOs, or as interval timers or real-time clocks. To facilitate this, all Clock/Trigger inputs and all Zero Count/Timeout outputs are brought to wire-wrap pins on the board, where they may be interconnected in any fashion.

OSCILLATOR SECTION (refer to sheet 2 of the schematics)

An on-board oscillator has been provided for the user's convenience. Crystal Y1, a 4.9152 MHz crystal, in conjunction with two sections of IC 1P, (a 74LS240 inverter), R20 and R21, and C1 and C2 capacitors are used to form a highly symmetrical buffered clock of 4.1952 MHz. The output of this clock is routed to IC 4S, a 74LS74, where it is divided by 2. Transistor Q1 and two more sections of inverter 1P, with their associated resistors and capacitors, form a pulse-squaring network which should provide a very clean clock with high symmetry. The oscillator output is routed to wire-wrap pins 7 through 14. The Q* output of IC 4S is routed to wire-wrap pin MM to provide an inverted 2.4576 MHz signal for the user's convenience.

DUAL ONE-SHOTS (refer to sheet 2 of the schematic)

Although an SIO driven by a CTC does not require any pulse stretching, three dual one-shots are provided on the board, with their inputs and outputs being connected to wire-wrap pins for the user's convenience.

RS232C LEVEL SHIFTERS (refer to sheet 2 of the schematic)

The serial data and modem control lines from the SIOs on the board are routed to a series of level shifters, with 75189s at 1A, 1K, 1S, and 1U being used as input buffers and 75188s at 1B, 1D, 1T, and 1V being used as output buffers.

These ICs are used to convert the +12V/-12V RS232 signals to TTL level signals which can be handled by the SIOs. The lines that connect to the board output pins at J1, J2, J4, and J5 are routed in such a way that a mass-terminated cable will properly connect to a DB-25 style connector for RS232C standard pinouts. These cables are available from JADE under part number WCA-2522A.

SIOs (refer to sheet 3 of the schematic)

SIO 0, selected by Chip Select 4, is located at IC position 2A and occupies the fifth bank of I/O port addresses on the board. SIO 1, selected by Chip Select 5, is located at IC position 2S and occupies the sixth bank of I/O port addresses on the board.

For a technical description of the SIO, please refer to the Zilog SIO technical manual.

JADE has selected bonding option 0 for the SIO, to preserve full modem controls. This bonding option ties the transmit and receive clocks for channel B together. The pinout used under this bonding option also allows the user to substitute the less expensive Zilog DART part for asynchronous operation only, and remain pin-to-pin compatible with the SIO part.

Since DMA is not used on the SPIO board, the SIO wait/ready lines for both channels on each chip are tied to IC 1E, a 74LS13 OR gate. Any low will result in a high being output from pin 8 of IC 1E. This is then routed to IC 2F, a 7438 open-collector NAND gate. Since pin 2, the second input to the gate, is tied high through resistor SIP 1, any low on any SIO wait/ready line will cause the output of IC 2F to go low, exerting S100 signal READY on S100 pin 72 false. The function of this circuitry is to synchronize the SIO to the CPU on block I/O moves.

SIO signals SYNC A and SYNC B are routed to J1, J2, J4, and J5. On the channel A ports, they are connected to pins 17. On the channel B ports, they are connected to pins 10. **CAUTION.** These signals, which are ordinarily used to synchronize the SIO, are TTL level signals, NOT RS232C. Do not apply RS232 levels to these pins. They are for the purpose of synchronous communication through the SIO when the SIO is programmed for External Synch mode. Under External Synch mode, these pins are inputs (see SIO technical manual page 4). Synchronization circuitry is not provided on the SPIO board and must be accomplished externally.

PARALLEL CIRCUITRY (refer to sheet 3 of the schematics)

One Z80 PIO has been included on the SPIO board for parallel communication. The PIO is located at IC position 3J and is selected by Chip Select 6; therefore, it occupies the seventh block of I/O port locations on the board. It also occupies the lowest priority slot in the on-board daisy chain circuitry. For a technical description of the PIO, refer to the Zilog PIO Technical Manual. Also refer to the PARALLEL INTERFACE section of this manual.

PARALLEL INTERFACE (refer to sheet 3 of the schematics)

One PIO is provided on the SPIO board. This gives two independent 8-bit I/O ports with two handshake (data transfer) control lines per port. All I/O lines are TTL buffered and have provisions for termination resistors on board. All port lines are brought to a 40-pin connector, where 20 signal lines alternate with 20 ground lines for reduced coupling.

One 14-pin socket is provided per port for resistor dual inline packages so that terminations may be placed on the data lines. A parallel termination is provided for each 8-bit port data line plus the input strobe handshake line. As shown in figure 3A, these termination resistors may be either simple pull-up resistors (port A) or an impedance matching network (port B). The SPIO board is shipped with one 1K pull-up terminator and one 220/330 impedance matching network. In addition to the parallel termination resistors, each ready handshake output line is terminated with a 47 ohm series resistor on the board. This is used to help damp and reduce any reflections on this output line.

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Handshake Line Buffers (STB*, RDY)

Standard TTL Exclusive OR gates (7486) are used to buffer and isolate the handshake lines. Switch options are provided to independently control the polarity or sense of each handshake signal to make the interfacing between the board and peripheral devices more flexible.

Port A Data Buffer

Port A data bus lines are buffered using two quad party line non-inverting transceivers (DS8833), which allows true bidirectional capability. Switch and jumper options allow for fixed INPUT, fixed OUTPUT, or BIDIRECTIONAL under software control. The DS8833 may also be replaced with a DS8835 to change the polarity of the output bits.

The drivers and receivers (designated by D and R respectively in Figure 3A) are enabled by switches and two jumper blocks K and E. The enable lines are listed as REC* for receiver enable and DVR* for driver enable, and the switch and jumper positions will be detailed later under the section entitled Switch and Jumper Option Information.

Port B Data Buffer

Port B data lines are arranged in a manner that allows the user to determine the port direction in increments of 4-bit sections. Sockets are provided for standard 14-pin 7400 series TTL packages. Depending upon the gate type inserted, the port may be dedicated as either IN or OUT. In the output mode, ports may be selected to provide standard or buffered drive, active pullups or open collector, low or high voltage, etc.

Figure 3A shows an arbitrary arrangement whereby four bits are buffered OUT by a 7400 NAND gate while four bits are buffered IN by a 7402 NOR gate. The Data and Control lines of these gates are marked D and C respectively. The control lines are routed to the switch 2K where they are appropriately switched. The control line for a NAND gate will be pulled high by the pullup resistor. The control line for a NOR gate needs to be pulled low, and the polarity of the x control line for an Exclulsive-OR gate will determine the output polarity.

The different types of devices that may be used to buffer Port B are shown below:

IN	OUT
7400 standard drive, inverting (NOR)	7400 standard drive, inverting (NAND)
	7403 open collector, inverting (NAND)
	7408 standard drive, non-inverting (AND)
	7409 open collector, non-inverting (AND)
	7426 open collector, high voltage, inverting (NAND)
	7432 standard drive, non-inverting (OR)
	7437 buffer, inverting (NAND)
	7438 open collector buffer, inverting (NAND)
	7486 standard drive, inverting or non-inverting (EX-OR)

Switch and Jumper Information

Switch 2K and jumpers E and K (a) determine the polarity of the handshake lines by altering the control line of the exclusive-OR buffer 2L; (b) strap the control line on the buffers of Port B for proper AND, NOR, or EX-OR operation, and (c) enable the receiver or driver portions of the Port A buffers.

Jumpers E and K control the bidirectional capability of Port A. The following tables summarize the switch and jumper options for the Parallel Interface.

1) Handshake Lines:	Switch 2K
READY A, INVERTED	Position 1, OPEN
READY A, NON-INVERTED	Position 1, CLOSED
STROBE A, INVERTED	Position 4, OPEN
STROBE A, NON-INVERTED	Position 4, CLOSED
READY B, INVERTED	Position 3, OPEN
READY B, NON—INVERTED	Position 3, CLOSED
STROBE B, INVERTED	Position 5, OPEN
STROBE B, NON-INVERTED	Position 5, CLOSED

2) Buffer Type	Switch 2K
7400, 7403, 7408, 7409, 7426, 7437, 7438	
@ IC 1L	Position 6, OPEN
@ IC 1M	Position 7, OPEN
7402, 7432	
@ 1L	Position 6, CLOSED
@ 1M	Position 7, CLOSED
7486	
@ 1L (INVERTING)	Position 6, OPEN
@ 1M (INVERTING)	Position 7, OPEN
@ 1L (NON-INVERTING)	Position 6, CLOSED
@ 1M (NON-INVERTING)	Position 7, CLOSED

Table 3 Port A Control Lines

	Switch 2K	Jumpers E & K
Port A is INPUT	Position 2, OPEN Position 8 CLOSED	E is OPEN K is OPEN
Port A is OUTPUT	Position 2, CLOSED Position 8, OPEN	E is OPEN K is OPEN
Port A is BIDIRECTIONAL	Position 2, OPEN Position 8, OPEN	E is JUMPERED K is JUMPERED

OPTIONS All option pin holes are marked with white circles.

A/B: three in-line pins located to the right bottom of 1E (near pin 8) – vertical

A (jumper from center pin to top pin) selects pullup resistor R7 as input to 7438 open-collector NAND gate at 2F, causing S100 pin 60 (SXTN*) to be asserted true when SXTNRQ* is asserted and the SPIO board is selected. This position is provided for future expansion use only, and should not be used.

Position B (center pin to bottom pin) grounds pin 4 of IC 2F, holding SXTN* false. *This is the normal position for this jumper* under this revision level.

C/D: three in-line pins located at top right of 1F (between 1F & 1H) - vertical

Position **C** (jumper from center pin to top pin) provides a 5V (high) input to pin 13 of IC 1F (7408). *This is the normal position* if your processor does not have a full 64K port address space.

Position **D** (jumper from center pin to bottom pin) selects the inverted output of comparator DM8131 at 4M, which decodes A10-A15 for extended I/O addressing. Position D would be used with a Z8000 processor providing 64K I/O port addressing.

E: two in-line pins located immediately below IC 1M -- horizontal

Position **E** is discussed under the PIO options section.

F: two in-line pins located at the bottom right of IC 1V -- vertical

F is J6 on the schematic, and provides a method of daisy-chaining multiple boards. It is the output of the daisy chain and should be connected to pin M of additional boards (or through a carry lookahead circuit, as discussed in the pertinent section of this manual).

H/J: four in-line pins located to the left of SIP 1, between SIO-0 and IC 2F - vertical

Jumper **H** (top pin and second pin down) grounds pin 10 of IC 2F. The effect of this jumper is to disable the output of an INT* signal on S100 pin 73 (or S100 pin 73–NMI*). *Non-interrupt driven systems should have this jumper installed.*

Jumper **J** (third pin to bottom pin) connects the output on pin 8 of IC 2F to S100 pin 60 (IEEE SXTN*). This is reserved for future expansion and should not be jumpered under this revision level.

K: two in-line pins located below and between IC 2L and IC 2M - horizontal

Position **K** is discussed under the PIO options section.

L/M: three in-line pins located to the immediate left of IC 3A (CTC0) - vertical

Position **L** provides a pullup through R15 for interrupt enable in to CTC0. Position **M** connects IEI on CTC0 to the bottom pin for interboard connection. To enable multi-board daisy-chained interrupt schemes, connect the F output from board 1 to the M input on board 2.

Position L is the normal position for board 1.

N, P, R, S single pins located immediately below IC 3D (CTC1) for N, P and below and between ICs 3J and 3P (PIO & CTC) for R, S - horizontal

Pin **S** is the reset input to the board. S should be connected to N, P, or R. **N** selects board reset from S100 pin 75 (RESET*). **R** selects board reset from S100 pin 99 (POC*); and **P** selects board reset from S100 pin 54 (SLAVE CLR*). For IEEE S-100 standard, connect S to P. For other types of CPU boards, connect S to N. For CPU boards that do not assert RESET* on a power-on-clear, connect S to R.

T: two in-line pins located between VR2 & VR3 - horizontal

Jumper **T** enables a connection between S100 pin 58 (IEEE SXTNRQ*) and pin 6 of IC 4F. This jumper is used for sixteen-bit response and is not used on this revision level of the SPIO board.

U/V: three in-line pins immediately below IC 4F - horizontal

Position **U** connects the internal SPIO interrupt line to S100 pin 12 (NMI*). Position **V** connects the internal SPIO interrupt line to S100 pin 73 (INT*). Position V is the normal connection.

W/X: three in-line pins located at right bottom of IC 4F - vertical

Position **W** grounds G2B* of IC 4H for 256-port addressing. This is the normal position for CPU boards that do not provide full 64K I/O addressing.

Position **X** connects the = output of IC 4M (comparator DM8131) to G2B* enable of IC 4H. This is the position that should be used if your CPU provides a full 64K I/O address space.

Y: two in-line pins located between ICs 4H and 4J - vertical

Jumper **Y** connects A4 (S100 pin 30) to the #3 input of DM8131 IC 4H through bus receiver 74LS244 at 4J. To enable 32-port addressing, connect jumper Y. To enable 16-port addressing, remove jumper Y.

Z: This is the first vertical two pin in-line group below switch 4K. This jumper, when connected, enables address line 15 to be transmitted to comparator DM8131 at 4M. (Used for 64K I/O addressing only)

AA: Second vertical two pin in-line group below switch 4K. This jumper enables address line 12 to be transmitted to comparator 4M.

BB/CC: Position **BB**, a horizontal three-group below switch 4K, grounds comparator input on IC 4L--the normal position for CPUs that do not provide 64K I/O space. Position **CC**, connecting the rightmost two pins of the horizontal three-group below IC 4L, connects address line A8 to comparator 4L.

DD/EE: second horizontal three-group below 4K and immediately below BB/CC

Position **DD** (leftmost group of two pins) grounds input pin 1 of comparator 4L. Position **EE** (rightmost group of two pins) enables address line A9 to pin 1 of comparator 4L (used in 64K I/O addressing systems only; otherwise connect DD).

FF: between ICs 4J and 4M -- vertical

Position **FF**, when jumpered, grounds input pin 15 of IC 4L. Alternatively, the upper pin of position FF may be jumpered to the upper (?) pin of the Y jumper. This option selects between 32-port addressing and 16-port addressing. For fully implemented SPIO boards, Y and FF should both be jumpered.

HH/JJ/KK/LL: double row of 4 pins below switch 4N – all jumpers are vertical

HH, when jumpered, connects A13 to comparator 4M. Jumper only if 64K I/O space. **JJ** connects A14 to comparator 4M. Above comment applies. **KK** connects A10 to 4M. **LL** connects A11 to 4M.

MM: single pin located between ICs 4R and 4S

MM is the inverted oscillator output, which may be useful for custom applications. It is not ordinarily used.

1,2,3 single in-line row of three pins above IC 4F – horizontal

1 connects to SIO 0 TxRx Clock, Channel B.
2 connects to SIO 0 Tx Clock, Channel A.
3 connects to SIO 0 Rx Clock, Channel A.

4,5,6,7,8,9,10 single in-line row of seven pins above IC 4J – horizontal

4 connects to J1/4 (Channel A External Rx Clock)
5 connects to J1/8 (Channel A External Tx Clock)
6 connects to J2/8 (Channel B External TxRx Clock)
7-10connects to the oscillator buffer output.

11,12,13,14,15,16,17 single in-line row of seven pins above ICs 4L & 4M – horizontal

11-14 connects to the oscillator buffer output.
15 connects to J5/8 (Channel D External TxRx Clock)
16 connects to J4/4 (Channel C External Tx Clock)
17 connects to J4/8 (Channel C External Rx Clock)

SPIO BOARD

18-46: single in-line row of 29 pins above ICs 4P through 4V – horizontal

18 connects to SIO 1 Rx Clock Channel C
19 connects to SIO 1 Tx Clock Channel C
20 connects to SIO 1 TxRx Clock Channel D

21 connects to CTC2 pin 23 (Channel 0 Clock/Trigger input)
22 connects to CTC2 pin 7 (Channel 0 Zero Count/Timeout output)
23 connects to CTC2 pin 22 (Channel 1 Clock/Trigger input)
24 connects to CTC2 pin 8 (Channel 1 Zero Count/Timeout output)
25 connects to CTC2 pin 21 (Channel 2 Clock/Trigger input)
26 connects to CTC2 pin 9 (Channel 2 Zero Count/Timeout output)
27 connects to CTC2 pin 20 (Channel 3 Clock/Trigger input)

28 connects to 123/0 input 1
29 connects to 123/0 output 2
30 connects to 123/0 input 2
31 connects to 123/0 output 1

74LS123 used for pulse stretcher or
retriggerable one-shots–provided as
auxiliary equipment for user requirements

32 connects to CTC2 pin 23 (Channel 0 Clock/Trigger input)
33 connects to CTC2 pin 7 (Channel 0 Zero Count/Timeout output)
34 connects to CTC2 pin 22 (Channel 1 Clock/Trigger input)
35 connects to CTC2 pin 8 (Channel 1 Zero Count/Timeout output)
36 connects to CTC2 pin 21 (Channel 2 Clock/Trigger input)
37 connects to CTC2 pin 9 (Channel 2 Zero Count/Timeout output)
38 connects to CTC2 pin 20 (Channel 3 Clock/Trigger input)

39, 40, 41, 42, follow same pattern as 28-31 except for 123/1

43, 44, 45, 46, follow same pattern as 28-31 except for 123/2

The JADE SPIO board is intended for those people who have had some prior experience with kit building and digital electronics. If you do not fall into this category, it is highly recommended that you find an experienced person to help you with the assembly and checkout of the board.

Although there is nothing sacred in the suggested steps that follow, if you will follow them step-by-step you should find your task much easier. We suggest that you start at a time when you will be able to complete the board. It will help to mark the boxes as you complete each step. Also, it is strongly suggested that you read Appendix B, Construction and Soldering Tips, before proceeding.

1. Make sure you have the tools you will need to assemble this kit. For this board you will need the following: a soldering iron (20 watts maximum, 700° optimum), *Rosin Core* solder (preferably 63/37), diagonal cutters, a small magnifying glass, a screwdriver, and a lead former or a pair of needle-nose pliers.

2. Check the parts received against the parts list. Take special care to corrrectly identify look-alike parts; i.e., resistors, capacitors and diodes. If anything is missing from your kit, please call JADE's Customer Service Department and report the shortage.

3. Read the section of this manual titled "Construction and Soldering Tips". If you have trouble identifying any of the parts, the section titled "Parts Identification" should help you. Do this now before you proceed any further.

CAUTION
USE EYE PROTECTION WHILE SOLDERING OR CUTTING WIRE

4. Install 14-pin sockets at 1A, 1B, 1C, 1D, 1E, 1F, 1H, 1L, 1M,1N, 1S, 1T, 1U, 1V, 2F, 2H, 2L, 2N, 4H, and, 4S. Do *not* solder them in yet.

5. Install 16-pin sockets at 1J, 1K, 2J, 2M, 4T, and 4V. Do *not* install sockets at 2K, a switch will go there. Do NOT solder these sockets in yet.

6. Install 20-pin sockets at 1P, 1S, 4F, 4J, 4P, and 4S. Do *not* solder them in yet.

7. Install 28-pin sockets at 3A, 3D, 3P, and 3T. Do *not* solder them in yet.

8. Install 40-pin sockets at 2A, 2S, and 3J. Do *not* solder them in yet.

9. A handy trick to help you construct your board is to inset all the above sockets into the board first, then place the flat styrofoam cover you received with your kit box firmly against the top of the board. Turn it over, holding the flat styrofoam piece tightly against the board. The IC sockets should now be on the bottom. Press the board down, forcing the sockets into the styrofoam. Now solder alternating corner pins of the IC sockets to hold them in place temporarily (pins 8 and 16 on a 16-pin socket, for instance).

   Now turn the board over and very carefully inspect it to determine that all the IC sockets are down flat against the board. If you find any that are not down flat, melt the solder joints at the corners of the IC socket while pressing it down against the board.

   When you have determined that all the IC sockets are down firmly on the board, turn the board back over and solder all the pins . Make sure that all the pins are sticking through the board.

10.

Install a 3-pin header at A/B (between 1E and 1F). Install a 3-pin header at C/D (between 1F and 1H). Install a 2-pin header at E (below 1M). Install a 2-pin header at F (to the right of 1V). Install a 3-pin header at H/J (at 2E). Install a 2-pin header at K (below and between 2L and 2M). Install a 3-pin header at L/M (to the left of 3A). Install a 2-pin header at N, P (above the TO-220 voltage regulators). Install a 2-pin header at R, S (below 3N). Install a 2-pin header at T (between the 2 TO-220 regulators). Install a 3-pin header at U/V (below 4F). Install a 3-pin header at W/X (to the right of 4F). Install a row of 5 double-row headers at Z, AA, BB, CC, DD, EE (below switch position 4K). Install a 2-pin header at FF (between 4L & 4M). Install a row of 4 double-row headers at HH, JJ, KK, LL (below 4N). Install a single pin header at MM (between 4R & 4S). Install a 3-pin header at 1, 2, 3 (above 4F). Install a 7-pin header at 4-10 (above 4J & 4K). Install a 7-pin header at 11-17 (above 4L & 4M). Install a 29-pin header at 18-46 (running from just above 4P to the right of the board). This completes the header installation.

11.

Install R1 and R2 below J3 47 ohm resistors (yellow, violet, black)

12.

Install R3, R4, R5, R6, R11, R12, R13, R14, 2.2K resistors (red, red, red)

13.

Install R7, R8, R9, R10, R15, and R21 4.7K resistors (yellow, violet, red)

14.

Install R16 and R20 820 ohm resistors (gray, red, brown)

15.

Install R17 1.2K resistor (brown, red, red)

16.

Install R18 220 ohm resistor (red, red, brown)

17.

Install R19 22 ohm resistor (red, red, black)

18.

Install C1 10 picofarad capacitor.

19.

Install C2 0.1 microfarad capacitor.

20.

Install C3 33 picofarad capacitor.

21.

Install C4, C5, C6, C7, C8, and C9 6.8 microfarad tantalum capacitors. **CAUTION:** Observe proper polarity. C6 and C7 are improperly polarized on the silkscreen--install them in reverse of the polarity marked.

22.

Install C10-C27 0.1 microfarad monolithic capacitors where marked. These are not polarized.

23.

If you are using the dual one-shots, install timing components C10-C15 and R22-R27 as required. Consult a TTL data book for the proper values.

24.

Install VR1, LM323 TO-5 voltage regulator, with heat sink.

25.

Install VR2, 7912 TO-220 -12V regulator. Heat sink is not required.

26.

Install VR3, 7812 TO-220 +12V regulator. Heat sink is not required.

27.

Install switches. Place the two 6-position switches at 4K and 4N. Place the 8-position switch at 2K. Position 1 should be oriented toward the top of the board.

28.

Install Q1, 2N3906 transistor.

29.

Install Y1, 4.91520 MHz crystal.

30.

Install SIP 1-4, 3.3K 9-pin resistor pack.

30a.

Install double-row 13-pin angle headers at J1,2,4, & 5. Install 40-pin header at J3.

31.

Check all your solder joints carefully. Inspect the board for cold solder joints or solder bridges, as per instructions in Appendix B.

32.

BEFORE INSTALLING ANY ICs - place the board in your computer and check all the board voltages to make sure that you do not have any power supply shorts on th board. The output pins of VR2 and VR3 will be the pins facing toward the S100 connector. Be careful not to let your probes short the voltage regulator pins together.. If all of the voltages are up to par (plus or minus half a volt), continue to step 33; otherwise, check the board again for shorts. Find the short and correct it before you install any ICs. This is especially important for expensive parts like the Z80 SIO chips.

Since this is a very dense board, the solder pads for the IC sockets are quite small and they are easily destroyed. Also, hairline bridges are relatively easy to form since the traces are thin and run close together. Be quite thorough in your inspection. It is a good idea to clean the board before inspecting it, since many things can hide underneath a rosin residue coverup.

33.

Install the ICs and resistor packs in the locations shown on the Assembly Drawing.

34.

Determine your use of this board and install jumpers and wire-wraps as required to meet your intentions. Do *not* solder to the wire-wrap connectors. Use the jumpers provided for the lettered options, and wire-wrap the numbered options.

35.

Set the switches and options as required. You should now be on the air.

36.

Bare boards are warranted to be free of manufacturing defects; JADE's warranty is limited to replacement of the bare board if, in our opinion, it has been properly assembled. JADE will *not* repair boards built from bare boards. The kit warranty covers all parts supplied by JADE, but does not apply to improperly assembled boards or to parts that have been abused.

Quantity	Jade Part No	Description
1	ICS-3884-4	Z80A SIO/0
1	ICS-3881-4	Z80A PIO
2	ICS-3882-4	Z80A CTC
4	ICT-74LS244	74LS244
2	ICT-74LS240	74LS240
1	ICT-74LS138	74LS138
3	ICT-74LS123	74LS123
1	ICT-74LS74	74LS74
1	ICT-74LS13	74LS13
1	ICT-74LS10	74LS10
4	ICT-74LS08	74LS08
1	ICT-74LS02	74LS02
1	ICT-7486	7486
1	ICT-7438	7438
2	ICT-DM8833N	DM8833
2	ICT-DM8131N	DM8131
4	ICX-1488	1488
5	ICX-1489	1489
1	ICL-LM323K	LM323K
1	ICL-LM340T12	LM340T12
1	ICL-LM320T12	LM320T12
1	SET-2N3909	2N3906
1	IOI-1045B	P.C. Board
1	IOI-1045D	Hardware Manual
1	IOI-1045M	Zilog SIO, PIO, & CTC Manuals
13	CAL-104P500	0.1 uf monolythic ceramic cap
6	CAS-471P500	470 pf 5% silver-mica cap
1	CAS-100P500	10 pf 5% silver-mica cap
1	CAS-100P500	33 pf 5% silver-mica cap
3	CAT-100M250	10 uf 25V dipped tantalum cap
3	CAT-275P300	2 uf 25V dipped tantalum cap
2	RCQ-47.0O	47 ohm 5% ¼W resistor
6	RCQ-4.70K	4.7K 5% ¼W resistor
8	RCQ-2.40K	2.4K 5% ¼W resistor
2	RCQ-820.O	820 ohm 5% ¼W resistor
1	RCQ-220.O	220 ohm 5% ¼W resistor
1	RCQ-22.0O	22 ohm 5% ¼W resistor
4	RCS-08074.70K	8 pin, 7 resistor, 4.7K SIP
1	RCD-16154.70K	16 pin, 15 resistor, 4.7K DIP
1	RCD-14242233T	14 pin, 220/330 DIP terminator
1	SWD-108	8 position DIP switch
2	SWD-106	6 position DIP switch
3	SKL-4001	40 pin lo pro sockets
4	SKL-2801	28 pin lo pro sockets
6	SKL-2001	20 pin lo pro sockets
10	SKL-1601	16 pin lo pro sockets
19	SKL-1401	14 pin lo pro sockets
1	CRY-049	4.9152 MHz crystal
1	HDH-42300	AHAM #423 heat sink (special)
1	HDH-41801	AHAM #418 heat sink
2		Card ejectors w/ pins
4		#6 x ½" bolts w/ nut & lock washer

Single-row male header pins

2	1 x 1
7	1 x 2
6	1 x 3
1	1 x 4
2	1 x 7
1	1 x 29

Double-row male header pins

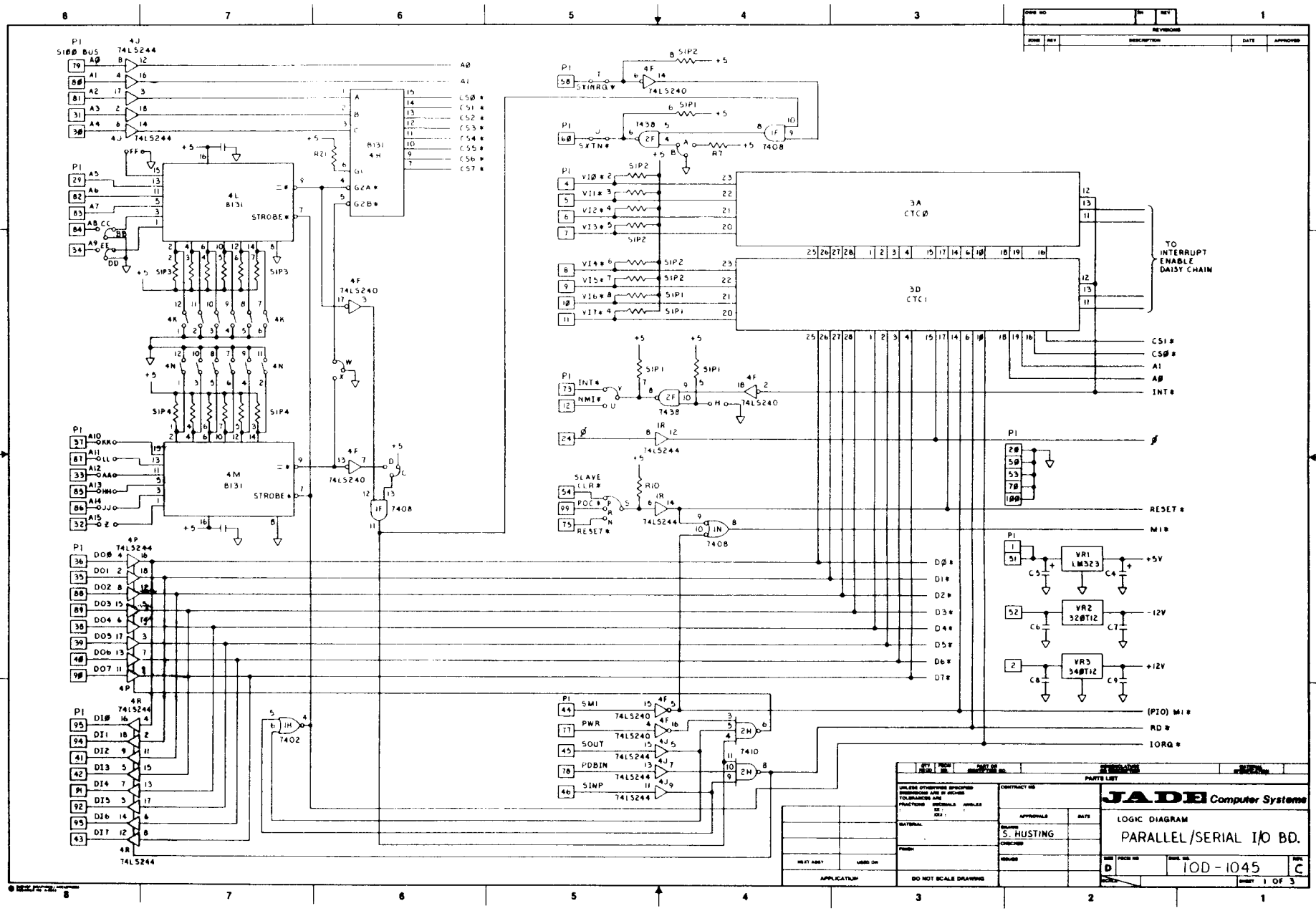
1	2 x 5
1	2 x 4

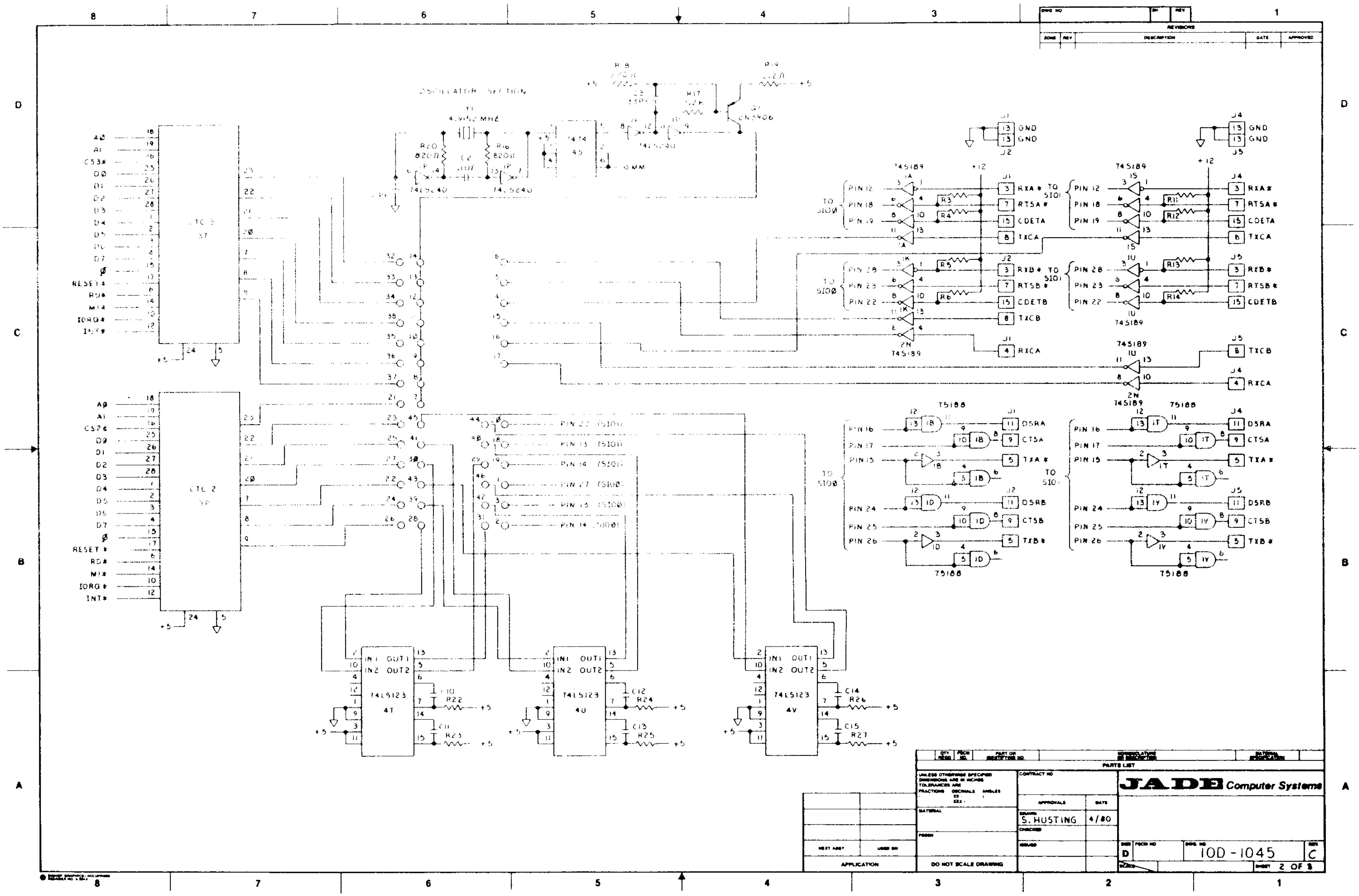
JADE COMPUTER PRODUCTS

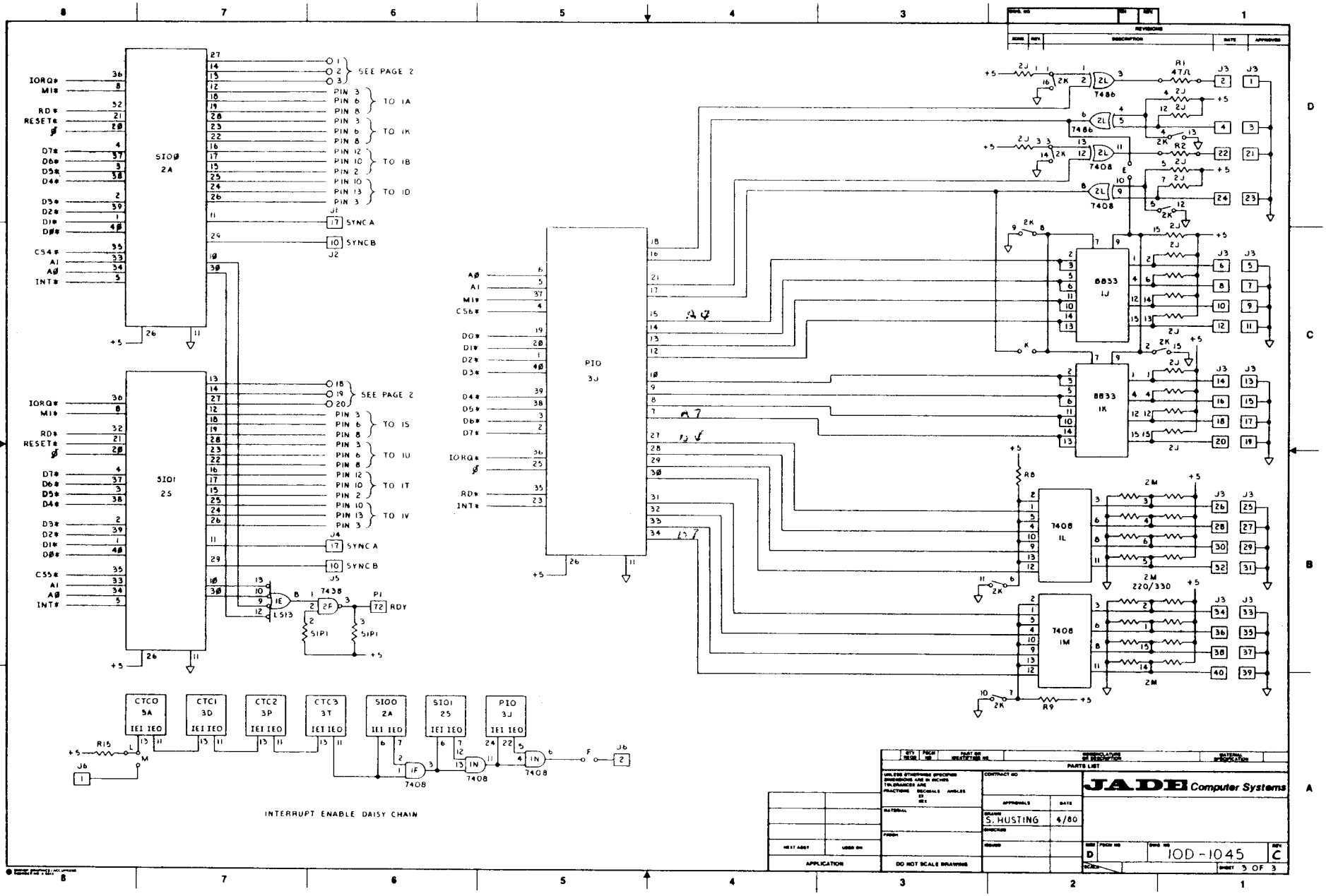
Subject: Engineering Product - Improvement Bulletin #1
Product: Serial Parallel Interrupt Controller Rev C
Date: March 26, 1981

Problem: Preliminary Manual errata. The following list contains corrections to the S.P.I.C. Preliminary Manual. Please check your manual for these corrections.

1. Page 4 - Board Addressing Section. For 64k I/O addressing, the "x" jumper should be installed, in place of the "w" jumper shown.
2. Page 12 - Assembly Step 10. The H/J header (at 2E) is a 4-pin header, not a 3-pin header as shown.
3. Page 12 - Assembly Step 22. This should read, "Install C16-C27 0.1 microfarad monolithic capacitors...", not C10-C27 as shown.
4. Page 13 - Assembly Step 25 & 26. If a heat sink is used, an insulating washer is required on the solder side of the board.
5. Page 13 - Assembly Step 30. This should read, "Install SIP 1-4, 4.7k 8-pin resistor pack".
6. Schematic Revision C - Page 1. IC 4H is marked as an 8131. It is a 74LS138.

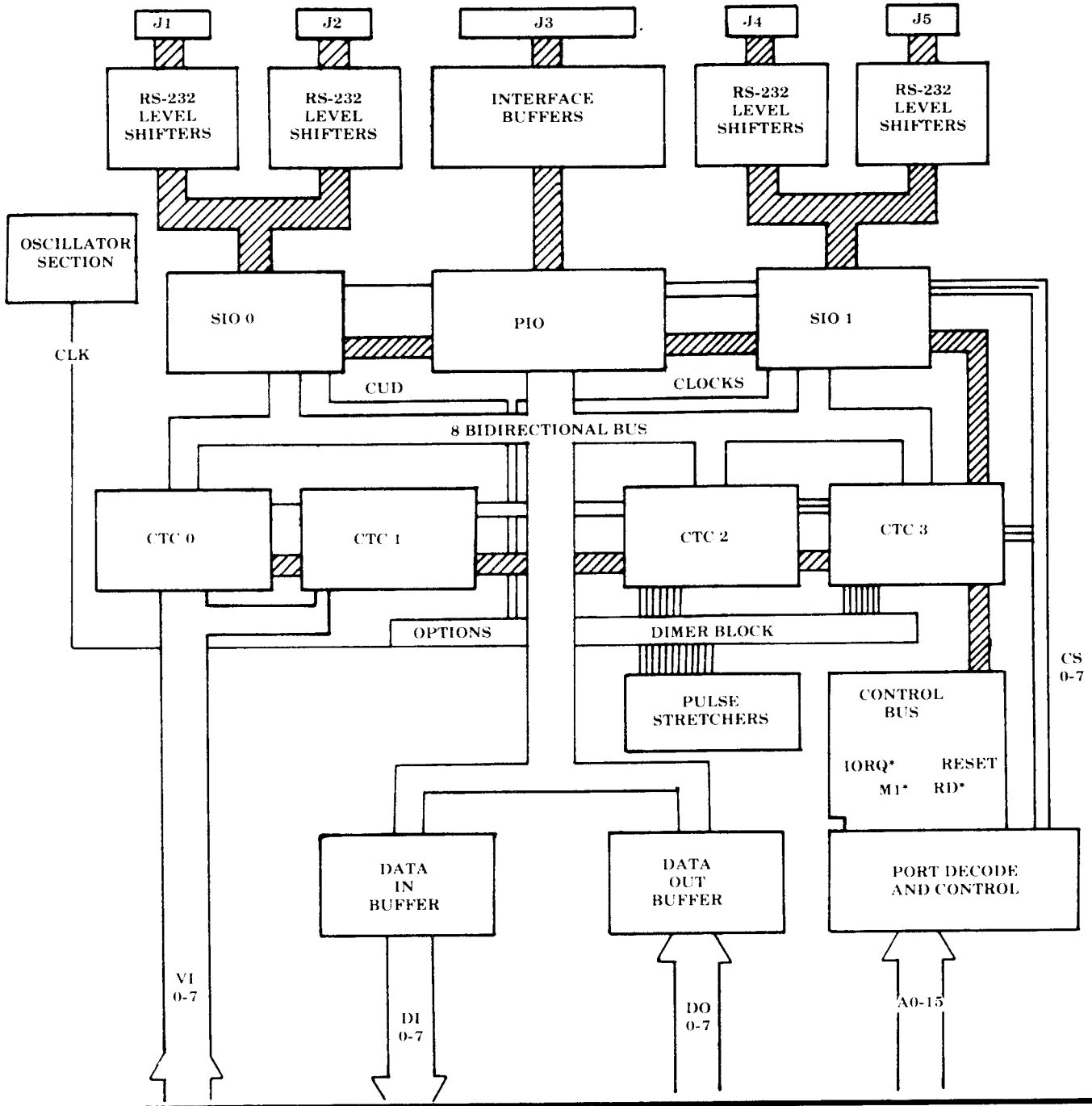

P1
S100 BUS
74LS244
8131
74LS240
7438
7408
7402
7410
3A
CTC0
3D
CTC1
TO INTERRUPT ENABLE DAISY CHAIN
VR1 LM323
VR2 320T12
VR3 340T12
+5V
-12V
+12V
RESET*
M1*
RD*
IORQ*
(PIO) M1*
IOD-1045
JADE Computer Systems
LOGIC DIAGRAM
PARALLEL/SERIAL I/O BD.
S. HUSTING
DO NOT SCALE DRAWING
SHEET 1 OF 3


OSCILLATOR SECTION
4.9152 MHZ
CTC 2
CTC 2
74LS123
74LS123
74LS123
74S189
75188
2N3906
TO SIO0
TO SIO1
JADE Computer Systems
S. HUSTING
4/80
DO NOT SCALE DRAWING
APPLICATION
10D-1045
C
2 OF 3

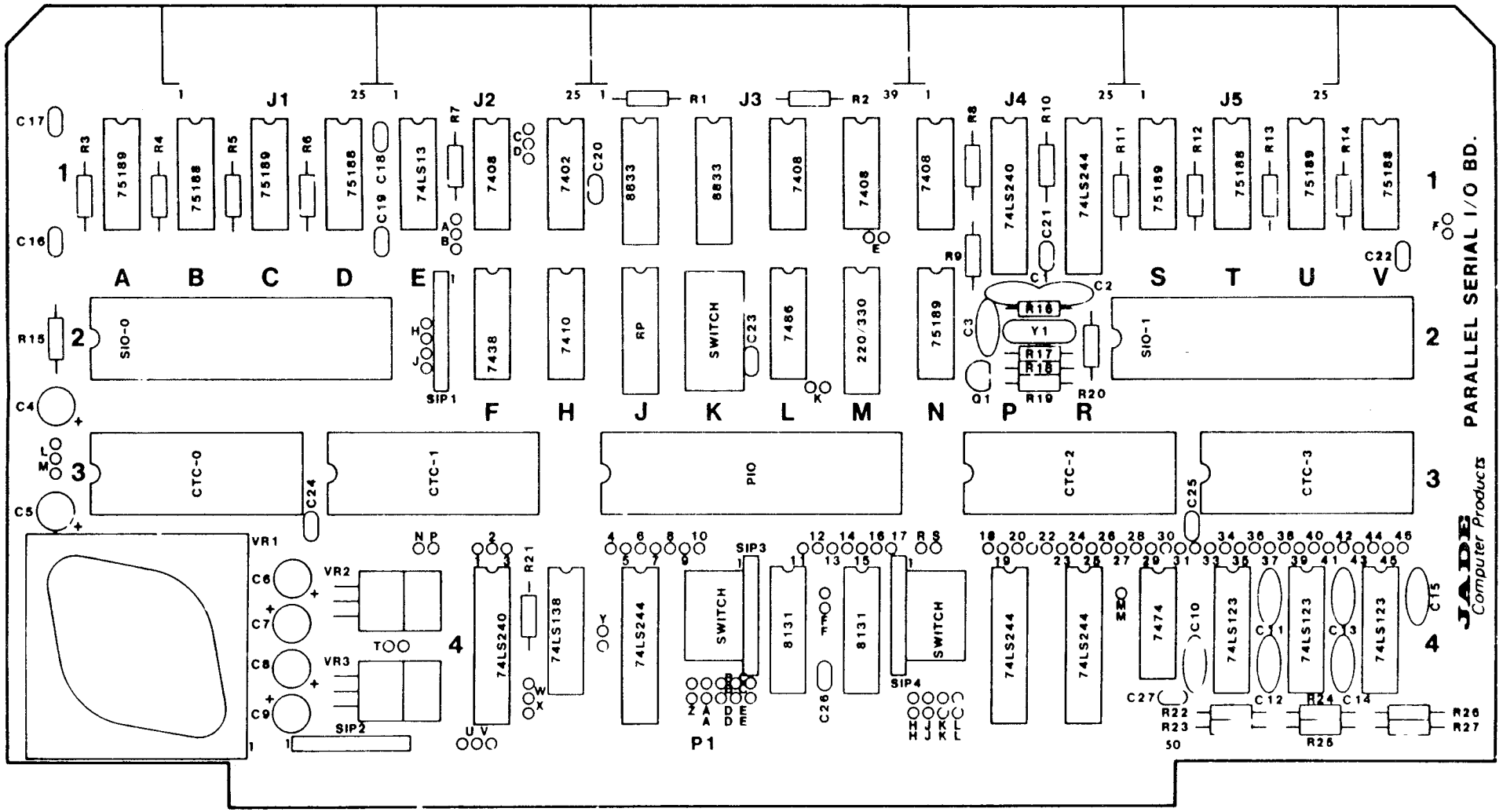

SIO0 2A
SIO1 2S
PIO 3J
SEE PAGE 2
TO 1A
TO 1K
TO 1B
TO 1D
TO 1S
TO 1U
TO 1T
TO 1V
SYNC A
SYNC B
RDY
7438
LS13
CTC0 5A
CTC1 3D
CTC2 3P
CTC3 3T
SIO0 2A
SIO1 2S
PIO 3J
7486
7408
8833 1J
8833 1K
7408 1L
7408 1M
INTERRUPT ENABLE DAISY CHAIN
JADE Computer Systems
S. HUSTING
4/80
10D-1045
SHEET 3 OF 3

REV.	APPLICATION		REVISIONS			
	NEXT ASSY	USED ON	REV.	DESCRIPTION	DATE	APPROVED

DWG. NO.



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	CONTRACT NO.	JADE Computer Systems	
	APPROVALS / DATE	SPIO BLOCK DIAGRAM	
MATERIAL	DRAWN B. Vallee 12-10-80		
FINISH	CHECKED	SIZE A / FSCM NO. / DWG. NO. / REV.	
DO NOT SCALE DRAWING	ISSUED	SCALE / SHEET	



JADE COMPUTER PRODUCTS
101-1045C
SHEET 4 OF 5