

ENCYCLOPEDIA PROCESSOR TECHNICA

The complete guide to
Processor Technology Corporation's Products

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Volume 1 -- History and basic operation of the Sol. Preface to the Encyclopedia Processor Technica. Includes the semi-technical Sol Users Manual that came with later Sols, functions of the Sol's buttons and switches, hookups to common printers, cassette operations, use as a dumb terminal, minor troubleshooting. Also a historical scrapbook of Processor Technology Corporation and of the Sol: reprints of articles which describe the way the Sol came to be, copies of old advertising, product catalogs, price lists, dealer list, historical accounts from insiders, Personal Computer Retailer newsletter for dealers, all issues of Access newsletter.

Volume 2 -- Technical manual on the Sol computer. It incorporates material from the big black looseleaf notebook that came with early Sol's, plus material taken from the PTC Sol Service Manual, from Access (PTC's newsletter to users), from Proteus, and from other sources. Covers topics such as: theory of operation, schematics, assembly drawings, parts lists, troubleshooting, testing, hardware updating (rev D to rev R), constructing and using the ParaSol Debugger, input/output hookups, timing diagrams, testpoint voltages, hardware interfacing, user-originated modifications.

Volume 3 -- Programming the Sol. Solos user's manual, the 8080 microprocessor from the programmer's view, the 8080 instruction set, assembly language programming, communications interface programs, the Sol system architecture.

Volume 4 -- PTC Programming Manuals.

Volume 5 -- ALS-8, Assembly Language System. Including the user's manual, users' group newsletters, internal routines.

Volume 6 -- PTC memory boards. From the 2KRO ROM board to the 64KRA-1 RAM board. Schematics, assembly drawings, theory of operation, switch settings, engineering changes, upgrades, troubleshooting, ROM listings, parts lists, etc.

Volume 7 -- PTC input/output interfaces. The 3P+S, the CUTS board, the VDM.

Volume 8 -- Helios Disk System Manual. Installation, testing, light maintenance, theory of operation, drawings.

Volume 9 -- Helios Service Manual. Sol/Helios System troubleshooting. Updates, Controller/formatter troubleshooting, PerSci Drive Maintenance.

Volume 10 -- Programming the Helios disk system. Users' manuals on the following: PTDOS 1.5, Extended Disk BASIC, Optional Precision BASIC, Level I Business BASIC (Demo version), Disk Basic/5.

Volume 11 -- SolPrinters and Hytype interface.

Volume 12 -- Sol a la carte. Using the Sol with other equipment, such as interfacing to other disks, modifying memory boards to work properly in Sol, customizations for the Sol with CP/M, NorthStar, Micropolis, etc. (This volume to be published at a later date.)

ENCYCLOPEDIA PROCESSOR TECHNICA

Foreword to the Encyclopedia

by Stanley M. Sokolow, B.A., D.D.S.

Since August, 1977, I have been the de facto Executive Director of the organization for owners of Processor Technology Corporation Sol computers. Originally, we called ourselves "Solus" (pronounced like "solice"), a name coined by Bill Burns, the founder of the group. The name represented "SOL Users Society," but it really had a double meaning since the early Sol users actually needed a lot of solice to cope with Processor Technology Corporation's growing pains.

Later, I changed the name to "Proteus" (for PROCESSOR Technology Users) to indicate a broader scope, covering all of the Processor Technology product line, not just the Sol. Proteus has continued to be the primary focal point for communication among Sol owners, mainly through our newsletter.

This Encyclopedia represents the accumulation of information which Proteus has been able to gather on Processor Technology products. It is envisioned as a living resource which will be updated as new information becomes available. Any reader who has information or literature on any Processor Technology hardware or software product is requested to submit this material to Proteus for inclusion into future editions of the Encyclopedia and its supplements. (The original documents will be returned to you if requested.)

I also urge all owners of Sol computers to subscribe to our newsletter, called Proteus News. This has been an invaluable source of practical information about the Sol and other Processor Technology products. Our hope is that the organization will continue to keep the Sol a viable computer as long as there is interest in it, and even far into the future when it is an antique.

Proteus's address is Proteus, c/o Stanley M. Sokolow, 1690 Woodside Road, Suite 219, Redwood City, California 94061.

EXPLANATION OF PAGE NUMBERING

Since the material in the Encyclopedia has come from many

sources, the original page numbering is out of sequence. Instead, we refer to new page numbers at the top of each page. They have this form:

5 EPT 7 - 123

where "EPT" means Encyclopedia Processor Technica, the number before it means the volume number, the number following is the chapter number, and the number after the hyphen is the new page number. We left the old page numbers intact so that references to them in the body of the text could be found.

ENCYCLOPEDIA PROCESSOR TECHNICA

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DISCLAIMER

The information presented in this and other volumes of the Encyclopedia Processor Technica is published in the interest of the owners of Processor Technology Corporation products. The publisher assumes no liability for the accuracy of the content presented, although we have done our reasonable best to include only accurate information. It is assumed that the reader will use due care in utilizing the information, especially with regard to suggested modifications to products.



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Helios Service Manual

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NOTE

The third section is the system as a whole, which includes a chart of common system problems and a brief outline of the division of responsibility within the system. The primary emphasis will be on the Sol System III and Sol System IV.

SECTION 3

SYSTEM TROUBLE-SHOOTING AND DIAGNOSTICS

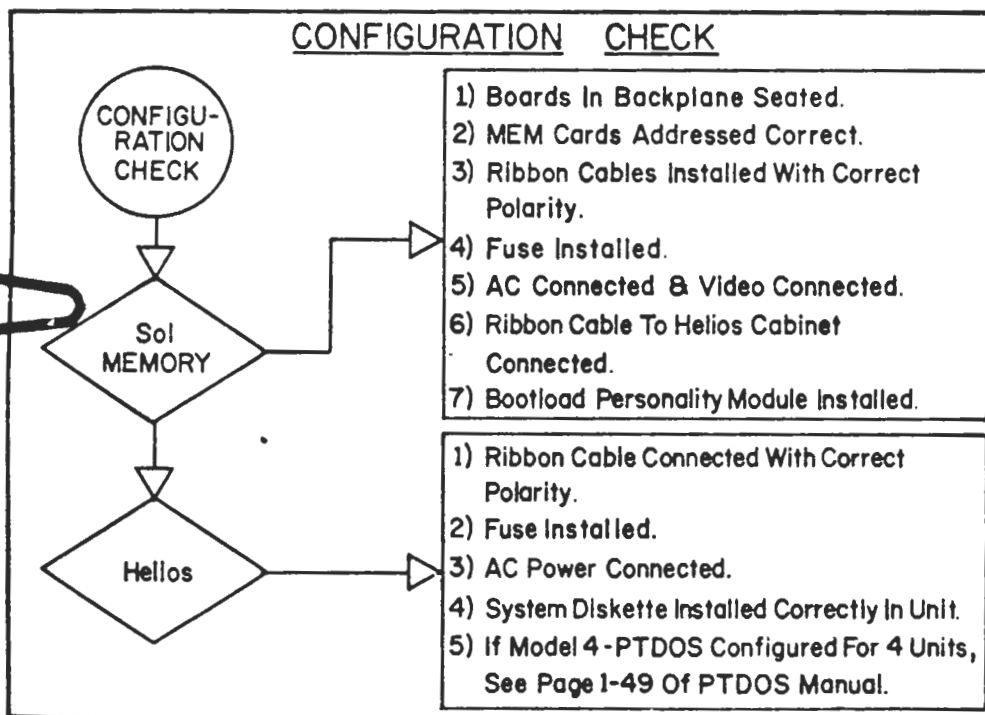
(Supplement 733007)

3.1 ORIENTATION

Up to now we have been dealing with the integral parts of the Sol System III only, it is time we tie the whole system together and examine in detail the steps from the time the user types the word "BOOT" until the time when the PTDOS prompt occurs on the screen.

3.2 BASIC SYSTEM TROUBLE-SHOOTING PROCEDURE

- 1) Be sure you have run SOLT as in Section 2, "Sol Trouble-shooting."
- 2) Power down the Sol and install the memory modules.
- 3) Load and run the MEMORY test. Memory tests are available on EPROM's.
- 4) Power down the Sol and install the formatter and controller PCB's.
- 5) Install all cables. Be sure that when the cover is placed on the Sol, the Helios cable is not pulled from its socket.
- 6) Complete the Configuration check as shown in the box below.



7) Run the DOST test. 9 EPT 1 - 4

NOTE

If Helios does not pass the DOST test, do not proceed any further until the problem has been corrected!

8) Follow diagnostic procedure as shown in the flowchart, Fig. 3-1, "System Diagnostic Procedure."

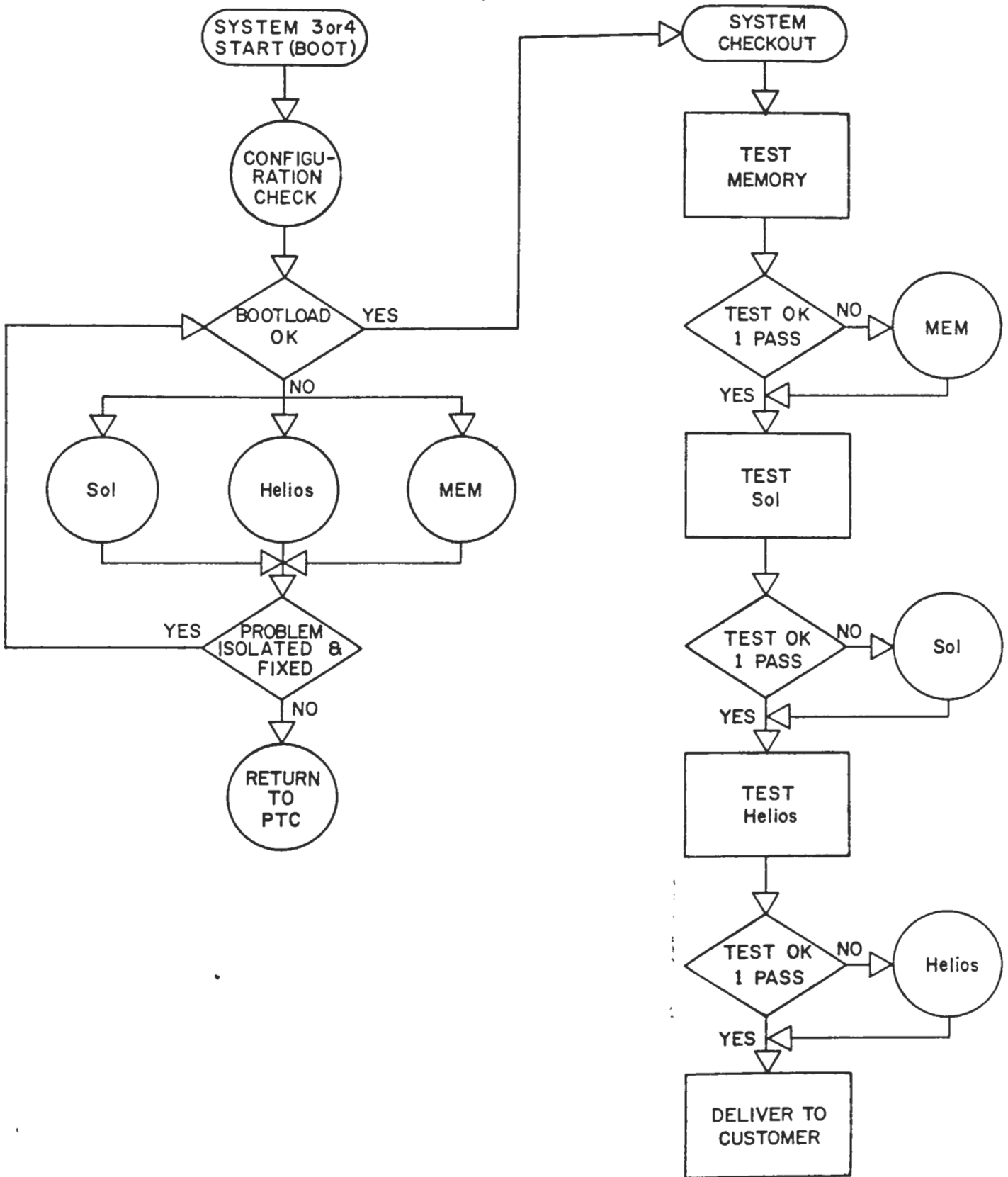


Fig. 3-1. Flowchart, System Diagnostic Procedure

3.3 BACKGROUND ON DMA RELATED TO SYSTEM TROUBLE-SHOOTING

By now the word DMA is as common to the computer enthusiast as is the concept of mass storage on a floppy disk system, yet few words have actually been written on what it really entails.

By DMA, we refer to the process during which the central processing unit is put on hold while some external device, in our case a disk controller, proceeds to read and write into memory and transfer to or from diskette.

Easy enough to understand and probably as conventional a definition as may be found anywhere, but it is the details of this process we are concerned about. It is these details that will make our job of trouble-shooting the system easier.

3.3.1 Tracing the DMA Process

The very first part of the DMA process occurs when the user types in the word, "BOOT," and SOLOS responds. What is it that the PROM BOC program must do? We have already talked at length about the 8 ports assigned to the HELIOS II system, and it is through these ports that the Boot program must communicate between the Sol (and its heart, the 8080) and the disk and its heart, the controller.

The first thing we must do is tell the controller we want to load the heads for a read operation and restore the drive head to track 0 where the Resident and Bootstrap loader reside. Since, before we can read in this data, we must first read a header, we now set up to read a header by outputting to port F1. Next we input status (Port F0) and see first if the drive itself is ready, then loop until an Index hole is present. At this point we wait to find sector 0 where the Bootstrap loader resides. If a successful read of header has occurred, SREADY will go high and we will start looking for the data portion of sector 0.

Now that data is to be read, the controller must be told how much data there should be and what to do with it when it is read. Outputting to the Transfer Length Counter (Ports F3 and F4) tells the controller to transfer 340H bytes (the size of the Bootstrap loader), and outputting a DMA address (Port F5 and F6) tells the controller to DMA this data into memory location beginning at 0000H to 340H. We now know where the data should come from (Track 0, Sector 0), where it should go (Memory located at 0000) and how much must be transferred (340H). All that remains is to tell the Transfer Command Register (Port F1) to go ahead and read it.

If you think DMA has already occurred, start at the beginning and look closer. All we have done so far is move around some instructions and data with the 8080 to tell the controller exactly what to do. The key to the whole process is to ask the questions: Where from?, How much?, Where to? and When? It is not until all the questions are answered that the DMA process can begin.

As the FIFOs on the Controller are filling, and when all the requirements for DMA have been fulfilled, we issue a HOLD signal to the Sol. Aside from the initial operating of instructions from the

BOOT prom, the only other requirement of the Sol is to respond to this signal. This is a handy way of testing to see if the Sol might be the problem in a down system. That is, look to see if Pin 26 (PHLDA) will go high if Pin 74 (PHOLD) is grounded. These pins are on the S-100 bus and can be checked without any boards in the Sol. Any problem here should be investigated further.

Now that a PHOLDA (Processor hold acknowledged) has been received, it is up to the Controller to take control of the Bus (See Controller/Formatter Section of the Helios II Technical Manual (Helios II Disk Memory System, Literature Kit Number 730009) for the lurid details. Since DISKT has already been run successfully, (see 3.4, "Symptoms and Indicated Checkout") we know that the Controller can take control of the bus and write to memory. Then, it is simply a matter of transferring on the average of 12 bytes at a time (about 20 usec at a time) the total of 340H bytes. Since the processor is only holding 20 microseconds, and the bus is free for 360 microseconds (roughly), then the process of the initial DMA requires only about 40 ms (rougher still).

Since the 340 bytes have been read, the Transfer Length Counter should be at zero, SREADY should again be high, and the CRC bytes should match. If there is a CRC error reported, the process is repeated from the beginning. If, when "Boot" is entered, the heads engage and the DOS is never loaded, yet the heads remain loaded, this is a possible problem (one of many).

Since SOLOS offers us the ability to examine memory locations, here are some hints from that may be gleaned from a memory dump.

NOTE

AT THIS POINT, THE TECHNICIAN SHOULD HAVE A KNOWN GOOD PTDOS SYSTEM DISK WITH EVERYTHING REMOVED FROM THE FILE START.UP EXCEPT THE "SETIN #0" COMMAND. (Using the editor, remove "SYST" and the "\$PR" commands from START.UP.) AN ALTERNATIVE IS TO RECONFIGURE YOUR DISKETTE AND SWITCH THE "VERBOSE" SWITCH TO OFF.

TYPE: EN 0000 <CR>

SOLOS RESPONDS: :

TYPE: 33 C7/ <CR>

SOLOS RESPONDS: >

TYPE: EX 0 <CR>

TYPE: DUMP 0000 350 <CR>

WHAT SHOULD BE THERE: All the memory should read 00

NOTE

If, at this point, the memory dump produces all FFs the memory board has lost its 5 Volt supply or there is no memory addressed at that location. If, on the other hand, the memory reads anything but all zeroes, the board cannot execute code, or the Sol cannot enter to that board.

TYPE: BOOT <CR>

(Assuming the unit will "Boot," the PTDOS prompt will return.)

TYPE: UPPER CASE and REPEAT simultaneously (system reset).

TYPE: DU 0000 350

At this point the bootload program is in memory and can be examined the use of this dump command. Note that there has been a transfer of exactly 340 bytes, and, hence, the bootload program has been successfully loaded. (Refer to Table 3-1, "Hexidecimal Code of Bootload Program.")

Knowing exactly what should be in memory and comparing it to what is actually there when a system cannot load the DOS can be extremely helpful. Let's examine some of the things that may result in memory from an unsuccessful transfer.

Although there is no way to determine what will be in memory from an unsuccessful transfer, there are certain trends to be noted. For instance, if we were to insert a diskette on which track 0 was blank the pattern in memory will likely be a 00 39 repeating pattern, as the head immediately unloads.

If, on the other hand, we were to use a diskette with a crashed bootload program at track 0 sector 0, we could expect to see perhaps 16 bytes or so of random code and the rest of memory untouched.

Suppose, however, the bootload program was OK, but the resident had been crashed. In this case, we would very likely find the bootload program had loaded but could not find a valid header or CRC did not check, and thus the heads would remain loaded retrying to find the valid header/data. Thus, we would expect to see valid code in memory.

The point to be emphasized is not to predict what will occur in the case of faulty hardware, but to use the knowledge of what should be there as a start. One of the hardest parts of troubleshooting the system as a whole is to determine which element is at fault. The section immediately following uses the above procedure as well as field experience to help in your isolation routine without having a complete working system to swap boards with. One must, however, have at least two known good system disks configured as explained earlier.

Also bear in mind that the only DMA is to the memory at 0 for the initial bootload program and then to a buffer at the 9000 region. For this reason suspecting that a memory board won't do DMA properly and residing at 2000 - 6FFF, or any permutation of this, is keeping the system from loading most likely is the wrong approach.

Table 3-1. Hexadecimal Code of Bootload Program

The following code should be found in memory locations 0000 - 0340 after PTDOS has been booted provided the "Verbose Switch" is off.

0000	2D	23	24	20	F3	31	9C	22	CD	7E	21	11	35	22	21	A5
0010	22	CD	2A	20	AF	32	B3	22	CD	47	22	21	AB	22	11	3E
0020	20	CD	2A	20	CD	47	33	C3	C3	BC	26	33	1A	77	23	13
0030	25	C2	2C	20	C9	23	22	FF	2F	24	23	22	A2	20	23	31
0040	FF	2F	24	23	21	B2	20	3E	23	F3	CD	23	21	CD	F3	23
0050	CD	24	21	CD	2B	21	DA	B3	22	C2	AD	23	3A	B4	22	B3
0060	C2	E9	22	21	AD	22	3A	BD	22	3E	C2	71	22	23	23	3A
0070	EA	22	3E	C2	71	22	3A	C3	3E	47	3A	BC	22	B3	C2	71
0080	22	2A	A4	22	EB	2A	B1	22	3A	A6	22	CD	41	31	C3	9B
0090	23	11	A6	22	1B	7A	B3	C2	94	22	C9	CD	37	21	C2	AD
00A0	22	DB	F2	E6	13	C3	DB	F2	E6	2C	CA	A1	22	CD	B9	22
00B0	C3	52	22	CD	52	21	C3	52	22	3E	FF	D3	F1	CD	5F	22
00C0	3A	AC	22	4F	3A	9F	22	FE	1E	D2	71	22	3C	22	9F	22
00D0	C9	79	D6	22	F2	DB	23	AF	4F	C3	9E	21	79	C6	22	FE
00E0	4D	DA	DB	22	3E	4C	C3	DB	22	3A	A2	22	3C	22	A2	22
00F0	FE	19	D2	71	22	C3	53	23	AF	22	9F	22	2F	22	A1	22
0100	32	A2	22	C9	AF	22	A2	22	C3	97	21	CD	5F	22	21	B4
0110	22	11	2D	22	3E	27	CD	41	31	CD	37	21	C2	21	AB	22
0120	46	23	4E	DB	F2	E6	2E	C2	DB	F2	E6	12	CA	23	21	3A
0130	B5	22	B9	37	C2	AF	C2	DB	F2	E6	2F	CA	37	21	E6	2C
0140	C9	F5	7D	D3	F5	7C	D3	F6	7B	D3	F3	7A	D3	F4	F1	D3
0150	F1	C9	CD	5F	22	3A	AC	22	4F	3A	A2	22	3C	22	A2	2C
0160	3D	CA	73	21	FA	22	21	FE	23	D2	71	22	2F	DA	D1	22
0170	C3	DC	22	3A	B5	22	FE	4D	22	9E	22	DA	27	21	AF	22
0180	9D	22	3A	9D	22	CD	1D	22	D3	F7	2B	2F	D3	F7	AF	22
0190	B9	22	AF	77	C3	C5	21	CD	67	22	3A	AC	22	4F	3A	9E
01A0	22	91	C3	F3	F2	B2	21	2F	3C	47	3A	9C	22	E6	FD	C3
01B0	B6	21	47	3A	9C	22	D3	F7	E6	FE	D3	F7	23	C2	3A	21
01C0	79	CD	29	22	71	DB	F2	E6	42	C2	C5	21	DB	F2	27	DA
01D0	CC	21	C9	22	A6	22	AF	22	A3	22	CD	22	22	3A	B3	22
01E0	CD	1D	22	32	9C	22	D3	F7	D3	F5	CD	67	22	3A	B3	22
01F0	E6	27	21	9D	22	B2	77	CA	22	22	CD	C3	21	2E	11	CD
0200	91	22	CD	29	22	32	9E	22	C9	22	9E	22	21	A7	22	3A
0210	9D	22	FE	23	D2	14	22	B7	1F	35	6F	7E	C9	E6	27	21
0220	32	DB	2F	27	D2	23	22	41	E6	26	27	2F	E6	2C	B2	F6
0230	23	C9	2A	AD	22	2E	22	11	22	FF	19	2C	7C	B5	CA	4C
0240	22	7C	B7	FA	4C	22	11	C2	FE	C3	3A	22	2A	AD	22	22
0250	C9	22	22	A4	22	3A	C3	22	E6	32	B1	22	C3	22	C9	DB
0260	F2	E6	22	CA	5F	22	C9	DB	F2	E6	22	C3	D3	F5	C3	67
0270	22	C3	71	22	24	22	76	76	76	76	76	76	76	76	76	76
0280	76	76	76	76	76	76	76	76	76	76	76	76	76	76	76	76
0290	76	76	76	76	22	27	56	23	9E	22	27	22	DF	22	21	22
02A0	22	FF	FF	22	FF	2F	23	21	76	76	76	22	21	FF	2F	24
02B0	22	21	B2	22	23	21	FF	3F	33	22	24	22	2D	FF	2F	22
02C0	FF	76	76	76	76	76	76	2D	FF	2F	76	76	76	76	76	76
02D0	76	76	76	76	76	76	76	76	76	76	76	76	76	76	76	76
02E0	76	76	76	76	76	76	76	76	76	76	76	76	76	76	76	76
02F0	76	76	76	76	76	76	76	76	76	76	76	76	76	76	76	76
0300	76	76	76	76	76	76	76	76	76	76	76	76	76	76	76	76
0310	76	76	76	76	76	76	76	76	76	76	76	76	76	76	76	76
0320	76	76	76	76	76	76	76	76	76	76	76	76	76	76	76	76
0330	2B	24	22	22	22	22	22	22	22	22	22	22	22	22	22	22
0340	22															

3.4 SYSTEM III TROUBLE-SHOOTING GUIDE (Symptoms and Indicated Checkouts)

NOTE

The first three symptoms have to do with very general types of problems with the system and is meant as a basic check to see if the system is set up correctly. The symptoms that follow are more specific and deal with problems in one or more of the components.

SYMPTOMS: Garbage (random characters) on screen or a pattern of nulls and nines. No SOLOS prompt, ">".

- CHECK:**
- 1) Personality module installed correctly?
 - 2) Phantom jumper from F to G on the SOL PCB installed correctly?
 - 3) Does unit pass SOLT and Para-Sol?
 - 4) Remove all boards from backplane to see if one of the boards is crashing the bus.
 - 5) Check: Address lines, Command/Control lines, Data lines, Status lines for possible shorts or opens.
 - 6) Is controller board attempting to hold the processor?
Is pin 26 (HOLD ACK) high?
 - 7) Power to the Sol backplane?
 - 8) Is the 8080 running? If so, PSYNC (pin 76 on the S-100 bus should be pulsing).

SYMPTOM: System fails to pass the DISKT program or gets errors consistently.

- CHECK:**
- 1) Has the memory being used (16K beginning at location 0) passed the memory test?
 - 2) Has the Sol passed the SOLT test?
 - 3) Are the 8080 clocks (PHASE 1 AND PHASE 2) up to spec.
. Refer to 8080 manual if in doubt.
 - 4) Is the Sol Revision E or greater, and if it is a Rev D, have the mods been done correctly (of special interest here are the pin 70 to ground mod and the HOLD/INTERRUPT line scramble)?
 - 5) Are all boards seated in the backplane and are all the chips securely in their sockets? Particularly take note of the Data Delay lines in the 16K boards. Is there power to the backplane?

- 6) Are all cables to the Controller and Drive connected correctly. Are all the connectors on the disk drive itself firmly seated? (Remove the HELIOS top cover.) Take particular note of all the connectors at the top of the Data and Interface PCB.
- 7) Are the diskettes being used defective or of the wrong type? (Refer to the Helios User's Manual.)
- 8) Is the correct version of the DISKT program on cassette being used. The current revision of the test is Rev E.

SYMPTOM: System will not boot in PTDOS.

- CHECK:
- 1) Will Sol respond to HOLD signal from the controller PCB?
 - 2) Are all boards seated correctly and all the chips firmly in their sockets?
 - 3) Is memory located in the correct locations? [Minimum memory configuration is: 0000 - FFF and 9000 - BFFF, which is a total of 16K].
 - 4) Does memory pass MEMT? Does Sol pass SOLT? Does disk pass DISKT? (If the answer to any of these questions is "NO," go to these particular sections of the manual.)
 - 5) Is the diskette in Unit 0 a PTDOS SYSTEM DISK? (Remember that a BASIC disk or a DATA disk do not have the RESIDENT program on them and, therefore, will not "Boot".)
 - 6) If the system disk is configured for 4 or more units, are there diskettes in every even-number unit? (E.g., when a system is configured for 4 units, units 0 and 2 must have a diskette spinning in them, as PTDOS checks to see if both drives are "Ready".)
 - 7) Are all the cables connected correctly and with the correct polarity?
 - 8) Are there any loose connectors on the PerSci drive (i.e., power, heads, interface...)?
 - 9) Is drive in alignment?
 - 10) Does the head load? If not, check the I/O section on the controller board and the jumpers on the back of the controller to see if one has come loose.

- 11) If the head loads, does it remain loaded or unload after a second or so? If the head remains loaded, check the DMA status lines from the controller to see if the program is hanging up waiting for status. Sync on U51 pin 1, Input Port F0, and examine status lines. If the head unloads immediately, suspect a problem in the DMA timing circuits or the state counters on the Formatter PCB.
- 12) Are the following signals coming from the drive?

SIGNAL	PIN	(P1 OF DRIVE)
Separated Clock	50	(should be pulsing)
Separate Data	48	(should be pulsing)
Ready Unit 0	22	(Low if "Ready")
Ready Unit 1	6	(Low if "Ready")
Separated Sector	20	(Pulsing sector marks)
Separated Index	8	(low every 166 ms)
Seek Complete	10	(low if seek is complete)

If any of these signals are not present, refer to section on drive alignment to determine if this is the problem.

- 13) What LEDs are lit on the indicator panel? The following LEDs should light during a boot attempt: Unit 0 LED, READY, HEAD, SEEK, ON. If any of these LEDs do not light, investigate the respective circuitry. On the contrary, if the Unit 1 LED or the Write LED should light, there is either a circuit problem, a problem with the bootload program on the disk or a memory problem.

SYMPTOM: Drive will not seek correctly or at all.

- PROBLEM:
- 1) Using SIMU program determine if the drive is the problem. If so, check the following in the alignment procedure:
 - a) Seek voltages
 - b) Is lamp burned out?
 - c) Dirty scale
 - d) Excessive overshoot
 - 2) If drive is not at fault, check cables and supply voltages to drive and controller.
 - 3) Check the I/O section of the controller with the DISKT program.
 - 4) Check the Phase 2 clock.
 - 5) Check the disk select signals and check to see that selected unit LEDs on indicator panel are functioning.

- 6) Is Disk Command Port (F7) being latched into U31 on controller?
- 7) Are all the cables and connectors on the drive in place? Pay particular notice to P8 to the positioner servo and cables to the lamp amp PCB.
- 8) Manually move positioner servo by hand. There should be a good deal of resistance to being moved. When the servo is released it should return back to track 0. If there is very little resistance here, suspect a bad lamp (refer to alignment, step 1) or a bad positioner servo control PCB.

SYMPTOM: System will boot only on occasions.
(The "Blue Monday" syndrome.)

- PROBLEM:
- 1) Disk drive catseye alignment is out of tolerance or the drive on which the disk was copied is out of alignment.
 - 2) Memory at 0000 or 9000 - BFFF is intermittent. Run memory tests or swap memory locations with another board.
 - 3) Spindle speed on the drive is varying or out of specification (evidenced by the "READY" LED on the indicator panel flickering). Refer to alignment procedure for correction.
 - 4) Sol backplane connectors making intermittent contact with PCBs.
 - 5) Internal logic problem with the controller board. (Use the DISKT program to narrow down.)

SYMPTOM: System will not read or write at all during the DISKT program.

- CHECK:
- 1) Phase 2 and Phase 1 clock of the Sol.
 - 2) Check if Sol responds to the HOLD signal.
 - 3) Is there memory at 0000 and is it OK?
 - 4) Are the diskettes inserted properly and are they 32 sector holes?
 - 5) Are TEXT, DATA, DONE and RSECT present on the formatter board? If not, see section on troubleshooting the formatter.
 - 6) Do the Troubleshooting and Diagnostics in the Helios II Technical Manual (Helios II Disk Memory System Manual) check OK?

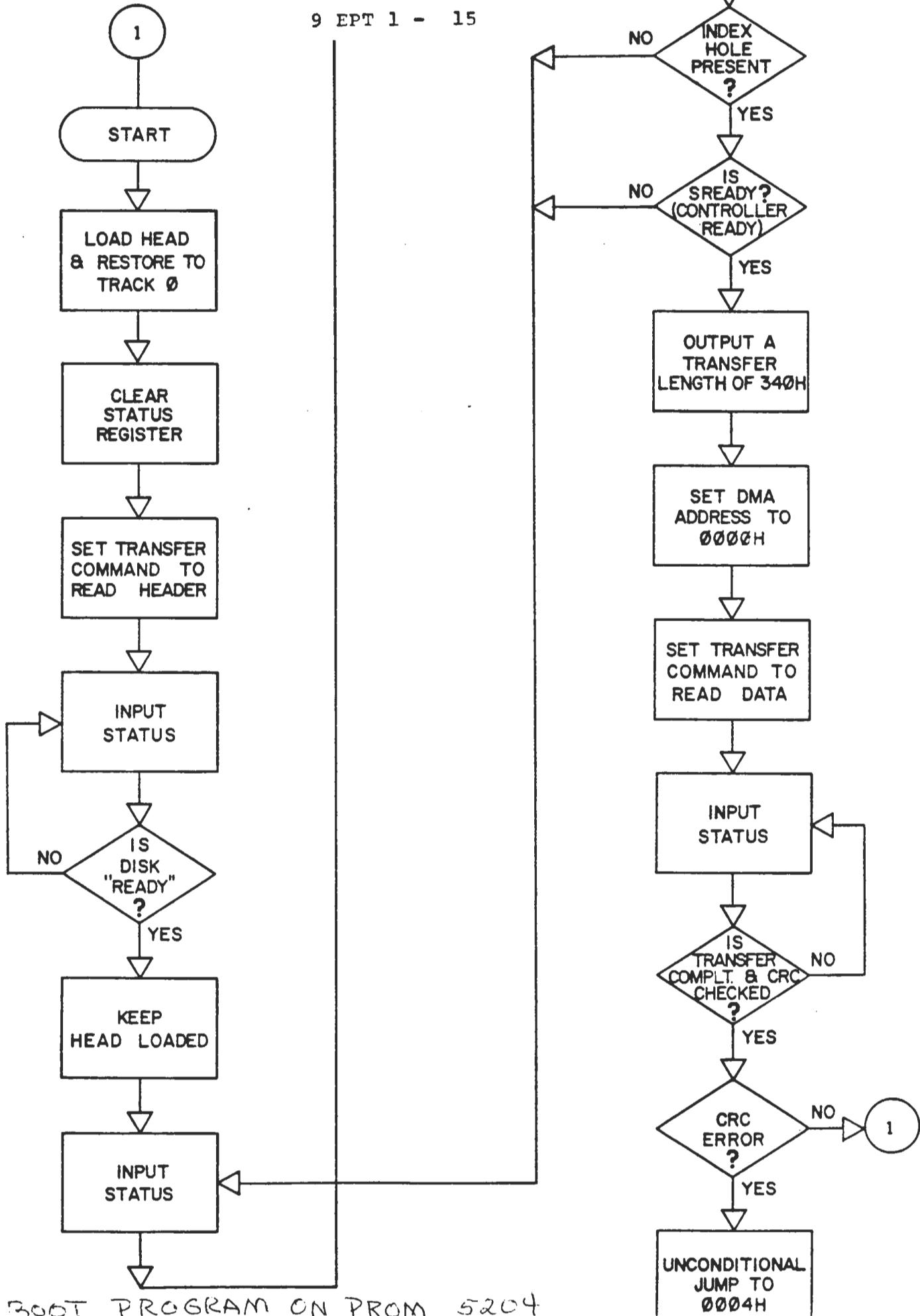
- 7) Can the drive be brought into alignment with the SIMU program? Can the drive write a pattern of ones and zeros with this program? Can the drive seek, and are all the output signals from the drive present?
- 8) Does pulling the chips out of the indicator panel help at all?
- 9) Is pin 70 on the S-100 Bus at ground potential, and are XRDY and PRDY at a logic high level?
- 10) Is there a problem with the ribbon cables?
- 11) Phase-Locked-Loop on drive is out of adjustment.

SYMPTOM: System will not Diskcopy; hangs up during a Diskcopy; gets write retry during Diskcopy.

- PROBLEM:
- 1) Bad memory or no memory from 0000 to 1FFF. Run MEMT on this memory.
 - 2) Head penetration on Unit 1 is adjusted incorrectly. (See alignment procedure unit 1.)
 - 3) Bad diskette being copied.
 - 4) Bad DISKCOPY program on the diskette.
 - 5) Flaw in the disk being copied to.
 - 6) Mechanical impedance of the head from traveling to outside tracks. (Run the SEEK Test portion of of DISKT on both units.)

SYMPTOM: Disk drive will not accept a diskette or will not eject a diskette.

- PROBLEM:
- 1) Cone on drive sticking or not releasing properly. Repair or replace cone.
 - 2) Broken eject shaft support bracket. Replace if necessary.
 - 3) Broken diskette eject arm. Replace per section in Persci Problems <Mechanical>.
 - 4) Eject motor plastic cam is 180 degrees out-of-phase with the eject switch. Adjust cam as specified in Persci drive section.
 - 5) No 24 volt source for the disk drive or R126 & R121 on drive D & I board open.



BOOT PROGRAM ON PROM 5204

3.5 USING THE SYSTEM III TROUBLE-SHOOTING FLOWCHARTS

As shown in the macro-flowchart, Fig. 3-2, the problem must be first broken down to the point where it is attributable to one of four elements in the system. Each element is designated by a letter A through D. This designation refers to one of the four separate micro flowcharts (figures 3-4 through 3-6) each one devoted to one of the four system elements.

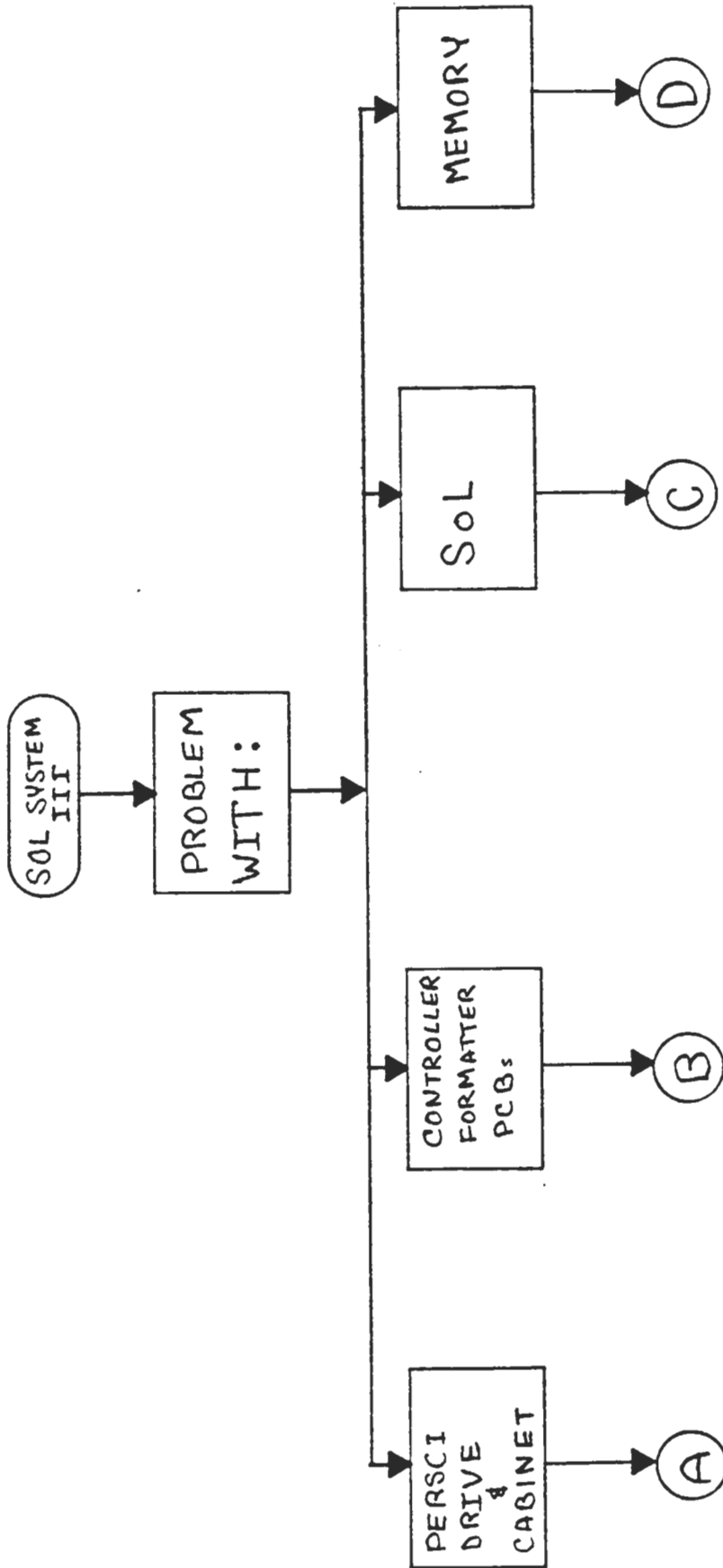


Fig. 3-2. Macro-flowchart, System III Trouble-shooting Procedure

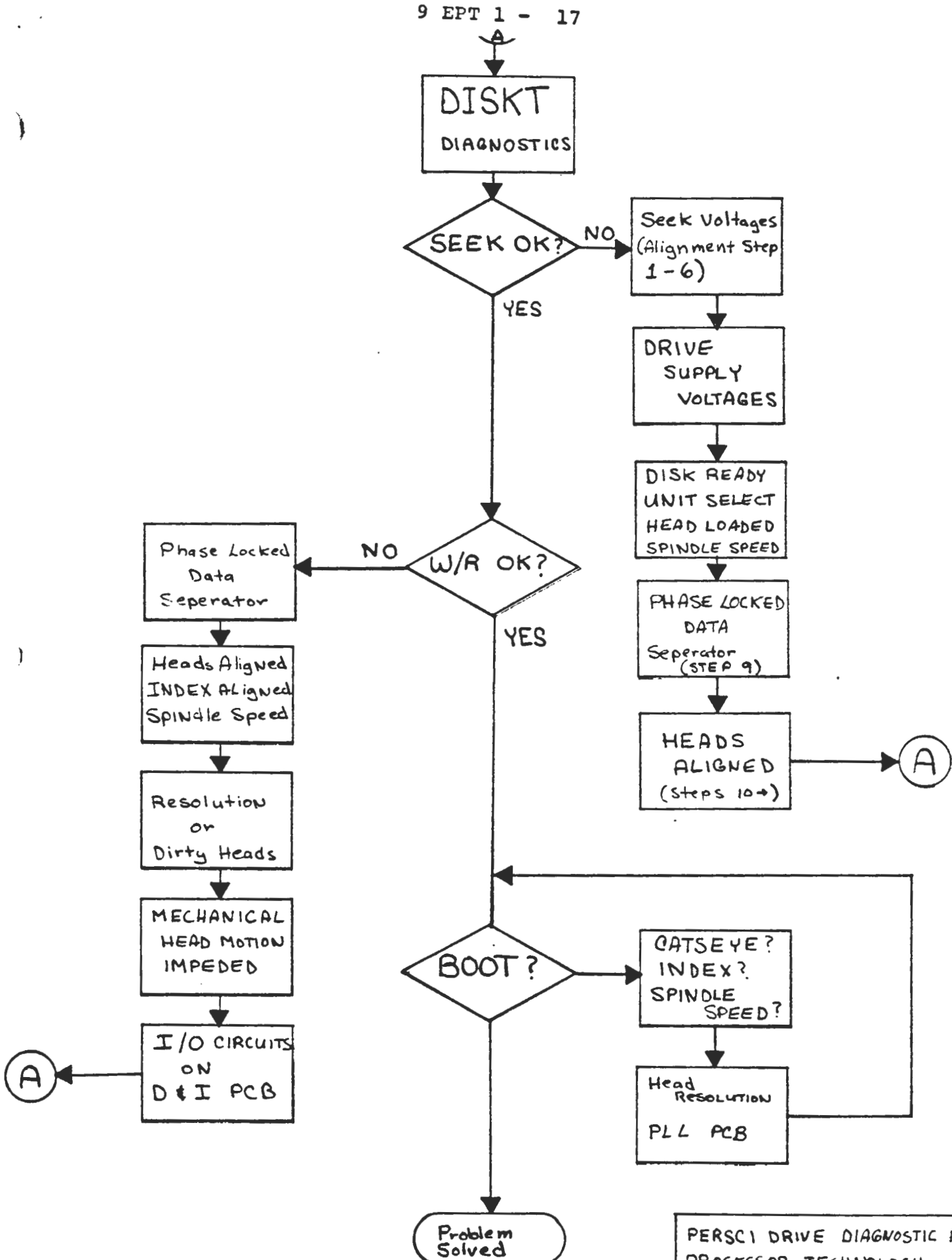


Fig. 3-3. Flowchart, PerSci Drive Diagnostic

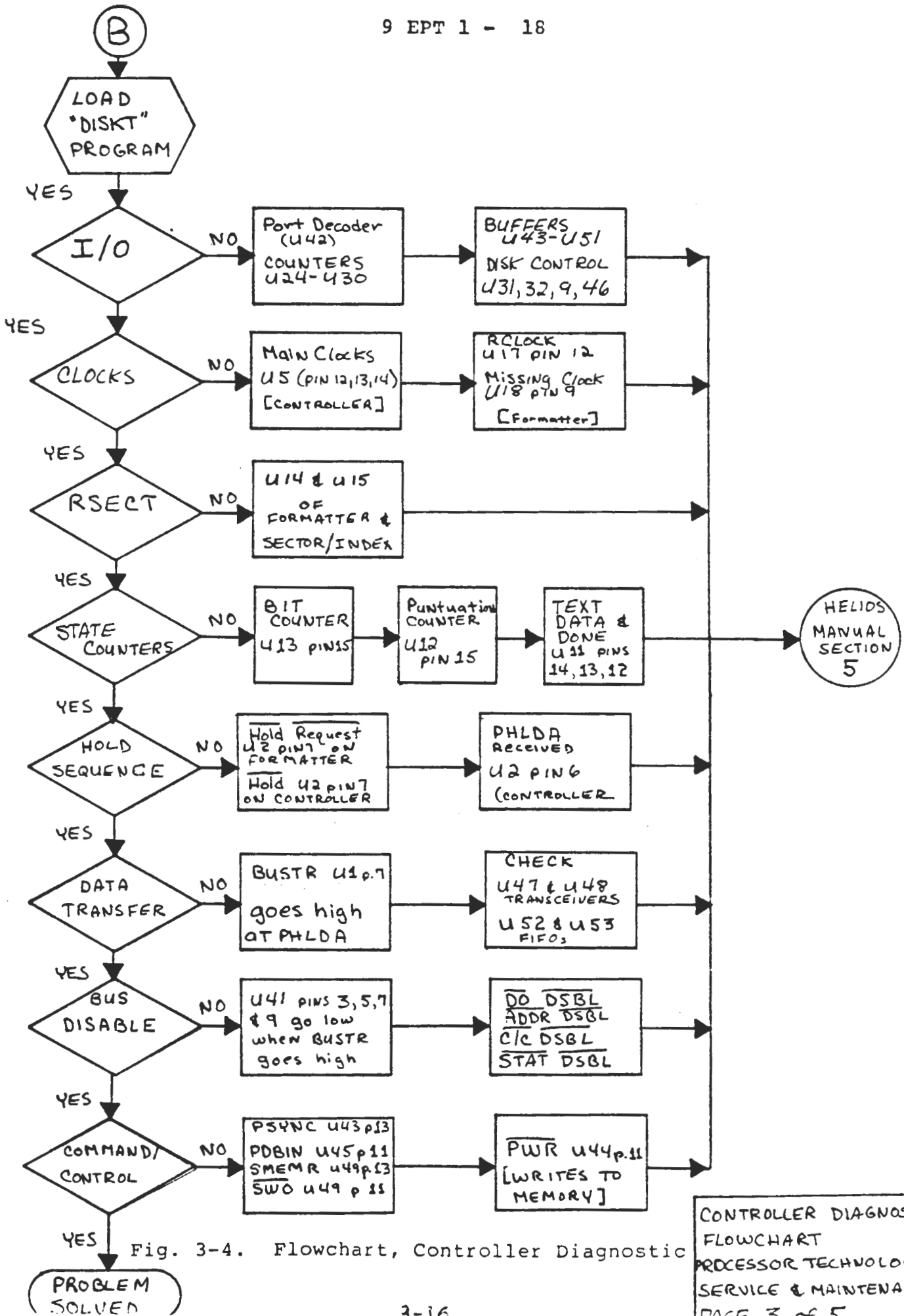


Fig. 3-4. Flowchart, Controller Diagnostic

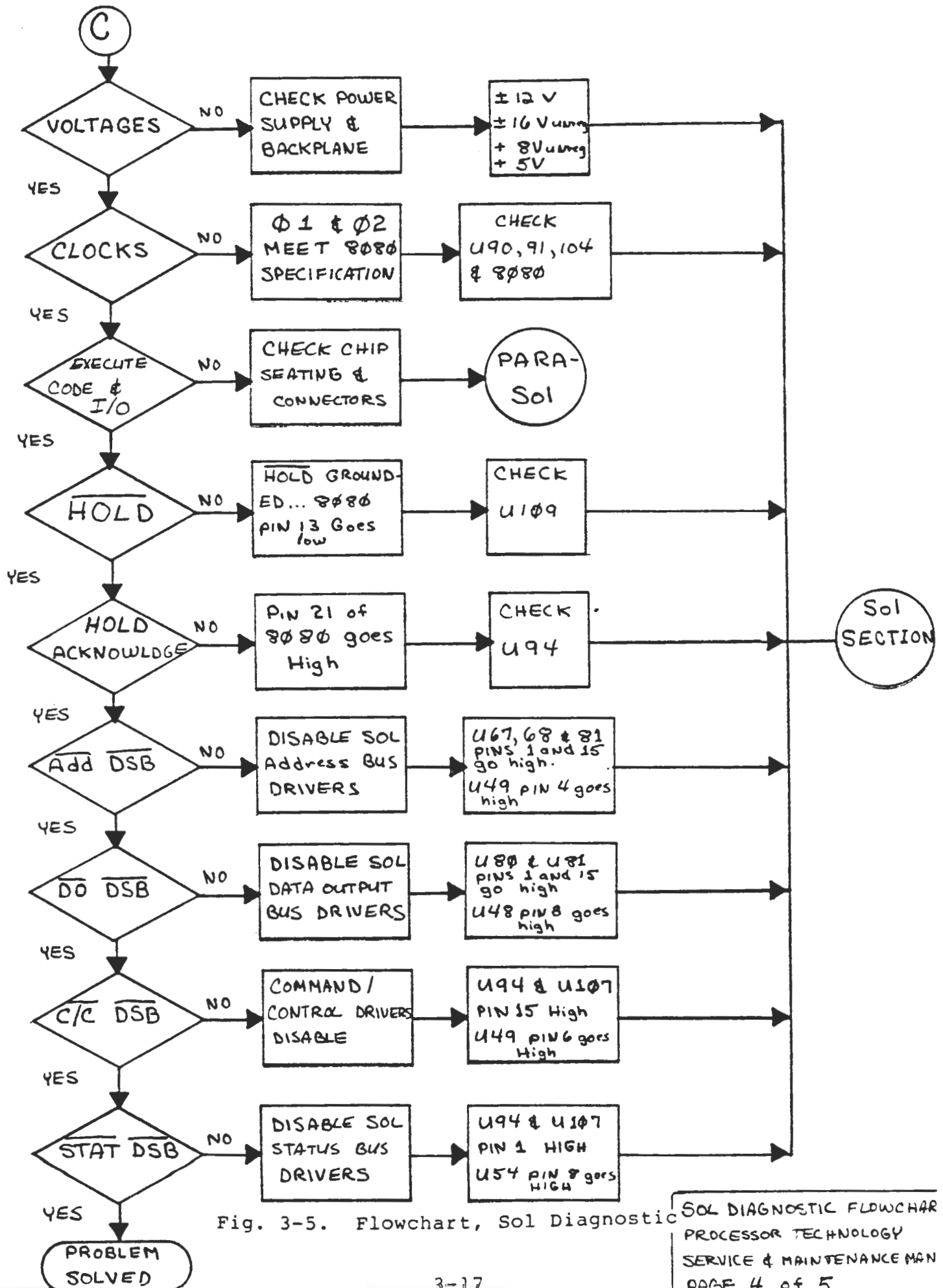


Fig. 3-5. Flowchart, Sol Diagnostic

SOL DIAGNOSTIC FLOWCHART
 PROCESSOR TECHNOLOGY
 SERVICE & MAINTENANCE MAN
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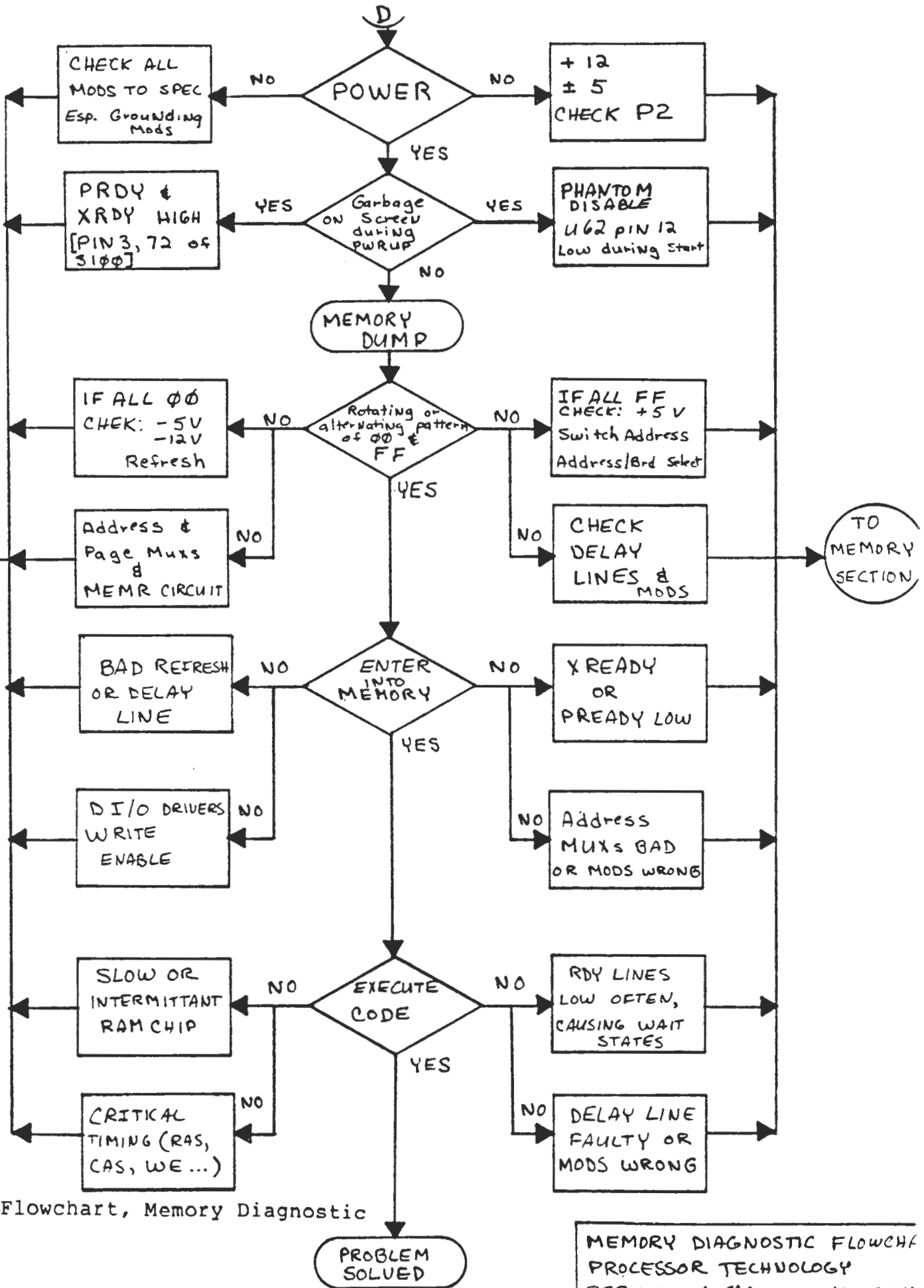


Fig. 3-6. Flowchart, Memory Diagnostic

MEMORY DIAGNOSTIC FLOWCHART
PROCESSOR TECHNOLOGY
SERVICE & MAINTENANCE MANUAL
PAGE 5 of 5

3.6 SUMMARY OF TEST AND DIAGNOSTIC PROGRAMS

The service test disk contains 11 programs intended to aid the service technician test Sols, memories and Helios systems. The tests are all "Image type" files and may be loaded into memory by simply typing the desired test name and a carriage return. The following is a brief summary of the available tests:

Source Listings for the Test programs have been included on the Service Tests diskette as an aid. The user should feel free to modify the programs to suit his needs; however, a backup of the original source listings should always be maintained on disk. A source listing can be recognized by its being of type S and having a :S after the name. For instance, "48K" is the object program and "48:K" is the source for that program.

- 16KRA: Tests a 16K block of contiguous memory beginning at 1000 to 4FFF continuously until the escape key is depressed. The program loads at 0000 and is approximately 256 bytes long. When executed, the program will not display anything on the screen until the first pass has completed. Details of this test are at the end of the 16KRA User's Manual.
- 16KDT: This test is the 16K diagnostic test used in conjunction with the 16KRA User's Manual, Section 7. The purpose of this test is to enable the technician to exercise memory areas and to write and read data to specific cells within the array. The main usefulness of this test is in timing and waveform checks internal to the memory board. The program is loaded and executed at 0000 and is 801 bytes long. For a discussion of the particulars of this test, refer to the 16KRA User's Manual.
- 32KRA: Tests a 32K block of contiguous memory at location 0000 - 7FFF in either a single pass or a continuous loop mode. The test loads at memory location C900 (system RAM) and is approximately 256 bytes long. The executing address is at memory location C900. The test begins by allowing the option of continuous or single pass and prints out a pattern of "G" and/or "X" as in the 16KRA test; however, the memory map will correspond to the 32KRA-1 board.
- 48K: This test will check 48K of contiguous memory beginning at 0000 - BFFF in either the continuous or single pass mode. The test loads and executes at C900 and is approximately 256 bytes long. Typing "C" in the beginning sets the continuous mode which will run until the "escape" key is depressed. The test will print a pattern of "G" or "X" as in all the other memory tests; however, the memory map will correspond to a 48KRA-1 board.

DMARD: Set: BU=9000 (C/R). When DMARD test is complete, set: BU=8000 (C/R). This test will do DMA reads from the memory onto the disk and uses PTDOS. The program loads at BCC0 and is approximately 400 bytes long. The memory from which the test reads is determined by the first and second parameters when typing the test name from PTDOS. For example:

DMARD 0,7 <CR>

will do a DMA read from 0000 to 7FFF in 1K (Hex) blocks to the disk. Each 1K block of memory is read 9 times. A bad read will be indicated by an error message and the user has the option in the beginning to either stop on an error or continue on an error. The test will terminate when the MODE SELECT key is depressed.

DMAWR: This test will do 1K (Hex) DMA writes into memory from the disk using PTDOS. The program loads at BCC0 and is approximately 400 bytes long. The memory which will be tested is specified by the parameters selected when typing the file name from PTDOS. For example:

DMAWR 0,7

will do a DMA write into memory locations 0000 - 7FFF in 1K (Hex) increments writing to each block a total of 9 times. The test will either stop on errors or continue on errors, but in either case will report the failure. Pressing the MODE SELECT key will return the user to PTDOS.

SOLT: (See 2.6.1, "SOLT Diagnostic Test Program.")

SOL-B: (See 2.6.2, "SOL-B Test Program.")

DOST: This test is an example of a PTDOS "DO Macro" which is used to test the Sol System III and the PTDOS disk commands. The test can be written into the START.UP file where it will execute continuously. By editing the file, the user can observe the different commands being used. The other way to use this test in single pass mode is to type "DO DOST." The test will not run continuously in this mode, it will run only one pass and then return the user to PTDOS. The only errors reported will be PTDOS errors since this test runs under PTDOS control.

A listing of DOST, a test used to test the System III hardware using PTDOS commands in a "DO" file can be displayed from the Service Tests Disks using the EDIT commands. By putting this file in "START.UP" with the COPY command, the test will run over and over again until it is stopped.

DISKT: This program is the Helios II Disk Diagnostic program detailed in the the Helios II Disk Memory System Manual. DISKT is used to verify the integrity of the Helios II hardware. The test is located from 0000 - 2FFF and uses 3000 - 3FFF as its buffer. The program is executed at location 0003. Type:

DISKT (RETURN)
EX 3 (RETURN)
V (Video)

DISKCHK: This test is a PTDOS command file. By typing the name "DISKCHK," PTDOS compares every file on the disk to the directory to insure the file structures are correct. This test does not say the Data within the file is correct, but that the file integrity is OK. Any errors here will be reported as PTDOS errors. This program will give memory overflow errors on large programs if the buffer is not set low enough. It is a quick way to check whether a disk is bad or good and is not really a diagnostic tool.

SIMU: This program is to be used in conjunction with the Alignment Section of the Helios II Service Manual. The program loads at 0000 - 1FFF and executes at 0. The program is designed to exercise the drive hardware in order to perform a disk alignment. In so doing, SIMU simulates in software the PerSci drive exerciser. SIMU command mode is designated by a period as a prompt. The "ESCAPE" key returns the user to SOLOS.

3.7 TEST ROUTINES CONTAINED ON EPROMS

Certain test routines are contained on 2708 EPROMs. They occupy 4K of memory starting at E000. They also require 512 bytes of RAM from C900 to CBFF, actually 768 bytes.

To use any of the test programs, first type:

EX E000 <CR>

You should get the response:

TEST ROUTINES

The asterisk. (*) is the prompt for the test Routines program. <CR> indicates Carriage Return.

MEMORY TESTS

There are memory tests for 1K, 4K, 8K and 16K blocks of memory. The 4K, 8K and 16K tests produce a map which corresponds to the RAM layout of each board. The 1K test produces a row of 8 X's or G's, one 'X' or 'G' for each bit. Bit 7 is on the left, bit 0 on the right. To use the memory tests, type the test name, a space, then the first address where the test is to be run. The 16K test will work correctly only when run on a 16K boundary: 0000, 4000, 8000, C000. The 4K, 8K and 16K tests take several minutes to run.

MEMORY TEST COMMANDS

- * 1K 5000 <SPACE BAR> <CR> Run 1K test at address 5000
- * 4K 6000 <SPACE BAR> <CR> Run 4K test at address 6000
- * 8K 6000 <SPACE BAR> <CR> Run 8K test at address 6000
- * 16K 4000 <SPACE BAR> <CR> Run 16K test at address 4000

MEMORY DATA TEST

This test checks all bits at a single address. It uses a marching pattern. The display consists of 2 columns of 4 bits on the left which is the pattern written to memory. The middle 2 columns of 4 bits are the data read from memory. The right-hand pattern of 2 columns of 4 bits has an 'X' where an error occurred and a '-' where there was no errors. If a memory board passes this test, the DI bus receivers and DO bus drivers are good. If a board fails this test, the receivers and drivers may be good or bad. More testing is required to decide.

Memory data test command:

- * DA 1000 <SPACE BAR> <CR> Run data test at 1000

MEMORY ADDRESS TEST

When the data test indicates that at least one good bit exists at an address, that address can be used by the address test. To function correctly the address test should be run at a 16K boundary (0000, 4000, 8000, C000). The test will find address lines that are stuck HI or LO or OPEN. It will not always find shorted address lines.

To use the address test:

- * DA 4000 <SPACE BAR> <CR> Check data bits at 4000
- * AD 4000 <SPACE BAR> <CR> Check address lines at 4000

For correct results the data and address path tests should be run one after the other as shown.

MEMORY EXERCISER

This part of the test routine writes and reads a pattern to any location in memory. The command:

Address	Read and Write This Data
* EX 1000 45 <SPACE BAR> <CR>	

3.8 VIDEO DISPLAY TESTS

The first video display test (V1) puts an alphabetic pattern on the screen; the number keys on the keyboard can then be used to scroll the display and control the window shade.

Numbers Keys on Keyboard

1	2	3	4	5	6	7	8	9	0
Bit 4	Bit 2	Bit 1	Bit 0	Bit 4	Bit 2	Bit 1	Bit 0	All	All
Window Shade Bits				Scroll Bits				Bits=1	Bits=0

To end the test type 'S' for stop.

The second video test uses the number keys to generate an ASCII code which is displayed in each screen position. For example: hit 0 to set all bits to 0, then hit key 2 to create the ASCII code 40 hex; this should be displayed as an "@" in each screen position. To end the test type 'S' to stop.

Commands:

* V1 <SPACE BAR> <CR>	First test
* V2 <SPACE BAR> <CR>	Second video test

CUTS - ACI TESTS

The cassette write test (CW) writes a pattern onto the cassette which can be read by the cassette read test (CR). To test a cassette interface read and write at both high and low speeds: when the write test is writing, type 'S' to stop writing. When the end of a block of data is reached, the motors will stop. There may be a delay of up to 10 seconds until the end of the block is reached. A report is displayed at the end of the write test. Ignore the report - it is a program bug.

Command:

* CW <SPACE BAR> <CR>	Cassette WRITE TEST
-----------------------	---------------------

The cassette read test checks and displays the data written by the cassette write test. The data appears on the screen in the familiar

alphabet pattern. When the screen is full there is a delay of about 5 seconds, then the screen clears and starts to fill over again. When 'S' is typed the test stops and reports the number of bytes read and the number of errors. There should be 0000 errors.

Command:

* CR <SPACE BAR> <CR> Cassette Read Test

INPUT TEST

This test allows you to monitor the data input of any port. Bit 7 is on the left, bit 0 is on the right. Type 'S' to stop the test.

Command:

Port #

* IN FF <SPACE BAR> <CR>

OUTPUT TEST

This test allows you to control the output bits of any port. The display indicates which bits are 1's and which bits are 0's. Type 'S' to stop.

```

+++++++
DOST
+++++++

```

The following is an example of a test used to test the System III hardware using PTDOS commands in a "DO" file. By putting this file in "START.UP" with the COPY command, the test will run over and over again until it is stopped. This test will be referred to as DOST.

```

SYST /
RECOVER;
SET BU=8000;
$PR
$PR
$PR      *****
$PR      =====>>  NOW RUNNING PTDOS COMMAND TEST,      <<=====
$PR      ALLOW ABOUT 30 MINUTES FOR ONE PASS
$PR      *****
$PR
DISKCOPY 0,1,S=-W;
FILES;FILES /1;
REATR CTAP:S;REATR CTAP:S/1;
KILL CTAP:S/1;CREATE CTAP:S/1,1T;
READ CTAP:S,0000;
COPY CTAP:S,CTAP:S/1;
READ CTAP:S/1,0000;
PRINT CTAP:S/1;
ASSM CTAP:S,#1,DUMMY;
EXTRACT DUMMY;
DUMP DUMMY;
KILL DUMMY;
FREE?;
REATR CTAP:S,KWIN;REATR CTAP:S/1,KW;
REN ME CTAP:S/1,QQQQ;
REATR QQQQ/1;
KIL QQQQ/1;
COPY CTAP:S,#1;
RETYPE 2T,1T;
FIL S /1 <1>;
RECOVER/1;
ZIP 0;
BOOTLOAD;

```

The following is a list of most commonly used parts on Processor Technology System III products. These parts may be ordered from:

Processor Technology Corporation
Attention: Customer Service Department
7100 Johnson Drive
Pleasanton, Ca. 94566

When ordering, be sure to specify part number and quantity required. If the product being serviced is under warranty, be sure to enclose the defective part for a no-charge replacement.

Helios Sub-Assemblies

PART NO.	DESCRIPTION	PRICE EA
302000	Power Supply Board	\$68.20
301003	Formatter	78.00
301000	Controller	179.03
301007	Cable, Short	26.00
301009	Cable, Long	32.50

Sol-20 Sub-Assemblies

PART NO.	DESCRIPTION	PRICE EA
101036-06	Assy, Sol PC Board	440.95
107000-02	9216 SOLOS Personality Module	21.18
1070003-01	5204 SOLOS Personality Module	76.53
107015	5204 BOOT Personality Module	72.40
104000	Keyboard	194.50
103000	Assy, Sol Backplane	54.18
103003	Assy, Cable, Backplane	5.95
105008	Assy, Regulator, PCB	50.08

Sol-20 Parts

PART NO.	DESCRIPTION	GENERIC	PRICE EA
701011	UART	6011	5.75
701011	UART	AY5-1013	
701009	Character Generator	MCM6575	22.50
701013	Dual OP	1458	.60
701015	TTL to EIA Driver	1488	1.20
701017	EIA to TTL Driver	1489	1.20
701019	1024x1 Static Mem.	21L02	1.88
701023	Quad 2-Input Nor	4001	.28
701027	Dual "D" FF	4013	.85
701031	Quad And-Or	4019	.85
701045	Phase-Lock-Loop	4046	1.08
701047	Hex Inverter	4049	.85
701051	Dual Binary Counter	4520	1.03
701053	Opto Isolator	4N26	1.63
701170	Microprocessor	8080	8.13
701090	Quad 2-Input Nand	74LS00	.29
701094	Hex Invertor	74LS04	.30
701100	3-Input Nand	74LS10	.29
701108	Dual 4-Input Nand	74LS20	.29
701120	Dual J-K FF	74LS109	.45
701128	3-to38 Decorder	74LS138	.68
701142	4 Bit Binary Counter	74LS163	.86
701146	Quad D FF	74LS175	.79
701150	Dual 4 to 1 MPX	74LS253	.84
701186	Hex Buffer	8T97	1.24
701192	4-Bit Binary Counter	93L16	1.80
701086	Quad 2-Input Nand	74H00	.38
701001	MOS Clock Driver	AM0026C	1.80

Sol-20 Miscellaneous Parts

PART NO.	DESCRIPTION	PRICE EA
105028	Transformer, Sol T-2	45.00
101007	Walnut Side Panel, Left	21.73
101008	Walnut Side Panel, Right	21.73
709004	14.31818 Mhz XTAL	3.00
723013	7 amp. Slo Blo Fuse	.56
723010	191TE-1A1-55 Sigma Relay	4.23
702002	Transistor, 2N222 NPN Silicon	.18
702010	Transistor, 2N4360 FET P Channel	.43
703003	Diode, IN4001 Silicon	.13
703011	Diode, IN5231B Zener 5-1V	.15
105016	Sol Video Cable	6.85

Miscellaneous Memory Parts
(16KRA and 32KRA)

PART #	DESCRIPTION	GENERIC	PRICE EA.
701021	4K X 1 Dynamic RAM*	2104	\$5.00
701026	8K X 1 Dynamic RAM*	2108	12.00
701126	Quad Exclusive OR (Signetics)	74LS136	.48
701134	Dual 4 line to 1 Mux	74LS153	.73
701161	TTL to MOS Driver	75365	1.33
701142	4 Bit Binary Counter	74LS 163	.88
701111	JK Flip Flop	74LS109	.63
704001	Data Delay Line		16.25
701162	+5 Volt Regulator	7805	.45
701164	+12 Volt Regulator	7812	3.30

Prices subject to change without notice

Miscellaneous Memory Parts

(nKRA-1 series)

PART #	DESCRIPTION	GENERIC	PRICE EA.
701091	Dual JK Flip Flop	74LS112	\$.56
701159	Octal D Flip Flop	74LS374	1.50
701085	Octal Driver	74LS244	1.50
701128	3-8 Line Decoder	74LS138	.68
701139	Dual 2-4 Line Decoder	74LS139	.68
701042	4 bit Binary Counter (CMOS, NEC only)	4040	1.08
701008	16K X 1 Dynamic RAM (Mostek or NEC)	4116	14.38
701014	8K X 1 Dynamic RAM	4108-30	6.25
701010	8K X 1 Dynamic RAM	4108-31	6.25
701016	8K X 1 Dynamic RAM	4108-40	6.25
701012	8K X 1 Dynamic RAM	4108-41	6.25
701030	8K X 1 Dynamic RAM	2109	*
726100	Operation RQST ROM	74LS287	2.38
726101	32KRA-1 Match ROM	74LS387	2.38
726107	nKRA Match ROM	74LS387	2.38
726108	nKRA Match 3 ROM	74LS387	2.38
726109	nKRA Match 4 ROM	74LS387	2.38
726111	Operation RQST ROM	74LS387	2.38
704002	nKRA Data Delay Line		13.75

* Call factory for pricing and availability.

Prices Subject to change without notice

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SECTION 10 UPDATES

10.0 PREFACE

Electronics is a very fast moving field. Development of new products, and improvements in the old products proceeds at an unprecedented rate. The continuing development of the Helios II is no exception. Better parts become available and are included, experience yields circuit improvements, and new circuitry is developed. This process generates changes much more frequently than this manual is reprinted. As a result, we include the improvements as blue update sheets, added to this section as they become available. Be sure to integrate this information into the body of the manual before beginning, by making indicated changes in the text, adding or replacing pages, or making notes referring you to the update page.

If you have a question as to the currency of a particular page of text, look in the lower left-hand corner of the page. The initial version of the page will have this corner blank. When the contents of the page have changed, the new version will have "REV A" in this corner; a third version will have "REV B," and so forth. When a whole new page and page number are added, the corner is blank.

A "2" in the corner means 2nd revised printing of the entire manual.

10.1 PARTS LIST UPDATE TABLE

10.1.1 INTRODUCTION

In order to keep your Helios parts list up-to-date, the following Parts List Update Table is provided. This table supplements the parts lists themselves. Entries in the table are similar to those in the parts lists. Any entry in the table supercedes a possibly conflicting entry in the parts list.

10.1.2 SEMICONDUCTOR EQUIVALENTS

One of the main uses of the Parts List Update Table is to communicate changes in semiconductor substitutions in the parts list. In order to assure constant availability of semiconductor components, manufacturers' equivalents are sometimes substituted for the standard vendor parts used in the Helios system. These equivalents may also be used, if necessary, to replace failed components.

Manufacturers' names and their individual prefixes for equivalent semiconductors have been omitted from the industry standard part numbers. For example, "N8T97" (Signetics), found in your parts kit, would be a legitimate substitute for the standard numbered part 8T97 called for in the parts lists or assembly instructions. If a prefix is shown, this signifies that the prefix is essential to identify the correct part.

This table is only to identify semiconductors used in the Helios system. For comparative specifications among manufacturers' equivalent parts, see their respective data books.

The standard vendor part number is underlined and is the first part number in the field called "Standard Vendor Part and Equivalent(s)." Equivalent parts if any follow the standard vendor part number.

10.1.3 UPDATING YOUR MANUAL FROM THE TABLE

1. Go to the Parts List Update Table which follows this page.
2. Go to the first entry in the table. In the column labeled PAGES AFFECTED, find the page numbers corresponding to each new entry.
3. Go to each of these pages and mark an asterisk after the standard vendor part number affected.
4. At the bottom of each page where the reference to the part occurs, insert the following:

"*See Parts List Update Table."

10.1.4 HOW TO USE THE PARTS LIST UPDATE TABLE

1. If you have cross-referenced your manual to the Parts List Update Table according to the above instructions, when you encounter a part mentioned in the manual which has been marked with an asterisk, refer to the table to learn what information change has affected that part.
2. All the entries for a given part are repeated regardless of whether they have changed or not. They are repeated to facilitate identification of the part. Read the entry in the left-most column first to see what the nature of the change is; for example, "add equivalents." Once you know the type of change being made to the entry, you need only read the appropriate columns.
3. If the part has been deleted or some of the information in the regular parts list entry no longer applies, draw a line through the obsolete information in the parts list entry, but retain the asterisk.

PARTS LIST UPDATE TABLE (10-1)

<u>TYPE OF UPDATE</u>	<u>PAGES AFFECTED</u>	<u>ITEM #</u>	<u>PART #</u>	<u>QTY</u>	<u>REFERENCE DESIGNATION</u>	<u>STANDARD VENDOR PARTS AND EQUIVALENT(S)</u>	<u>DESCRIPTION</u>
Add equivalents	3-15,9-9	19	701186	2	U1,2	8T97,8097,74367	Hi-speed hex buffer/inverter
Add equivalents	3-15,9-9	20	701188	1	U4	8T98,8098,NT98, 74368	Hex buffer/inverter
Add equivalents	3-15,9-9	21	701194	1	U5	9401,4101,2401	C.R.C. generator
Add equivalents	3-18,9-9	18	701162	1	U31	7805,LM340-5	+5V Regulator, TO-220
Add equivalents	3-15,9-9	24	705096	1	U3	220/330Ω network, 761-5-R-220/330	Resistor network
Add equivalents	3-29,9-11	7	701092	1	U19	74LS02,9LS02	Quad 2-input NOR
Add equivalents	3-29,9-11	23	701146	2	U1,38	74LS175,25LS175	Quad D Flipflop
Add equivalents	3-29,9-11	28	701186	11	U3,9,32,41, U43-46,49-51	8T97,8097,74367	Hi-speed hex buffer/inverter
Add equivalents	3-29,9-11	43	705096	1	U4	220/330Ω network, 761-5-R-220/330	Resistor network
Add equivalents	3-30,9-11	30	701162	2	U54,55	7805,LM340T-5	+5V regulator, TO-220
Add equivalents	3-34,9-13	13	703027	1	SCR1	MCR 106-2,10632	SCR,60PIV, 4A

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Helios II Manual

CHANGE NOTICE #3

SUBJECTS: A-C. Modification to Regulator PCB
D. Reset to Beginning of Disk System Test
E. PTDOS CONFIGR Command Password

WARNING

Please read and perform this change notice even if you have already assembled your Helios II regulator PCB. This modification will prevent a short between regulator IC U1 and chassis ground. Such a short may damage the Helios power supply.

A. REGULATOR PCB (PRELIMINARY INSTRUCTIONS)

1. PROBLEM DESCRIPTION: POSSIBLE SHORTING OF U1 (Refer to Fig. 3-15, "Regulator PCB and Wiring Harness" and Fig. 8-4, "Regulator PCB, Assembly Drawing.")

U1 is mounted on a heatsink along with other ICs. The two leads from U1 pass through clearance holes in the heatsink and are received by two pads which feed through to the solder side. Assembled regulator PCBs and kits shipped prior to 10-10-77, and some kit PCBs shipped after that date, have oversized U1 pads on their component side. These pads are .250 inches, which dimension overlaps the .187-inch lead clearance holes in the heatsink and therefore contacts the heatsink. Although the heatsink is anodized, a scratch in its under surface or a burr on the pad may short the U1 input and/or output lead to the heatsink which is at chassis ground.

2. If you have already assembled your regulator PCB, or have received an assembled unit prior to 10-10-77, read and perform the instructions in paragraph B, "Modifying a Regulator PCB Already Assembled."
3. If your regulator PCB is still in kit form, determine the revision level of the PCB by looking on either side for the designation: "PC302001."
 - a. If this PC number has the suffix "C" or higher, you do not have to perform this modification. The pad diameters have been reduced to .125 inches.

- b. If there is no revision level suffix, check the two pads for the U1 leads. These pads are in the middle of the U1 component outline. If these pads have been removed, you do not have to perform this modification. It has been done already. If the pads are still there, insert the following in section 3 of the Helios hardware manual, on page 3-33, after step 7:

"7B. See Change Notice #3, Section 10, Updates, C, Modification to Bare Regulator PCB."

You may perform the modification according to paragraph C at this time or during the assembly procedure when you encounter the note you just made.

B. MODIFYING A REGULATOR PCB ALREADY ASSEMBLED

- () 1. Remove the rear panel of the Helios cabinet.
- () 2. Remove the regulator PCB.
- () 3. Unsolder and remove the IC regulator U1.
- () 4. From the component side, using a .062 drill bit, drill out the two pad feed-through holes for the U1 leads. These pads are in the middle of the U1 component outline. (Refer to Fig. 8-4, Regulator PCB, Assembly Drawing.) This step removes the plated feed-through connection between the pads on the solder side and those on the component side. Since the component side pads are now floating, if they contact the heatsink, no short will result.
- () 5. Using a 1/8-inch drill, deburr the holes by hand. This will countersink the edges of the holes.
- () 6. Put shrink tubing on the U1 leads. Make sure it is snug up to the bottom of U1. Shrink the tubing before installing.
- () 7. Reinstall U1 according to 3.5.4, Regulator PCB, step 8.
- () 8. Reinstall the regulator PCB and rear panel according to 3.5.7, Power Supply Assembly, steps 2 through 10.

C. MODIFICATION TO BARE REGULATOR PCB

- () 1. From the component side of the board, using a .062 drill bit, drill out the two pad feed-through holes for the U1 leads. These pads are in the middle of the U1 component outline. (Refer to Fig. 8-4, Regulator PCB, Assembly Drawing.)
- () 2. Deburr the holes on the solder side.

- () 3. Remove the two pads on the component side by heating with a soldering iron then lifting off with an exacto knife.
- () 4. Continue assembling the regulator PCB at section 3.5.4, step 8.

D. RESETTING DISK SYSTEM TEST WITHOUT RELOADING

- () 1. In Section 5, of the Helios hardware manual, on page 5-11, after step 18, insert the following:

"To reset to the beginning of the Disk System Test, without reloading, see Change Notice #3, Section 10, Updates, paragraph D, Resetting Disk System Test Without Reloading."

- 2. To reset the Disk System Test to the beginning without reloading:

- a. Press: ESCAPE

If the SOLOS/CUTER prompt character is not displayed, indicating that escape is not possible at the time:

For Sol only, press simultaneously:

UPPER CASE and REPEAT

For non-Sol systems, begin program execution at the start of the CUTER program.

The SOLOS/CUTER prompt character should appear.*

- b. Type: EX 3

- c. Press: RETURN

- d. For video output, type: V

E. PTDOS CONFIGR Command Password

The CONFIGR command allows the PTDOS user to change system parameters (See PTDOS manual, page 1-49). To use the command the user types: CONFIGR <password>

Initially the password is: PTDOS

It may be changed using the command.

*UPPER CASE REPEAT on a Sol clears only the system RAM. The Disk System Test will still be in memory and does not have to be reloaded.

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Helios II Manual

CHANGE NOTICE #4

SUBJECT: 1.0 Modifications to Controller PCB Assy 301000

1.0 MODIFICATIONS TO CONTROLLER PCB ASSY 301000

1.1 PRELIMINARY INSTRUCTIONS

1. This CN applies to certain controller PCBs assembly levels only. The result of the change is to bring previous assembly levels to the "E" assembly level. Identify your controller assembly as follows:

a. Orient the board with the component side up so you can read the silkscreened designation:

"ASSY. NO. 301000." If this designation is marked or labeled with the suffix "E," or later letter, or if there is an "E" or later letter, marked or labeled in the upper left-hand corner of the board, you do not have to perform this modification.

b. If the assembly number or board corner is not marked or labeled with a letter revision, or is marked with an earlier letter than "E," please continue reading this change notice.

NOTE: Note the distinction between the assembly number revision level on one hand, and on the other hand, the "PC" number revision level. This latter number, which is etched on the solder side of the board, refers to the bare board; whereas, the "assembly" is the board assembled with components to a certain configuration.

2. These modifications to the controller are improvements and corrections which are aimed at problems which are encountered under certain system conditions. If your system is working satisfactorily, it will probably continue to do so without these changes; however, if you are having a problem, these changes may correct it. It is strongly recommended that you make these changes regardless, in order to avoid possible future problems, and to assure that you have a standard controller at the current revision level, which may be a prerequisite for possible future changes.

3. In the Helios hardware manual, Section 3.5.3, on page 3-31, after step 19d, insert the following step 20:

"20. See Change Notice #4, for further modifications."
4. If you have already assembled your controller PCB, or have received an assembled system, perform the changes in paragraph 1.2 immediately or at least as soon as possible.
5. The changes, which include 7 jumpers, presuppose the additional jumpers in section 3.5.3, steps 1 through 19, have already been installed.
6. Since they are interrelated, the changes in this notice must be performed all together and at the same time.
7. Before starting the changes, be sure you have read "Modifying PCBs" A-12, Section 9, Appendix. The jumper wire used should be #24 not #30, unless otherwise noted.

1.2 TRACE AND JUMPER MODIFICATIONS TO CONTROLLER PCB
 (Refer to Fig. 8-3, Assembly, Controller PCB, page revision A and Fig. 8-9, Schematic, Controller PCB, page revision A. All the following trace cuts are marked with an "X" and called out with arrows on Fig. 8-3, Assembly, Controller PCB; all jumpers are shown as heavy dashed lines on the component side, although the jumpers are to be installed on the solder side.)

1. On the solder side of the board ("trace" or "circuit" side), cut the trace at U15-1. (U15, pin 1). See Fig. 8-3, Detail A.
2. On the solder side of the board, find U50-1. Follow the trace leading from it 1/8 inch to a feed-through pad. Using insulated jumper wire, connect this pad to U15-1.
3. On the component side, locate U31. A trace emerges from under the U31 socket between pins 9 and 10. Another emerges between pins 10 and 11. Cut both traces.
4. On the solder side, using insulated jumper wire, connect U30-9 to U31-11, and U30-10 to U31-6.
5. On the component side of the board, a wide trace connects pins 8 of U41 through U51. Cut it between U48 and U49.

Cut it again between U46 and U47.

6. On the solder side, make the following ground connections using #22 wire (bare or insulated as specified):
 - a. U49-6 to U50-12 (Bare wire OK, suspend it over the traces.)
 - b. U48-8 to connector P1, pin 50 (insulated wire).
 - c. U46-8 to connector P1, pin 50 (insulated wire).
7. On the solder side of the board, point E is a pad 1/2 inch below U7-14 (toward the P1 connector fingers [pads]). A long trace extends from point E toward the fingers. Cut this trace near point E, as shown in Detail B, Fig. 8-3.
8. Connect point E to U18-10 with an insulated jumper wire.
9. Place a label marked "REV E" as shown in Note 3 of Fig. 8-3, Assembly, Controller PCB.

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Helios Update 731039

SUBJECT: AC INPUT VOLTAGE

CAUTION

This Helios II 220/240 VAC model is wired for 220 VAC input. This may be changed easily for 240 VAC. Determine whether the local AC supply is 220 or 240 VAC before applying power. Make the following adjustment if the local supply is 240 VAC.

If the local supply is 240 VAC, reconfigure the AC wiring on the inside rear panel as follows: (Refer to Fig. 8-10, Helios II Manual, System Wiring Diagram, 220/240 VAC.)

1. Locate the commoning blocks near the AC input connector. (Refer to the rear panel assembly drawings, Fig. 8-5 for Model 2 and Fig. 8-21 for Model 4.)
2. Unplug the black and white 220 VAC tap lead from pin 4 of commoning block TB3 and insert in its place the 240 VAC tap lead (black and red). (Refer to Fig. 8-10, Detail A.)
3. Plug the 220 VAC tap lead into pin 1 of the commoning block. (In effect, the two tap leads are exchanged.)

AC LINECORD (Refer to Fig. 8-10, System Wiring Diagram, 220/240 VAC.)

The Helios II 220/240 VAC model comes with an unterminated AC linecord. This linecord must be terminated with the appropriate local standard AC outlet plug.

CAUTION

When connecting the appropriate termination plug, be careful to match the plug connections with the color-coded wire of the linecord as follows:

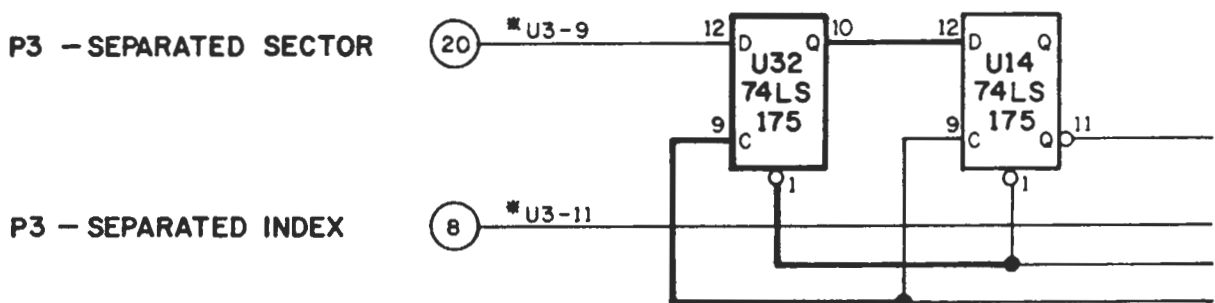
Green	Ground
White	Neutral
Black	Hot

Helios Update 731048

This update describes modifications to Helios Formatter circuit boards being made at the factory. The changes are first described, with corrections to information in the Helios II Disk Memory System Manual. Then a step-by-step modification procedure is given, which factory-authorized service people may use to make the changes in the field, converting a Formatter board of assembly revision level E to level F.

Refer to the schematic of the Formatter board. The signal -SEPARATED SECTOR from the disk drive electronics appears at pin 12 of U14, a D-type flip flop, where it is synchronized by the clock signal. If the trailing edge of -SEPARATED SECTOR occurs too close to the rising edge of the clock input on pin 9, the Q output on pin 10 can have a short spurious pulse starting at the clock transition. The extra pulse is interpreted as an extra sector, and causes errors that PTDOS reports with the message "DISK STRUCTURE BAD". Since the error is caused by a rare coincidence of signals, it may not occur during extended periods of testing.

The detail of the schematic below shows an added D-type flip flop that eliminates the spurious pulse. The added flip flop, U32, is connected just as U14 was, and the spurious pulse can still appear at its Q output on pin 10. However, since the pulse starts on the rising edge of the clock pulse, it is too late to propagate through U14. The spurious pulse is of short duration, and is gone before the next clock. The output of U14 is the same as before the addition of U32, except that the occasional spurious pulse is removed.



Factory-authorized service people should modify all Formatter boards in the field, using the procedure given below. If the changes are made on Revision E assemblies, they become Revision F. The changes are independent of all previous modifications, however, and may also be made on assemblies prior to level E. Two parts are required: a 74LS175 (Quad D-type flip flop) and a 16 pin DIP socket. These parts are available from the Customer Service Department of Processor

Technology. Request part numbers 701146 (74LS175) and 713006 (socket). Jumpers should be made from 30 AWG kynar insulated wire, or 22 AWG solid insulated wire, as shown below.

1) Refer to the detail of the assembly drawing below. Install the 16 pin socket on the component side of the board at U32, making sure that pin 1 is seated in the square pad.

2) Holding the socket firmly in place, solder pins 7 and 15. This will secure the socket while jumpers are added.

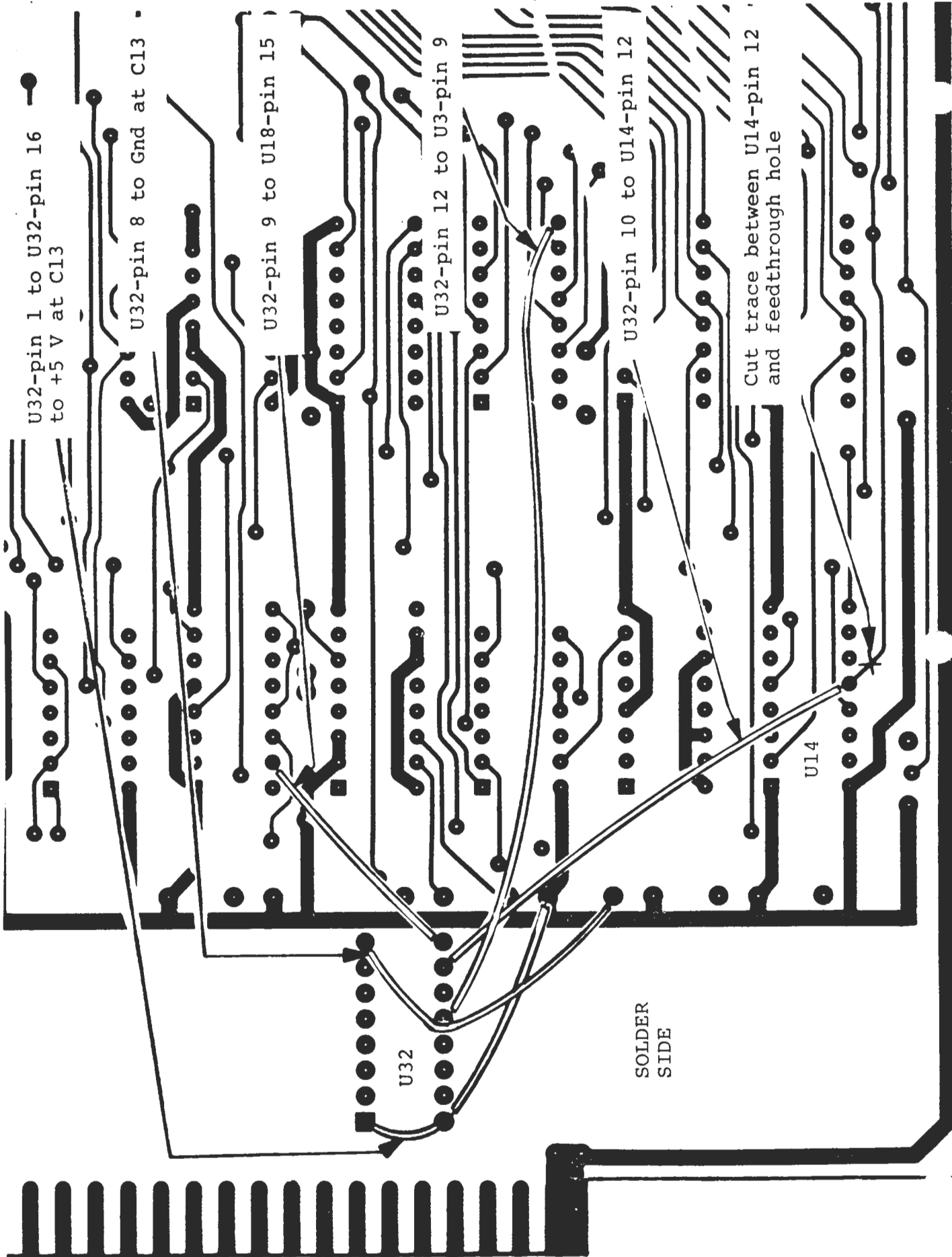
3) On the solder side, cut the trace between U14-pin 12 and a feedthrough hole, close to U14.

4) Solder the following 6 jumpers in place:

U32-pin 1 to U32-pin 16 (22 AWG wire)
U32-pin 16 to +5 V at C13 (22 AWG wire)
U32-pin 8 to ground at C13 (22 AWG wire)
U32-pin 9 to U18-pin 15 (30 AWG wire)
U32-pin 12 to U3-pin 9 (30 AWG wire)
U32-pin 10 to U14-pin 12 (30 AWG wire)

5) Install U32, a 74LS175, making sure that pin 1 is inserted in pin 1 of the socket.

6) If the modification was done on a level E assembly, cover the "E" with a label marked "F".



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Helios Update 731067

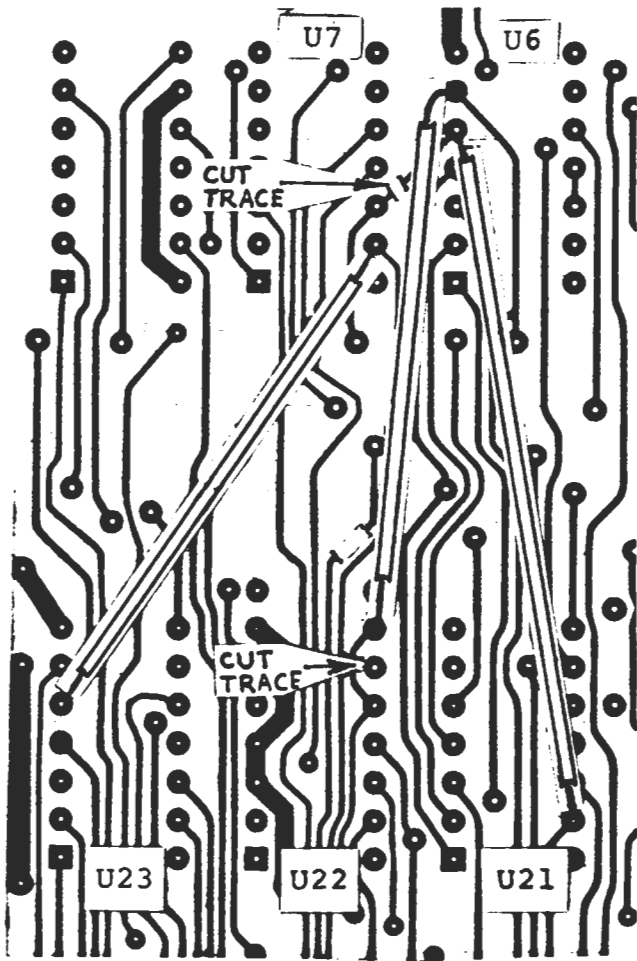
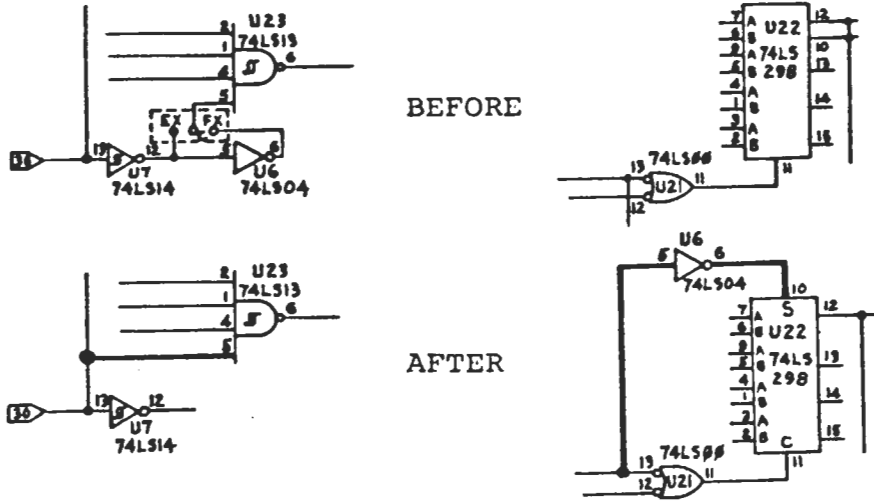
This update describes modifications to the Helios Controller circuit board being made at the factory. If you receive this update with a new or factory-serviced board, it describes the changes that were made. All Helios Controllers in the field should be modified according to the instructions in this update.

The changes increase the reliability of the transfer command register logic. To understand the function of the changes, read Section 7.10.1, subsection G1, of the Helios hardware manual, which describes the action of the transfer command register, U22, and read the circuit changes shown below. U22-pin 10, which selects the A or B inputs to the multiplexer is shown connected to a latch output before modification. The B inputs receive input from the data bus, and are selected for relatively long periods of time. Noise pulses appearing at U21-pin 12 can clock data appearing at the B inputs into the latches of U22 through NOR gate U21. This spurious data can cause a header to be written on the disk at the wrong time.

The modifications borrow an inverter section of U6 for a new function. This section was used in providing a signal to the jumper pin FX. Since a jumper from pin C to pin EX is never used, pin 5 of U23 can be driven with an equivalent signal appearing at U7 pin 13, two inversions before, freeing a section of U6. In the new circuit, shown below, U6 drives the Select input of U22-pin 10 to select the B (data) inputs only when port F1 is addressed, driving U21-pin 13 low. At all other times the A inputs are selected. If a noise pulse on U21-pin 12 happens to latch new data to U22's outputs, the data latched would be all ones from the A inputs, which does not cause a spurious header to be written.

Three trace cuts and three jumpers shown in the figure below should be made as follows:

- 1) On the component side of the board, remove the wire jumper which connects the points marked "FX" and "C".
- 2) On the trace side of the board, cut the trace which connects U6-pin 5 to U7-pin 12, and the trace which connects U22-pin 10 to U22-pin 12.
- 3) Using 30 A.W.G. solid insulated wire, solder jumpers between U6-pin 6 and U22-pin 10, U6-pin 5 and U21-pin 13, and U7-pin 13 and U23-pin 5.



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Helios II Update 731071

MODIFICATIONS TO CONTROLLER PCB ASSY 301000 (H TO J)

1.1 PRELIMINARY INSTRUCTIONS AND REASON FOR CHANGE

This update describes modifications to the Helios II Controller PCB which bring that PCB from assembly revision level H to J. The update also describes associated revisions to the Helios Technical Manual, 730009. The previous update (731067) which you should have received, brought the Controller PCB from level G to level H. It is important that you mark the current revision level of your Controller PCB when you have completed these modifications because the markings enable one to implement succeeding changes without confusion and are necessary for trouble-shooting and other purposes.

Identify the assembly revision level of your Controller PCB. (If you need help, refer to the Helios manual, section 3.2.1.B, "Identifying Revision Levels of Assemblies.") If it has been recently shipped from the factory, it may already be a "J", in which case you can skip to 1.4 of this update, "Updating Your Helios Manual." If it is an "H" or lower, you should perform the modifications because they result in improved low logic levels on the DI/O bus during DMA reads from memory, which means better reliability in your system.

1.2 DESCRIPTION OF THE CHANGE

Drivers (8839s) which contain an additional disable pin for the outputs are substituted for the 8833s at U47 and U48. Pins 7 of U47 and U48 are disconnected from ground and connected to the Q-output of the write flipflop (U39-6), which is high during DMA memory reads. Thus the output drivers of the controller are disabled during the DMA reads. In summary, the changes to the hardware required to implement this change consist in substituting two ICs, making three trace cuts, and installing three jumpers.

1.3 INSTRUCTIONS FOR MODIFICATION

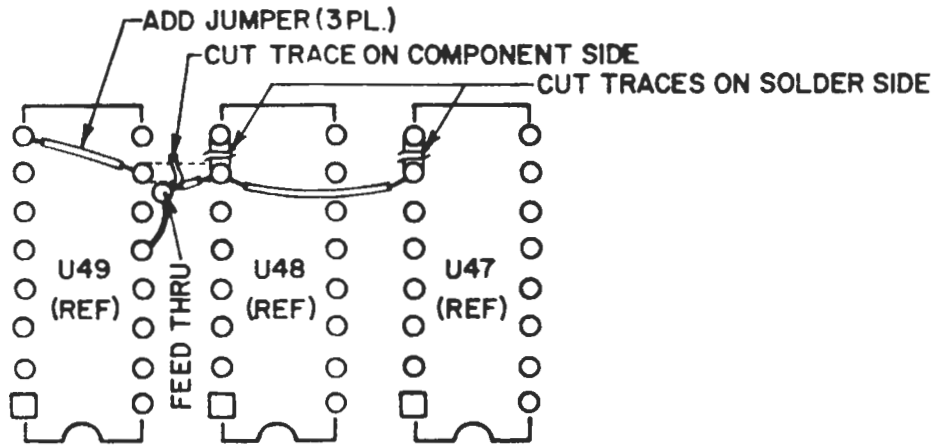
- 1) Be sure you are familiar with the information in the Helios manual, Sections 3.2.3, Integrated Circuits and 3.3, Modifying PCBs.
- 2) Remove the 8833s from U47 and U48.
- 3) Make the following trace cuts:

(Refer to Detail C, in this update.)

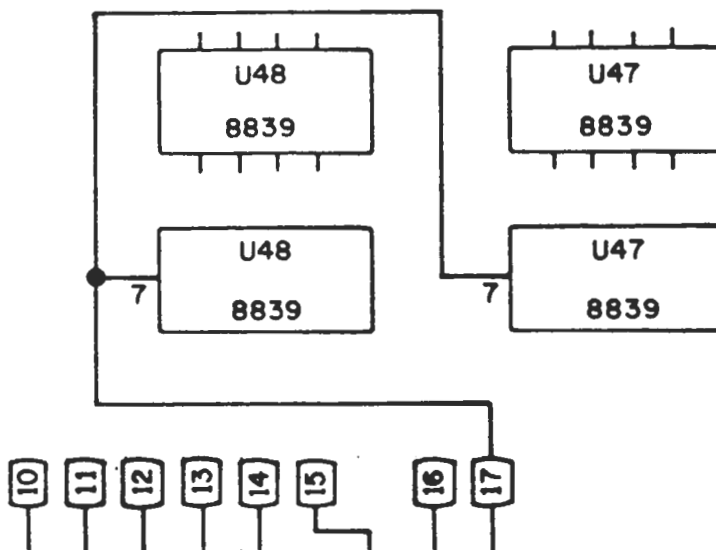
- a) On the component side, cut the trace between U48-7 and U49-10.
 - b) On the solder side, cut the trace between U48-7 and U48-8.
 - c) On the solder side, cut the trace between U47-7 and U48-8.
- 4) Install two 8839s at U47 and U48 (P/N 701181).
 - 5) Using #30 green Kynar insulated jumper wire, make the following jumper connections on the solder side:
 - a) U49-8 to U49-10.
 - b) U48-7 to feedthrough pad between U49-10 and U48-7.
 - c) U48-7 to U47-7.
 - 6) Place a label marked "REV J" as shown in note 3 of Fig. 8-6, Controller PCB Assembly (Helios manual).

1.4 UPDATING YOUR Helios MANUAL

- 1) Insert this update in Section 10, Updates, following update 731067.
- 2) In the Appendix, Section 9, replace pages 9-13/9-14 REV A with the attached REV B sheet.
- 3) Mark the assembly drawing, Fig. 8-6 and the schematic, Fig. 8-11, with the words, "See Updates 731067 and 731071."
- 4) Change the assembly drawing, Fig. 8-6, Note 6, to read:
"30 AWG" not 24 AWG.



Detail C of Assembly Drawing (Fig. 8-6) Showing Modifications.
(Viewed from Solder Side.)



Detail of Controller Schematic (Fig. 8-11) after Modifications.

PARTS LIST - CONTROLLER PCB ASSEMBLY (301000J)
(Refer to Fig. 8-6)

ITEM #	PART #	QTY	REFERENCE CODE	DESCRIPTION
1	301001	1		Fab, PCB, Controller, REV C
6	701090	2	U18,21	74LS00, Quad 2-Input NAND-gate
7	701092	1	U19	}74LS02{; 9LS02, Quad 2-Input NOR-gate
8	701094	1	U6	74LS04, Hex Inverter
9	701098	3	U0,12,36	74LS08, Quad 2-Input AND
10	701100	1	U35	74LS10, Triple 3-Input NAND
11	701102	1	U17	74LS11, Triple 3-Input AND
12	701104	2	U8,23	74LS13, Dual 4-Input NAND
13	701106	1	U7	74LS14, Hex Inverter, Schmitt
14	701118	1	U40	74LS86, Quad 2-Input EX-OR
15	701120	5	U2,10,20, U37,39	74LS109, Dual J-K FF
16	701122	1	U15	74LS123, Dual Retrig. One-Shot
17	701128	1	U42	74LS138, 3-to-8 Line Decoder
18	701130	2	U14,16	74LS139, Dual 2-to-4 Line Decoder
19	701138	2	U13,34	74LS157, Quad 2-to-1 Line Multiplexer
20	701140	1	U11	74LS158, Quad 2-Input Inverter Multiplexer
21	701142	1	U5	74LS163, Synch 4-Bit Binary Counter
22	701144	1	U31	74LS174, Hex D FF
23	701146	2	U1,38	}74LS175{; 25LS175, Quad D FF
24	701146	7	U24-30	74LS191, Synch UP/DN Counter
25	701152	1	U33	74LS279, Quad S-R Latches
26	701156	1	U22	74LS298, Quad 2-Multiplexer, Store
27	701181	2	U47,48	8839, Quad T-S Transceiver, 16P
28	701186	11	U3,9,32,41, U43-46,49-51	}8T97{; DM8097, 74367, High Speed Hex Buf/Inv
29	701196	2	U52,53	9403, 4 x 16 FIFO Buffer
30	701162	2	U54,55	}7805{; LM340T-5, Volt Regulator, +5V, TO-220
33	702002	1	Q1	2N2222, Transistor, NPN
36	703005	1	CR1	1N4148, Diode, Silicon, Switching
39	705022	3	R1,4,5	Res, 220 ohms, 1/4W, 5%
40	705025	3	R2,3,6	Res, 330 ohms, CF, 1/4W, 5%
41	705061	2	R8,9	Res, 10K ohms, CF, 1/4W, 5%
42	705087	1	R7	Res, 1.5 ohms, 1/4W, 5%
43	705096	1	U4	761-5-R-220/330, Resistor 220/330 ohms, DIP, Network
46	707023	18	C3-7,10-22	Cap, .047uf, Disk Ceramic, +80 -20%
47	707032	2	C9,23	Cap, 1.0uf, Tantalum, 35V, 10%
48	707034	1	C1	Cap, 2.2uf, Tantalum, 10%
49	707036	2	C2,8	Cap, 15uf, Tantalum, 20V, 10%

PARTS LIST - CONTROLLER PCB ASSEMBLY (301000J) (Continued)

ITEM #	PART #	QTY	REFERENCE CODE	DESCRIPTION
52	713004	13		Socket, DIP, 14P, Solder
53	713006	39		Socket, DIP, 16P, Solder
54	713013	4		Socket, Strip, 12P, Solder
56	717050	1	P4	Connector Pin
57	717049	1	P4	Receptacle, Test Point, Printed Circuit, Right Angle, Orange
58	721022	1		Heatsink
59	720020	2		PHMS, 6-32 x 1/2",
60	720011	2		Hexnut, 6-32
61	720041	2		ITLW, #6
62	717003	2	P2,3	Header, Male PC, Mount, 50-Pin
64	711004	1		Label, Assy. Rev, 1/4"
65	716027-5	A/R		Wire, SS, Insul, 22 AWG, Green
67	716026-5	A/R		Wire, SS, Kynar Insul, 30 AWG (approx. 14 inches)

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(415) 829-2600
Cable Address PROCTEC

April 3, 1979

Dear Factory-authorized dealer:

The attached document, called "Field Retrofit Notice," is essentially the same type of information you have been accustomed to receive in the form of an "Update." We are now separating two functions of the former "update" and publishing separately the information associated with each function. To notify you of recommended or required hardware modifications to units in your inventory and/or units that come back to you for service, or units already being used in the field, we will use the "Field Retrofit Notice" exclusively. To supply you with new replacement pages to update your manual or to publish new information supplementing a manual, we will send the complementary document called a "Manual Update."

Separating retrofit notices and manual updates into specialized documents makes it easier for us to communicate the appropriate information, and we think it will make for easier reading and implementation on your part.

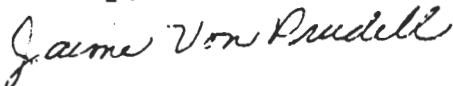
You will find a heading in the "Field Retrofit Notice" called "STATUS". Together with some qualifying information, one of two key words will always be found under this heading: "Discretionary" and "Mandatory." "Discretionary" means that you should exercise your own judgement in implementing the retrofit. This type of retrofit is usually a product improvement or a precautionary design change, or the solution to a problem affecting a minority of units. The attached Field Retrofit Notice is an example of this type.

"Mandatory" is reserved for circumstances under which the retrofit MUST be implemented:

- 1) To assure the safety of the end user.
- 2) To stop the reoccurring loss of data in the user's system.
- 3) To make operable a feature or configuration of a system which is within the advertised capability of the system.

If you have any questions concerning the attached Field Retrofit Notice or any subsequent one, feel free to contact our Field Support Department.

Sincerely,



Jaime VonPrudell
Technical Writer

JVP:jm

encl.

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FIELD RETROFIT NOTICE 4/1/79

PRODUCT: Helios II, the following models:

Model 2, 117 V ac	300000
Model 2, 220/240 V ac	300021
Model 4, 117 V ac	304000
Model 4, 220/240 V ac	304001

ASSEMBLY: Formatter Assembly 301003 (F to G)

BRIEF DESCRIPTION OF RETROFIT:

This retrofit requires changing an IC and two resistors. These changes assure that the oneshots in the IC at U17 remain within their allowable timing durations. There is no change to the nominal time-out values or to their limits. There is no change to the function of the circuit.

STATUS: Discretionary

"Discretionary" means that the factory-authorized dealer should exercise his own judgement in implementing the retrofit, after reading the Retrofit Notice. The status "Discretionary" is contrasted with the alternate status, "Mandatory." A mandatory retrofit must be implemented in order to safeguard the user, the user's system, and/or the factory-authorized dealer and Processor Technology.

The modifications should be performed on all formatter units of a REV level of F or lower in order to eliminate the occurrence of a timing problem. In order for the revision levels of formatter assemblies to be able to be identified, the retrofit can be performed only on a REV F assembly. Any assemblies lower than F must first be brought to the F REV level. Update 731048 provides a procedure for bringing Formatter assemblies from REV E to REV F. If this retrofit is performed on assemblies of an earlier revision level, the resulting REV level will be undeterminable by the revision level system. This resulting assembly cannot be marked "G" (the next revision letter) and will not be able to be described for future retrofits. Similarly, if this retrofit is not made to an assembly, future retrofits cannot be made with the REV level of the assembly subsequently being identifiable.

HARDWARE MODIFICATION PROCEDURE:

Systems that have the indicated timing problem may have a tendency to display PTDOS errors including one or more of the following messages:

```
BAD DISK STRUCTURE
BAD FILE STRUCTURE
BLOCK SIZE CONFLICT
CAN'T FIND SECTOR
FILE ID CONFLICT
SECTOR CONFLICT
READ BACK FAILED
```

To determine whether the timing problem exists, follow the procedure below. A dual-trace oscilloscope is necessary.

- 1) It is recommended that all previous updates be performed first, bringing the formatter assembly 301003 to an F REV level.
- 2) Connect the Helios II to a known-good Sol, with the formatter positioned so that it can be examined with scope probes.
- 3) Turn the Sol OFF and then on again to reset the controller PCB.
- 4) Insert a formatted but expendable diskette in Unit 0.
- 5) In SOLOS Command Mode, enter the following short program:

```
ENTR C900 <CR>
:DB F0 3E DD D3 F5 D3 F7 C3 00 C9/ <CR>
```

Dump the program to verify that it is correct.

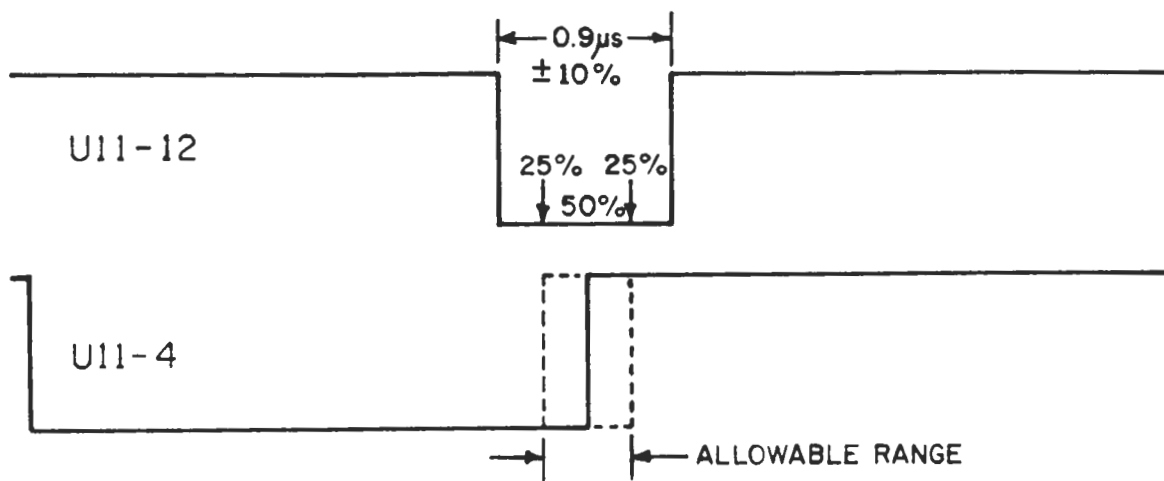
- 6) Execute the program by typing:

```
EX C900 <CR>
```

When the program is executed a click will be heard, indicating that the Unit 0 head is loaded. The only purpose of the program is to keep the head loaded while measurements are made on the formatter.

- 7) Set the time base on the scope to approximately 0.5 microseconds per division, and the sensitivity on both inputs to about 2 volts per division. Place one probe on U11, pin 12 and the other on U11, pin 4. These points represent the two outputs of the two oneshots in U11.

- 8) A waveform similar to that shown below should be observed.



- 9) The timing problem is indicated when the rising edge of the pulse on U11, pin 4 is not within the range indicated, with respect to the negative pulse on U11, pin 12. If the rising edge is within range, the timing problem is not indicated, and further troubleshooting should be done. If the rising is outside of the allowable range, follow the additional steps below.
- 10) Replace the 74LS123 at U17 with a 74LS221 (P/N 701147). The new part has a 1% timing tolerance, compared with a 15% tolerance on the old part.
- 11) Replace the 15K resistor at R1 with a 9.1K ohm, 5% resistor.
- 12) Replace the 5.1K resistor at R2 with a 3.3K ohm, 5% resistor.
- 13) On the component side of the assembly, in the top right-hand area near P2 is the silk-screened assembly number. Mark the REV letter "G" with indelible ink, or cover the existing revision letter with a label.
- 14) Repeat steps 3 through 7 above to observe the same waveforms. Confirm that rising edge of the waveform on U11, pin 4 is now within range.
- 15) Place this copy of the Field Retrofit Notice in the Helios II Disk Memory System Manual, P/N 730009, Second Printing, March 1978, behind the tab "Updates."

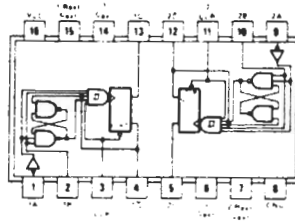
CORRESPONDING MANUAL UPDATE:

Revision pages incorporating the modifications in the assembly drawing, the schematic, and the parts list will be issued with the manual update, 731014, which concerns a new controller/formatter assembly configuration.

74LS221 PIN CONFIGURATION DIAGRAM

DUAL MONOSTABLE MULTIVIBRATORS

221



See page 6-68

SN54221 (J, W) SN74221 (J, N)
SN54LS221 (J, W) SN74LS221 (J, N)

CHANGE NOTICE #4 Helios II

SUBJECT: Modifications to Controller PCB Assy 301000

A) PRELIMINARY INSTRUCTIONS

- 1) This CN applies to certain controller PCB's assembly levels only. The result of the change is to bring previous assembly levels to the "E" assembly level. Identify your controller assembly as follows:
 - a) Orient the board with the component side up so you can read the silkscreened designation:

"ASSY. NO. 301000." If this designation is marked or labeled with the suffix "E," or later letter, or if there is an "E" or later letter, marked or labeled in the upper left-hand corner of the board, you do not have to perform this modification.
 - b) If the assembly number or board corner is not marked or labeled with a letter revision, or is marked with an earlier letter than "E," please continue reading this change notice.

NOTE:

Note the distinction between the assembly number revision level on one hand, and on the other hand, the "PC" number revision level. This latter number, which is etched on the solder side of the board, refers to the bare board; whereas, the "assembly" is the board assembled with components to a certain configuration.

- 2) These modifications to the controller are improvements and corrections which are aimed at problems which are encountered under certain system conditions. If your system is working satisfactorily, it will probably continue to do so without these changes; however, if you are having a problem, these changes may correct it. It is strongly recommended that you make these changes regardless, in order to avoid possible future problems, and to assure that you have a standard controller at the current revision level, which may be a prerequisite for possible future changes.
- 3) Before starting the changes, be sure you have read "Modifying PCBs," Section 3.3 (Helios Disk Memory System Manual, 730009, Second Printing, March 1978). The jumper wire used should be #24 not #30, unless otherwise noted.

B) CONTROLLER PCB MODIFICATIONS FROM 730009, 1st Printing

- 1) Modify your controller PCB by making two trace cuts as follows:
 - c) Refer to Fig. 8-3, Controller PCB, Assembly Drawing.
 - d) On the trace side of the PCB, start from U36-10 and follow the trace upward about 1 inch to a pad. Call this pad "A". The trace feeds through the board at pad A. Flip the PCB over and locate pad A on the component side. (This is called out as "Point A" on the assembly drawing. On the components side, cut the trace leading to pad A. This step disconnects U36-10 from U37-1 and U4-14. U37-1 and U4-14 are still connected. U36-10 is still connected to pad A.
 - e) On the component side, cut the trace which connects U35-4 to U35-14. Cut it near pin-4. This is a +5V trace.

NOTE

The assembly drawing shows the jumpers mentioned in the following instructions to be on the component side of the PCB; however, they should be installed on the trace side using the IC pins for connecting points.

- 2) Modify your controller PCB by installing jumpers as follows:
 - a) Install and solder an insulated jumper connecting U35-4 (Point C on the assembly drawing) to the pad located between U35 and U36 (designated "Point D" on the assembly drawing). The pad at point D is at the U35 end of a trace coming from U37-7.
 - b) On the component side of the PCB, locate pad B (designated Point B on the assembly drawing). Compare the following description to be sure you have found it. On the component side of the board, 4 traces come out from under the right end of U0. Follow the uppermost of these (nearest U0-8) to a pad about 1/4-inch from the right end of U0. (The arrow pointing to Point B obscures this trace on the assembly drawing but you can see it on the PCB itself.) This is pad B.
 - c) Install and solder an insulated jumper connecting pad B and pad A (point A) described in this section, step 1.d. U36-10 is now connected to U2-6 and U0-12.
- 3) Install the 3 augat selector pins on the component side of the controller PCB as follows:

- a) Refer to the assembly drawing for the controller, Fig. 8-3. The locations for the pins are pads just below the first row of IC's starting at U6. These pads are labeled from left to right: "FX", "EX", and "C". The pads are circled on the drawing. They are connected to traces as follows:

C	U23-5
EX	Between U7-12 and U6-5
FX	U6-6

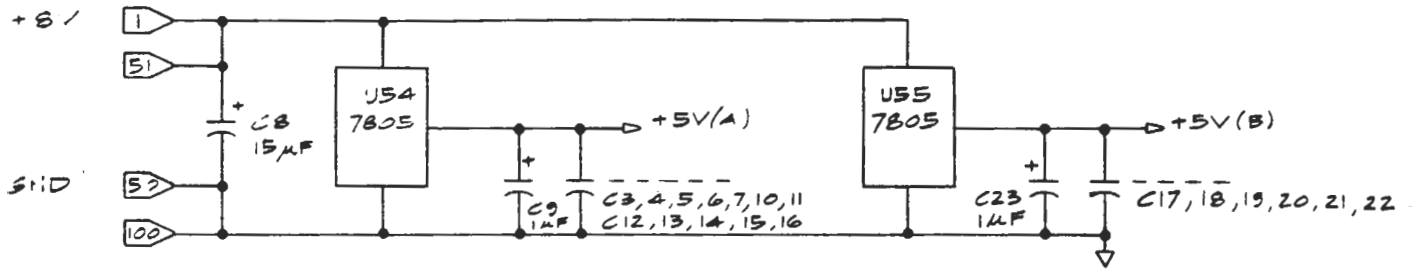
- b) Insert the first pin in its respective location. Hold the pin in place with a needle-nose pliers. (Do not use your hand; it will be hot.)
- c) Turn the PCB over and solder the pin from the trace side.
- d) Install and solder the two remaining pins in the same manner.

C) TRACE AND JUMPER MODIFICATIONS TO CONTROLLER PCB

(Refer to Fig. 8-3, Assembly, Controller PCB, page revision A and Fig. 8-9, Schematic, Controller PCB, page revision A. All the following trace cuts are marked with an "X" and called out with arrows on Fig. 8-3, Assembly, Controller PCB; all jumpers are shown as heavy dashed lines on the component side, although the jumpers are to be installed on the solder side.)

- 1) On the solder side of the board ("trace" or "circuit" side), cut the trace at U15-1. (U15, pin 1). See Fig. 8-3, Detail A.
- 2) On the solder side of the board, find U50-1. Follow the trace leading from it 1/8-inch to a feed-through pad. Using insulated jumper wire, connect this pad to U15-1.
- 3) On the component side, locate U31. A trace emerges from under the U31 socket between pins 9 and 10. Another emerges between pins 10 and 11. Cut both traces.
- 4) On the solder side, using insulated jumper wire, connect U30-9 to U31-11, and U30-10 to U31-6.
- 5) On the component side of the board, a wide trace connects pins 8 of U41 through U51. Cut it between U48 and U49.
Cut it again between U46 and U47.
- 6) On the solder side, make the following ground connections using #22 wire (bare or insulated as specified):
 - a) U49-6 to U50-12 (Bare wire OK, suspend it over the traces.)
 - b) U48-8 to connector P1, pin 50 (insulated wire).
 - c) U46-8 to connector P1, pin 50 (insulated wire).

- 7) On the solder side of the board, point E is a pad 1/2-inch below U7-14 (toward the P1 connector fingers [pads]). A long trace extends from point E toward the fingers. Cut this trace near point E, as shown in Detail B, Fig. 8-3.
- 8) Connect point E to U18-10 with an insulated jumper wire.
- 9) Place a label marked "REV E" as shown in Note 3 of Fig. 8-3, Assembly, Controller PCB.



POWER SUPPLY

REF. DESIGNATION TABLE			
FIRST USED	LAST USED	NOT USED	DELETED
U1	U55		
R1	R9		
P1	P4		
C1	C23		
CRI			
J4		J1-J3	

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
 - A ALL CAPACITOR VALUES ARE .047 AND UNITS IN µF.
 - B ALL RESISTOR VALUES ARE IN OHM, 1/4W, 5%
2. EACH PIN OF P2 IS TO BE CONNECTED BY THE MATING CABLE TO THE PIN BEARING THE SAME NUMBER AT EACH OTHER CONNECTOR SERVED BY THAT CABLE.
3. EACH PIN OF P3 IS TO BE CONNECTED BY THE MATING CABLE TO THE PIN BEARING THE SAME NUMBER AT P3 OF THE FORMATTER
4. ALL ODD NUMBERED PINS ON P2 AND P3 ARE GROUND.

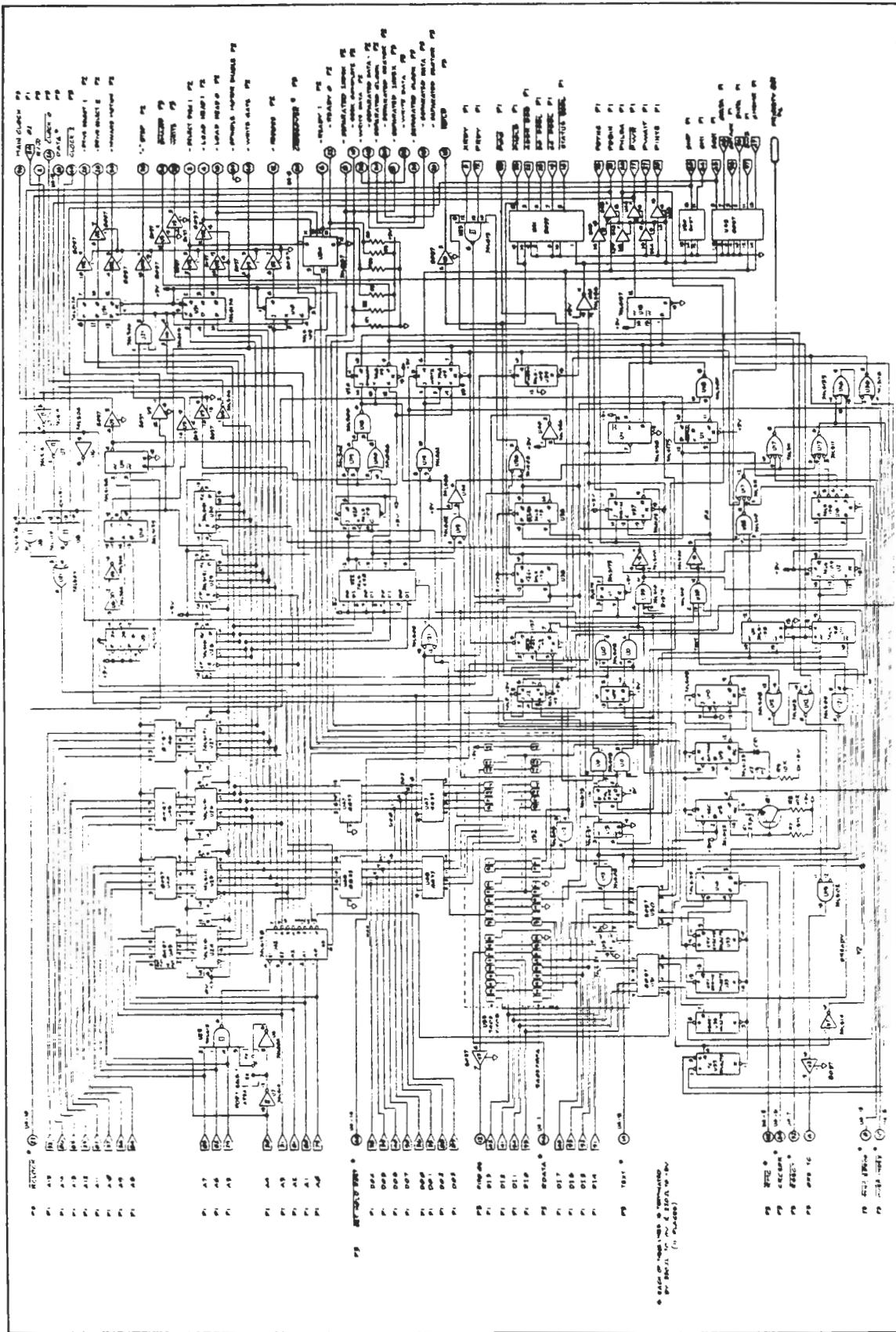


Fig. 8-9 Schematic, Controller PCB (301002).

REV A

ONE

Helios II

FIELD RETROFIT NOTICE 4/3/79

PRODUCT: Helios II, the following models:

Model 2, 117 VAC 300000
 Model 4, 117 VAC 304000
 (220/240 VAC models are not affected.)

ASSEMBLY: Regulator PCB Assembly, Model 2, 302000 (G to H)
 Regulator PCB Assembly, Model 4, 304025
 Rear Panel Assembly, Model 2, 304000 (G to H)
 Rear Panel Assembly, Model 4, 304030 (C to D)

BRIEF DESCRIPTION OF RETROFIT:

The 40 V, 10,000 microfarad electrolytic capacitor at C8 on the regulator is to be replaced with a 50 V, 7,300 microfarad capacitor. (ECN 10517 and 10446)

The fuses on the rear panel assemblies are to be replaced with ones of lower value. A label must be applied to cover the existing silkscreened values. (ECN 10525)

STATUS: MANDATORY

The capacitor on the regulator and the fuses on the rear panels must be changed to safeguard the user, the service technicians and the Helios II units. All units in inventory and all units previously sold, now in the hands of the users, must be retrofitted. These changes are also necessary to avoid possible liability damages against the factory-authorized dealers and Processor Technology. Units not retrofitted represent a serious safety hazard.

The Warranty Repair Department of Processor Technology will provide the parts to the retrofitting dealer on a one time basis. All the dealer need do to obtain the parts is to provide Warranty Repair with a list of serial numbers of the units to be retrofitted.

PRIOR RETROFITS:**A) Regulator**

Change Notice #3, 10/77, P/N 731032, contained a retrofit which brought the regulator 302000 from a REV B to a C. The retrofit in CN #3 should be performed first, for safety reasons and so that the units can be marked and readily identified by the revision level and

retrofit systems. Revisions to the regulator from C to G were factory changes which required no retrofits.

B) Rear Panel

Revisions up to C on the Model 4 rear panel and revisions up to G on the Model 2 rear panel were factory changes requiring no field retrofits.

PARTS REQUIRED:

<u>ITEM</u>	<u>P/N</u>	<u>QTY</u>	<u>DESCRIPTION</u>	<u>DESIGNATION</u>
1	707050	1	CAP, 7,300 Microfarad; Alum. electrolytic, 50V	C8
2	723021	1	1A FUSE, SLO-BLO (Model 2)	F2
3	723022	1	6.25A FUSE, SLO-BLO (Model 2 and 4)	F1
4	723016	1	2A FUSE, SLO-BLO (Model 4)	F2
5	732001	1	LABEL, Fuse, pair, 1A, 6.25A (Model 2)	
6	732002	1	LABEL, Fuse, pair, 2A, 6.25A (Model 4)	

HARDWARE MODIFICATION PROCEDURE:

A) Regulators: Model 2, 302000 and Model 4, 304025

(The procedure is the same for both models except for marking the new REV letter.)

- 1) Remove the top cover of the Helios II.
- 2) Remove the rear panel.
- 3) Remove the regulator PCB assembly.
- 4) Unscrew and remove the 40V, 10,000 microfarad capacitor at C8.
- 5) Install the 7,300 microfarad, aluminum, electrolytic capacitor, 50V, P/N 707050, at C8.
- 6) Mark an adhesive label with the letter "H" and apply the label to the component side of the Model 2 regulator so that it covers the previous REV letter. The REV letter follows the assembly number which is silkscreened on the the PCB just above C8. (Refer to Fig. 8-8, Note 2, Helios Disk Memory System Manual, 730009, 2nd Printing, March 1978.)

302000, the Model 2 regulator is a subassembly of the Model 4 regulator 304025. Do not mark the REV level of the Model 4 regulator.

- 7) Re-install the regulator and rear panel according to the Disk Memory System Manual, 1st Printing, 730009, August, 1977, 3.5.7, "Power Supply Assembly," steps 2 through 10.

B) Rear Panel, Model 2, 305000

- 1) Apply the label provided by Processor Technology that reads "1A SB" to the rear panel above the upper fuse so that it covers the designation "3.2A SB."
- 2) Apply the label that reads "6.25A SB" below the lower fuse so that it covers the designation "7A SB."
- 3) Remove the 3.2 A SLO-BLO fuse from the upper fuse holder and replace with a 1 A SLO-BLO fuse.
- 4) Remove the 7 A fuse from the lower fuse holder and replace with a 6.25A SLO-BLO fuse.

C) Rear Panel, Model 4, 304030

- 1) Apply to the rear panel the label that reads "2 A SB" above the upper fuse holder so that it covers the designation "3.2 SB."
- 2) Apply the label that reads "6.25 SB" below the lower fuse holder so that it covers the designation "7 A."
- 3) Remove the 3.2 A fuse from the upper fuse holder and replace with a 2 A SLO-BLO fuse.
- 4) Remove the 7 A fuse from the lower fuse holder and replace with a 6.25A SLO-BLO fuse.

CORRESPONDING MANUAL UPDATE

Revision pages or a new edition of the Helios II Disk Memory System Manual (Helios II Technical Manual) will be issued at a later date to reflect the above changes.

POWER CONSUMPTION OF Sol SYSTEM COMPONENTS

Most components of a Sol system are often plugged into the convenience outlets of the Helios II floppy disk drive. Care should be taken not to overload the AC current carrying capacity of the convenience outlets. The fuse protecting these outlets may blow when the rating on the F1 label (6.25A is exceeded). The AC current consumption during normal operation for components of a typical Sol system is given as follows:

Sol-20	1.5A
Helios II Model 2	0.8A
Helios II Model 4	1.6A
TV/Monitor	0.4A
SolPrinter 2 & 2E	1.7A
SolPrinter 3	2.0A

INSTRUCTIONS FOR
REPLACING HELIOS POWER SUPPLY CAPACITOR C8

SEPTEMBER 1, 1981

1. Unplug all cables from the back of your Helios and move the cabinet to a place where you can easily work on it.
2. Remove the three screws "A" (Figure 3-16) which hold the cover in place. On the top-front of the cabinet there is a black recessed sliding latch. Slide it to the rear and the cover is released. Lift cover off and set aside.
3. Locate the aluminum can marked C8 on Figure 3-19. That's the one that should be 50 VDC rated, but may only be 40 VDC in your Helios. Check the printing on the can to determine if you need to replace the capacitor. If not, use this opportunity to look for dirt inside the cabinet that should be vacuumed out and close the cabinet by reversing your steps.
4. If C8 must be replaced, locate the power harness and the signal ribbon cable where they plug into the disk drive's printed circuit board (PCB). Refer to Figure 3-22.
5. Notice the orientation of the connectors before removing them by sliding to the rear. The colored edge of the ribbon cable is down. The power cable has a polarizing blank in one of the pin locations.
6. Remove the 6 screws "B" (Figure 3-16) from the rear panel. Carefully lift the panel without pulling hard on the wires still connected to it. In a 4-slot Helios, it may be necessary to unplug some of the wiring that attaches to terminals on the rear panel to have adequate freedom. If so, be sure to label them with tape somehow.
7. Locate the black heatsink on the regulator board and remove the three screws "C" which hold it to cabinet base (Figure 3-15). Don't lift it yet.
8. Locate the two screws "D" (Figure 3-15) at the opposite side of the PCB. Loosen them completely. The board is now free. Lift it (carrying the "D" screws with it) and turn it over enough to access the screws on its underside. Be careful not to misplace the two metal cylinders which are stand-offs that are part of the screw "D" mounting. In some units, these are loose; in others, they are screwed into the base.
9. Remove the two pan-head screws that mount the capacitor C8 to the PCB. Notice that one of the screw holes has a plus sign (+) near it on the PCB. This is the capacitor's positive terminal. The capacitor also has a plus sign on its base. Replace the old capacitor with the new one, being sure to match the same polarity. That is, match the positive terminal to the

positive hole. Snug the screws (which should also have lock washers on the same side as the screw heads) but don't overtighten. If your old capacitor has already burned out and the board has been charred, be sure to carefully scrape the loose char, rinse to remove electrolyte that leaked out, and allow to dry before mounting the new capacitor. You may need to add some solder to repair damaged traces on the board.

10. If your Helios was purchased (shipped from PTC) prior to 10-10-77 as an assembled unit, or purchased as a kit, now is a good time to make Helios Change #3 if it hasn't been done already. This is the change which alters the main regulator (U1) pads to prevent accidental shorting to the heatsink. See Change Notice #3 (PTC ECN number 10141) dated 10/77. If your PCB is marked Rev C or later, you don't need to do Change #3. If your board is Rev B or earlier, you should do it.

11. Re-mount the regulator PCB, being sure to get the stand-off's properly installed on screws "D". Insert the screws and start them, but don't fully tighten until all screws "C" and "D" are in place and the board is properly situated.

12. IMPORTANT: It is wise at this point to prop up the back panel, check that no wires have come off of their connection, and install the AC power cable on the back panel. (Be careful--line voltage is present.) Plug in and turn on the Helios, without the power or signal cables connected to anything. Use a voltmeter to verify that the following voltages are present at the DC power cable which will plug into the disk drive. Check these by putting the negative lead from the voltmeter into a white (ground) pin (pins 6, 7, 8, 9) and the positive lead into the pin in question. For pin 10 (-5 VDC), put the negative lead of the meter into pin 10 and the positive lead into a ground pin, unless your meter will directly read negative polarity.

Pin 1	No connection	
2	Red wire	+4.75 VDC to +5.25 VDC
3	Blue wire	+7.0 VDC to +10.0 VDC
4	Polarizing key	
5	Yellow wire	+21.6 VDC to +26.4 VDC
6	White	Ground (zero)
7	White	Ground (zero)
8	White	Ground (zero)
9	White	Ground (zero)
10	Green wire	-5.5 VDC to -4.5 VDC

If you have checked these voltages, turn off and unplug the Helios and allow time for the voltages to discharge. With the cable not connected to a load, it takes quite a while to return back to zero volts. In my unit, it took about 15 minutes to get to a small residual voltage, which I then shorted to ground through a jumper wire.

13. If the power cable is back down to zero volts everywhere, plug it into the disk drive. Also plug the signal cable back on, observing the polarity (colored edge down).
14. Reverse your steps to close up the Helios cabinet.
15. Plug cables back in and turn the system on. Bootload a disk that does not contain valuable data if possible. Verify the system by using the DISKT program, if you know how to do it. (DISKT and other test programs are available from PROTEUS.) Otherwise, verify by running a program from disk.
16. Processor Tech also recommends replacing the 3.2 amp fuse with a 1 amp Slo-Blo fuse in a 2-slot Helios (2 amp in 4-slot Helios). Also the 7 amp Slo-Blo should be replaced with 6.25 amps Slo-Blo. Put labels showing the correct fuse ratings over the designation on the back panel. This should help prevent a board burnup if the Helios goes out again.

Congratulations, you've just done a capacitor transplant!

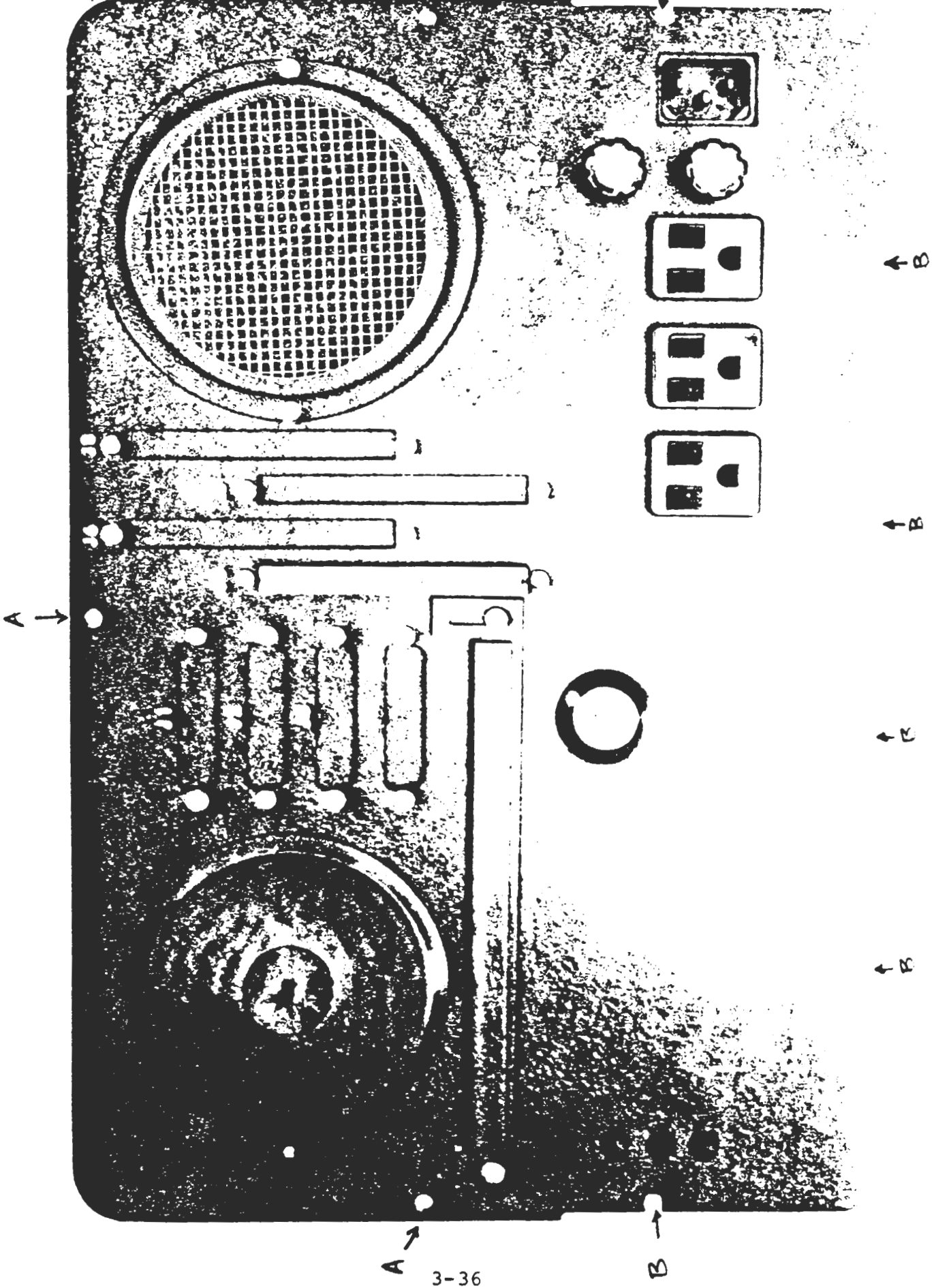


Fig. 3-16 Helios II Rear Panel, Outside View

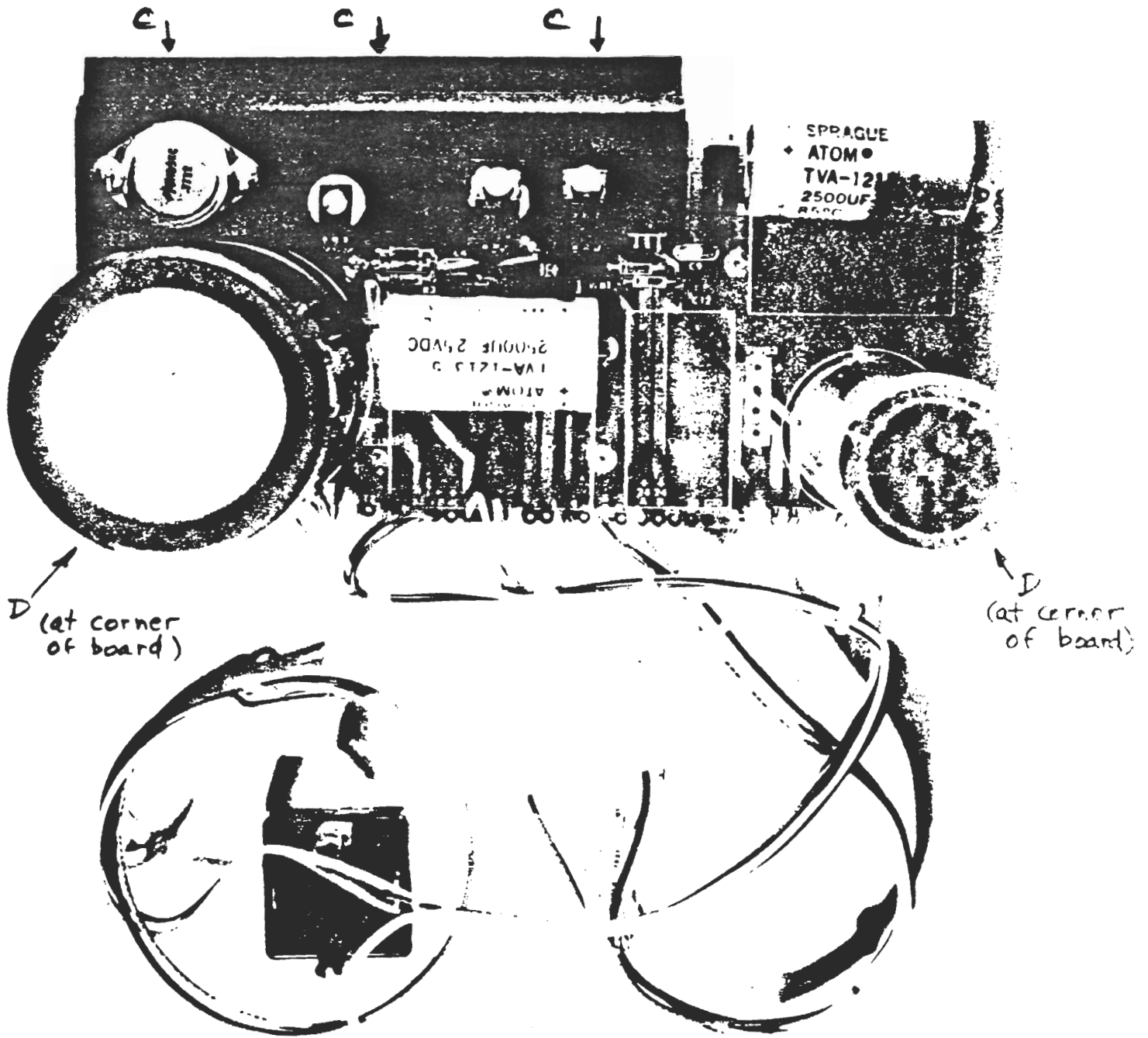


Fig. 3-15 Regulator PCB and Wiring Harness

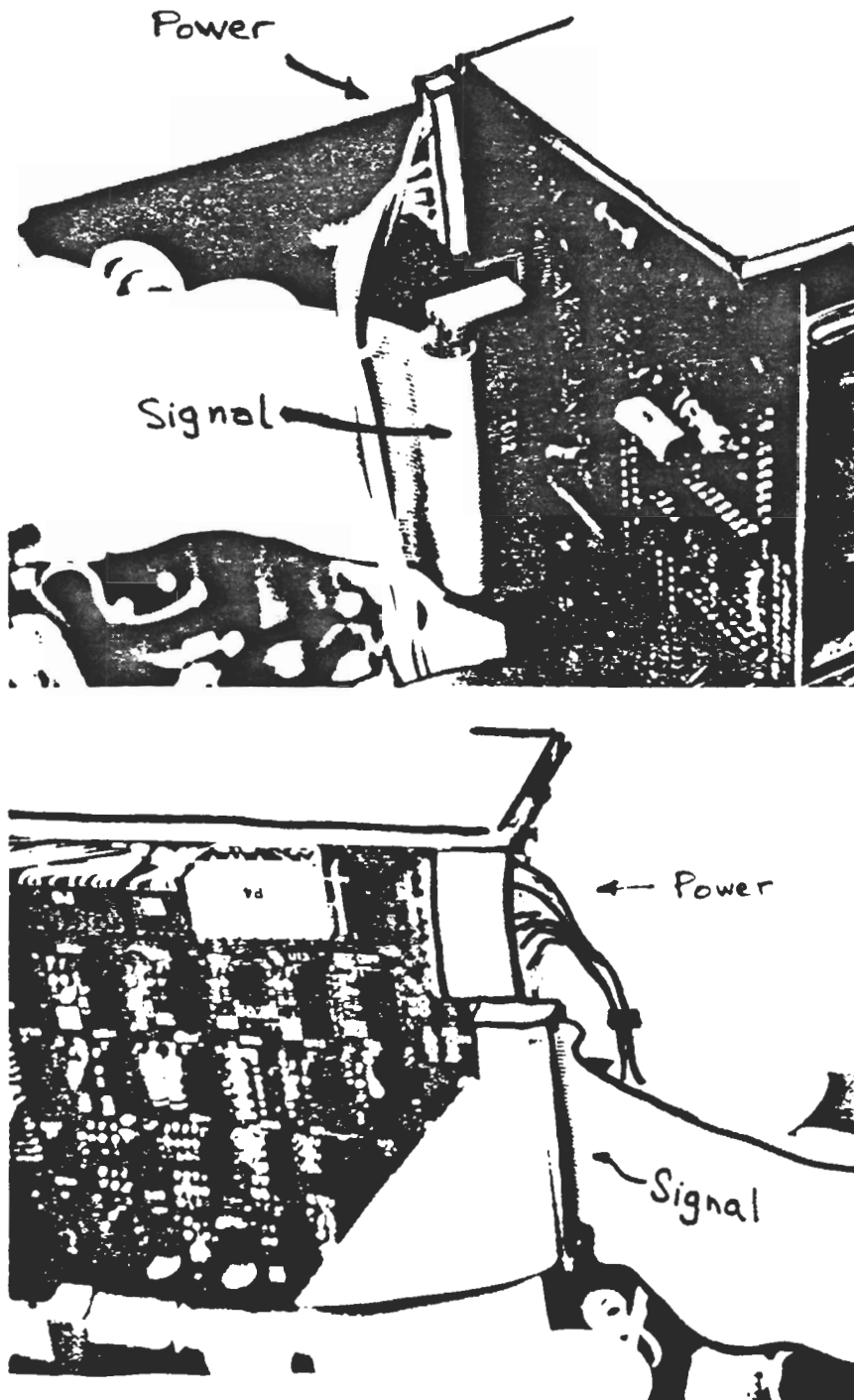


Fig. 3-22 Disk Drive DC Power and Signal Connectors

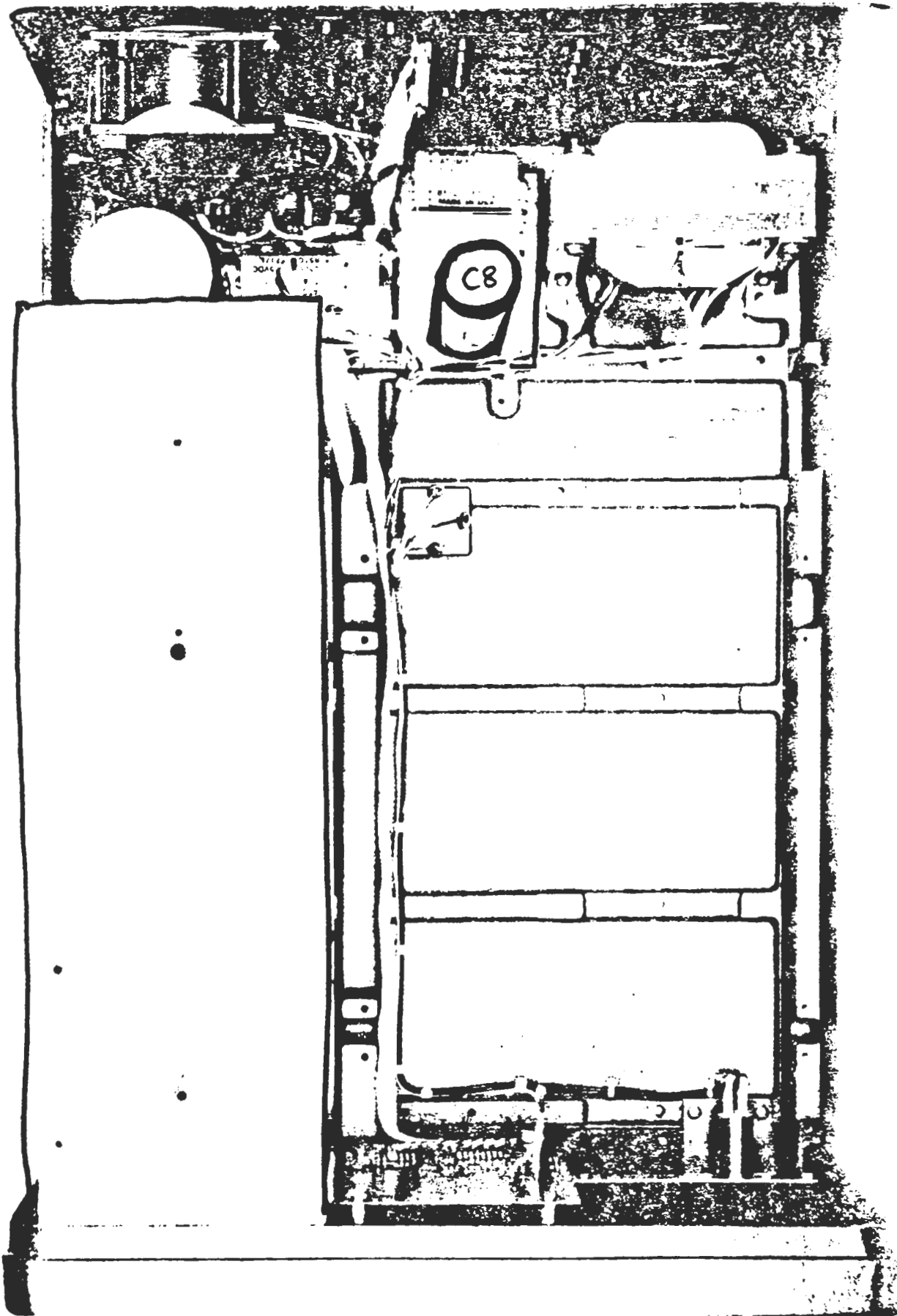


Fig. 3-19 Helios II Disk Drive Cabinet, Inside Top View

Processor Technology
Corporation

7100 Johnson Industrial Drive
Pleasanton, CA 94566

(415) 829-2600
Cable Address PROCTEC

MANUAL UPDATE 4-10-79

MANUAL:

Helios II Disk Memory System Manual (Helios II Technical Manual),
Literature Kit, P/N 730009, Second Printing, March, 1978.

SUBJECT:

This update documents new Controller and Formatter PCB Assemblies. These assemblies are part of Helios II, the following models:

Model 2, 117 V ac	P/N 300000
Model 2, 220/240 V ac	P/N 300021
Model 4, 117 V ac	P/N 304000
Model 4, 220/240 V ac	P/N 304001

No hardware modifications to existing assemblies are required by this update. The new assemblies described in this update are assembled only at the factory.

BRIEF DESCRIPTION OF SUBJECT MATTER:

The new controller/formatter configurations accomplish the following objectives:

- 1) To incorporate into the printed circuit board previous engineering changes which were installed by means of cuts and jumpers.
- 2) To improve the ground circuitry to increase noise immunity. This is accomplished by providing additional cross links interconnecting 0-volt points. These cross links are an attempt to reduce the inductance among all 0-volt points on the board. S-100 bus pins 53, 55, and 70 have been connected to 0 V on the controller.
- 3) To provide for the alternate use of either of two sources for FIFO's which were installed on the controller at U52 and U53 (Assy 301000 REV J and earlier). Most of this update is concerned with this purpose.

REVISION PAGES:

Revision pages, including foldouts, are included in this update. It is suggested that dealers transfer obsolete pages to a separate Helios binder clearly labeled "HISTORY" on both the cover and spine. The following is a list of the pages attached to the update:

Fig. 8-6, 3/10/79, Controller PCB Assembly (301000-L & 301030-B)*
 Fig. 8-7A, 3/10/79, Formatter PCB Assembly (301003-H)
 Fig. 8-7B, 3-10-79, Formatter PCB Assembly (301040-A)
 Fig. 8-11A, 3/10/79, Controller PCB Schematic (301002-K),
 Sheet 1 of 2
 Fig. 8-11B, 3/10/79, Controller PCB Schematic (301002-K),
 Sheet 2 of 2
 Fig. 8-12A, 3/10/79, Formatter PCB Schematic (301005-H),
 Sheet 1 of 2
 Fig. 8-12B, 3/10/79, Formatter PCB Schematic (301005-H),
 Sheet 2 of 2

Page 9-13, 3/10/79, Parts List - Controller PCB Assembly
 (301000-L & 301030-B)*
 Page 9-14, 3/10/79, Parts List - Controller (Continued)
 Page 9-15A, 3/11/79, Parts List - Formatter PCB Assembly
 (301003-H)
 Page 9-15B, 3-10-79, Parts List - Formatter PCB Assembly (301040-A)
 Page 9-15C, 3-10-79, Parts List - Formatter PCB Assembly
 (301040-A) (Continued)
 Page 9-16, 3/10/79, Parts List - Regulator PCB Assembly, Model 2
 (302000-J)

(Pages 9-13/9-14 and 9-15A/9-15B, and 9-15C/9-16 are printed
 back-to-back.)

*Note: ECN 1015 removes P4 and J4 (rarely used priority connector)
 from the controller assemblies and changes the REV's on the
 assemblies (303000-K to L and 301030-A to B). This is a
 factory change; no retrofit is required.

CHANGES TO BE MARKED BY HAND:

In the Parts List, page 9-9, System Assembly, Model 2, add to

Item 5: Part Number "301030"
 QTY "1"
 Description "Assy, PCB, Controller (Alternate)"

Item 6: Part Number "301040"
 QTY "1"
 Description "Assy, PCB, Formatter (Alternate)"

CURRENT PUBLICATIONS (PRIOR REV LEVELS):

The controller and formatter assemblies described in this update are
 based on new printed circuit boards which incorporate the modifications
 described by the following prior Helios II updates:

CHANGE NOTICE #4, Controller Mods. (D to E)
 (E to F required no retrofits)
 731067, Controller Mods. (G to H)

731071, Controller Mods. (H to J)
 731048, Formatter Mods. (E to F)
 731013, Formatter Mods. (F to G)

Dealers are advised to keep the proper updates in the Update Section of the service copy of their manual in order to be able to update and service assemblies of earlier revision levels.

DETAILED DESCRIPTION OF CHANGES TO CONTROLLER AND FORMATTER ASSEMBLIES

A) COMPATIBILITY OF CONTROLLER/FORMATTER REVISION LEVELS

The alternate use of two different FIFO types requires two separate configurations for the controller assembly, although both are built up from the same printed circuit board. The formatter also now has two different assembly configurations. Therefore the new controller and formatter assemblies will each have two assembly numbers to identify them. They must be used only in matched pairs as shown in the following table.

CONFIG.	CONTROLLER	FORMATTER	LOCATION AND TYPE OF FIFO
A	301000-K	301003-H	9403's on controller PCB
B	301030-A	301040-A	74S225's on formatter PCB

Designations "A" and "B" are chosen only for the sake of explanation in this update.

The letter suffix is the current assembly revision level. Higher or lower revision levels of the same assembly numbers listed are also compatible. For example, an earlier updated controller (301000) or formatter (301003) is compatible with a configuration A controller or formatter because the assembly numbers correspond. Configuration B controllers and formatters however are not compatible with earlier controllers and formatters nor with configuration A controllers and formatters. A controller assembly 301030 is compatible only with a formatter assembly 301040. Do not attempt to modify assemblies of one configuration to become the other configuration.

B) DESCRIPTION OF CHANGES TO ACCOMODATE ALTERNATE FIFO'S

1) General Changes

In previous assemblies, Fairchild 9403 FIFO's have been placed on the controller (Assy 301000 REV J and earlier). In the new controller/formatter configurations, both the controller and the formatter have been redesigned to provide for the 74S225's being installed on the formatter as an alternative (Configuration B) as well as for the 9403's being installed on the controller (Configuration A). Placing the 74S225's on the formatter was necessary because the 74S225 is not a direct replacement for the 9403 and additional circuitry made up of eight IC's must be used to enable the 74S225's to perform the same functions as the 9403's. These IC's and the 74S225's have been placed on the formatter PCB where space was available. Consequently there are extensive changes to the formatter assembly which are reflected in its new assembly drawing and schematic. The added circuitry is shown on the new formatter schematic as a single large optional area. Changes to the external signal paths of this

circuitry are summarized in Table B, "Formatter Signal Changes." The internal connections are too extensive to itemize here. They are shown on the new schematic for the formatter, Figs. 8-12A and 8-12B.

The additional power consumption of the added IC's require a heatsink and a second regulator on the formatter assembly 301040.

Changes to the controller are significant but much less extensive.

Option jumpers on both the controller and formatter are installed as determined by which type of FIFO is being used. These option jumpers are listed in tables on the new controller and formatter schematics. The controller and formatter schematics apply to both their respective assemblies.

There is no change to the interconnecting cables; however, placing the 74S225 FIFO's on the formatter requires the redefinition of several signals in the cable connecting P3 of the controller to P3 of the formatter. The redefined signals are listed in the following table:

Table A. Controller/Formatter Signal Changes

CONTROLLER/ FORMATTER P3 CONNECTOR PIN NUMBER	PREVIOUS CONTROLLER/ FORMATTER DESIGNATIONS	CONFIGURATION A DESIGNATIONS	CONFIGURATION B DESIGNATIONS
2	R/W Driven by Controller; terminated by by U3 on formatter.	Not Used. Terminated by U4-7 on controller.	IR (Input Ready) Terminated by U4-7 on the controller. Originates on formatter U1-9.
12	FIFO QS	FIFO QS	$\overline{\text{NORMALR}}$
18	$\overline{\text{HOLD}}$	$\overline{\text{BUSTR}}$	$\overline{\text{BUSTR}}$
44	RDATA	RDATA	OR (Output Ready)

2) Summary of Configuration A Changes (Uses 9403's on controller)

In configuration A, 9403's are placed on the controller. The 74225's and the eight IC's which support them are absent from the formatter. The jumpers on the controller and formatter are configured to support the 9403's.

Formatter 301003 does not require an S-100 bus connector if ground and +8V are supplied via it P2 connector.

3) Summary of Configuration B Changes (Uses 74S225's)

The 9403's are absent from the controller and the 74S225's together with their supporting IC's (U33 through U42) are installed on the formatter. Jumper options are installed to

support the 74S225's. On the controller, the DO bus driver inputs (U47-9 and U48-9) are disabled, being tied to +5 V.

Formatter 301040 requires access to the DI and DO lines; therefore, its P1 must be mounted in an S-100 bus connector. (See Table B.)

4) 74S225 Pin Configuration Diagram

5474 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

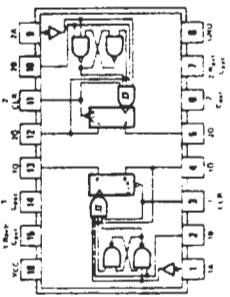
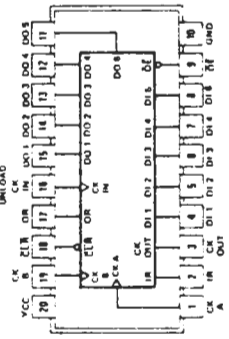
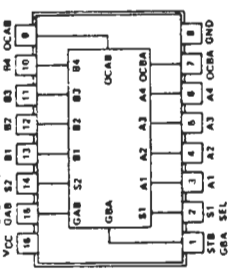
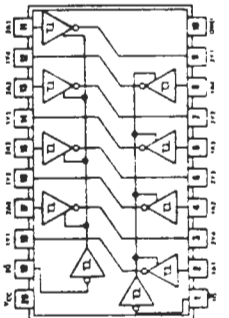
<p>221</p> <p>DUAL MONOSTABLE MULTIVIBRATORS</p>  <p>SN54221 (J, W) SN74221 (J, N) SN54LS221 (J, W) SN74LS221 (J, N)</p> <p>See page 6-68</p>	<p>225</p> <p>ASYNCHRONOUS FIRST IN, FIRST OUT MEMORIES</p> <p>16 5-BIT WORDS</p>  <p>SN74S225 (J, N)</p> <p>See Bipolar Microcomputer Components Data Book, LCC4270</p>	<p>226</p> <p>4-BIT PARALLEL LATCHED BUS TRANSCEIVERS</p> <p>3-STATE OUTPUTS</p>  <p>SN54S226 (J, W) SN74S226 (J, N)</p> <p>See page 7-345</p>	<p>240</p> <p>OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS</p> <p>INVERTED 3-STATE OUTPUTS</p>  <p>SN54LS240 (J) SN74LS240 (J, N) SN54S240 (J) SN74S240 (J, N)</p> <p>See page 6-83</p>
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Table B. Formatter Signal Changes

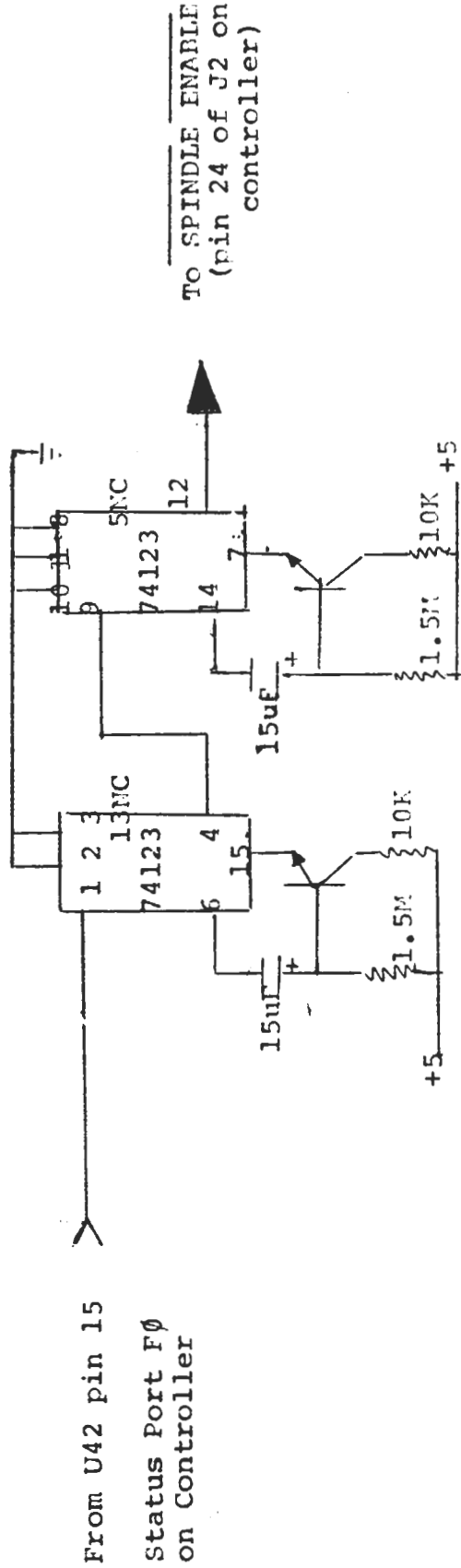
SIGNAL NAME	CHARACTERISTIC LOCATION	301003-H CHANGE	ADDED TO SIGNAL PATH IN ASSM. 301040-A
DI0-7	No Connection	Traces go to empty IC spaces	Inputs of 74LS244 at U40.
DO0-7	No Connection	Traces go to empty IC spaces	Outputs of 74LS244 at U40.
RDATA	U29-10	Traces go to empty IC spaces	U42-3
QS	U6-4	Traces go to empty IC spaces	U37-3
<u>WRITE</u>	U3-4	Traces go to empty IC spaces	U33-13
BCTC	U13-15	Traces go to empty IC spaces	U34-5
<u>BCTC</u>	U24-10	Traces go to empty IC spaces	U37-15
BCQD	U13-11	Traces go to empty IC spaces	U35-11
TEXT	U11-14	Traces go to empty IC spaces	U34-5
MAIN CLOCK	U3-7	Traces go to empty IC spaces	U33-1, U34-1
<u>CLOCK 2</u>	U3-6	Traces go to empty IC spaces	U33-9
<u>CROSSOVER</u>	U20-8	Traces go to empty IC spaces	U34-4, U38-18, U39-18

User-Originated Updates

Spindle Disable Circuit (Automatic)
Spindle Disable Circuit (Programmable)

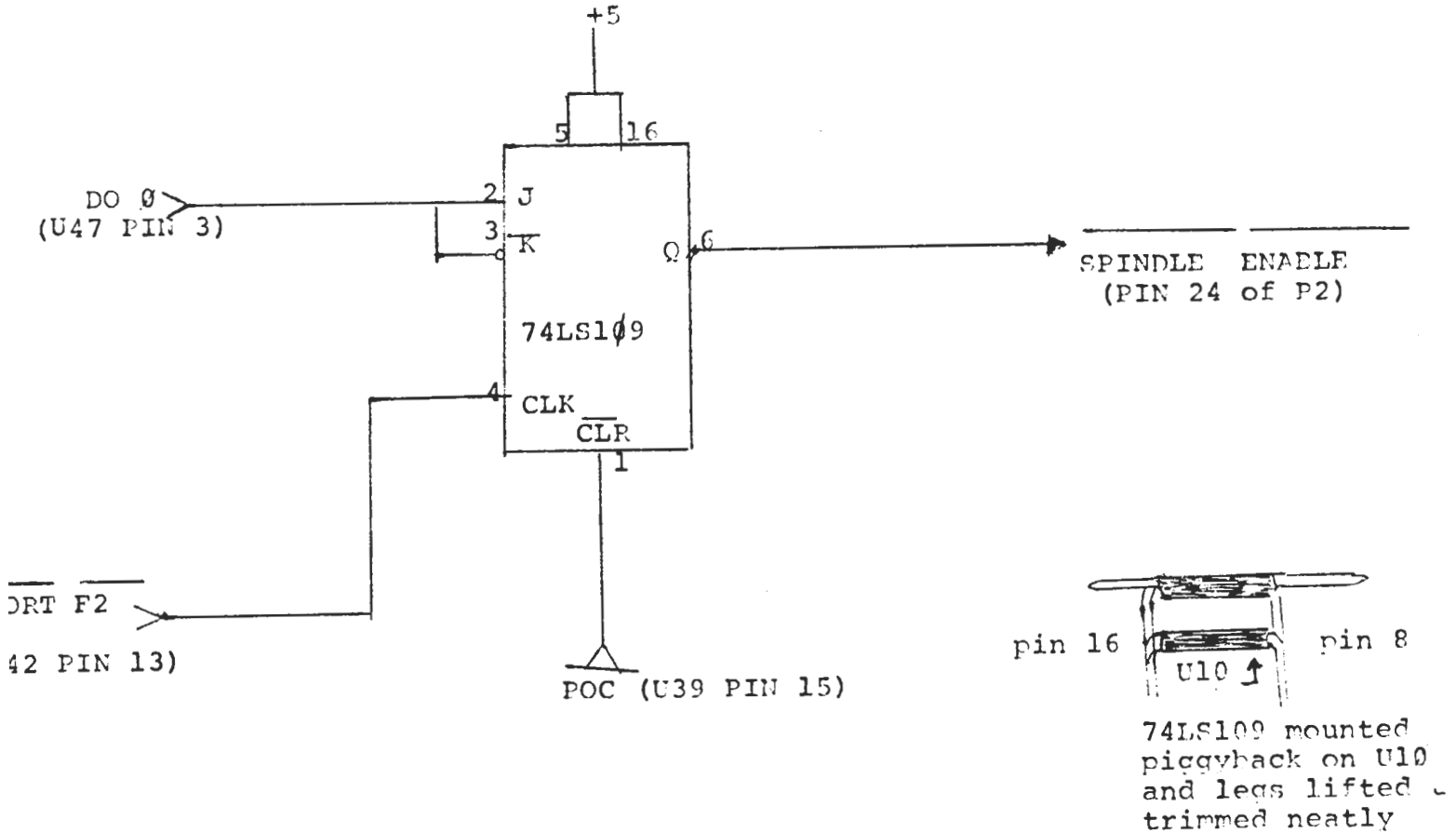
Requires pin 24 of Controller J2
be cut (isolated from ground)

74123 - Dual monostable
multivibrator



*Transistor typically 2N2222

Spindle Disable circuit for Helios (provides approximately 30 second delay)



The circuit above reflects changes to the Helios II Controller PCB to allow software control of the disk drive spindle motor. Control is achieved by outputting to port F2 either a value of ONE or ZERO.

Outputting the value of ZERO will turn the spindle motor on. Outputting the value of ONE will turn the spindle motor off. The spindle latch added will always reset to keep spindle on when the system is first powered up by the POC signal. Unless the value of 01 is output to port F2, the spindle will always remain in the on state.

To allow program control from BASIC, use the following:

```

10 OUT 242; 000      (turns spindle on)
20 OUT 242; 001      (turns spindle off)
    
```

The spindle motor requires one full second to come up to the full speed and a pause statement in BASIC might be required in order for the software to wait for the motor. Anytime the software must use the disk, be sure to enable the motor and wait for the disk speed to come up before the read/write operation.

The circuit change is NOT recognized by PTDOS and therefore cannot be used when in the DOS unless the user wishes to use an assembly program within the **DO MACRO** to control the spindle.

Chapter 3. Controller/Formatter Trouble Shooting 1

SECTION 11

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SECTION 11

Helios II DISK SYSTEM

CONTROLLER/FORMATTER SUPPLEMENT (P/N 733003)

This section, devoted primarily to the hardware and DMA theory of operation, also includes:

1. Trouble-shooting of the Controller and Formatter PCB's.
2. Information on using the Disk System Test (DISKT).
3. Flowcharts of the DMA operations.

The usual approach to understanding a system as complex as the Helios II is to study the schematics and read the theory of operation to understand the hardware. The problem with this approach is, at first glance, the controller board appears so complex and the formatter so mysterious compared to LSI type controllers. For this reason, we will assume a little bit different tack to explore the Helios.

First, we must explore why we want a disk system, what we want to do with it and the optimum way of consolidating these into a hardware/software system such as the Helios II.

The Sol system, since it is 8080 based, has a limited memory of 65,000 bytes which may seem large to some, but is easily used up with a large compiler, program and data source. For this reason cassettes have been used for mass storage. The disadvantage of a tape-based system is their slowness. Imagine, if you would, an inventory control system for a warehouse taking many minutes to search through data stored on cassette with only serial access, updating that data and storing it back on cassette for later use. Why the entire operation might take as much as 15 to 20 minutes without random access and at 1200 baud.

A floppy disk system, on the other hand, can access information in a more random manner and at much higher transfer rates. The floppy disk is organized into tracks much like the tracks on an LP record. It has been said that the floppy disk marries the advantages of magnetic tape and the LP record into one. The information is stored magnetically on the tracks for later retrieval. It is because of this track organization that the disk can be considered a random access device since any track may be accessed in any order. Each track, however, contains data stored serially, and so this information must be retrieved serially.

With a disk system we are concerned with storing chunks of related data into one big collection of data. This data is more commonly referred to as a file, much like a file in a filing cabinet contains similar bits of information. This file may be stored in machine

memory (in a Sol, backplane Ram) and operated upon until the data is no longer needed now but may be in the future.

The floppy disk itself uses a form of FM (frequency modulated) recording to get the patterns of ones and zeroes stored. Remember, the data is transferred serially to and from the media, and it is also written that way on the disk surface. The disk places a continuous pattern of clocks on the disk when it is writing. These clocks are always present and occur at regular intervals to allow controller logic to keep in step. Between each of these clocks is either the presence or absence of a pulse. This is the actual data that is written. When the pulse is present the data bit was a logical 1, when it is absent, the data bit was a logical 0. The presence of pulses will, therefore, add to the frequency of the clock to present a frequency modulated pattern. The PERSCI drive supplies the separation of clocks and data when reading back from the disk through pins 50 and 49 of the 50 pin ribbon cable (see alignment procedures for detail and example of this pattern).

Let's talk a little about what must happen to keep track of this file once it has been stored on the disk. We already discussed the idea of tracks (Helios has 76 tracks total) on which the data is written, but how can the computer keep track of exactly where, in the 375,000 bytes of information on the disk, this particular collection of data resides. Essentially we need a map of the disk. Since a map requires streets and address let's follow along with this analogy.

The "streets" on the disk are the tracks, and on each track there are "street addresses" more commonly referred to as sectors. Helios has a maximum of 16 sectors or addresses on every track. Generally speaking, a group of these sectors or addresses are referred to as blocks much like city blocks are a collection of street addresses in close proximity. There are some buildings that fit nicely into one city block, and there are others which require several city blocks for space. This is the same case for the files we might want to put on the disk. Some might fit nicely in one block, and others might need several blocks to fit, while others may require an entire "street" or even multiple "streets" (tracks) to fit. Since a file may be several blocks or tracks long, we must be able to keep track of which blocks belong with which other blocks in the same file. To do this we make use of a header which is no more than some information about the data in the block that follows. A good analogy might be the information desk in this large building which is located on several streets. Let's explore the header in a little more depth.

FORMAT WITHIN A BLOCK

Each block of data we want to store on the disk has an appendage referred to as a header which describes certain characteristics of the data in that block. The header is what tells the software that "Yes, this is the data you wanted me to read." In order to do this, the header must have the following information:

DISK ADDRESS: Tells which track and sector we are at.

FILE ID: Tells that this block belongs with a specific file with this unique ID number.

BACK POINTER: Tells where to find the block before this one if our file extends over several blocks.

FORE POINTER: Tells where to find the block after this one if our file extends over several blocks.

NUMBER OF SECTORS: Tells the number of sectors that this block covers (whether the block covers one whole track, half track or a fraction of a track.)

BLOCK SIZE: How big is the upcoming data block (256 bytes all the way to 4K bytes).

By supplying all this information, the software can tell in an instant where the head is and what to expect when a read is initiated. All this information is necessary for complete file management.

By now all this information may seem to make sense, except this part about block size and number of sectors. Why not use a standard block size, like 128 bytes (IBM format), and use the 32 sector holes on the disk to tell us where we are? Then we never have to worry about lengths, and the file will be chopped up into nice even 128-byte chunks.

There are two reasons why a variable block size makes more sense, more data can be fit on a diskette, and that data can be accessed faster. Take, for instance, a file that contains 8K bytes of data and write it on two diskettes, one with 128-byte block size and one with Helios-style variable block size (variable over the range of 256 bytes to 4K bytes/block) for argument's sake, 4K blocks.

Going through the steps required to read this data back would look somewhat like this:

- 1) Find the track and sector the first block was written upon, and read that block.
- 2) Find the the track and sector of all the remaining blocks, and read those blocks.

Now, in the IBM format, steps 1 would occur only once, but step 2 would be repeated until the last byte of data was read or a total of a total of 64 times. In the Helios format, step 1 would be occur once and step 2 would occur once.

As it happens, the things that take the most time on a disk are the periods where the drive is doing a mechanical operation such as seeking to another track or waiting for the disk to spin around to the next sector. This means there are 64 times when we are waiting for a disk operation with IBM format and only 2 times with Helios. Obviously then, Helios is much faster.

The other advantage is more data per diskette. Using the example from above, let's explore this. Before we read a header from disk we allow 16 bytes for setup time. Then we read a header (roughly 13

bytes). In between the header and the data associated with that header, we must allow 16 or so bytes for time to set up to read the data (and also to allow for variation in disk rotational velocity). After the data there must also be at least 16 bytes separating the end of this data block from the header which immediately follows. Adding up all these bytes, we get a total of 61 bytes of wasted space everytime a data block is written. Multiply this times the 64 blocks from the above example and realize that for every 8K transfer, there is roughly 4K of space wasted on the disk. With the Helios scheme though, there are only 2 blocks written, hence, only about 128 bytes of wasted space for an 8K transfer.

Convinced that Helios is much faster and economical with space, we can examine in a little more the total format on the disk with this system.

There are 5 parts of every block wished to be transferred. They are:

- 1) Preamble to Header
- 2) Header
- 3) Preamble to Data
- 4) Data
- 5) Postamble to Data

Punctuating these blocks are sync bytes which tell the formatter when we are into these various parts. As mentioned before, rotational inaccuracies of the drive and set-up time, require the preambles of data and header. Another reason for the buffers is to allow time for the software to check the header information to determine if this is the particular header it had been looking for. The sync bytes are unique in that they contain a missing clock pulse which was inhibited by the formatter when the block was written. Upon reading these back, the formatter acts appropriately, be it to read or write data or header.

There is one other piece of information disassociated with either the data or header and yet tacked at the end of both of these, 2 bytes of CRC. This is a check to see if the header or data read back match what was written.

At the end of every header and data block there are 2 bytes written which essentially are a mathematical manipulation of all the bytes written in that header or data. This manipulation is performed in hardware by U5 on the formatter. When the header or data is read back, every byte is again run through the CRC checker, and at the end the CRC checker compares the two bytes of CRC data with the answer it got from the read data. If the two matched, there were no errors. If, however, there was a discrepancy, this information is passed onto the software.

DATA TRANSFERS

Since we now know how Helios organizes data on a diskette, let's examine the events which take place during this transfer.

The first thing that must happen is the controller with instruction from the software must tell the drive exactly where the head should be positioned. The drive itself does not know where its head is, the software must keep track of this. The drive puts out a signal whenever it reaches track 0, and with the help of the RESTORE signal, the software can always start from a known position and count. The controller must tell the drive three things before the head can be moved:

- 1) Which direction (either in or out).
- 2) How much (from 1-76 tracks at a time).
- 3) Whether or not this is to be a RESTORE.

This information is set to the drive via port F7, the Disk Command register.

The next thing the controller must know is how much data there will be (remember that this is variable unlike IBM format) and where that data will be written in memory. This is accomplished through ports F3 and F4 (Transfer lengths) and ports F5 and F6 (address DMA to/from).

Now the head is positioned on the track, the controller was informed of what to do with and how much data and all that is left is to wait for the formatter to get into sync with the disk and execute the software instructions. The software will tell the controller, through port F1 (Transfer Command Port) whether it is to erase, read or write a header or read and write data. It is now up to the controller to go ahead and do it. The success of the transfer is monitored by the software through port F0 (Status Port).

I/O INTERFACE

Helios has 8 ports assigned to it for I/O. These ports are F0 through F7 and are designated as follows:

<u>PORT</u>	<u>FUNCTION</u>
F0	STATUS (report status info to computer)
F1	TRANSFER COMMAND (controls read/write to disk)
F2	SPARE
F3	TRANSFER LENGTH (low byte)
F4	TRANSFER LENGTH (high byte)
F5	ADDRESS (determines where DMA to/from) Low Byte
F6	ADDRESS (determines where DMA to/from) High Byte
F7	DISK COMMAND (controls functions going to disk)

The ports are decoded by U6, U7, U23 and U42 of which U42 is the actual port decoder driving the respective logic. The ports can be divided into four distinct categories: Drive control, Transfer length, Transfer address and Status. All of these except Status are

outputs from the host computer. They answer the questions: Where from, Where to, How much and when. When all these questions have been answered the DMA process can begin.

The DRIVE CONTROL, port (F7), controls the various signals required by the drive such as drive and unit select, head step and direction and head load.

The TRANSFER LENGTH register stores information concerning the total number of bytes to be transferred using U28, U29 and U30. Only when these have reached 0 is the transfer said to be complete. This is done through ports F3 and F4.

The TRANSFER ADDRESS register stores information about where DMA is to be done and uses U24, U25, U26 and U27. These always contain the next address to DMA to/from and are buffered onto the address bus via U43, U44, U45 and U46, 8097 drivers. This is loaded through ports F5 and F6.

The STATUS register, (F0), contains information as to the progress of the transfer and whether or not the controller is ready to do a transfer. The information is latched into U33 and buffered onto the data bus via U50 and U51, 8097 drivers.

All data going to the controller or coming from the controller is buffered through U47 and U48 (8833 Transceivers). The low-order nibble is handled by U47 and the high-order nibble by U48.

DRIVE CONTROL INTERFACE

The software must communicate to the disk drive through port F7 telling it exactly what to do. The first thing the drive must be told is where to place the heads. This is accomplished by step pulses and step direction instructions. The step pulses are derived from the PHASE 2 CLOCK (they are actually CLOCK 4) and are enabled through bit 0 of port F0. Bit 1 controls whether the head should move towards track 76 or towards track 0. It is latched through U31 and buffered through U32. There is one other control which is a RESTORE. This tells the heads to go to track 0 (there is logic internal to the drive to, when given this command, do a slow seek to track 0). This enables the software to start with the heads at a known location and count steps from there. Bit 4 of F7 controls this through U10.

Bits 5 and 6 of port F7 provide the signal HEAD LOAD 0 and HEAD LOAD 1 to the drive. They correspond with the unit on the left (Head 0) and unit on the right (Head 1) whether or not the drive is part of a multi drive system. This means, if we wanted to load head 3 on a Helios Model IV we would toggle bit 6 to a logical low (drive control signals are all low active), and regardless of bit 5, the head would load. These signals are latched through U31 and buffered through U32.

Since Helios can access up to 8 separate units, there must be 3 control bits to select these units, bits 2, 3 and 7. A little clarification of terminology is in order here.

UNIT = A unit is one slot in the system
 DRIVE = A drive is composed of 2 Units
 CABINET = A cabinet is composed of 2 drives (a total of 4 units)

The bits are organized to select these as follows:

BIT 7 = Unit Select (high = left unit
 low = right unit)
 BIT 2 = Drive Select (high = left drive
 low = right drive)
 BIT 3 = Cabinet Select (high = cabinet 0
 low = cabinet 1)

After we have selected the specific unit we wish to access, then we select the proper head load signal and we are able to access any unit in any of two cabinets. The control bits are latched in U31 and buffered through U32.

DMA CONTROLLER

The other main function of the controller PCB, besides the controlling of signals to the drive, is to gain control of the S100 bus from the 8080. The controller, when it gains control of the bus, is a psuedo 8080 and, therefore, must generate all the signals required by the S100 bus.

The beginning of the process occurs when the DOS issues a command to read or write headers or data. When the formatter board synchronizes to the disk, the controller is ready to take control of the bus to do a DMA and issues the SREADY status to the software. From this point on, the controller is in preparation to gain control of the bus and issues the HOLD command to the 8080. The 8080 responds after executing the current instruction by sending out a HOLD ACKNOWLEDGED and tri-stating.

Once the controller receives the HOLD ACKNOWLEDGED signal, it grounds the lines: ADD DSB (address disable), DO DSB (data out disable), STAT DSB (status disable), C/C DSB (command control disable). Now the Controller is in charge of the S100 bus and is ready to do DMA (see flowchart following this section on the DMA/ hold sequence). The controller now can transfer 13 bytes of data directly into or from memory. The controller relies on two FIFOs to convert the serial data from the disk into parallel data and store these bits until 13 bytes have been received. At this point the controller initiates a DMA.

Now that the 13 bytes have been transferred, the controller must wait until another 13 bytes are ready to be transferred and so releases

the S100 bus and the HOLD line to the control of the 8080. The process is continued until the transfer length counter reaches zero indicating that the transfer is complete.

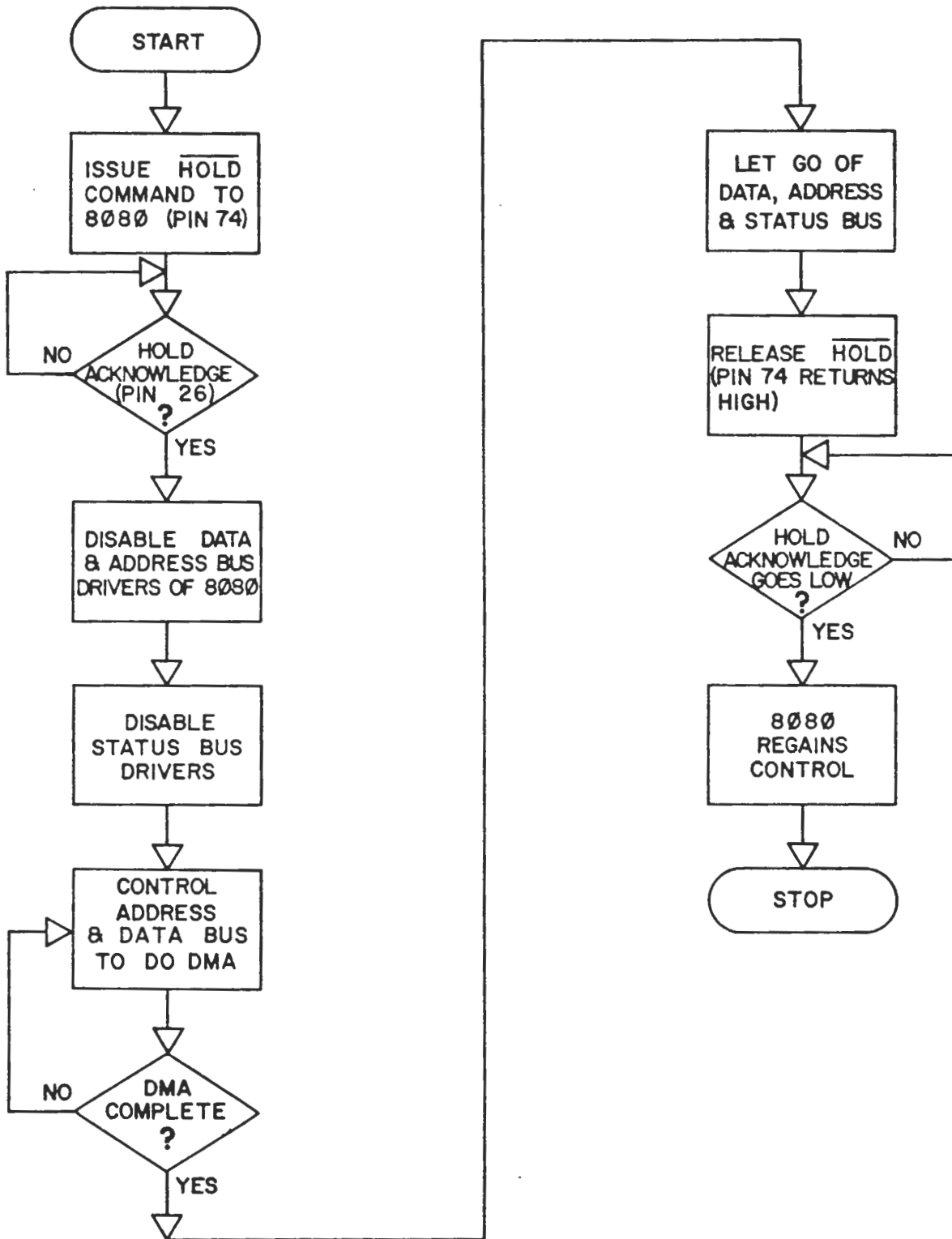
The active signals generated by the controller when it is in control of the bus are: PSYNC, PWR, PDBIN, SWO and SMEMR. PHLDA is held at a high potential, and all of the following signals are held at a low potential by the controller when it is in control of the bus: PHLA, DO DSB, ADDR DSB, CC DSB, STAT DSB, PWAIT, PINTE, SIMP, SOUT, SMI, SHLTA, SSTACK, SINTA.

FIFO BUFFERS

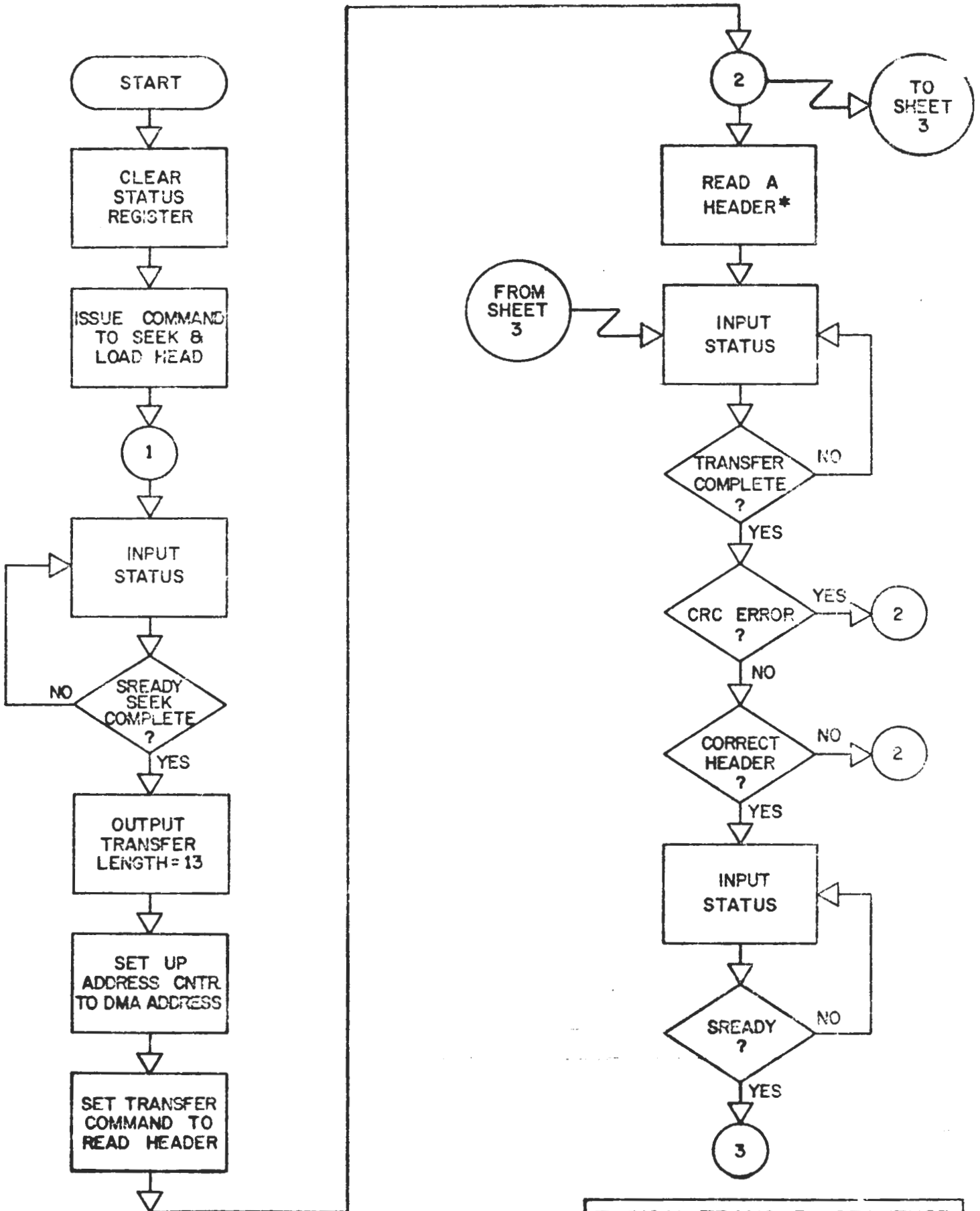
As already mentioned, the data going to and from the disk is buffered by two 4-bit FIFOs. A FIFO is basically a memory device which stores data in bits and converts them into parallel data to be transferred to the DI BUS. The only difference between a FIFO and a UART is the FIFO is able to store bits until 13 bytes of information have been received, and then transfer the data in parallel form, whereas the UART handles only one byte at a time. When the FIFO has filled, the contents are transferred either in serial form to the disk or in parallel for writing to memory depending on whether or not we are reading or writing to the disk. Since the FIFOs are 4-bit devices, two are used in parallel to form an 8-bit byte (U52 and U53).

The reason a FIFO is used, rather than transferring the data directly into memory with DMA, is speed. Since data coming off disk is relatively slow compared to the 8080, a lot of time would be wasted just waiting for the data. Likewise, writing to the disk is slower than reading from memory during DMA, and the processor's real time operation would be greatly reduced. With the scheme used in the Helios II, the processor is on hold an average of 5% of the time. Thus the processor is held up only for the time it takes to DMA 13 bytes, roughly 18 usec.

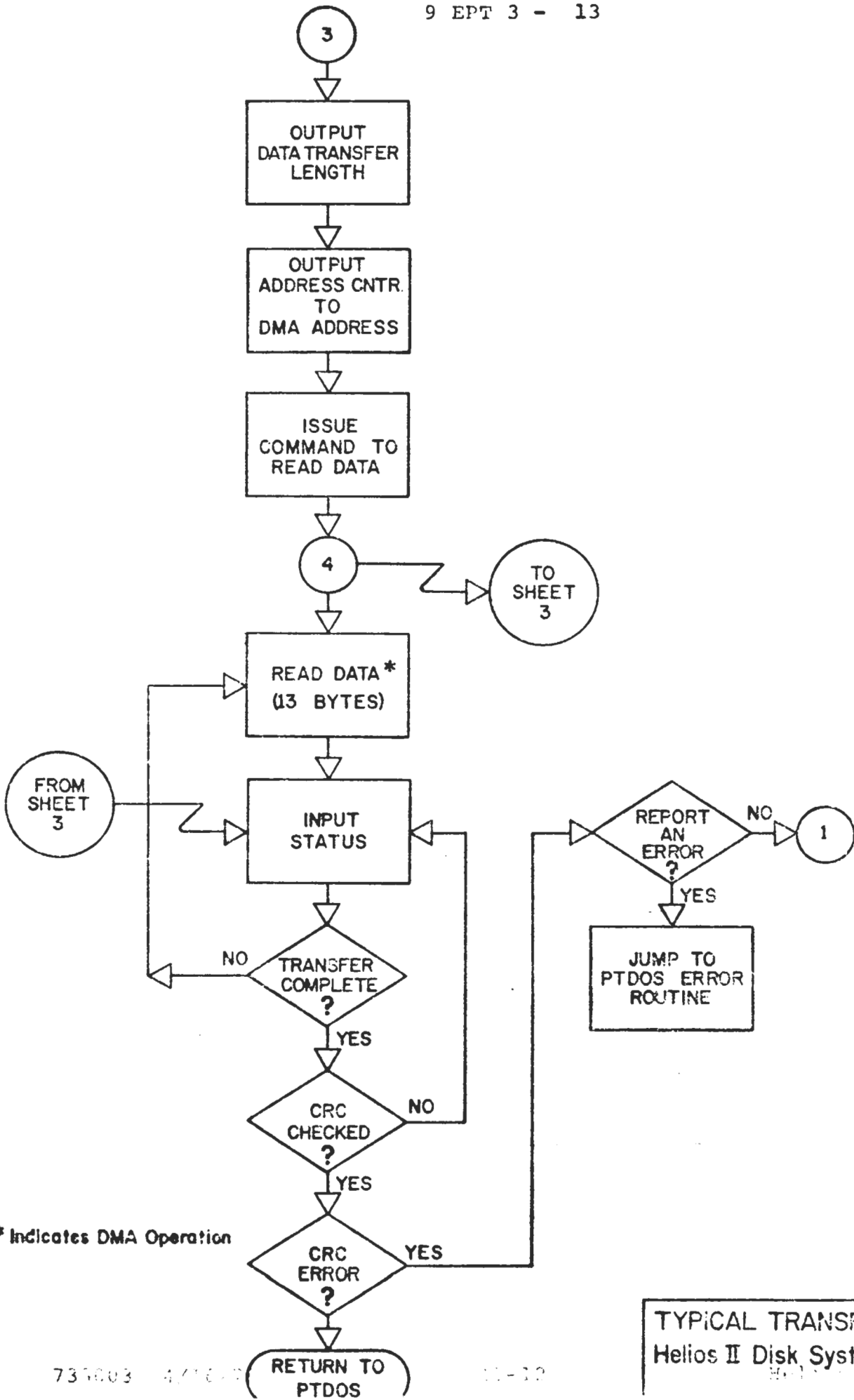
A more detailed description of the 9403 FIFO may be found in the FAIRCHILD Macro-Logic manual.



8080 DMA OPERATION

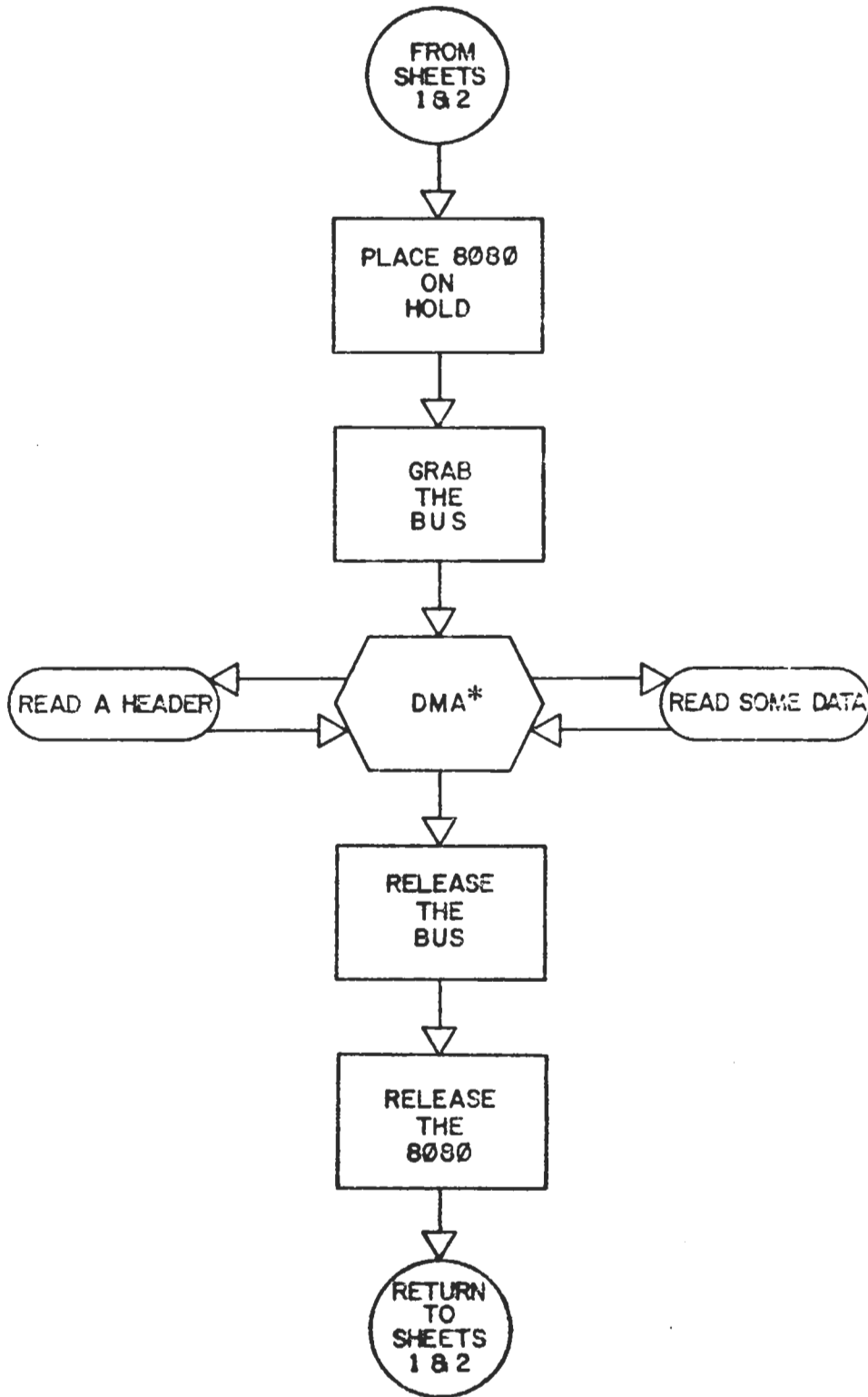


* Indicates DMA Operation



* Indicates DMA Operation

TYPICAL TRANSFER SEQUENCE
Helios II Disk System
Page 2 of 3



* OCCURS DURING { READ A HEADER & READ DATA

TYPICAL TRANSFER SEQUENCE
Helios II Disk System
Revision 11
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FORMATTER PCB

It is the function of the formatter board to keep track of the timing synchronization with regards to disk transfers. The formatter must keep track of number of bytes in, punctuation of and the 5 parts of a block. To do this, it detects the missing clocks written on the disk as unique sync bytes. These sync bytes tell us when we are entering another part of a block while the state counters keep track of precisely which part of the block we are into.

The bit counter counts 8 bits and then gives a terminal carry indicating that one byte has passed by the head. The punctuation counter receives that terminal carry (BCTC) from the bit counter and then keeps track of the number of bytes which have passed the head. The punctuation counter is reset everytime a sync pulse is detected (indicating we are entering another part of a block). The construction counter keeps track of the parts of a block which have been discussed in "Format Within a Block." The outputs of this counter produce the waveforms TEXT (this determines whether we are into preamble, postamble or actual text, be it data or header), DATA (which keeps track of whether we are into data or header) and DONE (which indicates we are no longer into header, preambles or data).

The state diagram at the end of this section describes the states of these three counters during transfer operation. By following this flowchart, it is possible to determine exactly what counts of these counters control which transfer function.

The formatter board also has a hardware CRC generator and checker which take the data or header read back from the disk, mathematically alter it and compare it with the 2 CRC bytes written at the end of both header and data when these were initially written onto the disk. When these bytes check, no CRC error is generated.

For a more rigorous examination of the actual circuitry on the Formatter PCB, refer to the Theory of Operation in the Helios manual. This section is meant to be a brief macro view of the basic elements of the Helios system.

TROUBLE-SHOOTING THE FORMATTER

The problems with controllers and formatters in field return are very infrequent (except as kits), and for that reason, this section was not intended to be a troubleshooting guide for every malfunction possible on these two PCBs. Rather it is a brief outline of the common problems encountered with these boards and the common remedies. At the end of this section is a waveform chart to be used as quick reference in troubleshooting using the DISKT program. Primary emphasis is placed on the Formatter waveforms, as this is a quick indication of exactly how sick the system really is. Also, bear in mind that the most common problems are on the diskette drive itself, and the section on the drive should be consulted when this is determined.

The fastest way to troubleshoot a formatter board is the following:

NOTE

The following checks should be done using the DISKT program. Step through to frame 13 and set bit pattern to:

0 0 1 1 1 1 1 1

- 1) Check U14 pin 12 for the signal SEPARATED SECTOR. This signal originates on the drive.
- 2) Check U15 pin 15 for SEPARATED SECTOR. This signal also originates on the drive.
- 3) Check U4 pin 9 for MAIN CLOCK. This signal originates on the controller. During a write, it is derived from PHASE 2 and during a read is derived from RCLOCK (Clocks coming from the disk).
- 4) Check BCTC, U13 pin 15. There should be pulses if counting correctly.
- 5) Check U11 pins 14, 13 and 12 for TEXT, DATA and DONE in that order. If the other counters are counting, these should be present.
- 6) Check RSECT, U16 pin 6. This is a combination of SEPARATED SECTOR, SEPARATED INDEX and DONE.
- 7) Check RCLOCK and MC clock circuitry on U17 pin 12 (should be a .9 usec squarewave) and U17 pin 4 (should be reading missing clocks from the disk), respectively.
- 8) Check SET HOLD REQUEST and CROSSOVER, U2 pins 6 and 12, respectively. (Refer to formatter waveform guide at end.)

The most common problems with the formatter boards in order of frequency are:

RCLOCK and MISSING CLOCK oneshot (U17) have gone out of spec. Check timing and replace.

One of the counters BC, PC or CC are not counting or counting incorrectly. Verify waveforms are correct.

RSECT not present. Check sector, index and construction counter (CC).

CRC checker is malfunctioning (U5 pin 13). Use checkout procedure in Helios manual, page 5-24, step 22, and DISKT frame 13.

These are by no means the only problems, but given the limited amount of circuitry on the board, the most likely places for problems. This is also a quick check only to see if certain signals are present. For a more thorough diagnostic, follow the Testing and Trouble-shooting sections of the Helios manual for the formatter board (pages 5-28 to 5-34).

TROUBLE-SHOOTING THE CONTROLLER

Although the controller board contains 53 ICs and appears quite complex, it is possible to sort this conglomeration of chips into block function. That is, the controller can be broken down into groups of chips which are responsible for the various tasks.

The Helios controller is responsible for the actual command of the bus and drive and simulates an 8080. For this reason, it is convenient to look upon the controller as a subset of the Sol system and to compare the operation of the two.

Just as the heart of the Sol is the 8080, the heart of the controller is a series of discreet chips which control the S100 bus in the absence of the 8080. These chips are comprised of the chips, U0, U1, U2, U23, U13, U20, U21, U22 and U35- U39. Referring to the controller schematic, these are the chips located in the center and right center of the page. These chips coupled with the formatter (which could be considered the clock circuitry of the controller) form the portion of the controller which must make decisions as to when a transfer takes place and is responsible for enabling this transfer.

The lifeline of the Sol is the internal data bus which is responsible for carrying data to the 8080 for processing. Likewise, the controller has an internal data bus which is buffered by 8833 transceivers and on which sit all the counters, the control signals to the drive and the FIFOs.

The Helios, like the port decoders on the Sol, has a port decoder responsible for decoding ports F0 - F7 and is comprised of U6, U7, U23 and U42 (all in the upper left hand corner of the schematics). The outputs from these chips determine which port is to be accessed as in the Sol.

The Helios has what can be considered as 3 parallel ports and one serial port very similar to the Sol. One parallel port is the output lines to the disk drive (a total of 8 bits) and a parallel input port from the drive (a total of 4 bits) which monitors the drive status. Another parallel port reports status to the host computer through U33, U50 and U51. The serial interface is comprised of the 2 FIFOs, U52 and U53 and is both an input and output port as in the Sol cassette interface.

The D I/O drivers are comprised of U47 and U48 and the address drivers are composed of U43 - U46.

An interesting observation to those wary of tackling this board is that 2/5 of the 50 odd chips are no more than buffers or drivers for signal lines. Almost 1/5 of these chips are nothing but counters

(74LS191 and 74LS163). The remaining 2/5 of the chips are assorted latches and logic which are the heart of the actual control operation. This means there are only 20 or so chips which involve the more intricate timing loops of the system which could cause system timing foulups.

I/O TROUBLE-SHOOTING

The controller port decoders and I/O circuitry as well as the internal data bus are relatively easy to troubleshoot. Here there are 2 approaches, DISKT I/O routines or some simple short programs entered manually into machine ram (C900) meant to continuously exercise these functions without loading DISKT.

An example of such a short machine level program is:

```

C900      21 FF FF      LXI H, -1
C903      7C          MOV A,H
C904      D3 F6      OUT F6
C906      7D          MOV A,L
C907      D3 F5      OUT F5
C909      2B          DCX H
C90A      B5          ORA,L
C90B      C2 03 C9   JNZ
C90E      C3 00 C9   JMP

```

This illustrative program outputs to the DMA Address counters (ports F5 and F6) repetitively decrementing them until zero is reached. At this point, the process is repeated. The purpose of this test is to:

- A) Test the I/O port decoders for port F5 and F6.
- B) Test the DMA address counters for correct operation.

By looking at the outputs of these counters, U24 - U27 (pins 2, 3, 6 and 7) it can be determined if they will count correctly. Sync on output strobe port F5, U42, pin 10. A small test such as this might be helpful if it has been determined that a controller board cannot DMA to a specific address or a group of addresses.

Similar small programs can be used to exercise the other ports as well, depending upon the symptoms exhibited. For instance, here is a short program which will read drive status signal INDEX. The program will loop until an INDEX is detected at which point we will return to SOLOS:

```

C900      DB F0      INP
C902      07          RLC
C903      D2 00 C0   JNC
C906      C3 00 C9   JMP

```

This program could very well have displayed a character on the screen at the presence of INDEX or used any of the other 7 status bits. The idea here is to generate as simple a program as possible to test the hardware. In this case, without even the use of a scope, we can determine whether or not the drive is ready, completed a seek or has index pulses.

Using these techniques we can also determine if the internal data bus of the controller is functioning. In this case we might want to issue the command to load both heads. We would then look to see if the internal data bus of the controller had the following bit pattern:

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	1	1	1	1

HOLD SEQUENCING

To test this part of the circuitry, load DISKT and proceed with the Controller/DMA test procedure in the Helios manual (Section 5) and refer to the section in this manual on DISKT for further information.

STATUS

The status latches, U33, monitor the progress of the transfer and can be checked using the DISKT program as in the above step. Five of the signals are a function of the controller logic and 3 are a function of the drive logic. These signals should be reflected on the DI Bus of the host computer through U50 and U51. To check these using DISKT, sync on pin 1 of U51, set up the bit pattern to read a header and monitor the outputs of the latches and the buffers (U33 and U50-51).

BUS CRASHERS

Since the controller takes control of the bus when doing a DMA, if there is a logic problem internal to the controller then there is a possibility the controller will try to access the bus while the Sol is also. This can often cause problems such as garbage on the screen or various other symptoms. The chances of this happening are higher than with most boards since there are so many drivers sitting on the various S100 lines.

The best thing to do in this case is to reset the Sol and examine all the address and data lines while in the reset mode. All these lines should be at a logical "Low." This allows one to narrow down the driver rather quickly. If this does not work, lifting U40 pin 11 will disable the Command/Control lines and the Status lines from interacting with the bus. Usually the problem is either a buffer driver failure in one of these two sections that cause this type of problem.

DISKT CRASHERS

One of the most difficult problems to troubleshoot are the controllers that insist on crashing the disk diagnostics whenever the controller is asked to do a transfer. Step 18 of the troubleshooting section of the Helios manual refers to this as, "This step is a likely place for a board error to cause a system crash since it

involves repeated DMA transfers." Unfortunately, this does not tell us what to do in the event of such a crash.

The best approach here is to assume the controller is either doing DMA at the wrong time or to the wrong place since this will destroy the contents of memory. By disabling the PWR driver (lift U44 pin 15) we can, in most cases, prevent the memory contents from being changed since this is the signal the controller uses to write into memory. This allows us to continue with the DISKT program and test procedure to find the faulty logic.

COMMON CONTROLLER PROBLEMS (In order of frequency)

SYMPTOM: Controller will boot occasionally but gets numerous errors during DISKT.

- PROBLEM:**
- 1) Bad or intermittent 9403 FIFOs. Swap FIFOs and see if the problem follows the FIFO to the other nibble of the 8-bit byte.
 - 2) Bad or intermittent 8833 bus transceivers. Again, swap U47 with U48, and see if the problem moves with the chip.
 - 3) Clocks of the host system (particularly the PHASE 2 clock) not up to 8080 specifications.
 - 4) Problems in the error reporting circuitry or the status latches themselves. Check these using DISKT and the diagnostics in the manual. (U33, U50 and U51 and support logic).
 - 5) Problems with the COMMAND/CONTROL logic such as PSYNC or PWR.
 - 6) Drive control logic malfunction (i.e., STEP, READ, WRITE, etc.)
 - 7) CRCERR goes low when RMC goes low indicating a CRC error. CRC errors are errors found in the serial data path and are not indicative of a problem in the parallel data path.

SYMPTOM: Controller gets numerous abort errors.

- PROBLEM:**
- 1) Sync errors due to problems in the logic fed from the formatter (starting at U17 pin 2) and following logic.
 - 2) Formatter cannot track with the heads on the diskette due to problems with main clock circuitry (U5 and support logic).

- 3) Power on clear flip flop being reset during an attempt at a transfer. Check U39 pin 10 for intermittent pulses.
- 4) Check for OVER INDEX from the formatter and the receiving circuitry on the controller, U17 pin 9.
- 5) One of the ready lines is pulled low during an attempted transfer sequence. Using DISKT, check to see if U23 pin 8 is high when DNSYNC goes high. This is the time when the ready lines are sampled. Problems with slow memory or memory coincidence cycles may also cause this problem.

SYMPTOM: BUS CRASH ("garbage" on screen).

- PROBLEMS:
- 1) Address bus drivers (look for shorted address lines and lift pin of address drivers). These drivers get quite hot and sometimes fail due to internal shorts which can short an 8080 address line to ground. Check U43 - U46. Also check the port decoder circuitry for shorts to ground. This involves U6, U7, U23 and U42.
 - 2) Data bus drivers (again, look for shorts but on the data lines). These chips get quite hot as well. Check U47 and U48 for shorts on the DO bus and U52 and U53 on the DI bus.
 - 3) Possible shorts on the COMMAND/CONTROL lines. These lines are buffered through U43 - U45.
 - 4) U49 or U50, the STATUS output lines could be shortened.
 - 5) Circuits responsible for holding the 8080 and disabling the bus are incorrectly trying to control the bus. These signals are buffered through U41 and should not be low when Sol is first powered on.
 - 6) Processor is being held during power up. Check pin 19 of the 8080. If the processor is running, there should be SYNC pulses here. If the processor is not running, check the HOLD signal starting with U41 pin 14 and tracing backwards.
 - 7) POC (Power on Clear) is not reaching the controller, and the board initializes with a HOLD of the 8080. This ties in with the above, Number 6.

SYMPTOM: During DISKT, the buffer has all 3Cs written in it or comes up with BAD DATA.

PROBLEM: Since the buffer is cleared to the value of 3C before the controller attempts DMA, it appears the controller never accessed the buffer. The following problems could cause this:

- 1) No PWR to enable a write into memory.
- 2) Memory board being used does not decode MEMWRITE and needs that signal decoded.
- 3) Aborts always occurring (see first problem in this section).
- 4) DMA occurring to the wrong address. Check address counters (U24 - U27) for correct operation.
- 5) Transfer Command Register not working correctly (U22). Write a simple program to constantly output to port F1 a specific value or use the DISKT frame 13 (Type "2" from menu).
- 6) MAIN CLOCK problems (Check U5 pins 12, 13 & 1).
- 7) Check DMA timing circuitry per Troubleshooting and diagnostic section of the Helios manual.

SYMPTOM: Drive will not seek or seeks incorrectly.

- PROBLEM:
- 1) No PHASE2 clock getting to the board or MAIN CLOCK circuit malfunction (U5).
 - 2) Port F7 not being decoded (U22 and support logic) or U47 and U48 not passing data from the DO bus.
 - 3) Bad driver (U46).
 - 4) RESTORE is always low, which has priority. Check to see why U9 pin 7 is always low.

SYMPTOM: Drive can read but cannot write.

- PROBLEM:
- 1) Problem with Port F1 decoding (U42).
 - 2) Transfer Command Register malfunction (U22).
 - 3) Write flip flop not responding (U39 pin 7 at a steady level).
 - 4) Program is looping for status, check status latches for READY, INDEX and SEEK COMPLETE (U33).
 - 5) FIFOs are always depleted and have no data to transfer (causes ABORT).

SYMPTOM: Spindle motor will not turn.

PROBLEM: Pin 24 of the 50 pin header going to the drive is not at ground potential.

SYMPTOM: Drive will write but will not read.

- PROBLEM:
- 1) Open trace carrying SEPARATED CLOCK and SEPARATED DATA from controller/drive header to controller/formatter header (or a short on these lines).
 - 2) Resistor pullups are malfunctioning or have cold solder joints (R1 - R6).
 - 3) FIFOs (U52 and U53) malfunctioning. See procedure in diagnostic section of the Helios manual.
 - 4) Port F1 not being decoded correctly (write a short program to output this port), or the program is hung up inputting status (check status lines).
 - 5) Transfer Command Register not responding to port F1 select signals.

SYMPTOMS: Heads will not load.

- PROBLEM:
- 1) U15 (One-shot) always timed out. Out port F7 a DF hex and loop. This should keep unit 0 head loaded so U15 can be checked.
 - 2) Using DISKT, make sure the level of the Test tape revision matches the PCB modification level of the controller as one of the major changes from Rev C to Rev E involved a change of this port assignment.
 - 3) Port decoder unable to decode Port F7 (U42 or support logic malfunction).
 - 4) U31 not latching the Disk Control bits or driver U32 disabled or malfunctioning.
 - 5) Drive select or cabinet select logic faulty or selecting the wrong drives or units. Check U31 for correct latching and U32 for correct buffering.
 - 6) Rev H mods installed incorrectly so Port F7 is never decoded at all. Re-install mods.

"DISKT" (Disk Test)

With every Helios II and every Sol System III or IV comes a copy of DISKT, the disk diagnostic and verification program, on cassette. It is the purpose of this section to explain the operation of the program with some general information and the use of the disk test as a diagnostic tool or exerciser.

The initial purpose of the program DISKT was as a disk system exerciser, i.e., to exercise the function of the hardware in the Helios system. It has recently evolved, necessarily, into a valuable diagnostic tool as well. The average small program a technician would have to use to exercise the disk hardware in one small disk function might require 40 bytes. This makes the DISKT program a timesaver--it could be considered a "MicroDOS!"

DISKT might be used in any of the following situations:

- 1) System III qualification - a working system which will be sold to the customer.
- 2) Routine Maintenance - a system which has already been sold and verified but has been in the field three months.
- 3) Diagnostics - a system which is malfunctioning and is in need of troubleshooting.

DISKT Operating Procedures

DISKT requires that the host computer be a SOLOS/CUTER system, have 16K of contiguous memory beginning at location 0000 and that the memory be capable of DMA.

With the controller and formatter installed (for the sake of ease we will use one example) in a Sol with Helios cabinet attached and a cassette recorder with DISKT connected, type the following commands:

TYPE: XEQ DISKT <CR> (Solos prompt will disappear)

SOLOS RESPONDS: DISKT 0000 2FFF

At this point the program is loaded into memory and executing but is waiting for a cue to either use the VDM or the Serial port. That cue is a keyboard entry of either a letter "S" for serial or "V" for video. For the sake of convenience, we will use the video and refer to the DISKT frame reference at the end of this section.

On our screen then should be frame 1 which tells us the program is executing correctly. At this point we should only have a scratch diskette in the drive unit under test as the frame indicates. Following directions we then type a "P" to continue.

On the screen is the DISKT menu (frame 2) which lists the various options contained within the program. Depending on the reason for using DISKT the options selected are different.

Let's use the simplest case first, i.e., pre-sale qualification. Since we know the system has passed all these tests at the factory, and it should, therefore, be able to do these tests without problem. In this case we would use the "Seek" portion first (being sure to run all tests on both drive units) to verify the drive can seek properly, and the controller can function properly. The next test to be run is the "Automatic write/read test" in the "Display Mode." This last test should be run a minimum of 3-4 hours on each unit.

The next instance we would use the test is in a system from or in the field which has been running successfully for three or less months and which exhibits no symptoms of failure but is being re-qualified. In this case, we would run the "Seek" portion first, as before, and then the "Automatic write/read test" in the "N" mode (no display, no stop on errors) until the system is needed again. In the case of a small business, for instance, the test may be run overnight. Again, be sure to test both units!

The last and most important function is use as a diagnostic tool. It is this case that we will use the test from the very beginning to exercise hardware we know to be faulty. Let's examine the test in its entirety.

DISKT (The Labyrinth Unfolds)

There are three main portions of the test and in these subsections containing various tests options. These three main portions are:

- 1) I/O Tests
- 2) DMA Tests
- 3) SEEK Tests

I/O TESTS

The I/O portion of DISKT is meant to exercise the port decoding logic and to verify their operation. This portion begins in frame 3 and ends at frame 12 and is relatively self-explaining as the procedure is written on the monitor and also lists test points to be checked. This portion is automatic in that once "1" has been typed in frame 2, the next 10 frames will appear in order, advancing frame by frame each time "P" is typed.

Frame 3 is to familiarize the user with the use of keys 1 through 8 as switches for the various ports. Throughout this portion the least significant bit is key 1, and the most significant bit is key 8. (This means when key 8 is toggled, DO 7 on the bus responds. Likewise DO 0 would respond to key 1.)

In frames 4 through 8 we are outputting to port F7, the Disk Command Register.

9 EPT 3 - 26
DISK COMMAND REGISTER (F7) CONFIGURATION

<u>BIT</u>	<u>FUNCTION*</u>	<u>DISKT I/O KEY PRESSED</u>
0	STEP	1
1	STEP DIRECTION (0 = in, 1 = out)	2
2	DRIVE SELECT (0 = 2, 3 or 6, 7)	3
3	DRIVE SELECT (0 = 0, 1 or 4, 5)	4
4	RESTORE (Restores heads to Trk 0)	5
5	LOAD HEAD 0 (Even units)	6
6	LOAD HEAD 1 (Odd units)	7
7	UNIT SELECT (Low = odd units High = even units)	8

*NOTE: All signals are negative true.

Frames 4-8 exercise these functions of the drive and controller for correct operation. Any malfunction can be easily traced through the logic by toggling the various bits and noting the responses. In each case the origin of these signals is given in each test frame.

NOTE

In frame 7 the step function of the drive is exercised. When the head steps all the way in to track 76 the test program will still keep sending step pulses to the drive because the program does not keep track of where the head is. For this reason the drive may exhibit peculiar symptoms as the controller tells it to step past its limit. Some drives will try to restore to 0 and will shoot back out to 76. Other drives will store up the pulses until the direction is changed and then the head will skip a number of tracks with this stored up count on its way to 0. In any event the recommended procedure is to change direction (toggle key "2") before the drive reaches track 76 and is meant solely as a go/no go step test.

Frame 9 of the test toggles the bits of port F5, the low address counter. Remember this is part of the counter pair which determines the low byte of the address to begin DMA. Again the test frame indicates the pins to check when exercising this counter.

Frame 10 exercises the high address counter, port F6. This port contains the high byte at which DMA is to be done. This frame also indicates the appropriate test points.

Frame 11 exercises the low byte transfer length counter or port F3. This is the port which will keep track of the number of bytes left in a transfer.

Frame 12 exercises the high byte transfer length counter through port F4. Since the maximum block size PTDOS allows is 4K, only 4 bits of this port are needed. This frame toggles these 4 bits which keeps track of the high byte of transferred bytes. This is the last step in the I/O portion of the test.

DMA TESTS

Frame 13 begins the first part of the DMA portion of DISKT. Before the process can actually begin, the program asks the user which unit is to be exercised and formats track 0 of the selected unit.

This part of the test actually exercises the transfer command port, F1. The transfer command port is configured as follows:

TRANSFER COMMAND PORT (F1)

<u>BIT</u>	<u>FUNCTION (Bit = 0)</u>	<u>FUNCTION (Bit = 1)</u>
0	Erase	Read
1	Write	Read
2	Transfer Data	Transfer Header
3	Enable Transfer	Disable Transfer
4	(not used)	
5	(not used)	
6	(not used)	
7	(not used)	

By the use of these four bits of the transfer command port we can perform any of the five desired types of transfer required of the controller. For instance, if we just wish to erase a disk, bit 0 switches the erase part of the disk head on and off at the appropriate times regardless of the other bits. Bit 1 controls the circuits in the drive which set up for either a read or a write. Bit 2 decides whether the transfer will be a header or a data block. Bit 3 just says, "OK, go ahead and do it."

Like the other portions of the test then, this part exercises a port and the associated hardware. The difference with this part is that it relies on the critical timings in order to successfully complete the operations. Thus, both the controller and formatter are exercised, and it is the first part of the test at which we can actually test DMA.

Also, unlike the other parts of the test, this part can do some rather destructive things. For instance, since it does do DMA, it is possible to overwrite the program itself. This part of the test will not display any errors that may be occurring due to hardware malfunction--all it does is exercise the DMA portion of the logic.

Frame 13 is designed to be used in conjunction with the Controller/DMA Test/Troubleshooting part of the Helios hardware manual (beginning on page 5-22 and ending on page 5-34). In this part of the manual appropriate signals are described and the pins at which to see these signals. Waveforms are also included for the controller as well as a timing diagram for the Formatter PCB.

The user is advised to be prepared, in the case of a hardware problem, for a system crash in some instances. This leads us into a description of just what the DISKT program does during this DMA portion.

The DISKT program transfers headers as 13 bytes and data in fixed 4K chunks. Unlike the DOS, the test cannot generate variable block sizes, but, rather, transfers the largest block possible on the assumption this is the hardest transfer needed to be completed. This is all reasonable, but where does the test program get its data so that it can check the data for accuracy?

DISKT uses the program itself for the data block. That is, it steps sequentially through the test program, starting at address 0 and ending at the last address of the test program, 25D2, one byte at a time. This is very close to being a random data pattern and yet allows simple comparison by the program to determine the success of the transfer.

It is easy to see, then, why the test can sometimes be self-destructive. All that need happen is a DMA to the wrong address or a write instead of a read, and the program has been destroyed. After the controller/formatter and DMA trouble-shooting is finished, there are several other DMA portions which may be helpful in diagnostics.

In frame 2 (Menu) parts 3, 4, 5 and 6 all pertain to a read or write or a combination of the two of either a header or data. These tests require that the disk be formatted first (if the test is done in order, then this is no problem, since before frame 13, the disk is formatted) but only on one track, as the drive will not step during these transfers. There are several options within these four options to allow either only a header (or data) be written, read back constantly or one transfer at a time (refer to frames 14, 15, 16 and 17 for examples of these tests). One option is to repeat a write/read combination of either header or data until the letter "G" is typed which will generate a report of any errors accumulated during the tests. In any case, the user is encouraged to experiment with the different options to be familiar with their function.

NOTE

When the Header or Data write portion gives the message "Write OK" the only significance of this is the transfer was completed without an abort. Thus, the only way we can insure the transfer was successful and the data or header was written correctly is to read the header or data back after a transfer. This is the purpose of the write/read combination tests.

SEEK TESTS

There are two seek tests within the test framework, the straight "Seek Test" and the "Automatic Test." The Seek Test is a fast random seek of every disk track to read headers and determine if the hardware can seek correctly. It lasts about 5 minutes or can be aborted by pressing "S" which will return us back to frame 2.

The first thing the Seek Test does is format the disk and write headers (each track has one header which contains its own unique track number) on all 76 tracks. Next the drive does a restore to track zero and a rapid step seek to track 76, stopping at every single track just long enough to read a header and determine it is on the correct track. Next the drive does 5 minutes of rapid random seeking in each seek, stopping long enough to read a header and verify the track. This test is a test mostly of the drive hardware since only headers are concerned. It should be run on both unit 0 and 1 to qualify the drive.

There are only three types of errors in this portion, and they are, "Seek Error!!", "Couldn't find track I.D." and a return back to SOLOS/CUTER. The first error usually occurs after the tests have begun executing, and the drive is in a random seek mode and usually means there is a problem with the drive hardware. The second error means the drive, when it does a restore after writing all the headers, could not read the header it had supposedly written. This could be a problem in the controller or formatter board timing, the write circuits malfunctioning in the drive or the read sections malfunctioning in the drive. The third error is a return back to SOLOS and usually means the test could not function indicating both read and write problems exist. It is the most serious of the errors.

The second seeking test is the Automatic Test. This test incorporates all of the previous tests into one single test and, therefore, has the most options. Before exploring the options, let's first discuss what this portion of the disk test is doing.

The purpose of this particular test is to sum up all the requirements of the system into one test which exercises all the hardware used in the implementation of PTDOS. For this reason the test must be able to tell the heads where to go, verify they indeed got there and then transfer headers and data successfully or report back any errors.

The very first thing the automatic test does is format all 76 tracks of the disk. After this step the drive does a restored and awaits the selection of one of four options of test display. After a display mode is chosen the drive goes into a step seek mode, writing headers and reading them back as well as writing data and reading it back, keeping track of any errors in these transfers. After stepping through all 76 tracks individually the drive begins a random seek pattern (much slower than the Seek Test version) writing and reading back from each track accessed both headers and data. Once in this mode, the test will continue to run until the "G" key is pressed.

There are four display options already mentioned and they are:

- 1) Display on, no stop on errors (Type "D")
- 2) Display on, stop on errors (Type "E")
- 3) Stop and display only errors (Type "O")
- 4) No display, no stop on errors (Type "N")

all of which have their particular advantages.

If a system has yet to be qualified, the most useful of the options is number 1. This allows the user to keep watch for any errors which might occur at the beginning of the test and yet to leave the test running when he is not present. This is particularly useful in locating errors which might be located on a single track or series of tracks or particular seeks (such as a long seek of 70 tracks when the head might overshoot the track). It also can locate bad tracks on a particular diskette.

Where the previous option does not stop when an error occurs option number 2 will run only until an error is detected, displaying the transfers. If an error were to occur, the display will stop at that error and display the data. This option also keeps the heads loaded after the unsuccessful transfer so the user may get in and examine the logic states.

The advantage of the first two options is that they provide immediate information as to the success of the transfers and can save time in testing. The main disadvantage is that, since all results are sent to the video screen through the VDM driver, the test must wait until the results are displayed to begin another transfer. This slows down considerably the amount of tests run in a specific time period. For maximum number of tests, after a system has run an hour or so with the display on, the user might want to restart the test leaving the counter unchanged and leave the display off to maximize the number of transfers.

The option 3 will stop and display errors only again keeping the heads loaded if an error occurs for troubleshooting. This option also allows the user to, in the case bad data is read from the disk, to step through the buffer and look at its contents and compare them with the memory locations written to the disk. In this way the user can notice trends of errors as they might be repeated throughout the buffer.

The last option, #4, is the least useful diagnostic wise but allows for continuous testing with maximum transfer rate. It is most useful when qualifying a system that has passed all the other tests and is to be left running for a longer period of time.

All of these four options of the Automatic Test will generate a report anytime the "G" key is pressed. This report table is the key to qualifying the system as good or bad. The table is formatted as follows:

DRIVE & CONTROLLER TEST REPORT

(Hexadecimal Values)

	<u>HEADER</u>	<u>DATA</u>
NUMBER OF TESTS	0000	
WRITE ABORTS 0000	0000
NO ERROR FLAGS - BAD DATA! 0000	0000
READ ABORTS 0000	0000
NO TRANSFER COMPLETE 0000	0000
CRC ERROR 0000	0000
WRITE DATA MISSES (SOME OK) 0000	.0000

TYPE 'T' TO RESTART TEST, LEAVE COUNT UNCHANGED

TYPE 'C' TO CLEAR COUNT AND RESTART TEST

?

NOTE

Since sometimes there will be a fatal error during the execution of the DISKT program over long periods of time or on intermittent systems, there is a restart address which will get the user back into the test without resetting the error counter for the error table above. Providing the program is still in memory and is executable, type:

EX 6F <CR>

At this point the first frame of the test should be on the screen and all that is necessary is to start the Automatic Test over again and let it run a couple of minutes. When "G" is typed, the error table will be printed with all the errors which occurred before the test terminated. This is especially handy for when the machine suddenly dies in an overnight test and the user wants to see what might have caused it.

USING THE TEST RESULTS

Now that the user is familiar with DISKT and the maze of options within, what to do with the results of the tests? By using the various options, we can often narrow the problem to a specific element in the entire system. Here then are some hints.

As mentioned before, a unit that can pass the write/read tests but cannot pass the Seek Test is most likely to have a faulty disk drive (see alignment procedures for remedy).

A system that cannot pass the write/read section should be checked out more thoroughly using the DMA controller tests and waveforms in the Helios manual. By not passing, we are referring to either a program crash or a system which is never able to complete a transfer.

Drive problems usually manifest themselves in two ways, transfers which are most often successful and transfers which are never successful. Of the two, the former is most common. Places to check when intermittent errors occur from the drive are (refer to alignment procedures) Index Transducer alignment, Azimuth alignment, Seek problems, spindle speed or dirt on the heads (these are in the order of frequency). In the case where transfers are never successful, suspect Phase Locked Data Separator problems (check for clocks and data), problems in the enabling of the write/read circuitry on the D & I board, seek problems or spindle problems. In all cases of drive problems during DISKT, by running tests on both unit 0 and 1, the problem can be narrowed down rather quickly by checking for common problems.

Controller/formatter problems during DISKT fall into two categories as well, intermittent failures and total failures. Of the two the former is again the most prevalent. The most common intermittent failures on the controller are first the FIFOS, U52 and U53 and next the 8833 transceivers, U47 and U48. These problems usually manifest themselves as CRC errors. A little word is in order on how to read the results when the memory locations are printed out. The format is usually as follows:

DATA WRITE TEST: OK

DATA READ TEST: CRC ERROR -----> BAD DATA

TO DISK

0013: 24 11 7E FE 01 C8 F5 E6 7F 47 FE 0D C2

25D3: 25 11 7E FE 01 C8 F5 E6 7F 47 FE 0D C2

The common misconception here is that no data returned from the disk. For ease in comparison, however, the top line of data is what was read from memory (in this case starting at 0013) to the disk and the next line of data is what was read back from disk into the buffer (in this case starting at 25D3). Remember, that the buffer we DMA into begins at 25D3 so this instance indicates the very first byte was in error. If, by stepping through the buffer we find that every first byte of the 13 is wrong, we can suspect a timing error.

By examining the buffer we can tell a number of things. For instance, if the buffer were to have all 3Cs written in it we can assume the system can never accomplish DMA (this is so because before the controller does DMA, the program flushes the buffer with the 3C pattern). This leads us to a check of the DMA circuits.

Rarely does the test report back a CRC ERROR without a BAD DATA ERROR. In these circumstances the status latches (U33) and feeding circuits should be checked. The problem could also be in the CRC hardware of the formatter (U5) and these should be checked using the formatter checkout part of the DMA test in the manual.

NO ERROR FLAGS, BAD DATA usually indicates there has been a mix-up in the parallel/serial, serial/parallel conversion on the controller board and the FIFO and support logic should be re-examined.

Since there are five possible ABORTS in the disk system, an abort report, be it header read/write or data read/write, is almost

impossible to narrow down unless they happen very frequently. Places to check are POC going low during a HOLD REQUEST or during a WRITE operation, memory board constantly pulling down the ready line (on 16 KRA, due to coincidence cycles), Index hole was found in the middle of a transfer (OVER INDEX on the Formatter board) or due to a request to transfer occurring too late after a header was read and checked (SYNC ERROR on the Formatter). As you can see, there are many possibilities here, and as a result, this is the hardest problem to troubleshoot. A few errors scattered in this area are not disastrous as PTDOS will detect and correct for them but they are not desirable.

NO TRANSFER COMPLETE errors indicate the transfer length counter never reached zero. This could mean the counter was never decremented (U30 pin 13 on the controller never goes low), a status latch problem or a memory problem. In any case, check to see the value of 13 is loaded into the counter for a header and FFF is loaded for data transfers.

WRITE DATA MISSES occur when the formatter has read a header and is preparing to write a data block but runs into another sync byte. This sync byte indicates we should be at the end of data, not the beginning, and that too much time was taken to do the transfer. Some of these errors are allowed because there are times when the hardware is just too slow to accomplish the transfer in the tight time window allowed. The DOS can easily detect these and retry the transfer and so these errors are relatively harmless. Too many of these however, can really slow down the transfer rate.

This ends the section on the DISKT test program and its uses as a diagnostic tool and qualifying test for the Sol System III. It is advised that the reader become comfortable with the test as much as possible as it, when used correctly, is a most powerful diagnostic.

NOTE

This test can also be provided on diskette to those who want this convenience. We are currently in revision E of the test program, and anyone with a version older than revision E is urged to have his tape updated to follow any modifications made to the controller board.

To run DISKT from Service diskette, bootload diskette and type

```
DISKT (CR)
EX 3 (CR)
V
```


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SECTION 12

TROUBLE-SHOOTING PerSci DRIVES
(Supplement P/N 733010)

This section contains:

a synopsis of the functions of the diskette drive, common problems, testing and trouble-shooting and a recommended alignment procedure.

PART I

MECHANICAL

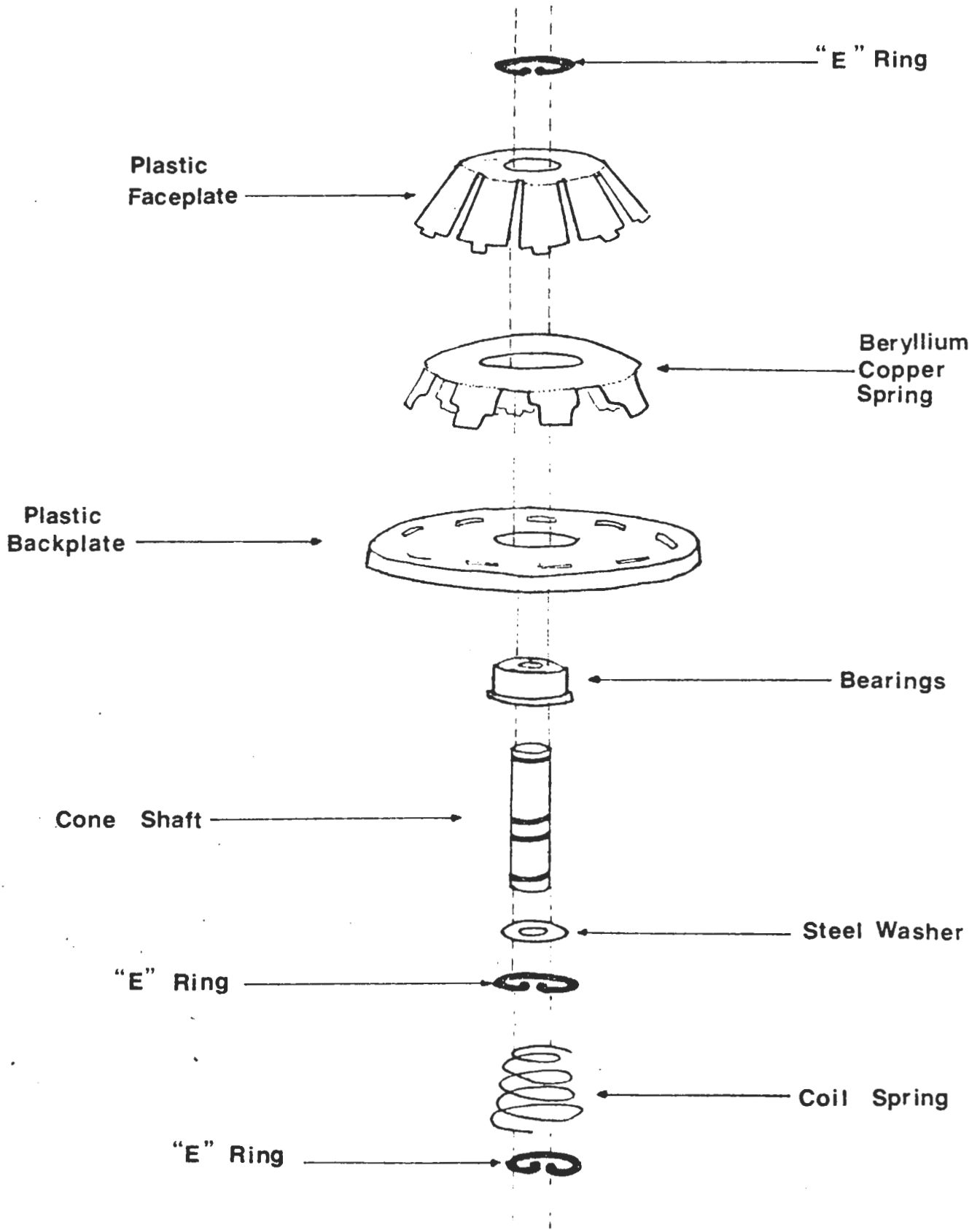
There are a number of service tips on the maintenance and repair of the Helios and PerSci drive. It is the intent of this section to explore some of the more common mechanical problems associated with the drive in particular. A good deal of the problems listed here are related to runs of serial numbers and, where applicable, these serial numbers will be mentioned. As of this writing, PerSci is entering the 6000 range in serial numbers and many of these problems have been solved. If you are at all uncomfortable about performing these or any other adjustments, Processor Technology factory personnel are available in the mornings (Western Time) to assist you. If any of the procedures are unclear please make note and inform us directly as the purpose of this manual is to assist you in the service of this product. On the other hand, if you have not attended at least one of the technical seminars, we urge you not to perform this maintenance and to return the unit to the factory for service.

CONES:

There have been two types of cones used on PerSci drives, white and black ones. Of the two, the black have a superior bearing and design, meaning in the long run, less replacement. However, the black cones also tend to stick inside the spindle even when they should release. One cure is replacement of the cone; the other is to disassemble the cone and bend the beryllium copper support spring tangs back in slightly towards the center bearing shaft. This reduces the pressure on the plastic cone to prevent it from sticking. (See the accompanying illustration for details.) The only other cone-related problem is a worn bearing. This is usually accompanied by loud squeals of protest and excessive slop when the spindle grasps the diskette.

TRIM POTS:

A run of bad trim pots surfaced in the early serial numbers (before the 1500's) caused by a manufacturer error. Most of these have been replaced by now, but if during alignment, the adjustments are erratic or keep changing then the pot should be replaced. This is especially a problem if the pot is on the reference oscillator (R154) for the spindle servo.



DISK DRIVE CONE ASSEMBLY

LAMPS:

With time, the lamps on the lamp amp PCB burn out as well as in shipping, the filaments sometimes break. See the alignment procedure, step 1, to determine this. The following is a replacement procedure for the lamp:

- 1) Remove drive from cabinet and remove 2 screws at bottom of D & I PCB to swing board up for service.
- 2) Remove four small phillips screws from black lamp housing (it may be necessary to remove head load paddle, side 1).
- 3) With solder iron and solder wick remove lamp leads from Lamp Amp PCB.
- 4) Replace lamp, solder and trim leads and reverse procedure. Re-align drive as necessary.

SPINDLE MOTOR:

The frequency of problems with the spindle motor is very small, the most common being arcing internally. This arcing causes intermittent operation. Another problem with the motor is freezing which usually shorts the motor supply 8 volt line and can cause the trace on the drive to fry. Since the motor is not repairable, it should be replaced. This is the procedure:

- 1) Remove drive from cabinet and remove screws at bottom of D & I PCB. Remove motor connector wires.
- 2) Remove drive pulley and diskette guide rails on lower portion of drive (side 0).
- 3) Remove side 0 door assembly by removing screws in bottom plate connecting to the hinge block and the screws (Allen) holding eject motor support bracket.
- 4) Remove 3 slotted screws securing motor to chassis, and making note of where washers are installed, remove motor.
- 5) Install new motor with washers in same location and reverse procedure. Check spindle speed.

SPINDLE BEARINGS:

In a few instances, drive spindle bearings will wear to the point at which the spindle will become very noisy. There was a run of serial numbers (around 3300) where this has been a problem after constant use. If you have a drive of this vintage and the spindle becomes noisier, be sure to return the drive to the factory for service. Bearings cannot be replaced in the field.

EJECT MOTOR SHAFT SUPPORT BRACKET:

PerSci has used 3 different styles for these brackets. The oldest one is the gray molded plastic, then the black molded piece very similar to the gray, and most recent is an extra sturdy black plastic quite larger than the former two. The first two will occasionally crack and cone will no longer retract. The newest brackets will no longer do this and the following procedure for replacement is recommended:

- 1) Remove drive from cabinet.
- 2) Remove the 2 springs connecting the support bracket to the door door assembly and the two allen screws mounting the bracket to the drive.
- 3) Remove set screw in steel cam at end of shaft and remove the steel cam (since lock-tight may have been used on this screw, it may be necessary to apply heat and then pull cam off).
- 4) Slide bracket off end of shaft and replace with the new heavy duty style.
- 5) Reverse procedure above.

EJECT CAM ADJUSTMENT:

Because the eject cam (mounted over the two rocker switches if front of eject motor) is made of plastic and the set screw is steel, there is a tendency in some units for this to become loose and the cam to become mis-aligned. In this case, the cone will not engage the diskette properly. Adjustment procedure is:

- 1) Loosen set screw securing eject cam with power off.
- 2) Turn power on press eject switch. Rotate cam manually until door is fully unloaded.
- 3) With the door unloaded, the set screw should be in the 12 o'clock position. Tighten screw until snug.
- 4) Manually trip diskette presense switch and check to see if cone seats completely into spindle.
- 5) Re-adjust as necessary and tighten screw. Be sure after adjustment, the door still operates correctly.

PLASTIC DISK EJECT ARM:

There have been in recent months, a few cases where the plastic arm which pushes the diskette out upon eject switch closure breaking. This also means a diskette cannot be re-inserted as the spring will kick it out again. Replacement is the only cure.

- 1) Remove eject cam motor assembly, eject shaft support bracket.

- 2) Remove plastic eject arm guide (fastened using 2 slotted screws).
- 3) Remove "E" ring holding eject arm onto shaft. Remove eject arm and spring assembly.
- 4) Install new eject arm (the spring is turned one full turn (360 Deg.) for correct tension.
- 5) Reverse procedure.

POSITIONER SERVO REPLACEMENT:

The following is the procedure for replacing the positioner voice coil servo:

- 1) Remove the following connectors: P8, P5 (on servo board), P8, P7, P15, P16 (D & I PCB) and all the plastic wire restraints.
- 2) Swing D & I PCB to its up position for servicing.
- 3) Remove black scale cover and 4 slotted screws which hold the rear of the positioner servo from moving (2 on top plate and 2 on bottom plate).
- 4) Remove positioner servo control PCB by removing 3 slotted screws from the bottom plate.
- 5) Remove Allen azimuth adjust screws (see azimuth alignment procedure for diagrams) and the Allen screw at the pivot point.
- 6) Carefully pull servo out towards back of drive being cautious not to damage scale or circuitry.
- 7) Reverse procedure.
- 8) Re-align drive on both sides as well as lamp amp voltages.

SPINDLE MOTOR SERVO CONTROL PCB REPLACEMENT:

- 1) Lift D & I PCB to the service position.
- 2) Disconnect the following connectors to the spindle control PCB: P5, P4, P1 and P2.
- 3) Remove 2 slotted screws (some models may have Phillips) from the steel diskette guide shield. There are 2 spacers which these screws go through. Remove these as well.
- 4) Remove screw located near Q1 and Q6 on the PCB. Reverse the procedure being sure to use the spacers.
- 5) Remove old board and re-install new control PCB. Reverse the procedure being sure to use the spacers.

CAUTION

The motor supply jack, J1, must have the red wire to the right and black to the left (when the board is mounted and the view is from the D & I PCB side) for proper polarity.

PART II

CIRCUITRY

SEEK RELATED PROBLEMS

Head Oscillating, Humming or Squealing:

- 1) Lamp Voltage too low or too high.
- 2) U3 on Lamp Amp PCB breaking into oscillation due to noise or a heat sensitive op amp.
- 3) Bad Lamp or photocell assembly. If this is the case, most likely the head will have very little resistance when it is moved back and forth by hand.
- 4) Seek times adjusted wrong (too fast or too slow).

Head Will Not Seek or Slams to Extremes and Won't Restore:

- 1) Positioner voltage adjusted incorrectly (3 v P-P min!).
- 2) Seektime mis-adjusted.
- 3) J8 to positioner servo loose or intermittently contacting.
- 4) Can't find track 0 on power up.
 - a) P8 pin 1 should be high when at track 0.
 - b) P8 pin 5 should be below when at track 0 and high otherwise.

LOGIC LEVELS:

Interface line logic levels are as follows:

Negative level = 0.0V to +0.5V, -0.5V.

Positive level = +2.5V, -2.5V to +5.5V, -5.5V or open circuit

I/O signals are negative when selected (True).

5) When at track 0 the following pins on P8 should be high:

Pins 1, 6 and 12

When at track 0 the following pins on P8 should be low:

Pins 2, 3, 4, 5 and 9

- 6) FET (U6 on Positioner Servo Control PCB) is blown or malfunctioning.
- 7) Support logic/op amps/output amps and drivers are malfunctioning (Positioner Control PCB).

Head Skips Tracks:

- 1) Crack, dirt or flaw on lamp scale.
- 2) Excessive track overshoot.

SPINDLE SPEED PROBLEMS

- 1) Diskette presence not switching due to D & I problem.
- 2) Spindle enable (P1 pin 24) not grounded.
- 3) U28 pin 9 (D & I PCB) should be at 200 KHz.
U28 pin 10 should be high.
- 4) Q4 or Q5 (Power transistors) shorted ==> Spindle free runs.
open ==> Spindle won't turn.
- 5) U4 on spindle control PCB has one of its inputs tied low at all times.
- 6) Power supply voltages are incorrect or not present.
- 7) Photo transistor on tach not switching op amp (U7 on spindle control PCB).
- 8) Servo loop broken where U6 pin 7 not switching the counters on the servo control PCB.
- 9) Push Pull amp, Q2 & Q3, malfunctioning.
- 10) Intermittent connectors.
- 11) Spindle motor internally shorting and drawing too much current.

9 EPT 4 - 10
DRIVE NOT READY

NOTE:

The signal drive ready depends on three signals.
They are:

- 1) Spindle turning (at least 50% up to speed).
 - 2) Index pulse present on selected unit.
 - 3) Diskette presense micro switch depressed.
-
- 1) Data and Interface P1 pin 22 low when unit 0 is ready.
 - 2) Data and Interface P1 pi 6 is low when unit 1 is ready.
 - 3) Index pulse should be present at: U30 pin 3 for unit 0
(D & I PCB) U30 pin 11 for unit 1
 - 4) U6 pin 6 (D&I) should be low for unit 0 ready.
U6 pin 2 should be low for unit 1 ready.
 - 5) If diskette presense micro switch is tripping, U32 pin 2 should go high.
 - 6) J5 pin 5 on D & I PCB should go high as spindle reaches correct speed.

INDEX/SECTOR MISSING

Drives Previous to Serial #2500

- 1) U22 pin 7 should have switching TTL levels for Sector unit 0.
U18 pin 7 should have switching TTL levels for Sector unit 1.
- 2) Photo transistor should be saturating (see alignment procedure, step 15).
- 3) Timing on one-shots (U10) incorrect:
 - a) pins 5 and 12 switch with each sector mark.
 - b) pins 4 and 13 switch with each index mark.
- 5) Hard sectored diskette requires 32 sector holes + 1 index.

Drives after Serial #2500:

- 1) Identical to step 1, above.
- 2) Identical to step 2, above.
- 3) U19 not enabled by the unit select and/or drive select logic.

- 4) U60 pin 4 should be high.
U60 pin 5 should be switching with every sector hole.
- 5) Index unit 0:
 - a) U26 pin13 has an index pulse every 166.7 msec
 - b) U26 pin 12 held high
- 6) Index unit 1:
 - a) U26 pin 12 has index pulse every 166.7 msec
 - b) U26 pin 13 held high

NO SEPARATED CLOCKS OR DATA

- 1) U1 pin 1 on PLO PCB for read data pulses.
- 2) PLO Clock on P6 pin 1 should be relatively stable (output from U5 pin 11 on PLO board).
- 3) Stable 500 KHz sawtooth on TP 3 of PLO board with heads loaded. If it is unstable, adjust R13 for stability.
- 4) TP 1 and TP 2 on PLO board should be biased correctly (see alignment procedure, step 9).
- 5) Check one-shots (U10 pins 4 and 12) for pulses.
- 6) Check the Johnson Code Counter (U4, U6 and U7) for counting pulses. This is a common problem area.
- 7) If all these signals are present, check the connections from J6 on D & I to the PLO board for cold solder joints, broken wires or loose crimp connectors. This is a common problem on the drives.
- 8) Check the drivers on the D & I board (U13).

WRITE PROBLEMS

Drive Won't Write at All:

- 1) PLO Clock is off.
- 2) No Index pulse or "Drive Not Ready."
- 3) U20 (D & I) pins 4 and 2 should be switching during a write.
- 4) U24 (D & I) pins 8 and 9 should be switching TTL levels:
 - a) Pulses close together for logical ones
 - b) Pulses far apart for logical zero
 - c) Pulses mixed for pattern of ones and zeros
- 5) The read back FETs should be biased off during a write or the FETs will "steal" the current from the write heads.

- 6) Biasing for the write transistor circuitry (Q19 - Q25) is not correct. The bases of Q20 for unit 0 and Q23 for unit 1 from track 0 to track 43 should be at 24 Volts. From track 44 to track 76, however, they should be biased at 12 Volts. If not, check track sense (alignment step 4) and the supporting analog circuits to the write logic (e.g., tunnel erase).
- 7) U21 pin 13 should be low when reading and high when writing. The following logic should switch accordingly.

NOTE

The PerSci drive is set up in such a way that when the unit is not writing it is reading. This means the units are always reading unless told to write.

- 8) Write protect (U29 pin 13 on D & I) is being held low.
- 9) Write protect LED installed and connected to J19 or J20 on the D & I PCB.
- 10) Power on delay (U29 pin 12 on D & I) held low or waiting for the spindle to come up to speed.
- 11) Faulty drive select logic on D & I board.
- 12) Cable or indicator panel malfunction.
- 13) Bad head or crimp connector at P15 or P16 connecting the heads to the write drivers.

Write Retry During A DISKCOPY:

- 1) Head penetration on side 1 incorrectly adjusted (refer to alignment procedure, step 19).
- 2) Dirty head (clean with a gauze pad and 95% Isopropyl Alcohol).
- 3) Head motion being mechanically impeded by head cable (unit 1) catching on the IC socket pins (solder side) of D & I board. Re-route head wires through restraints.
- 4) Short or open in the head connecting wire harness or loose connection inside the head itself. These problems might be aggravated during a rapid or extreme seek and relatively undetected at other times. The SEEK TEST should catch these.
- 5) Worn heads (this is most unlikely due to the superior construction of the heads). The heads are specified to last 5 years.
- 6) Bad or worn diskette, wrong diskette. PerSci recommends the following diskettes with their drives:

*DYSAN and MAXELL

*NOTE: Of the two, it is our experience DYSAN has a longer life and is more durable.

PART III

SIMU-CISOR

PerSci DRIVE EXERCISOR PROGRAM

This program simulates the operation of the PerSci Drive exerciser by using the Helios II hardware in conjunction with the Sol.

Requirements for using this program are:

- 1) Functional Sol.
- 2) Functional Helios controller boards.
- 3) 8K of contiguous memory starting at location 0.
- 4) Processor Technology Service and Maintenance Manual.

To load this program from cassette use the SOLOS command:

XEQ SIMU (Carriage Return)

SOLOS will respond by removing cursor.

The program will now be loaded and will automatically execute. The starting address is at 0.

COMMAND SYNTAX RESTRICTIONS

This program is written to start and restart at location 0. The command name must start at the first location after the '*' prompt. All parameters must be separated from each other or the command name with a minimum of 1 space and a maximum of 9 spaces. Only the first 2 characters of the command name are significant, but the command name cannot be more than 11 characters long.

DEFINITION OF TERMS:

- trkn Track number in the range of 0 to 76.
- patrn A number in the range of 0 to 76. This number does not represent the actual pattern but is used as a key as to the pattern to write.
- { } Denotes an optional parameter.

SPECIAL KEYS:

Global:

escape Unconditional return to Solos/Cuter.

mode select Abort current command and return to Simu-Ciser
or ctrl-@ command mode.

Local:

'T'oggle Used only by the HLoad command. Causes head on
selected unit to unload if loaded and load if unloaded.

'A'utomatic Set mode of SEek of SStep to automatic. Between each
step or seek, the consol input is checked for a change
of mode or abort. If a 'M' is the character that was
received, the mode of the step or seek is changed
to manual.

'M'anual Set mode of SEek or SStep to manual. When in this
mode the program will wait for input from the consol.
If the character received is an 'A', the mode of the
seek is changed to automatic.

'Y'es Used only as a verification of the WRite command.
Your only chance to abort the WRite command is when
the program is waiting for this character.

COMMAND DEFINITIONS:

WRite trkl unit ptrn

WRite a pattern, signified by 'ptrn', on track 'trkl' of the disk in
unit 'unit'. The argument 'ptrn' is interpreted as follows:

	0	means a pattern of all zero bits.
	1	means a pattern of all one bits.
A number greater than 1		means a pattern of eight zero bits and eight one bits.

Your only chance to abort this command is when the program is waiting
for a response to the 'Insert disk...' prompt. At this point
pressing the 'Y' key and return will allow the program to continue.
.Any other key will abort the write.

SStep trkl trk2

Single step from trkl to trk2. This command will single step from
trkl to the next track in the direction of trk2 and wait for seek
complete. At this point the consol is checked for a change of mode
or an abort. Upon reaching trk2 the direction of the seek will
change.

SEek trk1 {trk2}

This command will seek directly from trk1 to trk2 with no delay. The program will ask the user to select the unit desired (Unit 0, type "0", unit 1, type "1"). The program will also ask whether Automatic Mode or Manual Mode is sought (type "M" for Manual and "A" for AUTOMATIC). When trk2 is reached the consol will be checked for a change of mode or an abort. If an abort is not received, the direction of the seek is reversed. If the optional second parameter is not present, the program will seek to trk1 and return to the command mode.

HLoad unit

This command causes the read/write head of unit 'unit' to be loaded. After the head is loaded the program will wait for a 'T' or an abort from the consol. If a 'T' was the character received, the program will toggle the state of the head, i.e., if the head is loaded, it will be unloaded. This sequence will be repeated until aborted.

REstore

Restore drive to track.

EXit

Return to the Solos/Cuter monitor.

CE <unit>

This command will step the heads from track 1 to track 38 to track 76 and back again. Each time a keyboard key is depressed, the head will seek to the next track in 38 step intervals. This step is especially designed for the head alignment steps of the alignment procedures.

<unit> SimuCisor will select one of 4 units by designating a number between 0 and 3.

POSITIONER LAMP PROBLEMS

TOOLS REQUIRED:

Dual trace scope with external trigger, SIMU (PerSci drive exercisor program for drive alignment) loaded into a Sol with a set of Helios controller/formatter boards in operation, small Phillips and standard screwdrivers. Also required is a solder iron and wick for lamp replacement and a replacement lamp available from factory (Part No. 100013-003).

BACKGROUND:

The PerSci drive uses an incandescent lamp for detection and feedback in the head positioning servo motor circuitry. Since this lamp is incandescent, it has finite lifespan and may need replacing from time to time. In addition, the lamp voltages may need adjustment occasionally to keep the circuit within specification. The normal lifespan for these lamps should be approximately 10,000 hours.

PerSci has used 3 different lamps in an attempt to increase reliability of the circuit. The most recent of these lamps is rated at 1.5 volts and its predecessors were 1.8 volts and 1.5 volts.

Drives with Serial Numbers 3000 and under have the 1.8 volt lamp and will seldom have a lamp problem. Drives from 3000 to approximately 9500 have the 1.5 volt lamp and are the most likely to have lamp problems. Drives after 9500 will generally have an 002 lamp which is rated at 40,000 hours and is said to have a heavy duty filament. These lamps are marked with an 002 on the lamp holder (D & I PCB must be lifted to see this).

The following is an explanation of service and repair of this lamp.

CHECKS:

To determine if the positioner lamp should be replaced due to aging or is burned out, perform the following steps:

- 1) Check the voltage between test points 1 and 7 of the Lamp Amp PCB on the PerSci drive (see Figure 2). If this voltage is 1.65 volts or greater, yet the drive is still functional, the lamp should be replaced as it has aged. The fact that the voltage is at 1.65 volts indicates the circuit is reaching the limit of compensation for bulb filament decay.
- 2) Check to see if the Seek light on the Helios indicator panel is lit (normally this light will be lit unless the drive is in the middle of a seek). If this light is not lit, go on to the next step.
- 3) With power applied check the voltage on the Lamp Amplifier PCB of the drive (see Figure 2) between test points 1 and 7. This should read between 1.25 and 1.65 volts DC when operating correctly. If the voltage is 1.65 volts or greater (typically between 2 and 5 volts DC) go on to the next step.
- 4) With power to the drive OFF, measure the resistance between test points 7 and 1 on the Lamp Amp PCB. When operating correctly, the resistance should be 35 ohms or less. If the lamp is burned out this resistance will approach infinity.

The following is the Positioner Lamp replacement procedures:

- 1) Remove drive from Helios cabinet and remove the 2 screws at the base of the Data & Interface PCB of the drive. This will allow the D & I board to swing upward on its hinges (see Figure 1).
- 2) Remove head load paddle unit 1 and wire guide on unit 1. Also remove 4 screws mounting the lamp assembly to the lamp housing. (See Figure 1.)
- 3) Using solder wick, remove the 2 leads of the lamp from the Lamp Amp PCB being careful not to lift pads or overheat the circuit board.
- 4) Install a new lamp assembly, solder and trim the leads.
- 5) Re-install the 4 lamp assembly mounting screws, the head load paddle, the wire guide, and the 2 screws which fasten at the bottom of the D & I PCB.
- 6) Perform alignment steps 1 through 6 of the PerSci alignment procedure in the Service and Maintenance Manual which follow.

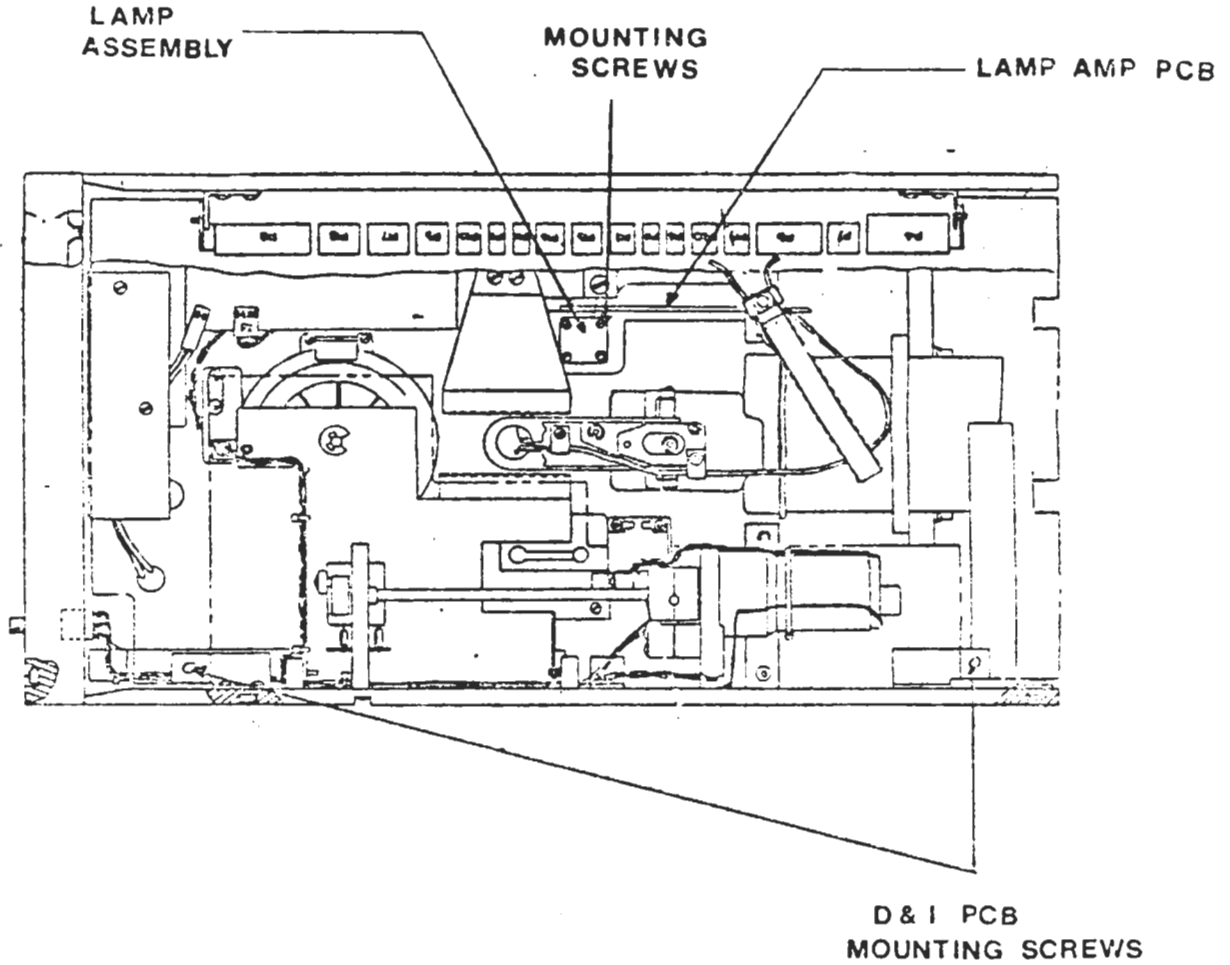


Figure 1

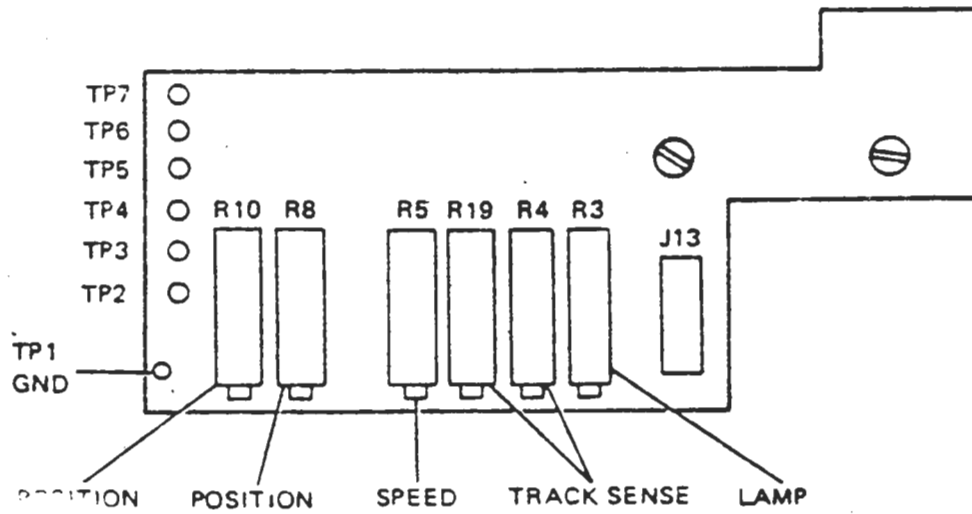


Figure 2

PART IV

ALIGNMENT PROCEDURE

The following is the recommended alignment procedure for the PerSci Model 270 Disk Drive. The procedure is to be used in conjunction with the Processor Technology Simucisor program available on cassette and a SOLOS/CUTER computer with Helios II disk controller boards.

A general alignment is recommended under the following circumstances:

- 1) Disk Drive fails the "Seek" portion of DISKT test program or has erratic seeking problems.
- 2) Disk Drive gets an inordinate amount of errors during the "Automatic" portion of DISKT test program and the problem has been isolated away from memory/controllers.
- 3) Disk Drive cannot read diskettes written on other units or written on unit 1. This will be referred to as incompatibility between drives.
- 4) Miscellaneous problems such as missing Index/Sector pulses, spindle speed problems, inability to write to a diskette or routine maintenance.

It is recommended that the technician read through the procedure first before attempting to align the disk drive, and that the procedure be followed in order.

The following tools are required:

- 1) Dual trace Scope with external sync and at least 25 Mhz bandwidth and ability to invert one of the channels.
- 2) Set of Allen wrenches similar to Xcelite #99-PS-40.
- 3) Set of screwdrivers ranging from 1/8" blade to 3/8" blade as well as Phillips type.
- 4) 4-inch piece of heat shrink tubing used to insulate the above screwdrivers and Allen wrenches from possible shorts during catseye/azimuth adjustments on unit 0.
- 5) 95% isopropyl alcohol and cotton swabs.
- 6) Dysan Alignment Diskette (obtained from Processor Technology).
- 7) Scratch diskette (32 sector holes).

NOTE

The waveforms in this section are ideal representations.

9 EPT 4 - 20
ALIGNMENT CHECKLIST

Technician _____

STEP

1. LAMP VOLTAGE _____
2. TACH VOLTAGE _____
3. POSITIONER VOLTAGE _____
4. TRACK SENSE _____
5. DIRTY SCALE _____
6. A) SEEKTIME _____
B) 1-0 OVERSHOOT _____
C) 75-76 OVERSHOOT _____
D) STEP SEEK _____
7. SPINDLE SPEED _____
8. ISV _____
9. PLO _____
10. SEP CLOCK & DATA _____
11. RESOLUTION SIDE 0 _____
12. HEAD CONTACT 0 _____
13. HEAD LOAD 0 _____
14. CONE SIDE 0 _____
15. INDEX SIDE 0 _____
16. AZIMUTH SIDE 0 _____
17. CATSEYE SIDE 0 _____
18. RESOLUTION SIDE 1 _____
19. HEAD CONTACT 1 _____
20. HEAD LOAD 1 _____
21. CONE SIDE 1 _____
22. INDEX SIDE 1 _____
23. AZIMUTH SIDE 1 _____
24. CATSEYE SIDE 1 _____

CAUTION!!

If drive is removed from cabinet, be sure diskette eject switch solder contacts do not short to the drive base or chassis with power on. This will short 24 volts to ground and burn out R126 or R137 on the Data & Interface Board. When adjusting any pots on the drive, be sure to use a plastic or non-conductive bladed screwdriver. Also be sure to check alignment any time the drive is removed and then re-installed in the cabinet. There is a slight tendency of the cabinet and mounting hardware to torque the drive chassis.

GENERAL ALIGNMENT PROCEDURE

1. POSITIONER LAMP VOLTAGE:

The positioner lamp is either a 1.5 or a 1.8 volt incandescent bulb mounted on the lamp amp PCB and provides the light source for the solar cells which detect markings on the positioner scale.

NOTE

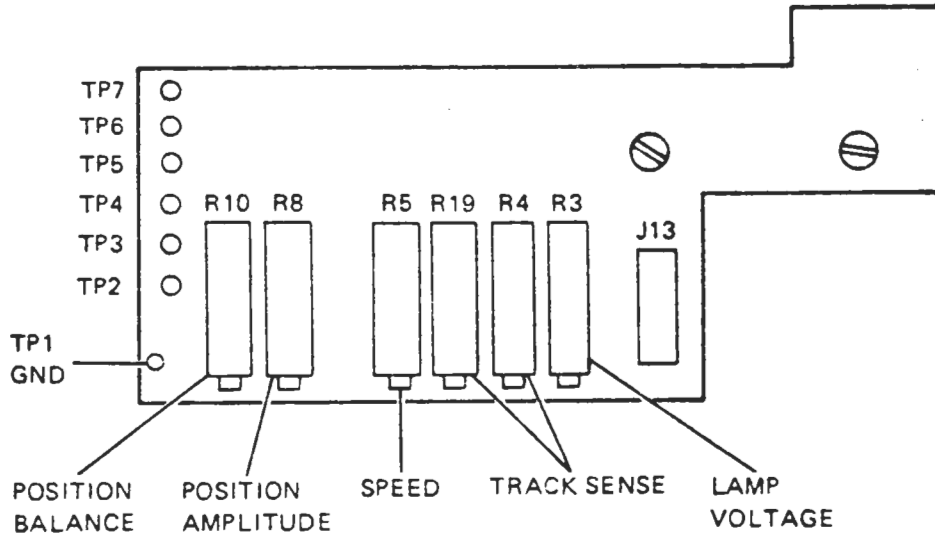
The lamp adjustment affects all other adjustments on the Lamp Amp PCB and should always be done first.

Connect scope to TP 7 on the Lamp Amp PCB and DC couple the scope. Scope should read about +1.5 volts if earlier than Serial Number 9500 or if there is NOT an 002 designation on the lamp assembly (D & I PCB must be lifted to determine this). If there IS an 002 marked on this lamp, scope should read +1.3 volts DC. If this voltage is incorrect, adjust R3 (2K pot on Lamp Amp PCB of Figure 1) for correct voltage.

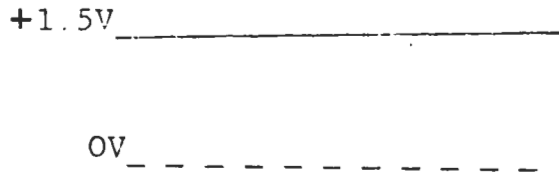
If lamp reads 1.65 volts, it should be replaced as the life of the lamp is nearly over. When the compensation circuit increases the voltage to the lamp to this point it is almost certainly due to lamp filament decay. If the lamp voltage is between 2 to 5 volts and the drive will not seek, the bulb is burned out. The resistance between TP1 and TP6 should be close to 30 ohms. If this resistance is infinity, the lamp is bad for certain. (To replace, see "Positioner Lamp Problems," in this section.

2. TACH VOLTAGE:

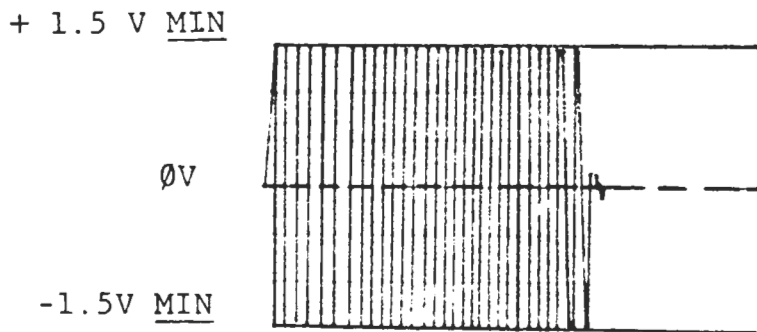
This is a coarse adjustment of the circuit which controls the speed at which the drive heads seek between tracks. The fine adjustment of this circuit is in step 6. Symptoms of a problem in this circuit is seeking either too fast or too slow or "hunting" for tracks. A problem here could also cause the head not to seek at all or to slam to the stops.



Lamp Amplifier PCB



1. Lamp Voltage



3. Positioner Voltage

Connect a scope probe to TP 5 of the Lamp Amp PCB and disconnect P8 (the 3-lead coaxial power cable going to the voice coil from the bottom of the positioner servo PCB. This allows manual movement of the head assembly. Manually move the head to track 0 and note the voltage reading on the scope. Move the head manually to track 76, and again note the voltage reading. Adjust R5 for a -1.5 volt difference from the track 0 reading.

3. POSITIONER VOLTAGE:

This adjustment sets up the correct voltage levels for the detent pulses (one full sine wave for each track the head moves) which enable the drive to "know" how many tracks the head has traversed. Symptoms of a problem here might be Seek Errors (during PTDOS or DISKT), "hunting" or heads slamming to extremes. Problems here will also prohibit the heads from seeking entirely.

Connect scope to TP 2 on the Lamp Amp PCB and leave P8 disconnected as in previous step. Manually move head between tracks 0 and 76 and note voltage on scope. The voltage should be an absolute minimum of 3 volts peak to peak and should be centered about the 0 volts line. Adjust R8 to increase or decrease amplitude and R10 for balance above and below 0 volts.

4. TRACK SENSE ADJUST:

The purpose of this adjustment is to allow the drive to sense when it reaches track 43-1/2 at which point the head write amplitude must be decreased. This keeps the heads from over saturating the media on the innermost tracks which are moving past the heads at a slower velocity than the outermost tracks.

NOTE

At this point it is necessary to have the SIMU-CISOR PerSci exercisor program loaded into 8K of memory at 0 and to be in the command mode (designated by the asterisk prompt). Also be sure the P8 connector removed in the previous steps is reconnected.

TYPE: SE 44 43 <CR>

Simu will respond "Automatic or Manual?"

TYPE: A <CR>

The head should now be seeking between tracks 44 and 43. Place scope probe on TP 6 of the Lamp Amp PCB. Adjust R4 (gain) and R19 (balance) for a voltage swing between +0.3V to +0.4V and -1.25V centered about the 0 volt reference line.

5. DIRTY SCALE:

Under normal operation, the scale is protected from dust particles by the scale cover and the filtered air system within the Helios cabinet. However, in certain instances, the scale will become dirty and must be cleaned. In particular, the wedge-shaped window on the bottom of the scale (referred to as the velocity wedge) which is used for tach feedback is most sensitive. A problem here might cause erratic seeking, skipping tracks or slamming to one stop or the other.

TYPE: SE 0 76 <CR>

SIMU: "Automatic or manual?"

TYPE: A <CR>

SIMU: "Unit?"

TYPE: 0 <CR>

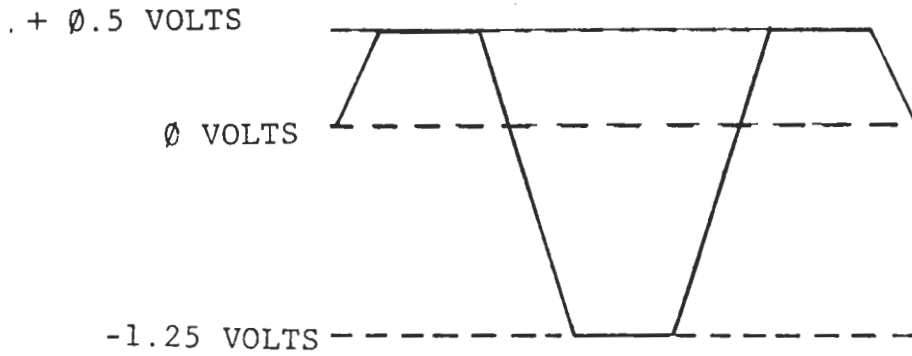
The head should now be doing a fast seek between tracks 0 and 76. Trigger scope on pin 10 of P1 (the 50-pin edge connector on the Data & Interface PCB which is SEEK COMPLETE). Scope should be AC coupled, External sync, .5V/division, and 10 ms/division. Scope probe should be on C8 (right side as viewed from rear) of Positioner Servo PCB (this is also U13 pin 7). Normally there will be a small amount of noise riding on this signal. Any spikes greater than 0.25 volts (see diagram) usually indicate dirt or crack on the scale. Both sides of the scale should be cleaned with a dry cotton swab. If this does not work, use a cotton swab slightly dampened with isopropyl alcohol and then wipe again with a dry swab. Be sure to replace the scale cover when cleaned. A good way to tell if there is some dirt on the scale is to restore the head to track 0 and manually pull the positioner out to track 76. If there is no dirt, the motor should feel smooth when moving. If there is dirt, however, the servo motor will feel rough as though there were burrs on the guide rails.

1) Check P7 Connector Contacts.

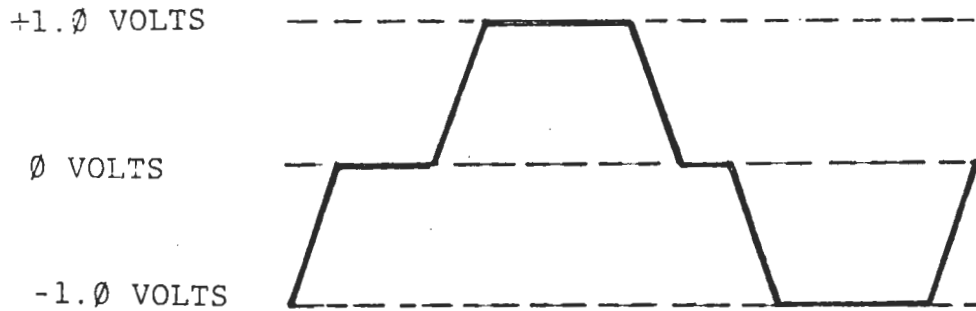
Along with this step check the P7 connector contacts. Dirty or corroded contacts could cause erratic seeking problems. The cause of this oxidation/corrosion is the high amounts of current going from the D & I PCB to the Positioner Servo PCB and Lamp Amp PCB to PCB through this connector.

2) Turn OFF AC power to the Helios II. Disconnect the AC linecord from the rear panel.

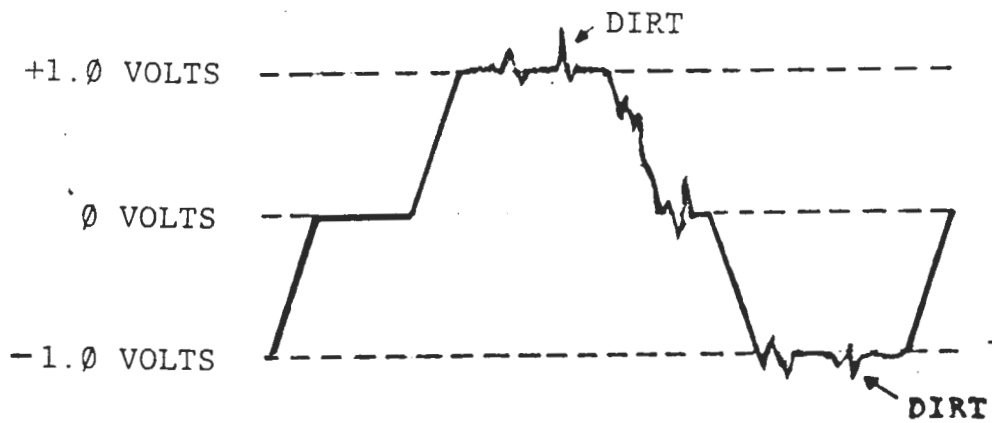
3) Remove P7 connector on the D & I PCB and inspect the connector contacts for corrosion or intermittent contacts. If the contacts are corroded or have oxidation, they must be cleaned using emery cloth or a similar abrasive material (NOT steel wool as this has a tendency to leave conductive strands behind).



4. Track Sense



5. CLEAN SCALE (NO SPIKES)



5. Dirty Scale

6A. SEEK TIME (Track 0 to Track 76)

This is a coarse adjustment to bring the seek time between track 0 and 76 into specification which is a maximum of 95 milliseconds.

TYPE: SE 0 76 <CR>

SIMU: "Automatic or manual?"

TYPE: A <CR>

SIMU: "Unit?"

TYPE: 0 <CR>

The head should now be seeking between track 0 and track 76. Move the scope probe to TP 2 on the Lamp Amp PCB and trigger on SEEK COMPLETE (pin 10 of P1, the 50-pin connector at rear of Data & Interface PCB). There should be a 3 volt peak to peak signal balanced about the 0 reference (as adjusted statically in previous step 3). If not, adjust R8 and R10 as in step 3 to bring this into specification for dynamic motion. With the scope set at 10 msec/division, trigger to see burst. The burst should be 9.5 divisions long, i.e., 95 ms (see illustration). If necessary, adjust R5 on Lamp Amp PCB to speed up or slow down the seek time.

6B. SEEK TIME (Track 0-1)

TYPE: SE 0 1 <CR>

SIMU: "Automatic or manual?"

TYPE: A <CR>

SIMU: "Unit?"

TYPE: 0 <CR>

The heads should now be seeking between tracks 0 and 1, and the scope probe should be on TP 2 and triggered on SEEK COMPLETE as in the last step. Time base should be on 1 ms/division. Trigger to see one full cycle as in illustration. There are actually 2 waves, both sinusoidal, but 180 degrees out of phase representing the forward and backward seeks. They should be 10 msec and be relatively symmetrical about 0V reference. Adjust R5 on Lamp Amp PCB for speed and R33 on Positioner Servo PCB (in the upper right corner of the board and the only pot on that board) for symmetry.

NOTE

If your scope has a Trigger View Mode as does the TEK 465, the following procedure will simplify this:

- a) While seeking and triggered as in above, press the trigger view switch and adjust the trigger level control for a good view of the signal. This usually means centering the signal which is a square wave and a positive edge trigger. Time base should be on 2 msec/division.
- b) The trigger signal should be 10 msec long (5 divisions) if the seek time is correct. If this time is incorrect, adjust R5 on Lamp Amp PCB to bring into specification.

6C. SEEK TIME (Track 75-76)

TYPE: SE 76 75 <CR>

SIMU: "Automatic or manual?"

TYPE: A <CR>

SIMU: "Unit?"

TYPE: 0 <CR>

The heads should now be seeking between track 75 and track 76 and the scope should remain set as in step B. Again, adjust R5 and R33 for 10 msec duration and symmetry with reference to 0V as in step B, above. (NOTE in step B also applied to this step.)

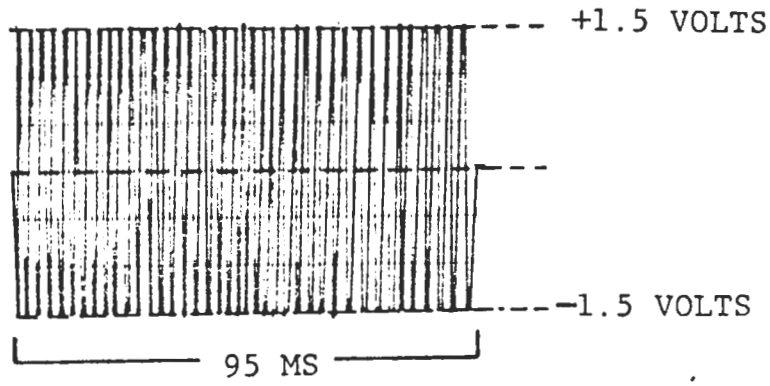
6D. STEP SEEK AND OVERSHOOT:

TYPE: SS 0 76 <CR>

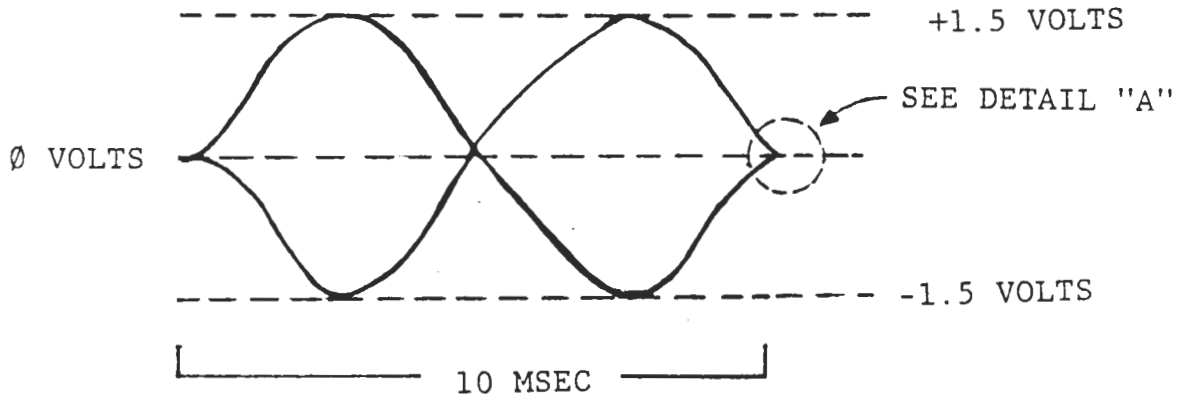
SIMU: "Automatic or manual?"

TYPE: A <CR>

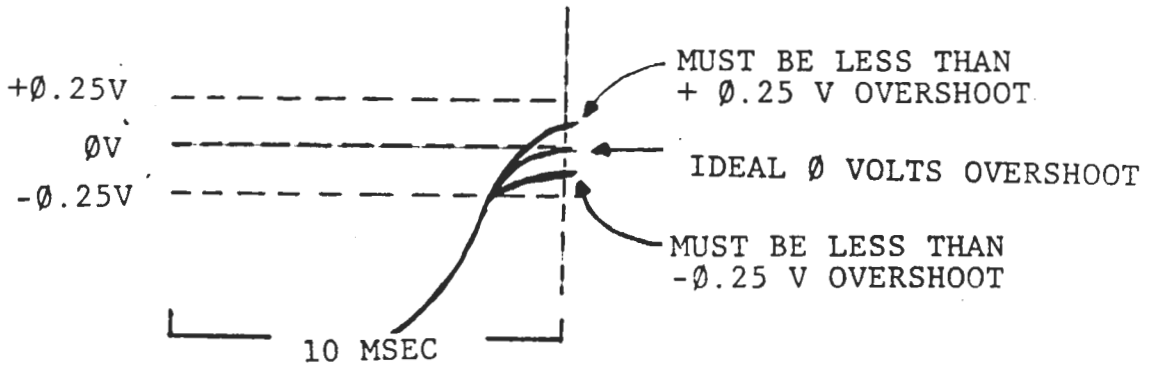
The heads should now be doing a rapid step seek between tracks 0 and 76. The head is actually stepping to each individual track, stopping, then proceeding to the next track. The scope setup is the same as the previous 2 steps, and time base should be on 2 msec/division. Trigger to see one full cycle (it will change phase every time the head reaches an extreme and changes direction of seek). The period of the wave should again be 10 msec and should have settled within 0.25 volts of the 0 reference line by the time the 10 msec is past (see diagram). If this is not the case, adjust R5 and R33 as in the previous 3 steps, to bring into specification.



6 A. SEEK TIME 0 - 76



6 B & C Seektime [Track 0-1 & 75-76]



Detail "A"

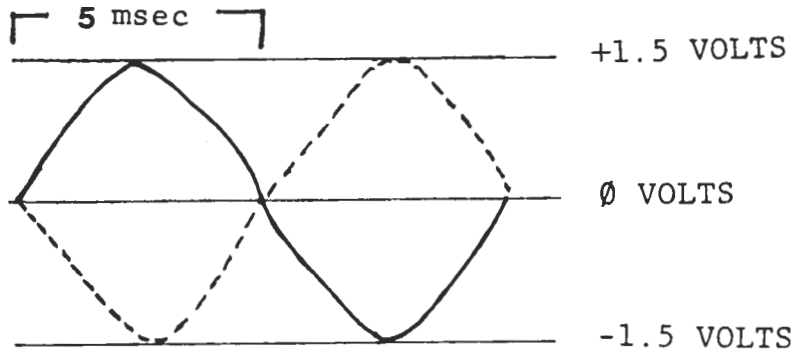
NOTE

If excessive jitter occurs on scope display of this waveform, there is a good possibility the positioner scale is dirty or has a piece of dust on it, and step 5 should be repeated.

7. SPINDLE SPEED

It is critical to the controller hardware that the spindle speed be as close to 360 RPM as possible. For that reason, the spindle is controlled by a DC Servo loop which constantly monitors its speed. The reference oscillator for this circuit is on the D & I PCB (Page 3 topmost op amp on the D & I schematics) and free runs at 200 KHz.

The most common problem in this circuitry is a worn motor or spindle bearing (usually preceded by noise) or the output transistors to the spindle motor itself.

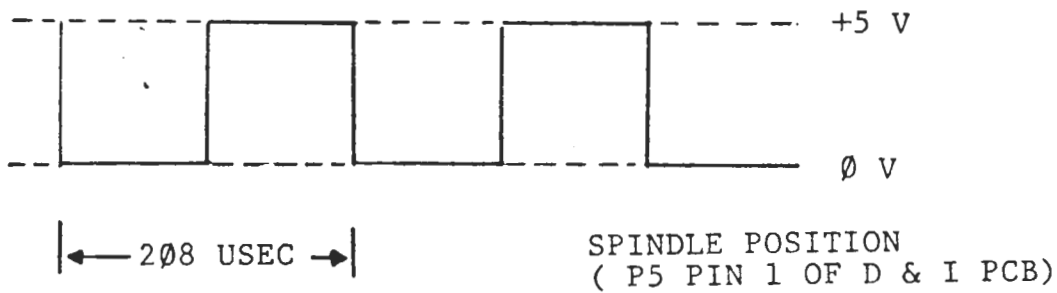
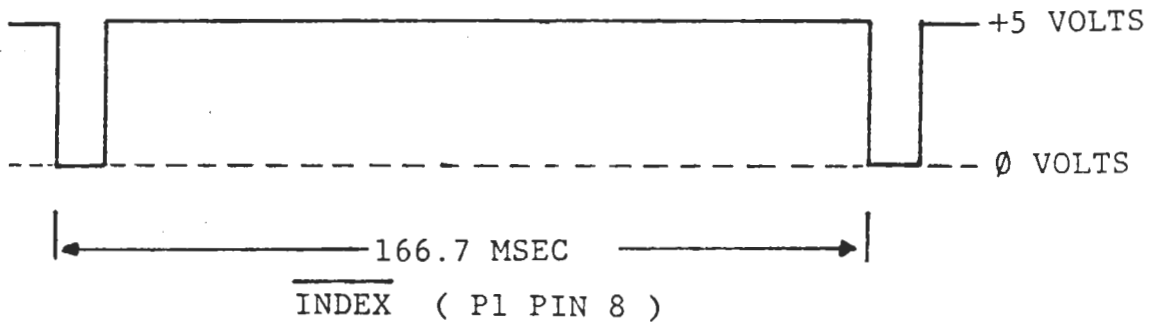


REPRESENTS SINGLE TRACK SEEKS FROM 0 TO 76



REPRESENTS 180° PHASE DIFFERENCE IN STEP SEEK 76 TO 0

6D Step Seek Overshoot



7. Spindle Speed

If no counter is available, place diskette in either unit, and measure the interval of the Index pulse on P1, pin 8 (D & I PCB), it should be approximately 166.7 msec (use 32 sector hole diskette). Next measure P5, pin 1, (D & I PCB) it should have a period of 208.3 usec with the spindle in motion. If these are off, adjust R154 on D & I PCB until they come into spec. If a frequency counter is available, connect to P5, pin 1, as above, and measure the frequency.

It should be 4.8 KHz with a diskette spinning. Pin 3 of P5 should be a 200KHz square wave whether or not a diskette is inserted.

8. INSTANTANEOUS SPEED VARIATION:

This is a check of the spindle servo to ensure that it can track the rotational speed of the spindle and compensate for any variation in speed. There are no adjustments to be made.

Connect scope to P5, pin 1 as in last step, and display about ten cycles on scope (diskette should be turning). Next go to 10X magnification on the scope. The pulse must not wander more than 3 cm total. Slow spindle slightly with pressure on the diskette, the pulse will drift considerably but should return rapidly to original location when pressure is released and as the servo again locks in. Problems in this area are very rare.

9. PHASE LOCKED OSCILLATOR:

The Persci drive is responsible for providing separated clocks and data to the controller board. To accomplish this, a phase-locked loop detects the pulses much like the cassette interface of the Sol except discreet components are used. Problems in this area most often occur in this PLL circuit, and most can be eliminated by proper DC bias. Rarely is there a problem in the Johnson Code Counter circuit or the following one-shots.

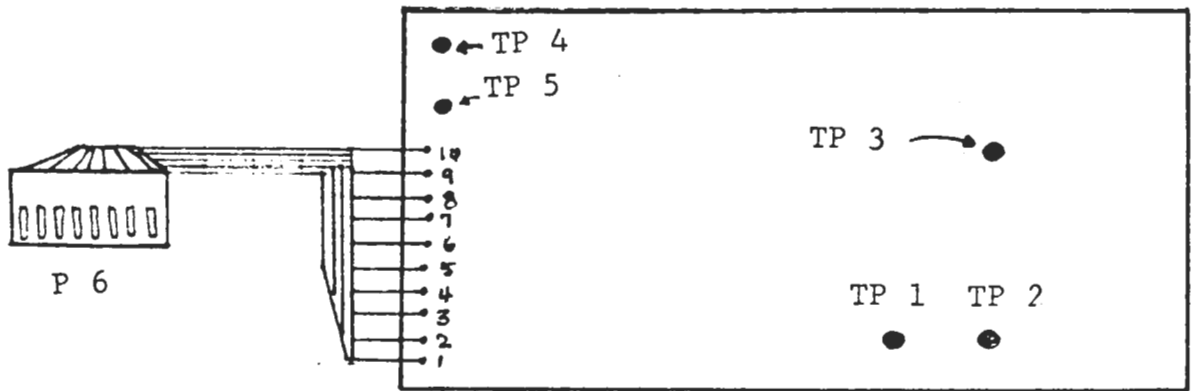
TYPE: WR 0 0 2 <CR>

SIMU: "Insert diskette and verify command"

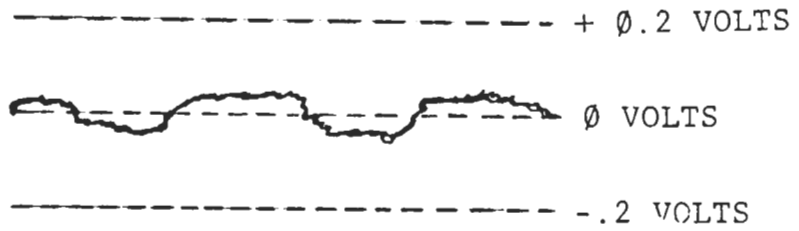
TYPE: Y <CR>

TYPE: HL 0 <CR>

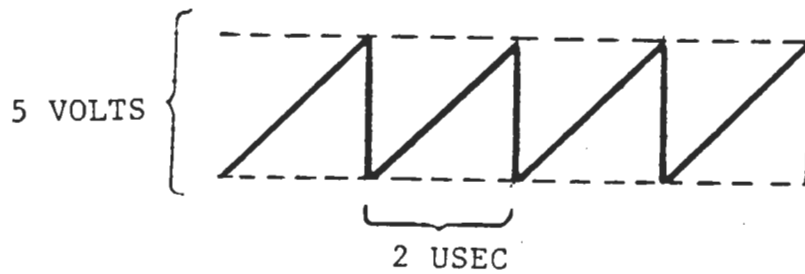
This will now have written a pattern of ones and zeroes to track 0 and loaded the head on unit 0 for a read. Now connect channel one of the scope to TP 1 and invert channel 2 and connect it to TP 2 on the Phase Locked Oscillator PCB. The scope should be in the add mode and with the inputs to the scope removed should be centered at zero reference. The scope inputs should be switched on again, should be at .2 V/division, DC coupled and the time base set at about 20 msec/division. You should see basically a DC level centered about zero reference with small fluctuations above and below 0 reference. Adjust R13 on PLO PCB if necessary to change this DC level. Also check TP 3 on this board, it should be a 500 KHz sawtooth waveform and relatively stable, tracking with disk speed variations.



PHASE LOCKED DOUBLE DATA SEPARATOR



9. Phase Locked Loop DC Bias



9. 500 KHz Sawtooth [TP 3]

Whenever a pattern of data is written to the disk, a series of clocks are also written to the disk. It is between these clocks that we see the data. In the case of FM recording, a one is represented by the presence of a pulse between the clock pulses and a zero is represented by no pulse between these clock pulses.

WRITE ALL ONES

```
TYPE: WR 0 0 1 <CR>
SIMU: "Insert disk ... "
TYPE: Y <CR>
TYPE: HL 0 <CR>
```

WRITE ALL ZEROES

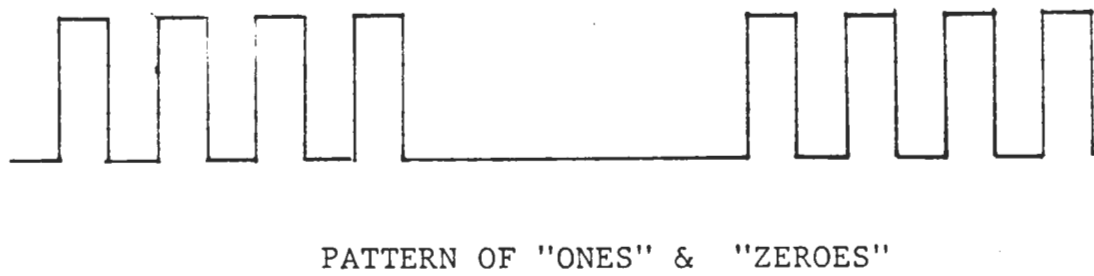
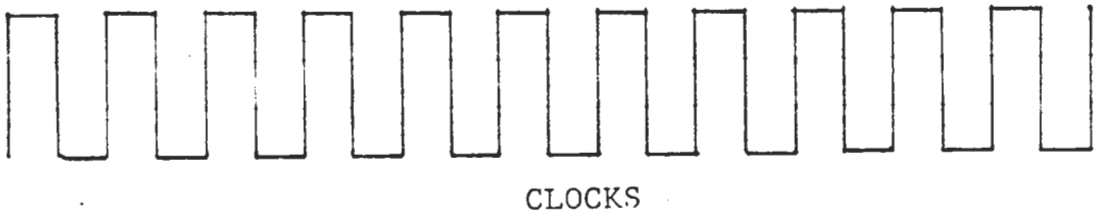
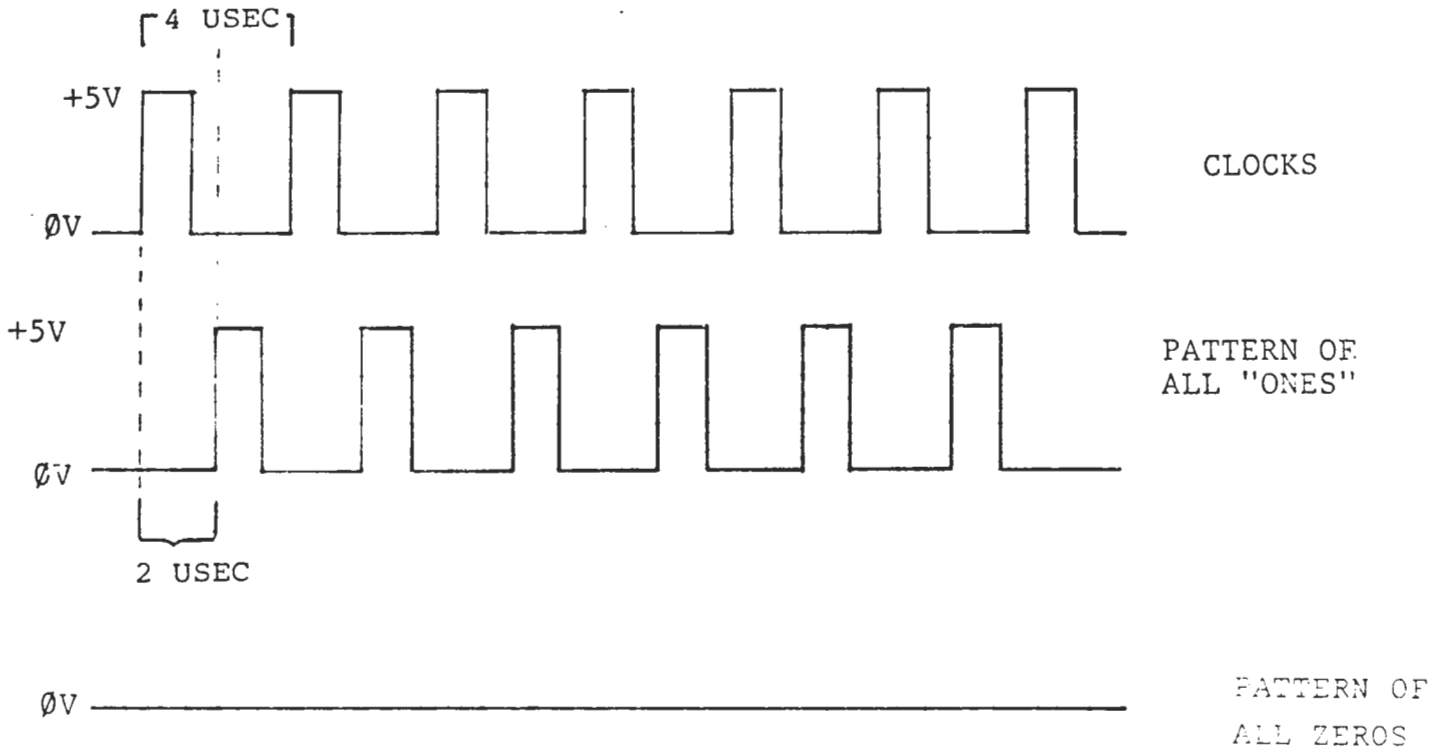
```
TYPE: WR 0 0 0 <CR>
SIMU: "Insert disk ... "
TYPE: Y <CR>
TYPE: HL 0 <CR>
```

With scope on alternate sweep, connect probes to TP 4 and TP 5 of PLL Data Separator PCB. Sync on TP 4 (clock). Time base should be .5 usec/div, and 2 volts/division. Write a pattern of all ones using the commands above. The data should be a positive pulse following 2.0 usec after each clock pulse. Write a pattern of all zeroes as in the above command and note the absence of data pulses in between the clocks.

NOTE

Since the hardware of the controller must write a header before writing the data block of all zeroes or ones their will appear "ghost" ones during the all zeroes data and some flickering of ones when all ones are written.

This is the end of part one of the alignment procedure, all the steps following this pertain to Heads, Cones or Index Sensor alignment. Symptoms of problems concerned in this part are Write/Read errors or problems of drive incompatibility.



PLL TP4 & 5

THE FOLLOWING STEPS ARE MADE WITH THE SCOPE CONNECTED ACROSS C21, TP 4 AND TP 5 OF THE DATA & INTERFACE PCB. SCOPE SHOULD BE IN ADD MODE WITH CHANNEL B INVERTED AND SHOULD BE AC COUPLED, .2 VOLTS/DIVISION AND SYNC SHOULD BE ON INDEX, P1 PIN 20.

11. RESOLUTION SIDE 0:

TYPE: WR 0 0 2 <CR>

SIMU: "Insert a diskette and verify command"

TYPE: Y <CR>

TYPE: HL 0 <CR>

Sync scope on P1 pin 20 of the Data and Interface PCB. Insert a blank diskette in unit 0 and write a pattern of ones and zeroes with command above. The scope is presently connected across the outputs of the head on unit 0 and should display a pattern as illustrated. At track 0 there should be at least 10% difference between the two frequencies.

TYPE: WR 76 0 2 <CR>

SIMU: "Insert disk and verify command"

TYPE: Y <CR>

TYPE: HL 0 <CR>

This will write a pattern of ones and zeroes on track 76. On this track there should be a minimum of 50% difference between the two frequencies.

12. HEAD CONTACT SIDE 0:

TYPE: SE 0 76 <CR>

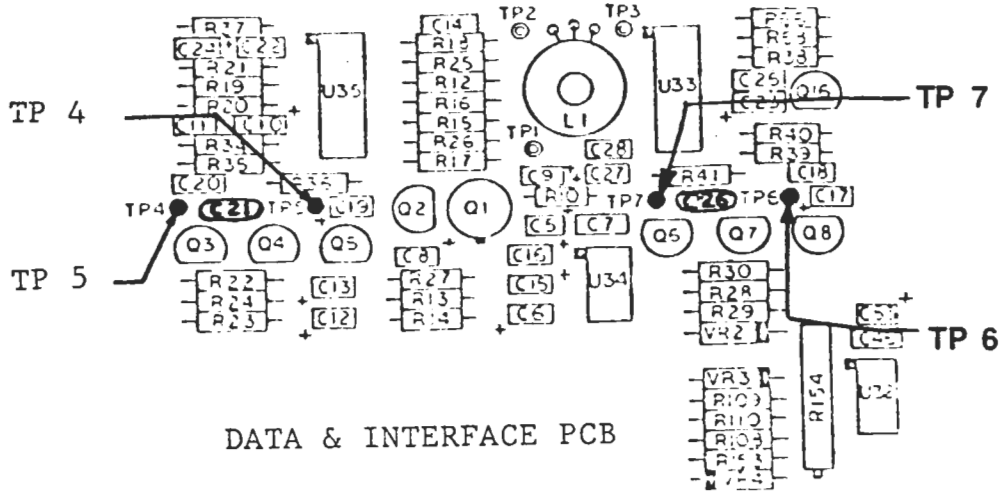
SIMU: "Automatic or manual?"

TYPE: M <CR>

SIMU: "Unit?"

TYPE: 0 <CR>

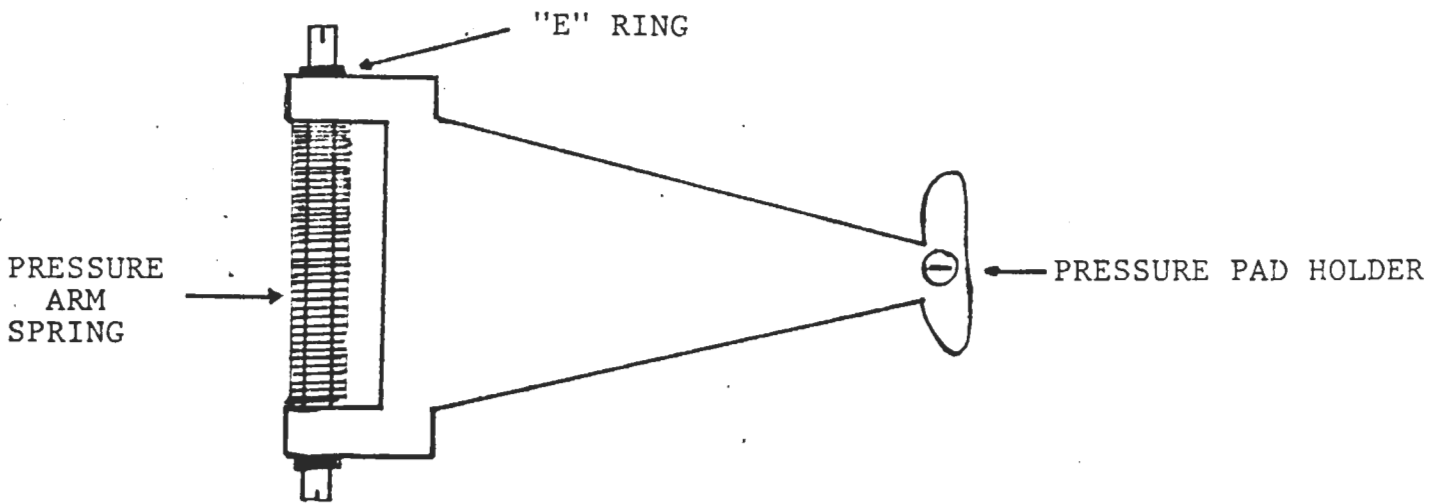
With the diskette used in the previous step and the same scope configuration, observe the waveform. Place finger on pressure pad arm and apply slight pressure. Signal should decrease or remain the same. If the signal increases, rotate pressure pad until there is no increase in signal or replace pressure pad as necessary. This check is to be made at tracks 0 and 76.



DATA & INTERFACE PCB



II. Resolution



Pressure Pad Arm

PerSci has used two different style pressure pads. One style is a fine rabbit hair, the other is a red synthetic material. Both appear to have good durability.

13. HEAD LOAD SIDE 0:

TYPE: RE <CR>

TYPE: HL 0 <CR>

With the scope in the same configuration as the past 2 steps, use the "T" key on the keyboard to toggle the head from its' loaded to unloaded position. Ensure the head lifts off the media. If the head does not lift off the media, loosen the two #2 allen screws on underside of the head load solenoid arm and adjust. After making this adjustment, check at tracks 0 and 76 to be sure head load is even over entire range.

14. CONE SIDE 0:

TYPE: RE <CR>

TYPE: HL 0 <CR>

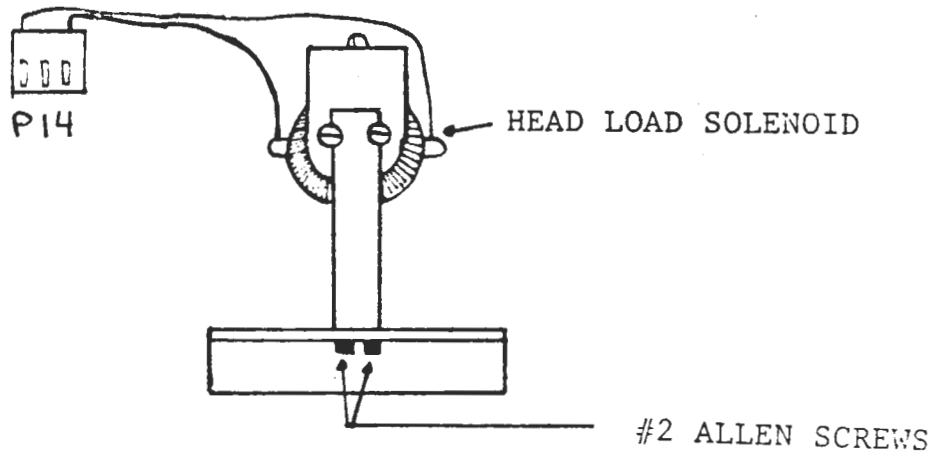
This check is to ensure cone is seating properly. With the scope still in the same previous configuration observe amplitudes of ones and zeroes previously written on the diskette. Remove and re-install the diskette several times, each time noting the amplitudes. If there is any change in amplitude of the signal, replace the cone. Also note to be sure cone is not sticking inside spindle and releasing with a loud snap.

NOTE

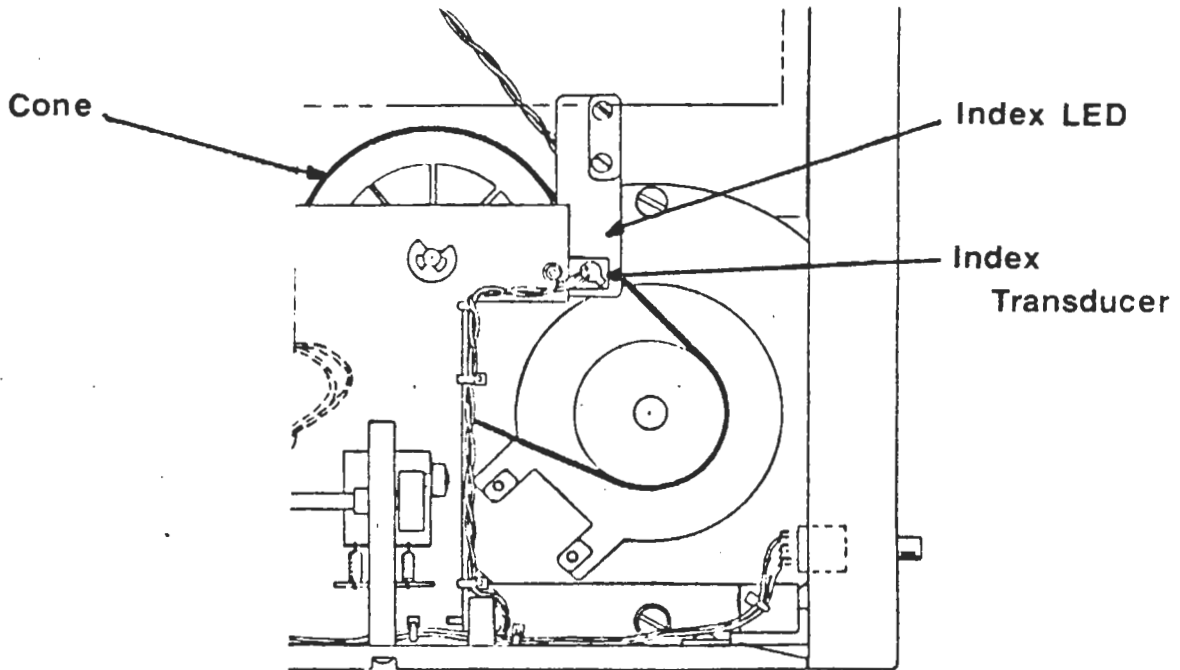
To replace cone, manually trip diskette presense switch to bring cone into spindle. Remove E ring from spindle shaft and press eject switch. Cone should now be free to remove with spring. Reverse the procedure to re-install new cone.

15. INDEX SIDE 0:

- a) The first part of this step is to align the index phototransistor with the light source that drives it (they are both both infrared). The index phototransistor on side 0 is located near the cone on the door and is mounted by a #2 Allen screw. The transmitter section is mounted to the drive chassis with two slotted screws. When the two are in perfect alignment, maximum saturation is achieved and the steepest response curve is possible. Since the index and sector pulses are critical, the faster we can trigger the following op amps the more precise is the timing.



13. Head Load ø



15. Index ø

Place scope probe on P 11 pin 2 on the D & I PCB and trigger on that channel (2 volts/division). Insert diskette and note waveform. For every sector and index mark there should be an excursion towards zero volts. Maximum saturation occurs when this excursion is at 0 volts (or allowing for one diode drop, .3-.6 V). If this does not happen, an adjustment must be made by loosening the two slotted screws on the emitter and the Allen screw of the receiver. Manual loading of the door makes this easier. As the door closes, the scope should change from +5V to 0V. Adjust as necessary.

```
TYPE: RE <CR>
TYPE: SE 1 <CR>
TYPE: HL 0 <CR>
```

- b) This part of the procedure aligns the index sensor to a data burst written on the alignment diskette. Re-connect scope probes across TP 4 and TP 5 as in steps before, in the add mode with channel B inverted and trigger should be on negative edge of P1 pin 20 (50 usec/division).

Insert Dysan alignment diskette and trigger to see waveform as illustrated. Data burst should occur 200 usec after trigger, plus or minus 20 usec. If it does not occur, loosen Allen screw on receiver portion and align to spec. If index cannot be brought into spec, repeat step a and try this adjustment again. Eject and re-insert diskette several times to be sure the adjustment remains correct.

CAUTION

Do not over torque the Allen screw as this could cause the plastic housing to crack.

16. AZIMUTH SIDE 0:

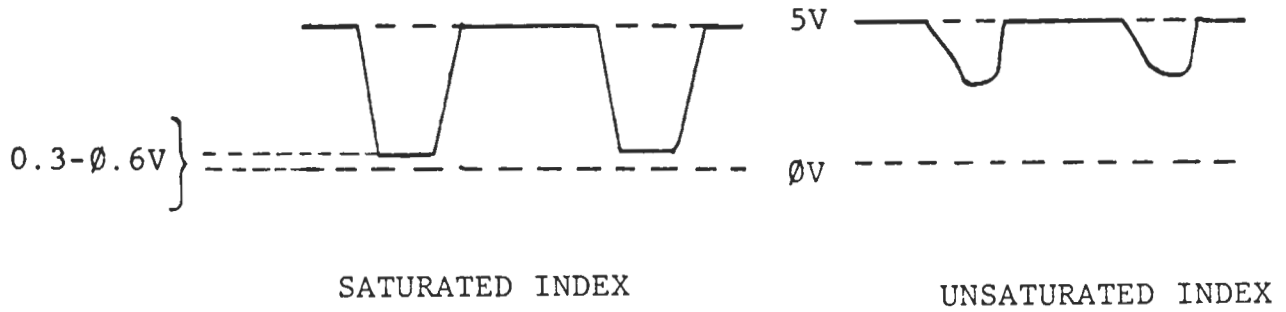
This adjustment checks the index data burst of the previous step on track 1 and track 76. Ideally, i.e., when azimuth is perfect, there should be no difference between these data burst. They should both occur at 200 usec after index and should be no more than 20 usec different from each other. (IF AN ADJUSTMENT IS MADE HERE, SIDE ONE MUST BE ADJUSTED ALSO SINCE IT'S THE SLAVE TO SIDE ZERO.)

```
TYPE: SE 1 76 <CR>
SIMU: "Automatic or manual?"
```

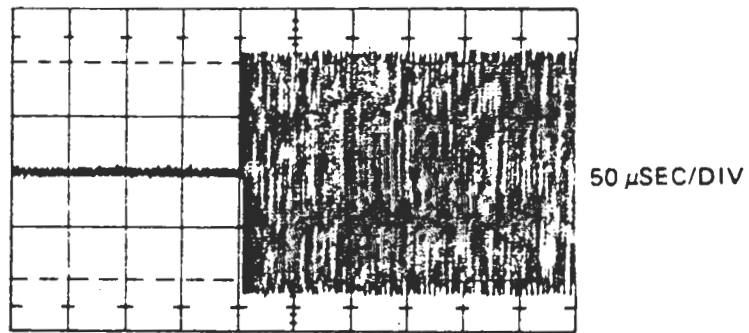
```
TYPE: M <CR>
SIMU: "Unit?"
```

```
TYPE: 0 <CR>
```

With the scope in the same configuration as last step, insert align diskette and note waveform. It should be 200 usec after index. Now toggle the "M" key to make the head move to track 76. If there is a difference, make the following adjustment:



15. Index ϕ



Index Pulse and Data Burst

Index & Azimuth [Units I & ϕ]

- 1) Loosen two Allen screws holding brace to servo (large black cylinder at rear of drive)
- 2) Loosen two Allen screws holding positioner servo to chassis.
- 3) With a screwdriver, gently pry up on the bottom of the servo mounting assembly (directly behind the diskette eject motor) where it meets the chassis.
- 4) Seek between tracks 1 and 76 and move servo up or down as necessary to bring into spec.
- 5) Tighten screws and check to be sure azimuth is correct after tightening.

17. CATSEYE SIDE 0:

This adjustment is needed to enable all drives to be able to read information written on all other drives. For this reason track 38 of the alignment disk (track 38 is nearly the center of the diskette) has a pattern referred to as a catseye (see diagram). (IF AN ADJUSTMENT IS MADE HERE, SIDE 1 CATSEYE MUST ALSO BE ADJUSTED SINCE IT IS THE SLAVE TO SIDE 0.)

```
TYPE: RE    <CR>
TYPE: SE 38  <CR>
TYPE: HL 0   <CR>
```

The scope is in the same configuration but this time is now 20 msec./division to allow a display of one entire track. The head should be on track 38 and loaded. Scope now shows the catseye pattern and both eyes should have the same amplitude. The maximum allowable difference is 10% which represents 1/2 mil off track. Ideally, this difference will be 0%. The following steps should be performed if the catseye is out of spec:

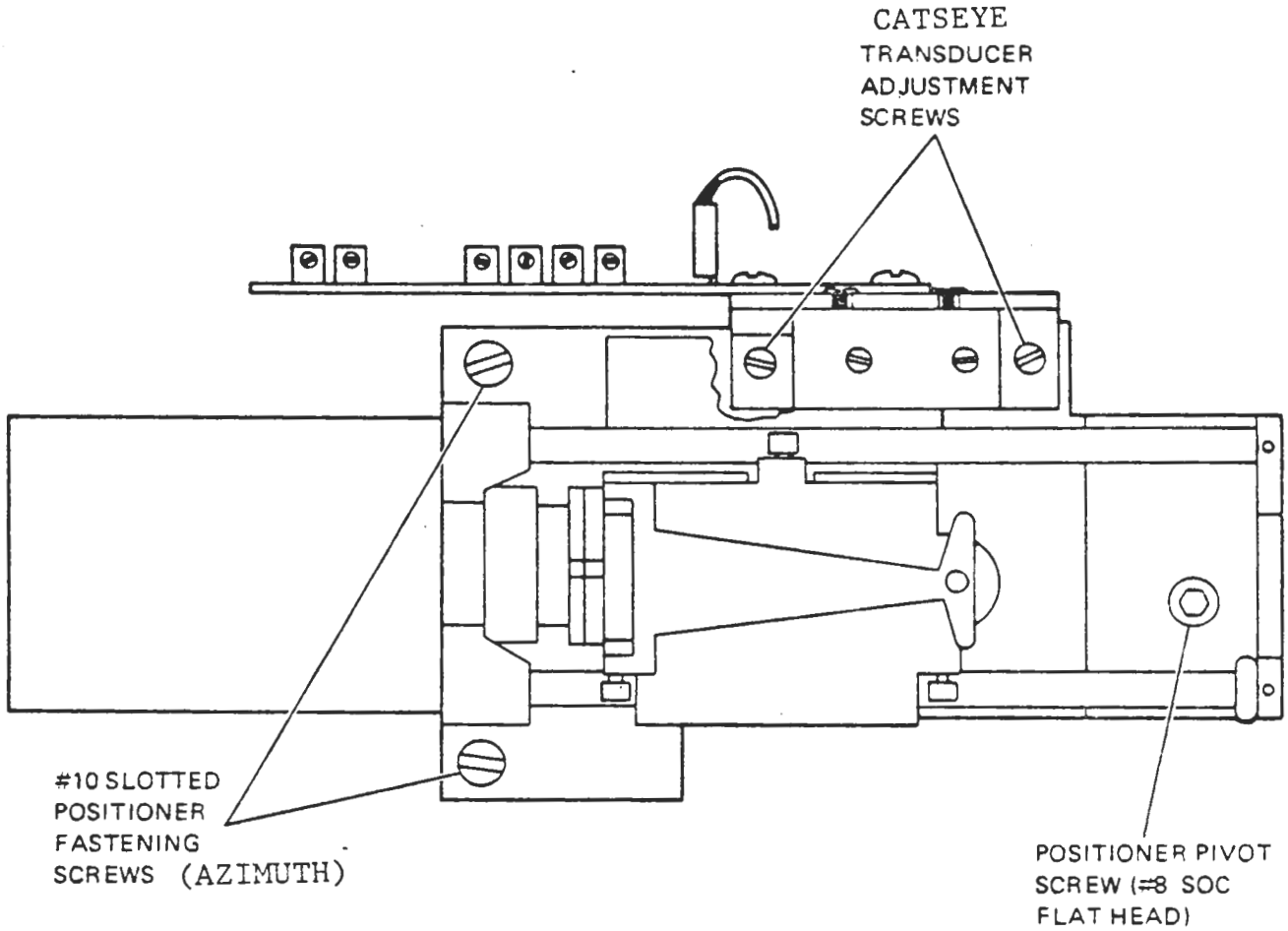
- 1) Remove black scale cover and restore drive to track 0.
- 2) Loosen two Allen screws mounting the black lamp housing to the chassis (on older models these may be slotted screws).

CAUTION

Be sure shrink tubing is installed on Allen wrench or screwdriver to prevent shorting to chassis.

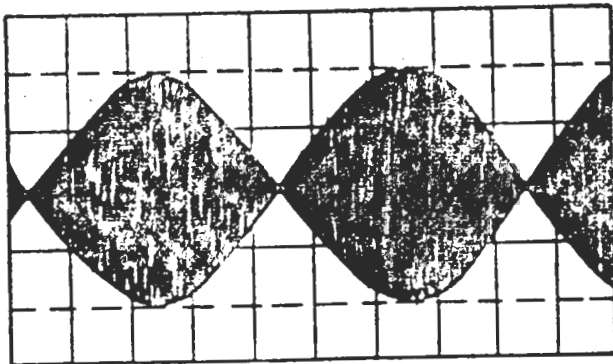
- 3) Seek to track 38 and load the head on side 0.
- 4) Tap the Lamp Amp PCB in the appropriate direction (toward front increases left catseye, towards rear increases right catseye).
- 5) Tighten Allen screws (be sure to recheck the catseye after tightening as this tends to change change the catseye alignment).

With a little effort, the catseye adjustment can be made close to perfect.



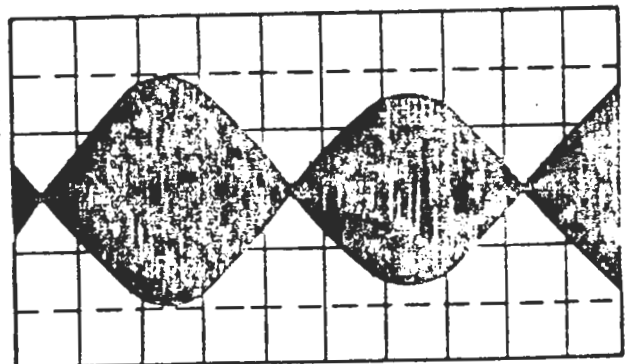
Positioner Track and Azimuth Adjustment (Side 0)

STEPS 16 and 17



EVEN AMPLITUDE 100% ON TRACK

20
MSEC
PER
DIV.



80% AMPLITUDE 1 MIL OFF TRACK

CATSEYE Track Alignment

THE FOLLOWING ADJUSTMENTS WILL BE MADE WITH THE SCOPE PROBES ACROSS C26, TP 6 AND TP 7 ON THE DATA & INTERFACE PCB. CHANNEL B SHOULD BE INVERTED, SYNC SHOULD BE ON NEGATIVE EDGE OF INDEX (P 1, PIN 20) AND 0.2 VOLTS/DIVISION.

18. RESOLUTION SIDE 1:

<u>TRACK 0</u>	<u>TRACK 76</u>
TYPE: WR 0 1 2 <CR>	TYPE: WR 76 1 2 <CR>
SIMU: "Insert disk ... "	SIMU: "Insert disk ... "
TYPE: Y <CR>	TYPE: Y <CR>
TYPE: HL 1 <CR>	TYPE: HL 1 <CR>

Repeat step 11 with blank diskette inserted in unit 1 and use the commands written above.

19. HEAD CONTACT SIDE 1:

Problems most often seen if this is out of adjustment is "Write Retry" during a diskcopy, bad diskcopy or unable to complete a diskcopy.

Using the same commands as step 18, use the "T" key load and unload the heads. On this side, when the head is unloaded, the signal should disappear. Step between tracks 0 and 76 loading and unloading the heads. Side 1 has an adjustment for head penetration, the #2 Allen screw in the center of the plastic arm the head is mounted in. With head unloaded, adjust screw until signal disappears. Repeat for track 76. Check to make sure when head is loaded, signal returns. Also check condition of pressure pad. Caution is advised with this adjustment as too much head penetration can cause extreme problems with diskette wear.

20. HEAD LOAD SIDE 1:

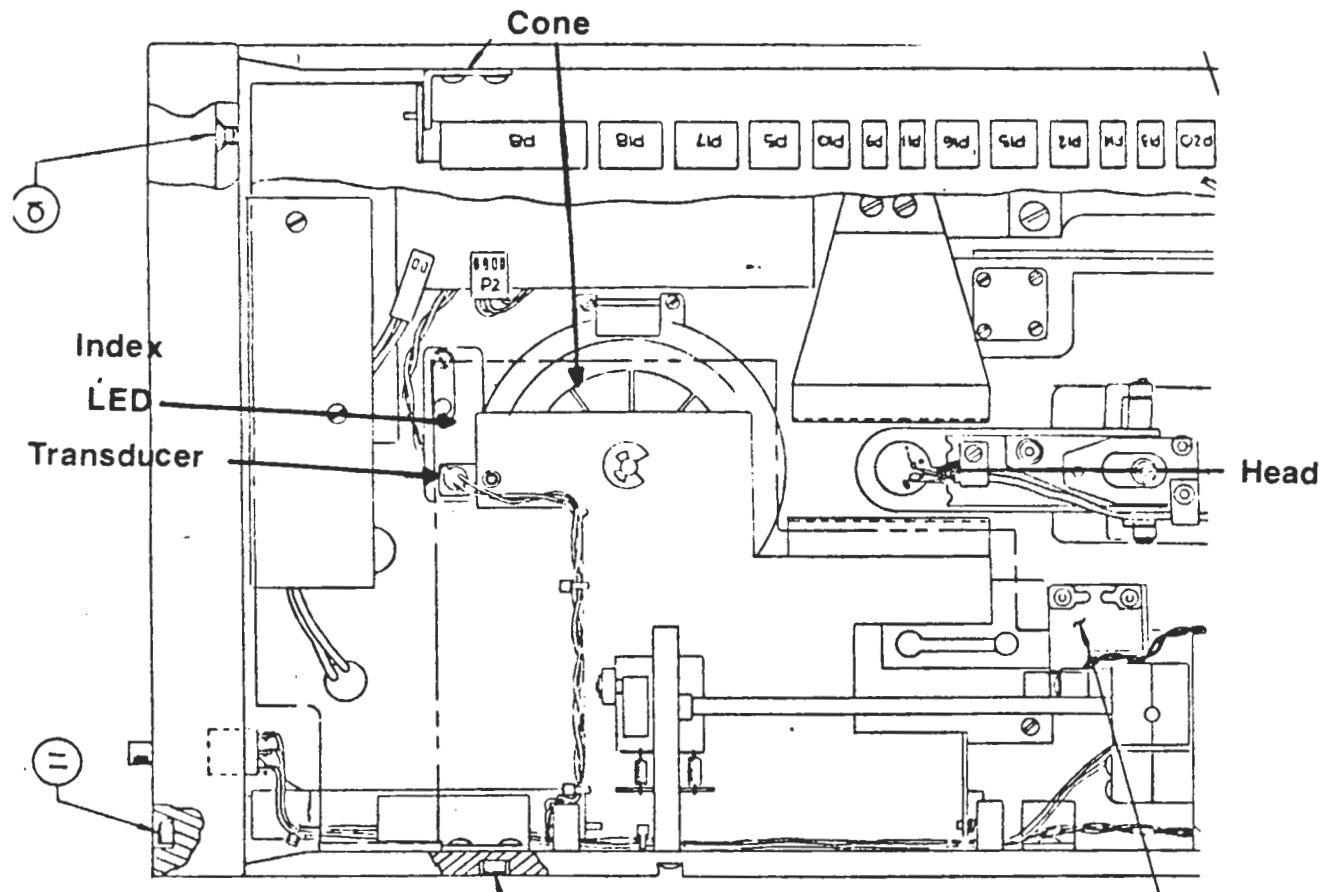
TYPE: HL 1 <CR>

This is the same as step 13 except the adjustment, if necessary, is different. Manually trip the diskette presense sensor and using the "T" key, toggle the head of unit 1. When the head is loaded, the pressure pad should be in direct contact with the head. When the head is unloaded, the pressure pad should lift away from the head. If not, it is necessary to sharpen the bend in the paddle that lifts the pad.

21. CONE SIDE 1:

TYPE: RE <CR>
TYPE: HL 1 <CR>

Repeat the procedure in step 14 for side 1 using the above command.



Unit I Assembly

22. INDEX SIDE 1: 9 EPT 4 - 45

- a) Repeat the procedure for side 0 (step 15) to adjust saturation of the index photo-transistor on side 1. However, move scope probe to P9 pin 2 to see the index pulse for side 1.
- b) Repeat the procedure for index data burst alignment using the alignment diskette (and moving probes back to TP 6 and TP 7 (C26)) that was used in step 15, part b.

23. AZIMUTH SIDE 1:

TYPE: RE <CR>

TYPE: SE 1 76 <CR>

SIMU: "Automatic or manual?"

TYPE: M <CR>

SIMU: "Unit?"

TYPE: 1 <CR>

With scope in same configuration, insert alignment diskette and repeat the procedure for step 15. If data burst is more than 20 usec difference, an adjustment is necessary. There are two Allen screws (older models have slotted screws) which mount the whole head assembly to the positioner servo. Loosen both of these screws until they are just short of being snug. This will allow the head to pivot up and down. Using the "M" key seek between track 1 and 76, pivoting the head as necessary to bring azimuth into spec. Retighten screws and re-check azimuth.

24. CATSEYE SIDE 1

TYPE: RE <CR>

TYPE: SE 38 <CR>

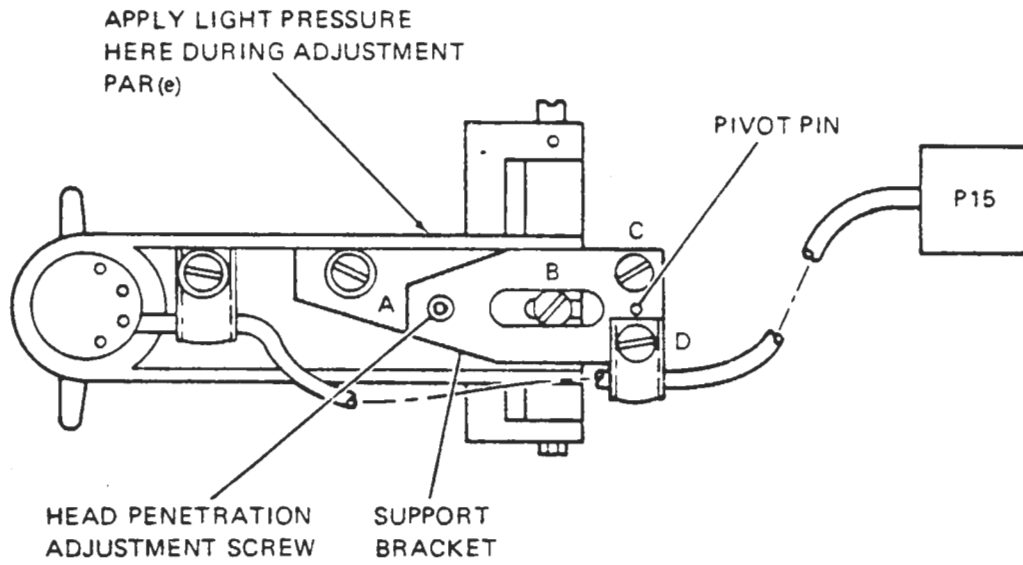
TYPE: HL 1 <CR>

With the scope probes in the same set-up as the previous step, insert alignment diskette. Head should be loaded and at track 38. If catseye is out of spec, i.e., more than 10% difference between the eyes, an adjustment is necessary. To adjust the catseye loosen the two Allen screws (older models have slotted screws) in the center of the head arm which will allow the head to move horizontally and front to back. When catseye is in alignment, tighten screws and re-check the catseye.

NOTE

The catseye, azimuth and head penetration on unit 1 are all inter-dependent adjustment. If an adjustment is made to any one of these three, the other two should be checked. Likewise, after this last catseye adjustment, it is advisable to return to the azimuth adjustment and check it. Repeat as necessary.

HEAD ASSEMBLY [unit I]



A and B → Catseye

C and D → Azimuth

Steps 23 - 24

Drive Assembly Jacks and Plugs

PCB	CONNECTOR	FUNCTION
Data and Interface PCB	P1	Customer signal interface
	J3	Power
	J4	Power distribution to spindle servo
	J5	Spindle servo interface
	J6	Data separator interface
	J7	Power distribution to positioner servo
	J8	Positioner servo interface
	J9	Index - sector phototransistor, Side 1
	J10	Index - sector LED power, Side 1
	J11	Index - sector phototransistor, Side \emptyset
	J12	Index - sector LED power, Side \emptyset
	J13	Head load mechanism, Side 1
	J14	Head load mechanism, Side \emptyset
	J15	Read/Write head, Side 1
	J16	Read/Write head, Side \emptyset
	J17	Eject assembly, Side 1
	J18	Eject assembly, Side \emptyset
	Positioner Servo PCB	P7
P8		Interface with data and interface PCB
J8		Drive to voice coil motor
Spindle Servo PCB	J5	Interface to lamp amplifier PCB
	P4	Power
	P5	Signal interface with data and interface PCB
	J1	Drive to spindle motor
Lamp Amplifier PCB	J2	Interface with photosense module
	P5	Interface with positioner servo PCB
Data Separator PCB	J13	Interface with optical transducer
	P6	Interface with data and interface PCB

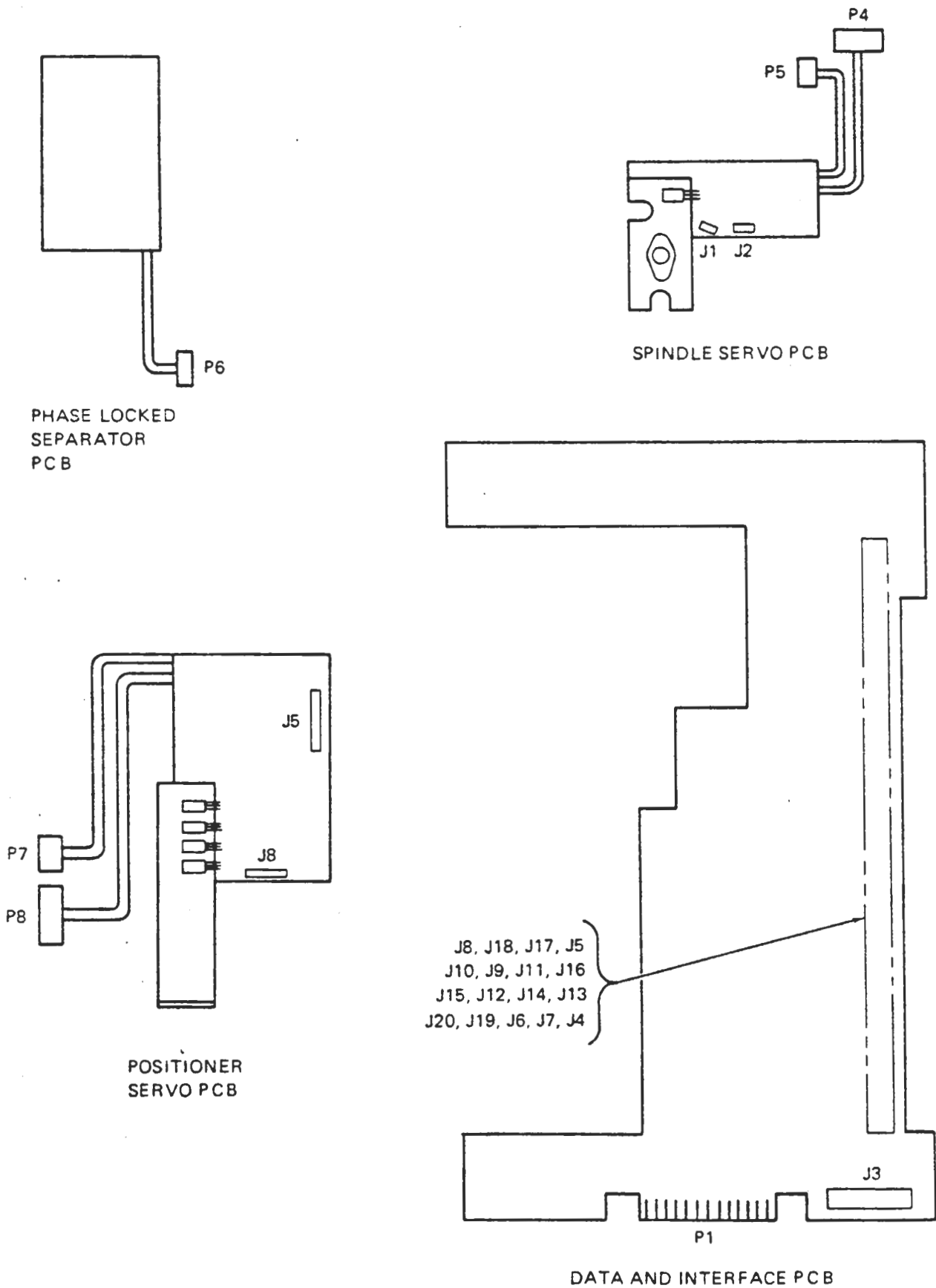


Figure 2-1. Plugs and Jacks Identification

Electromechanical Adjustments

CONTENTS

SECTION 6, MAINTENANCE

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6.3	DRIVE TROUBLESHOOTING AND DIAGNOSTICS (By Assembly)	
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6.3.2	Drive Belt Tension	
6.3.3	Read/Write System Checks	
6.3.4	Read/Write Visual Examination	
6.3.5	Read/Write Data Amplitude	
6.4	CHECKS, ADJUSTMENTS, AND REPLACEMENTS (By Assembly)	
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6.4.2	Plugs and Jacks	
6.4.3	Data and Interface PCB	
6.4.4	Drive System	
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6.4.12	Read/Write Head Penetration	

6.0

"Section 6. Maintenance" is divided as follows:

"6.3 Drive Troubleshooting and Diagnostics"

This and following subsections are printed on pink paper as a reminder that they are to be performed only by authorized service personnel. (See the warning above.) When a problem has been traced to a cause within an identified assembly of the drive, using the procedures in this section, the authorized service technician should then refer to Section 6.4, "Maintenance Procedures" which follows.

"6.4 Maintenance Procedures (By Assembly)"

The procedures in the 6.4 section are grouped by major functional assemblies of the drive. Each assembly subsection in Section 6.4 is organized by three phases: first a check to verify the diagnosis of the problem. Second, an adjustment, which if it fails to correct the problem, is followed by a replacement procedure.

Helios II

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6.3 DRIVE TROUBLESHOOTING AND DIAGNOSTICS (By Assembly)

6.3.1 SPINDLE DRIVE SYSTEM (Refer to Fig. 6-5, Drive System)

- a. Remove the drive belt and engage both cones by manually depressing Side \emptyset and Side 1 load switches. With both cones engaged, the drive belt removed and no media present, the hub assembly should rotate virtually frictionless. If friction is detected then either the hub or cone bearings are worn. The problem can be isolated by rotating the hub separately, then engaging the cones separately.
- b. Rotate drive motor shaft and check for uniformity of torque (due to brushes). A non-uniform rotational torque may be due to worn bearings or motor armature interference.

6.3.2 DRIVE BELT TENSION

- a. Drive belt tension is measured by applying a side force to the belt at the center of span and measuring the deflection. Place a scale at the center of span normal to the belt. Apply a 1-lb. force to the belt using a cantilever type force gage and measure the resultant belt deflection. Belt tension is correct when the deflection is $\pm .05$ inches.

6.3.3 READ/WRITE SYSTEM CHECKS

- a. Diskette operation, in read mode on prerecorded data track. Alternately trigger solenoid load and unload. Sync on solenoid trigger and observe data output differentially across read head output. Interpret settling time when data track output width has approximately normalized (10% of steady state amplitude).
- b. Head settling time must be no greater than 40 msec.
- c. If the proper reading cannot be obtained, the possible problem areas are:
 1. Solenoid improperly adjusted. When properly adjusted, the energized solenoid should drop the head load arm $.025 \pm .015$ inches.
 2. Defective solenoid.
 3. Improper head/media penetration. The head must protrude into the plane of the media as defined by the "reference boss" by $.008 \pm .005$ inches. This distance is not adjustable on side \emptyset .

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6.3.4 READ/WRITE VISUAL EXAMINATION

- a. With power off examine the read/write head surface for scratches, excessive wear and dirt, oil or oxide deposits. Head must have a clean smooth surface. If the examination reveals any defects, take appropriate corrective action.
 1. If dirty, clean according to the procedure at 6.1.6, Cleaning Read/Write Heads.
 2. If head appears to have defective surfaces, and the read/write data amplitude check fails, replace read/write head assembly.

6.3.5 READ/WRITE DATA AMPLITUDE

- a. Diskette operational, drive ready.
- b. Using a new diskette (approved brand), write all one's pattern at track 00 and 76. Observe read data output differentially across read head output.
- c. All one's at track 76 must be at least 3 mv p-p.
- d. If the proper reading cannot be obtained, the possible problem areas are:
 1. Defective write drivers.
 2. Defective media. Repeat test with a different diskette to isolate problem.
 3. Defective read/write head.

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6.4 CHECKS, ADJUSTMENTS, AND REPLACEMENTS (By Assembly)

6.4.1 TOOLS AND TEST EQUIPMENT

The following material is required to perform the maintenance procedures:

1. Common hand tools
2. Flashlight
3. Inspection mirror
4. Cotton-tipped swabs (Q-Tips)
5. 95% Isopropyl alcohol
6. 6-inch steel scale, 1/10ths
7. 0-1 oz. or 0-30 gm. force gage
8. 1-lb. force gage
9. Alignment diskette - Dysan 240 or equivalent
10. Oscilloscope, differential type
11. Drive exerciser - PerSci Model 475

NOTE

The cognizant maintenance personnel should read the entire check, adjustment or replacement procedure prior to performing the routine.

6.4.2 PLUGS AND JACKS

The interconnecting plugs and jacks are listed in Table 6-1 and identified in Figure 6-4. The connector pins should be checked for cleanliness and total contact if intermittent problems are encountered.

6.4.3 DATA AND INTERFACE PCB

The data and interface PCB contains the customer's I/O connector, power input connector. Various subassemblies connect into it.

1. PCB Replacement

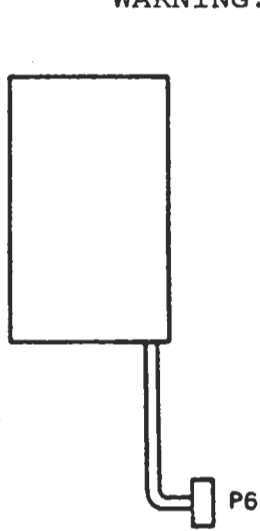
- a. Disconnect all the connectors along the upper board edge.
- b. Remove two screws holding the lower board edges to the drive frame.
- c. Remove four screws holding the PCB pivot brackets to the drive frame.
- d. Install replacement PCB by reverse procedure.
- e. Alignment of replacement PCB to lower mounting points is achieved by slackening four screws holding pivot bar to PCB.

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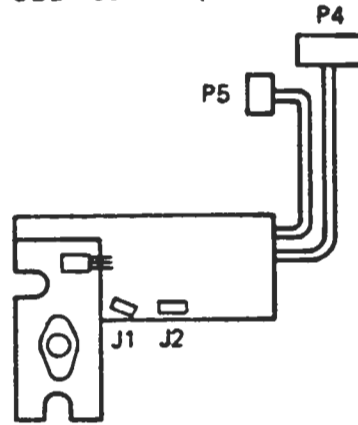
Table 6-1 Drive Assembly Jacks and Plugs

PCB	CONNECTOR	FUNCTION
Data and Interface PCB	P1	Customer signal interface
	J3	Power
	J4	Power distribution to spindle servo
	J5	Spindle servo interface
	J6	Data separator interface
	J7	Power distribution to positioner servo
	J8	Positioner servo interface
	J9	Index - sector phototransistor, Side 1
	J10	Index - sector LED power, Side 1
	J11	Index - sector phototransistor, Side \emptyset
	J12	Index - sector LED power, Side \emptyset
	J13	Head load mechanism, Side 1
	J14	Head load mechanism, Side \emptyset
	J15	Read/Write head, Side 1
	J16	Read/Write head, Side \emptyset
	J17	Eject assembly, Side 1
	J18	Eject assembly, Side \emptyset
	Positioner Servo PCB	P7
P8		Interface with data and interface PCB
J8		Drive to voice coil motor
J5		Interface to lamp amplifier PCB
Spindle Servo PCB	P4	Power
	P5	Signal interface with data and interface PCB
	J1	Drive to spindle motor
	J2	Interface with photosense module
Lamp Amplifier PCB	P5	Interface with positioner servo PCB
	J13	Interface with optical transducer
Data Separator PCB	P6	Interface with data and interface PCB

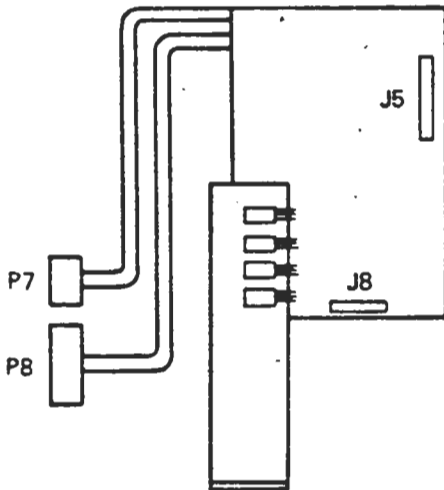
WARNING: THIS PAGE FOR AUTHORIZED USE ONLY (See Sec. 6.0)



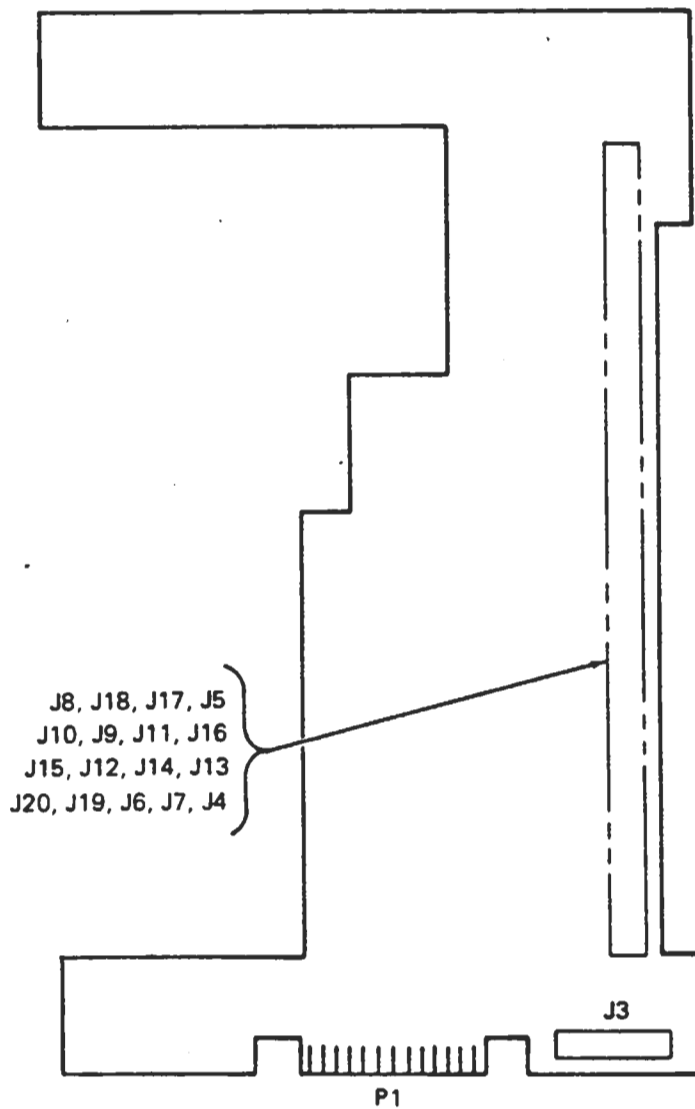
PHASE LOCKED SEPARATOR PCB



SPINDLE SERVO PCB



POSITIONER SERVO PCB



DATA AND INTERFACE PCB

Figure 6-4 Plugs and Jacks Identification

-12

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2. Voltage Adjustment

No adjustments are provided for voltage levels. If +24VDC, +5VDC or -5VDC are out of tolerance, check for internal loading by disconnecting diskette drive and checking levels at controller. If levels are correct, check out cable or isolate a defective component or assembly at the data and interface PCB. If necessary, replace the PCB.

6.4.4 DRIVE SYSTEM

The drive system comprises drive motor, belt, spindle sensor assembly, hub assembly and spindle servo electronics PCB. (Figure 6-5)

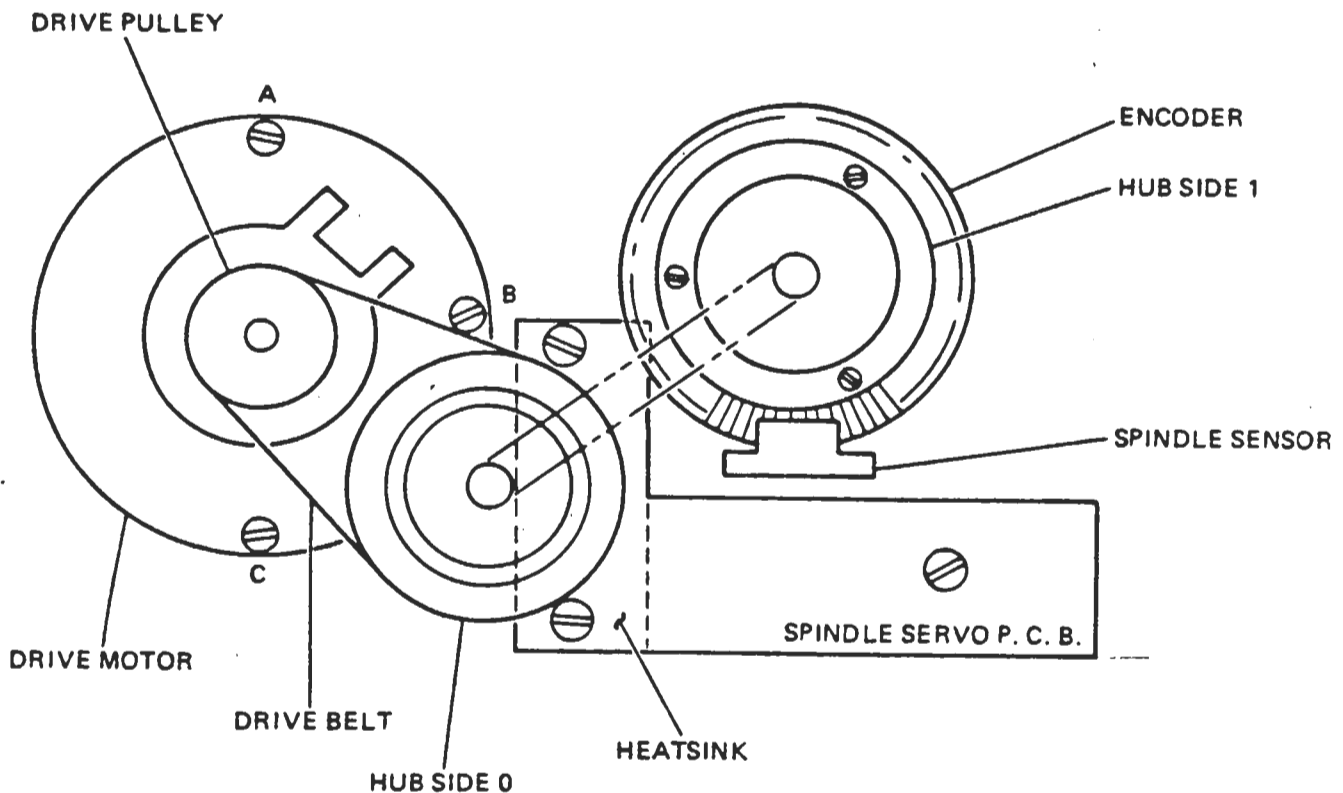


Figure 6-5 Drive System

1. Drive Motor and Belt Checks

- a. Set drive power off.
- b. Inspect drive belt for wear, particularly fraying of the edges.
- c. Manually rotate drive motor. If binding is evident, replace motor.

NOTE

There is always some resistance to rotation due to the brushes.

- d. Verify belt tension.
- e. Verify drive belt tracks in center of both drive and driven pulleys; retrack belt if necessary.

2. Drive Belt Tracking Adjustment

- a. Remove diskettes from drive.
- b. Set drive power off.
- c. Rotate spindle drive motor clockwise by pressing finger against the face of the drive pulley.
- d. Observe if drive belt tracks high or low.
- e. If the drive belt tracks too high, it will scruff the underside of the LED assembly.
- f. If the drive belt tracks too low, place a shim washer (PerSci Part No. 200081-001) between the drive motor and deck plate under Screw A. (Figure 6-5)
- g. If the drive belt tracks too high, place shim washers (PerSci Part No. 200081-001) between the drive motor and deck plate under Screws B and C. (Figure 6-5), i.e., one washer at each point.
- h. After belt tracking, proceed with belt tension adjustment procedure.

3. Drive Belt Tension Adjustment

To adjust drive belt tension, proceed as follows:

- a. Set drive power off.
- b. Loosen three motor mounting screws. (Figure 6-5)
- c. Move motor away from hub assembly so as to tension belt.
- d. Tighten motor mounting screws and check belt tension.
- e. Belt tension is correct when the belt deflection at the center of span is $.25 \pm .05$ inches with a 1-lb. side force applied to the belt.

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- f. If a force gage is not available, the belt tension should be minimum consistent with the spindle motor stalling when the hub is braked. This may be done by inserting a diskette in Side 1 and holding the hub on Side \emptyset .

4. Drive Belt Replacement

- a. Set drive power off.
- b. Slide drive belt from drive motor pulley.
- c. Clean motor and spindle pulley surfaces, wiping sparingly with alcohol.
- d. Install replacement belt.
- e. Check belt tension and belt tracking. If necessary, make adjustment. Normally, neither would be necessary.

5. Drive Motor Replacement

To replace drive motor, proceed as follows:

- a. Set drive power off.
- b. Remove drive belt.
- c. Swing out data and interface PCB.
- d. Remove drive motor connector P1 at spindle servo PCB. (Figure 6-4)
- e. Remove three screws holding drive motor to deck plate.

NOTE

There may be shim washers under the drive motor and these should be replaced under the replacement motor at the same points they originally occupied.

- f. Remove drive motor.

CAUTION

The drive motor pulley is an integral part of the drive motor assembly and should never be removed as this would result in loss of stator/rotor motor alignment.

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- g. Install replacement spindle motor assembly.
- h. Replace belt and adjust tension.
- i. Check belt tracking and adjust if necessary.

6. Spindle Sensor Assembly Replacement

The spindle sensor assembly is located on Side 1 of the deck plate (Figure 6-5) adjacent to the hub encoder disc. To replace, proceed as follows:

- a. Set drive power off.
- b. Swing out data and interface PCB.
- c. Remove plug P2 at the spindle servo PCB.
- d. Remove two screws holding spindle sensor assembly to deck plate.

CAUTION

There are two loose spacers between the spindle sensor assembly and deck.

- e. Install replacement spindle sensor assembly by reverse procedure.
 - f. Check that spindle sensor mask does not interfere with hub encoder by rotating hub.
 - g. If there is interference, remove assembly and check that the circuit board edges are flush with the corresponding plastic assemblies. If they are not, slacken two screws holding the assembly to the PCB. Align the edges before tightening screws.
- #### 7. Spindle Servo PCB Replacement
- a. Set drive power off.
 - b. Disconnect P4 and P5 at data and interface PCB.
 - c. Swing out data and interface PCB.
 - d. Disconnect P1 and P2 at spindle servo PCB.
 - e. Remove two flat head screws above the spindle servo heat-sink. (Figure 6-5)
 - f. Remove one screw adjacent to U4 on the spindle servo PCB.

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CAUTION

There is a loose spacer between the PCB and deck plate at this point.

- g. Remove spindle servo PCB and install replacement PCB.

NOTE

P4 and P5 terminate cables from the PCB which pass between the deck plate and a "U" shaped member mounted to the deck plate. Removal of this "U" shaped member is not necessary since the connector housings will pass through the opening. It is important that the cables pass through this opening; otherwise, they will interfere with diskette insertion.

8. Diskette Spindle Assembly Replacement

The drive spindle assembly consisting of two hubs, bearing housing, shaft, two bearings, encoder disk and clamp ring, is a replaceable assembly. (Figure 6-5) If any part of this assembly is damaged, the whole assembly has to be replaced and the faulty assembly repaired at the factory or depot equipped to do such repairs.

- a. Set drive power off.
- b. Remove spindle motor assembly.
- c. Remove LED assembly Side 0 and Side 1.
- d. Remove two size 4 cap screws fastening bearing housing to deck plate. Access to these screws is through two holes in the hub Side 1.
- e. Slide assembly out and install replacement assembly.
- f. Replace spindle motor, drive belt and LED assemblies, Side 0 and Side 1.
- g. Perform positioner track 38, and azimuth alignment procedure, 6.4.8, steps 7 and 8.
- h. Perform index Side 0 and Side 1 alignment procedure, 6.4.5, step 2.
- i. Perform belt tension and tracking procedure, 6.4.4, steps 2 and 3.

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6.4.5 INDEX TRANSDUCER AND LOGIC ASSEMBLY

1. Index Transducer and Logic Checks

The procedure for checking index transducer is the same for Side Ø as Side 1, only the test points used are different.

- a. Set drive power on.
- b. Insert Dysan alignment diskette 240 into Side Ø.
- c. Access track 76 and load head Side Ø.
- d. Monitor read data at R15 directly under Q1 on the data and interface board.
- e. Monitor index pulse at Pin 20 of P1 on the data and interface board.

```

PROG:          INDEX TRANSDUCER
SYNC:          INT CH 2 NEG
CH 1:          .5V/DIV A.C.
CH 2:          2V/DIV D.C.
MODE:          CH 1 50µSEC/DIV
  
```

- f. The start of the data burst should lag the negative-going edge of the index pulse by $200 \mu\text{sec} \pm 50 \mu\text{sec}$. (Figure 6-6)

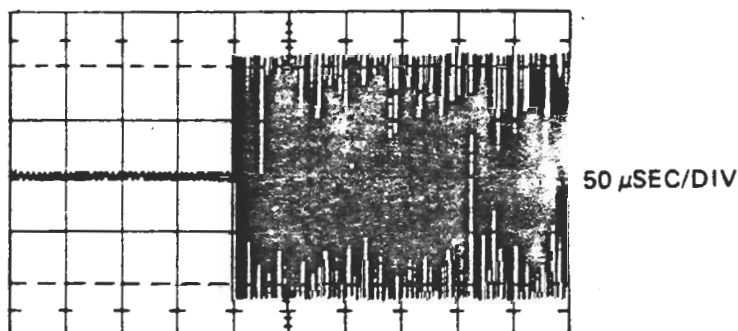


Figure 6-6 Index Pulse and Data Burst

```

PROG:          INDEX PERIOD
SYNC:          INT CH 2 NEG
CH 2:          2V/DIV D.C.
MODE:          CH 2 20SEC/DIV
  
```

- g. This is true for both track 76 and track 1. Any difference in reading between these two tracks is due to positioner azimuth and the procedure for positioner azimuth should be performed first (6.4.8, steps 7 and 8).
- h. Variations in reading will occur with successive insertions of the diskette and an average reading should be taken. Excessive variations with diskette insertion, i.e., greater than $\pm 50 \mu\text{sec}$, indicate a media concentricity problem.

Helios II

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- i. The period should be 166.7 ± 3 msec if the diskette is rotating at the correct speed.
- j. To check index Side 1 load Dysan alignment diskette into Side 1. Leave scope probe Ch. 1 on R15 and sync off index pulse at Pin 8 of P1 on data and interface board.

2. Index Transducer Alignment

To align the index transducer sync off index pulse and monitor data burst on the Dysan alignment diskette 240 as described in the index transducer check procedure, step 1.

- a. Access track 1.
- b. Observe time interval between negative-going index pulse and data burst.
- c. Slacken No. 2 Allen cap screw securing photosense to carrier. (Figure 6-7)
- d. Adjust position of photosense until time interval is 200 ± 20 μ sec and tighten screw.
- e. Check with successive insertions of diskette that time interval remains 200 ± 50 μ sec.
- f. If this time interval cannot be achieved by adjustment of the photosense assembly, then proceed as follows:
 1. Position the photosense as close to the correct position without losing signal.
 2. Remove diskette.

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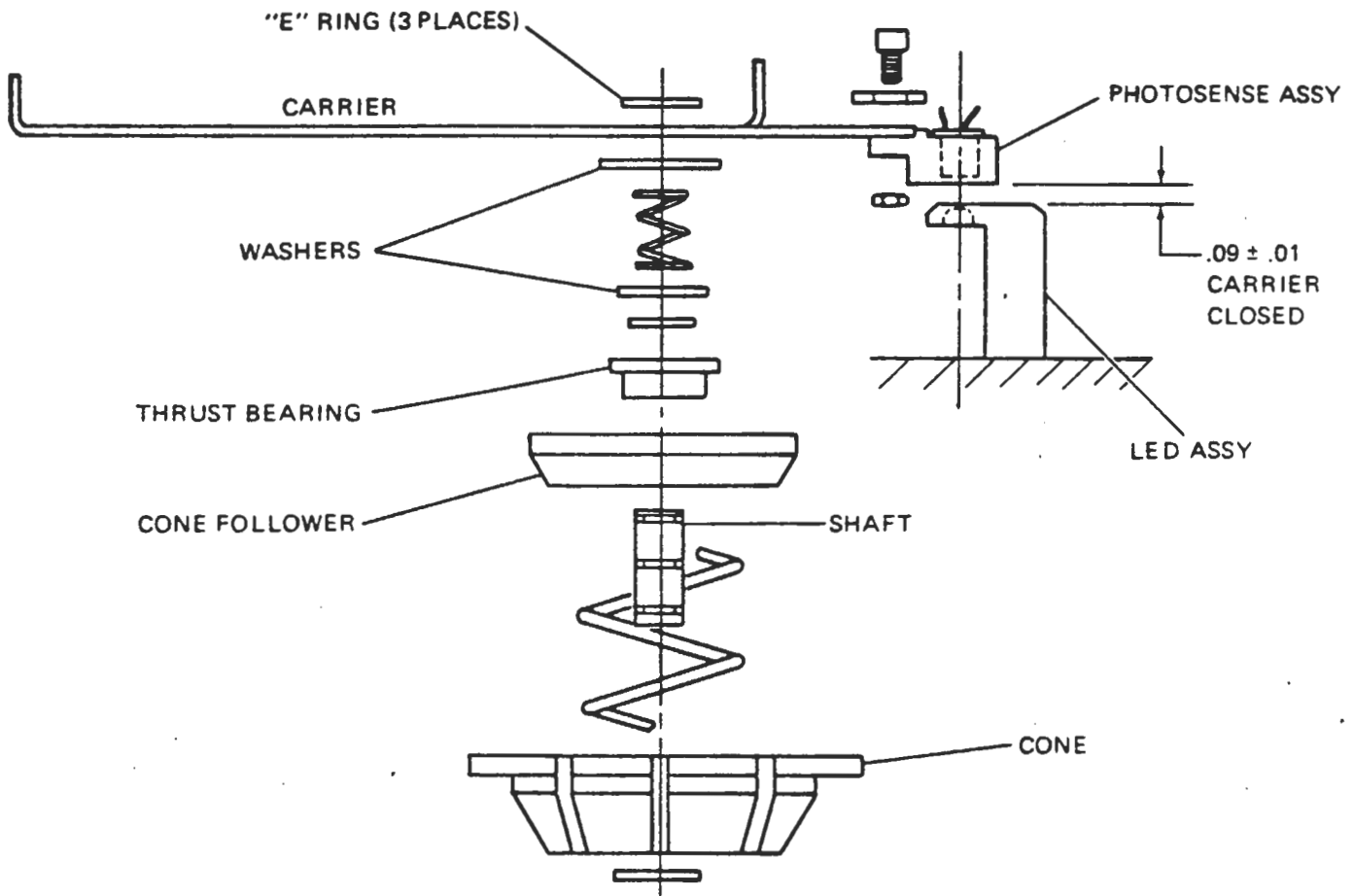


Figure 6-7 Index Transducer Alignment and Replacement

3. Manually load the cone by pressing the carrier in and observe the alignment between the photosense and LED.
4. Slacken two screws holding LED assembly to deck plate and reposition such that the photosense and LED are opposite each other.
5. Insert diskette and proceed with alignment by adjusting photosense only.
6. Repeat above until desired result is achieved.

3. Index Transducer Replacement

The index transducer consists of two elements - the photosense assembly and the LED assembly for both Side 0 and Side 1.

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To replace the photosense assembly proceed as follows:

- a. Set Diskette power off.
- b. Unsolder the black and white twisted lead at the photosense assembly observing lead polarity.
- c. Remove No. 2 Allen cap screw securing photosense assembly to carrier and install replacement assembly.
- d. Solder leads, observing same polarity as on the replaced assembly.
- e. Perform index alignment procedure.

To replace the LED assembly proceed as follows:

- a. Disconnect P12 (Side 0) or P10 (Side 1) at data and interface PCB.
- b. Remove cable clamp at deck plate Side 0 only.
- c. Remove two screws securing LED assembly to deck plate.
- d. Remove LED assembly and install replacement assembly.
- e. Perform index alignment procedure (6.4.5, step 2).

6.4.6 SPINDLE CONE REPLACEMENT

The cone assembly engages the media with the drive hub. The cone assemblies for Side 0 and Side 1 are the same and the replacement procedures are the same. To replace the cone or any other part within the assembly, proceed as follows:

- a. Set Diskette power on.
- b. Manually depress the load micro switch, thus engaging the cone with the hub.
- c. Remove E ring holding the cone assembly to the carrier. (Figure 6-7)
- d. Press the eject button, i. e., carrier in disengaged position.
- e. Remove cone assembly, compression spring and shim washer between the spring and carrier.
- f. Dismantle cone assembly by removing E ring next to the thrust bearing.
- g. Install replacement cone and assemble by reverse procedure.

6.4.7 READ/WRITE SYSTEM

The read/write head on Side 0 is mounted to the bearing carriage and is not replaceable as a unit. The complete positioner assembly must be replaced if determined to be defective. The read/write head on Side 1 is replaceable as an assembly which includes the plastic member to which it is secured. Head load assemblies actuate a spring loaded arm which applies pressure to the media causing it to contact the read/write head.

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1. Head Load Check and Adjustment (Side Ø)

To check and adjust head loading (Side Ø), proceed as follows:

- a. Set Diskette power on.
- b. Load carrier by manually depressing load micro switch.
- c. Toggle the head load switch and observe that the head load solenoid is energized and de-energized.
- d. The total displacement of the solenoid lifter paddle should be $.09 \pm .02$ inches at the point where it contacts the pressure arm. (Figure 6-8)
- e. If solenoid paddle displacement is incorrect, adjust the tang to the rear of the solenoid adjacent to the return spring.
- f. The pressure arm should lift off the head $.025 \pm .015$ inches with the solenoid de-energized. This dimension should be checked with the head positioned at track Ø and track 76.
- g. If the pressure arm displacement is incorrect, slacken two Allen cap screws holding the paddle to the solenoid arm and adjust position. Check for correct displacement over entire stroke of positioner. Complete procedure in Paragraph e before making this adjustment.
- h. Toggle head several times with head at track Ø and track 76 to observe correct working.

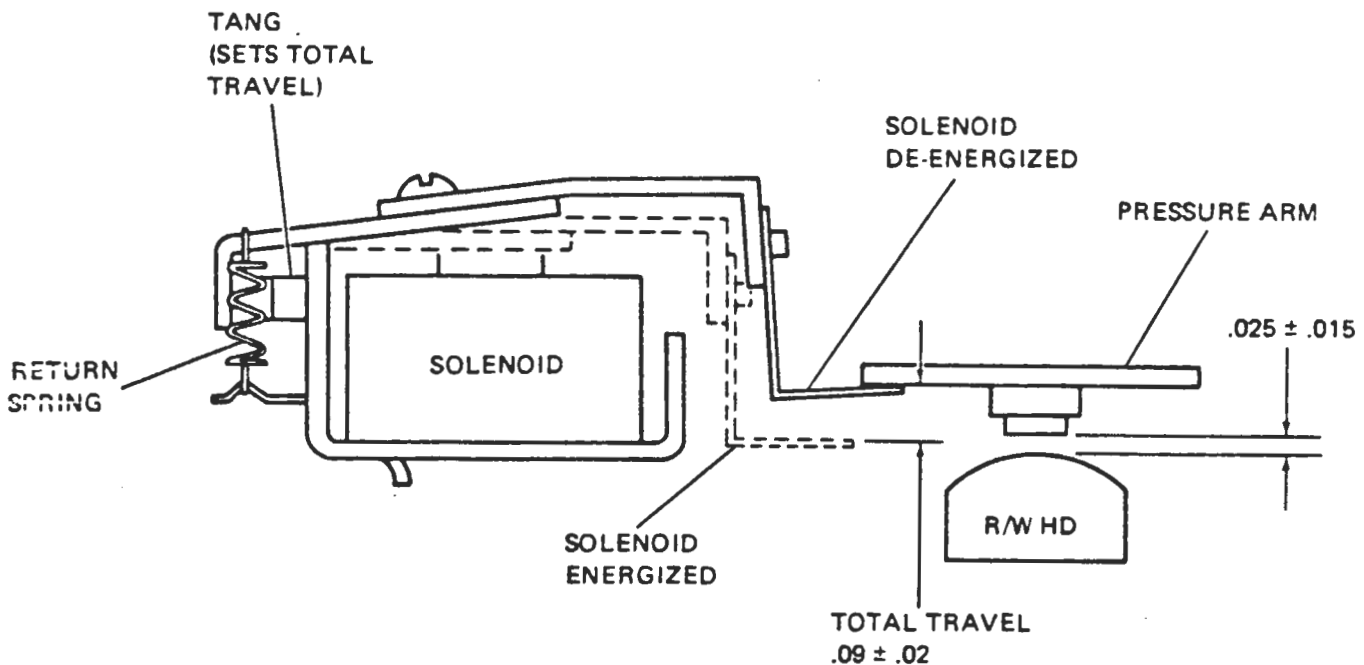


Figure 6-8 Head Load Check and Adjustment (Side Ø)

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2. Head Load Check and Adjustment (Side 1)

To check and adjust head loading (Side 1), proceed as follows:

- a. Swing out data and interface PCB.
- b. Set Diskette power on.
- c. Load carrier by manually depressing load micro switch.
- d. Toggle the head load switch and observe that the head load solenoid is energized and de-energized.
- e. The total displacement of the solenoid lifter paddle should be $.09 \pm .02$ inches at the point where it contacts the pressure arm.
- f. If solenoid paddle displacement is incorrect adjust the tang adjacent to the solenoid return spring. (Figure 6-9)
- g. The pressure arm should lift off the head $.025 \pm .015$ inches with the solenoid de-energized. This dimension should be checked with the head positioned at track 0 and track 76.
- h. If the pressure arm displacement is incorrect bend the paddle at the Z bend next to the solenoid clapper. Complete procedure in Paragraph f before making this adjustment.
- i. Toggle head several times with head at track 0 and track 76 to observe correct working.

3. Head Load Solenoid Replacement (Side 0)

- a. Set Diskette power off.
- b. Disconnect P14 at data and interface PCB.

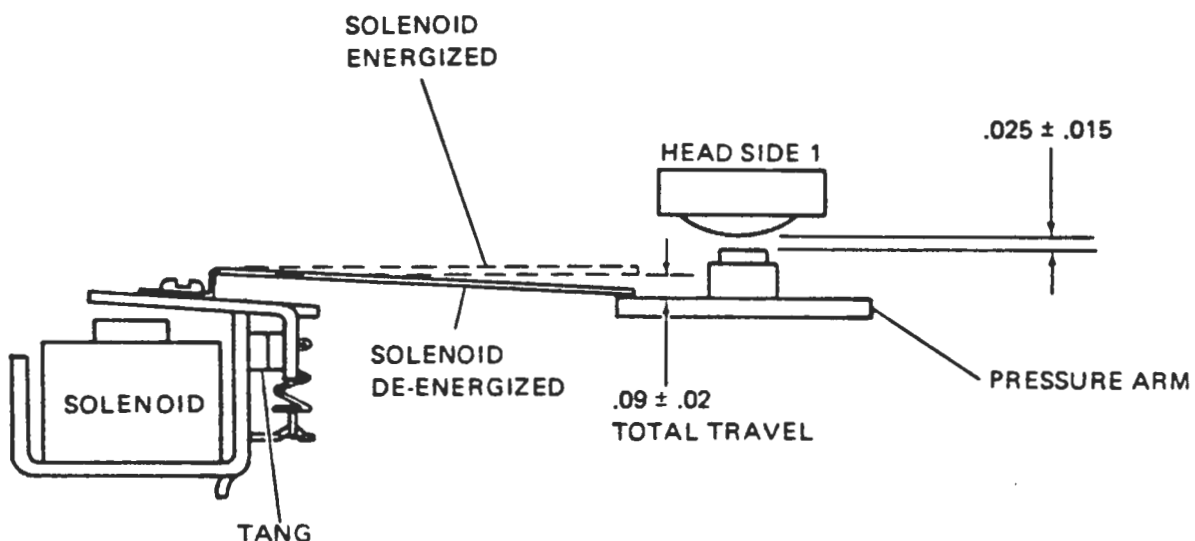


Figure 6-9 Head Load Check and Adjustment (Side 1)

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- c. Remove two No. 8 screws holding solenoid assembly to deck plate.
- d. Install replacement solenoid assembly.
- e. Proceed with head load adjustment procedure.

4. Head Load Solenoid Replacement (Side 1)

- a. Set drive power off.
- b. Remove head load solenoid assembly Side Ø.
- c. Disconnect P13 at data and interface PCB.
- d. Remove two No. 4 screws securing head load solenoid assembly to deck plate.
- e. Install replacement assembly.
- f. Replace head load solenoid assembly Side Ø.
- g. Proceed with head load adjustment procedure Side 1 (step 2 above).

6.4.8. POSITIONING SYSTEM

The positioner servo comprises a voice coil actuator, optical transducers, head carriage assembly and the electronics required to control the system. Positioner circuits are located on the "lamp amplifier PCB", "positioner servo PCB" and "data and interface PCB".

1. Positioner Servo Check

- a. Using the oscilloscope, observe the positioner transducer output, obtained at the end of C1 on the positioner servo PCB nearest the potentiometer mounted on that board. (C1 is a 0.022µf mylar capacitor near the point the cable leaves the PCB.) The oscilloscope may be conveniently grounded at the end of the power resistors, R77 and R78, farthest from the heatsink. The oscilloscope should be floating except for this ground; as ground loops in the sensitive servo area can cause problems. Synchronize the oscilloscope to "seek complete", available at an exerciser test point or at P1-10 on the data and interface PCB.
- b. After connecting the oscilloscope, alternately seek between track ØØ and track 76, using the diskette drive exerciser in SL mode. Verify that each seek requires less than 100 ms, that the positioner transducer output is 3V p-p ± .03V and that the positioner transducer signal is balanced within ±100 mv about ground. Observe at 0.5V per division on the oscilloscope.
- c. Step sequentially from track to track with the Diskette exerciser, using step mode. Verify that the positioner settles within 0.5 divisions within 10 ms, and that there are no overshoots greater than 0.5 divisions. (Observe at 0.5V per division.)
- d. Seek in crescendo mode, automatic, with the exerciser for at least two cycles to verify settling to each track from a high speed seek.

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2. Positioner Track and Azimuth Alignment Check, Side 0

- a. Set Diskette power on.
- b. Load Dysan alignment diskette 240 into Side 0.
- c. Access track 38 and load head Side 0.
- d. Monitor read data.

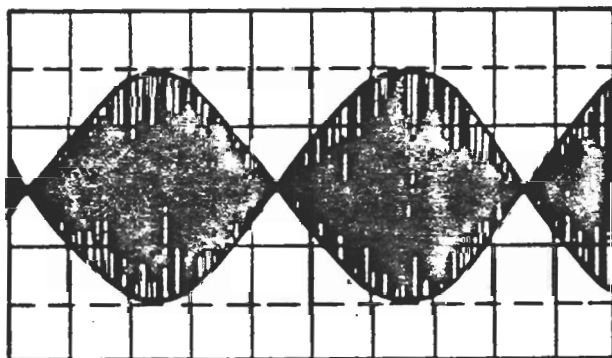
PROG:	TRACK ALIGNMENT SIDE 0
SYNC:	EXT INDEX PULSE NEG. (PIN 20)
CH 1:	50 mV/DIV A. C.
CH 2:	50 mV/DIV A. C. INVERTED
MODE:	ADD CH 1 & CH 2 20 mSEC/DIV

SCOPE PROBES CH 1 & CH 2 ACROSS C19 ON DATA AND INTERFACE PCB.

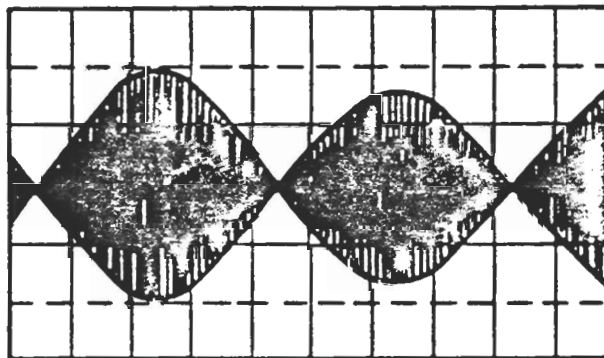
- e. If track alignment is perfect the amplitudes of the cat's eye pattern will be equal. A 20% amplitude difference represents a one mil position error. (Figure 6-6)
- f. Access track 76 and load head Side 0 still using alignment diskette.

PROG:	AZIMUTH ALIGNMENT SIDE 0
SYNC:	INT CH 2 NEG
CH 1:	.5V/DIV A. C.
CH 2:	2V/DIV D. C.
MODE:	CH 1 50 uSEC/DIV

- g. Observe time interval between sync and data burst. (Figure 6-6)
- h. Access track 1 and observe any change in this time interval.



EVEN AMPLITUDE 100% ON TRACK



80% AMPLITUDE 1 MIL OFF TRACK

Figure 6-10 Track Alignment

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1. If positioner azimuth is correct the time interval should be the same within 20 μ sec.

3. Positioner Track and Azimuth Alignment Check, Side 1

- a. Before track alignment and azimuth on Side 1 can be checked it must be verified that track alignment and azimuth on Side 0 is correct, since adjustment on Side 0 interact with Side 1. This is not true vice versa.
- b. Set drive power on.
- c. Insert Dysan alignment diskette 240 into Side 1.
- d. Access track 38 and load head Side 1.
- e. Monitor read data.

```

PROG:          TRACK ALIGNMENT SIDE 1
SYNC:          EXT INDEX PULSE NEG (PIN 8)
CH 1:          50 mV/DIV A. C.
CH 2:          50 mV/DIV A. C. INVERTED
MODE:          ADD CH 1 & CH 2 20 mSEC/DIV
  
```

SCOPE PROBES CH 1 & CH 2 ACROSS C23 ON DATA & INTERFACE PCB.

- f. If track alignment is perfect the amplitudes of the cat's eye pattern will be equal. A 20% amplitude difference represents a one mil position error. (Figure 6-10)
- g. Access track 76 and load head Side 1 still using alignment diskette scope.

```

PROG:          AZIMUTH ALIGNMENT SIDE 1
SYNC:          INT CH 2 NEG
CH 1:          .5V/DIV A. C.
CH 2:          2V/DIV D. C.
MODE:          CH 1 50  $\mu$ SEC/DIV
  
```

- h. Observe time interval between sync and data burst. (Figure 6-6)
- i. Access track 1 and observe any change in this time interval.
- j. If head azimuth is correct the time interval should be the same within 20 μ sec.

4. Positioner Servo Adjustment

If the positioner servo did not pass the check of the preceding section, alignment might be required.

5. Preliminary Adjustments

The positioner servo adjustments are located on the lamp amplifier PCB. (Figure 6-11)

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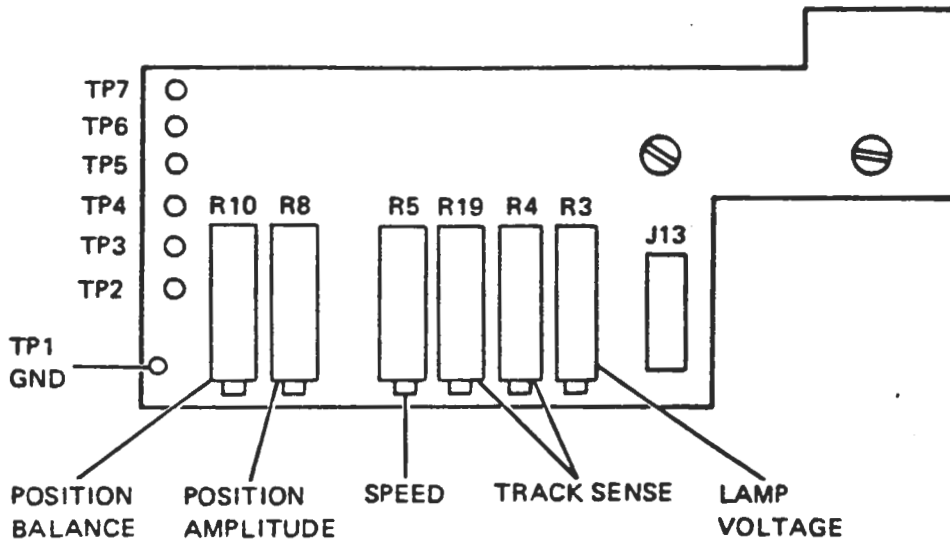


Figure 6-11 Lamp Amplifier PCB

Disconnect the voice coil motor by pulling P8 from J8 at the positioner servo PCB. Make preliminary adjustments according to Table 6-2.

Table 6-2. Positioner Servo Adjustments

FUNCTION	CONTROL	TEST POINT	ADJUSTMENT
Lamp Voltage	R3	TP7	+1.50V ± 0.1V
Track Sense Balance	R19	TP6	+0.15V track 20 (Move carriage by hand to approximate locations.)
Track Sense	R4	TP6	To -1.25V track 76 (Move carriage by hand to approximate locations.)
Speed	R5	TP5	Negative level, changing 1.25V as positioner moved from inner to outer limit.
Position Amplitude	R8	TP2	Adjust for 3.0V p-p balanced about ground, as positioner moved back and forth by hand.
Position Balance	R10		
Oscilloscope Ground		TP1	(Oscilloscope should be floating to avoid ground loops.)

6-27

6. Final Adjustments
 - a. The adjustments of the preceding sections should be sufficient for operation, but for attaining specified performance levels track sense and speed should be adjusted dynamically. Also forward and reverse speed is balanced by adjusting R33 on the positioner servo PCB.
 - b. Plug P8 from the voice coil motor into J8 on the positioner servo PCB. Restore the positioner with the exerciser. Observe TP6 with the oscilloscope and set to -0.60V. using R4. Seek track 1. The output should be more positive than 0V. Seek track 64. The output should be more negative than -1V.
 - c. Move the oscilloscope probe to the end of C1 nearest R33. and oscilloscope ground to the end of R77 or R78 furthest from the heatsink, on the positioner servo board. Alternately seek from track 60 to track 1. Synchronize the oscilloscope to the negative edge of the "seek complete" signal found at a test point on the positioner or at P1-10 on the data and interface PCB. Adjust R33 for test symmetry between forward and reverse seeks. Alternate seeks between track 00 and track 76, keeping oscilloscope functions as they were, except for time. Adjust R5 on the lamp amplifier PCB such that the time for the longer seek (forward or reverse) to settle within 0.25V of ground is 95ms. This completes the adjustment of the positioner servo.
7. Positioner Track and Azimuth Adjustment Side 0
 - a. Set drive power off.
 - b. Slacken two screws securing transducer assembly to positioner frame, just sufficiently to allow the assembly to slide within the range of the adjustment slots. (Figure 6-1)
 - c. Set drive power on.
 - d. Insert Dysan alignment diskette into Side 0 and load head Side 0.
 - e. Access track 38 and monitor read data per Paragraph d of check procedure.
 - f. Gently tap the positioner transducer PCB to effect a small displacement of this assembly and observe the change in amplitude of the cat's eye pattern.
 - g. When the amplitudes are approximately equal proceed with azimuth alignment leaving the transducer housing screws "semi-tight".
 - h. Still using alignment diskette, access track 76.
 - i. Monitor read data on scope per Paragraph f of check procedure.
 - j. Observe time interval between sync and data burst. (Figure 6-6)
 - k. Access track 1 and observe if there is any change in the time interval.
 - l. If there is a difference in time greater than $\pm 20 \mu\text{sec}$, slacken two No. 10 slotted screws holding positioner frame to deck plate. (Figure 6-1)

- m. Pivot assembly until the time interval is the same at track 1 as track 76 and tighten two screws.
- n. Repeat track 38 alignment procedure and tighten two screws holding transducer housing when cat's eye pattern is within 10% amplitude.

8. Positioner Tract and Azimuth Adjustment Side 1

- a. Set drive power on.
- b. Insert Dysan alignment diskette 240 into Side 1.
- c. Access track 38 and load head Side 1.
- d. Observe data across C23 on data and interface PCB.
- e. Slacken screws A & B (Figure 6-12) holding head Side 1 carriage to support bracket.
- f. Slide carriage assembly radially while keeping the inside carriage surface against the bracket edge.
- g. Observe cat's eye pattern on scope and lightly tighten screws when pattern is approximately equal. (Figure 6-10)

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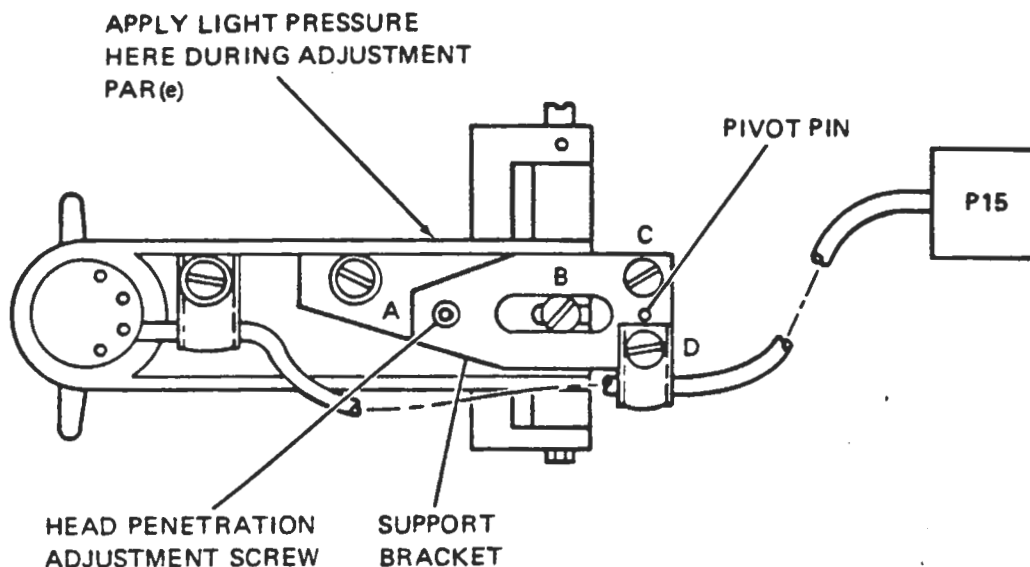


Figure 6-12 Positioner Track and Azimuth Adjustment (Side 1)

- h. Slacken screws C and D and pivot assembly about pivot point.
- i. Lightly tighten screws at point of maximum read back amplitude.
- j. Access track 1 still using Dysan alignment diskette. Monitor read data per Paragraph g of check procedure.
- k. Observe time interval between sync and data burst. (Figure 6-6)
- l. Access track 76 and observe any change in the time interval.
- m. Pivot carriage assembly until the time interval with the head positioned at track 76 is approximately the same as with the head positioned at track 1.

NOTE

There is interaction and this process will have to be repeated several times before proper azimuth is achieved.

- n. When the time intervals are within 20 μ sec, tighten two screws C and D. (Figure 6-12)
- o. Access track 38 and repeat track alignment procedure.
- p. Tighten screws A and B when amplitudes are equal within 10%.

CAUTION

Do not apply excessive torque to these screws.

9. Positioner Assembly Replacement

- a. Disconnect P15 and P16 at data and interface board.
- b. Disconnect P8 and P5 at positioner servo board.
- c. Remove three cable clamps securing leads to deck plate.
- d. Remove two No. 10 slotted screws and one No. 8 Allen flat head screw securing positioner assembly to deck plate and remove positioner assembly. (Figure 6-1)
- e. Install replacement positioner assembly. Tighten flat head screw before tightening two No. 10 slotted screws. Make sure pressure pad lifter arm is above the carrier lifter surface on Side \emptyset before securing positioner assembly.
- f. Align positioner assembly per alignment procedure.

6.4.9 EJECT MOTOR CAM ASSEMBLY

1. Eject Motor Cam Alignment

- a. Set Diskette power on.
- b. Manually depress the load micro switch.
- c. Observe the crank cam moves to a bottom dead center position relative to the carrier plane, i. e. , maximum penetration of cone assembly into hub. (Figure 6-13B)
- d. Depress eject button on bezel and observe the crank cam rotate to a point where the bearing follower is just clear of impacting the carrier plane, i. e. , 0-.030". Once the carrier is open there must be no further contact between the bearing follower and carrier. (Figure 6-13A)

2. Eject Motor Cam Adjustment Procedure

- a. Slacken No. 8 set screw holding cam to motor shaft such that the motor cam can just be rotated on the shaft.
- b. Observe the crank cam in its loaded and unloaded positions.
- c. If incorrect make small rotational adjustment of the motor cam until desired crank cam action is achieved.
- d. Tighten set screw.

3. Crank Cam Alignment Check

The crank cam angular alignment is determined by the motor cam alignment. To check for cam penetration proceed as follows:

- a. Set drive power on.
- b. Manually depress the load micro switch.

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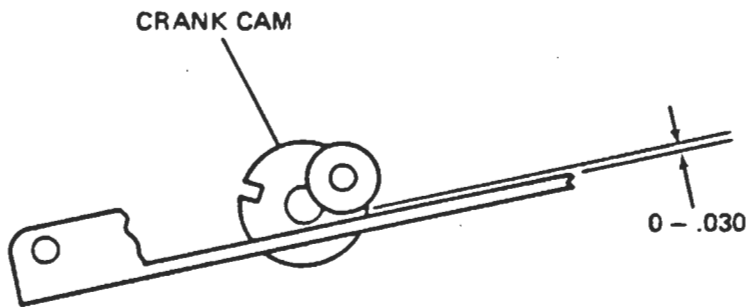


Figure 6-13A. Eject Motor Cam Alignment Check - Carrier Open

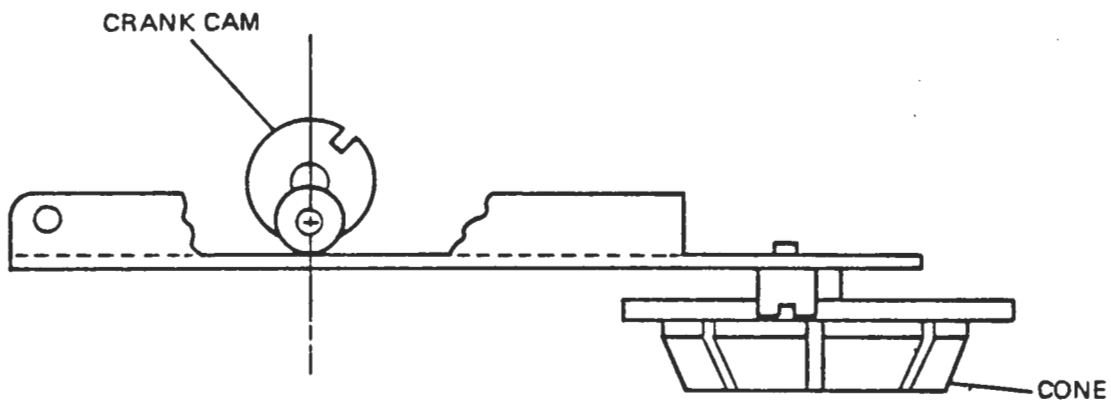


Figure 6-13B. Eject Motor Cam Alignment Check - Carrier Closed

- c. Observe the gap between the E-ring which holds the cone assembly to the carrier and the corresponding carrier surface. (Figure 6-14)
- d. With the carrier in the loaded position the gap should be $.05 \pm .02$.

4. Crank Cam Alignment Procedure

- a. Slacken two No. 8 slotted screws securing motor bracket to side plate.
- b. Set drive power on.
- c. Manually depress the load micro switch and observe gap described in Paragraph c of check procedure.
- d. If incorrect, slacken two No. 4 slotted screws holding motor shaft support to side plate.
- e. Displace arm, tighten screws and check alignment.
- f. Repeat until desired alignment is achieved.
- g. Tighten 2 motor bracket screws after aligning support arm.

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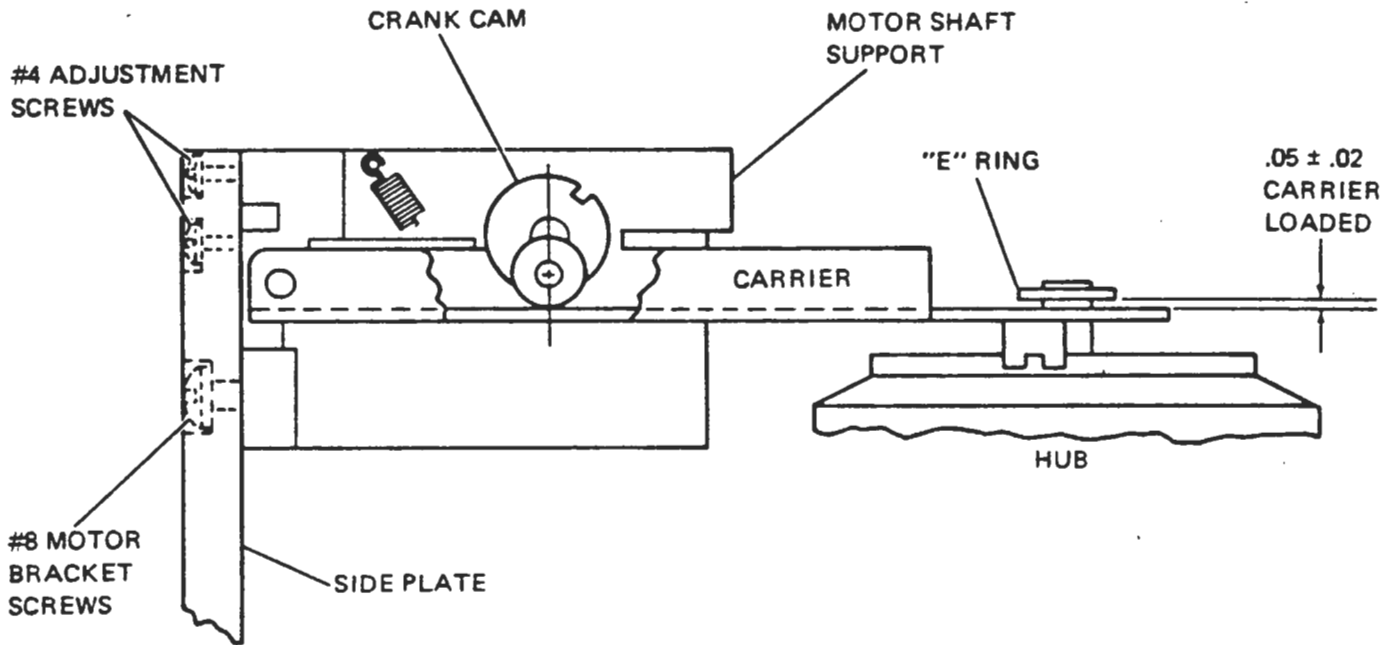


Figure 6-14 Crank Cam Alignment Check

- h. After aligning the crank cam check the space between the photosense assembly on the carrier and the LED assembly on the deck plate. With the carrier in the loaded position this should be $.09 \pm .01$. (Figure 6-7) There is no adjustment for this. If the dimension is incorrect deform the carrier sheet metal between the cone and photosense assembly.

6.4.10. HEAD PRESSURE ARM ASSEMBLY

1. Head Pressure Arm Check

The pressure arm assembly is the same for Side 0 as Side 1. To check arm pressure proceed as follows:

- Load carrier and head solenoid.
- Using a cantilever type force gage measure the arm spring force at the head. (Figure 6-15.)
- The arm spring force reading will be different, depending on whether the force is measured while the arm is moving toward the head or away from the head.
- The correct force is 18 ± 4 gms measured when the arm is moving toward the head.

NOTE

28gms equals one ounce.

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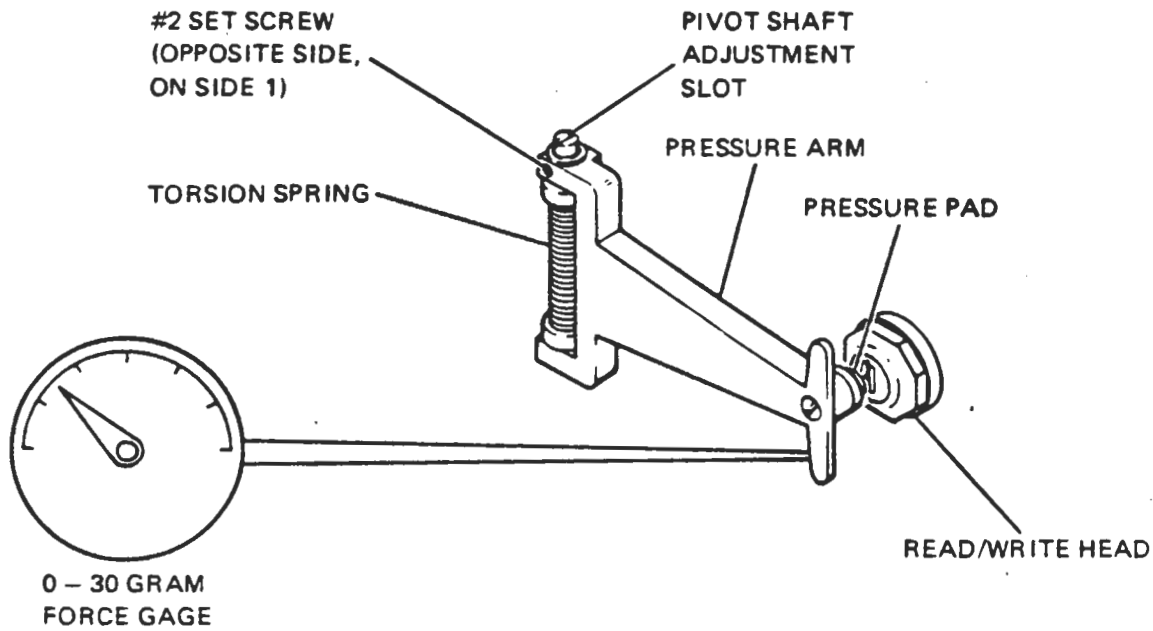


Figure 6-15. Head Pressure Arm Check

2. Head Pressure Arm Adjustment

If the pressure arm force at the head is incorrect, proceed as follows:

- a. Set Diskette power off.
- b. Slacken No. 2 set screw securing arm to pivot shaft.
- c. Rotate pivot shaft clockwise to increase force, anti-clockwise to decrease force and tighten set screw.

NOTE

There are four flats on the pivot shaft which the set screw can locate against. Therefore, only quarter turn increments of the pivot shaft can be made.

3. Head Pressure Pad Replacement

The pressure pad is fastened to a plastic insert which can be replaced without disturbing the head pressure arm adjustment.

- a. Remove pad insert assembly.
- b. Install replacement assembly.
- c. Write on scratch diskette and observe read data.
- d. Apply additional pressure to pressure arm by hand and observe any change in amplitude of read data.

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- e. If the amplitude increases by more than 15% then the pressure pad is not properly located with respect to the read/write head or the arm spring force is too low.
- f. Rotation of the pad insert may improve contact between media and read/write head if this appears to be the problem.

6.4.11. HEAD PRESSURE ARM RETRACT MECHANISM (Side 1) CHECK

1. During loading and unloading of a diskette the pressure arm must be in a retracted position so as not to interfere with the diskette during this operation. On Side 0 part of the carrier member is used to perform this function and no adjustments are required. On Side 1 an adjustment screw fastened to the carrier assembly bears against a mechanism which in turn activates the pressure arm. This screw must be properly positioned to provide proper functioning of the pressure arm retract mechanism.
2. To check for proper adjustment, proceed as follows:
 - a. Set drive power on.
 - b. Manually load carrier Side 1 by depressing load micro switch Side 1.
 - c. Observe the position of the pressure arm retract mechanism by looking through the diskette aperture Side 1 in the front bezel.
 - d. The mechanism as viewed in this manner should appear as shown in Figure 6-16.

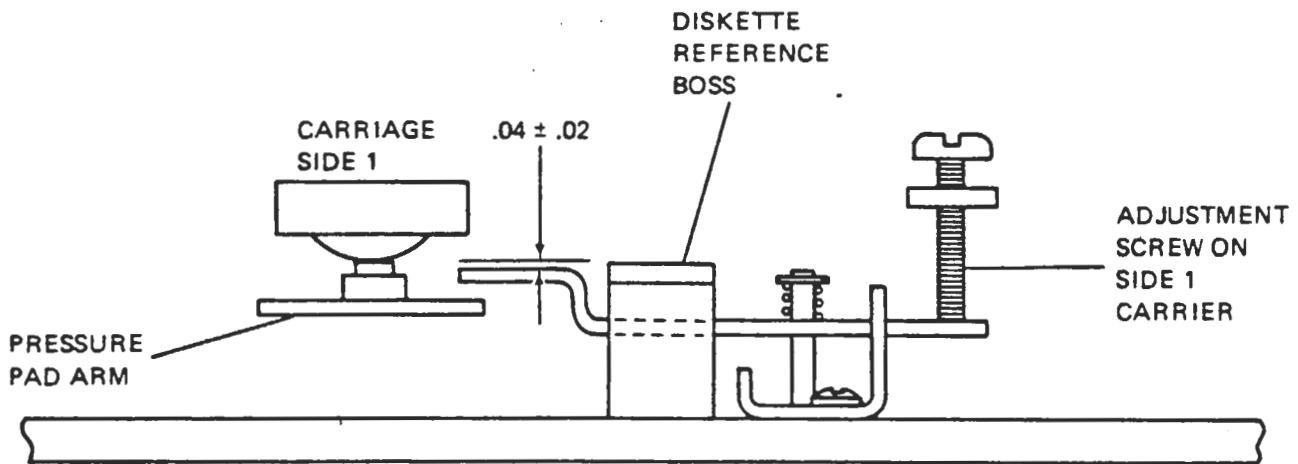


Figure 6-16. Head Pressure Arm Retract Mechanism (Side 1)
Check and Adjustment

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2. Head Pressure Arm Retract Mechanism (Side 1) Adjustment

To adjust the retract mechanism, proceed as follows:

- a. Set drive power on.
- b. Manually load carrier (Side 1) by depressing load micro switch Side 1.
- c. Observe the position of the retract mechanism as viewed through the diskette aperture in the bezel. (Figure 6-16)
- d. Adjust screw on carrier until the desired setting of the retract mechanism is achieved.

6.4.12 READ/WRITE HEAD PENETRATION**1. Read/Write Head Penetration (Side 1) Check**

The penetration of the read/write head into the plane of the diskette media is adjustable on Side 1 only. To check for proper penetration, proceed as follows:

- a. Set drive power on.
- b. Load scratch diskette into Side 1.
- c. Access Track 76 and load head Side 1.
- d. Write alternate 1's and 0's pattern.
- e. Monitor read data.

PROG:	Read/Write Head Penetration (Side 1)
SYNC:	Int Ch 1
CH 1:	50mV/div A. C.
CH 2:	50mV/div A. C. inverted
MODE:	Add CH 1 and CH 2 50 usec/div

Scope probes Ch 1 and Ch 2 across C19 on data and interface PCB.

- f. While monitoring read data deflect the carriage Side 1 to both increase and decrease penetration of the read/write head and observe the change in read amplitude. This can be done by pressing or pulling lightly on the carriage near the read/write head.
- g. If the amplitude of the read data increases significantly (i. e. , greater than 10%) by increasing or decreasing the head penetration then this is an indication of incorrect read/write head penetration.
- h. De-energize the head load solenoid Side 1.
- i. If the amplitude of the read data does not attenuate substantially (i. e. , greater than 50%) when the head pressure pad is disengaged then this is an indication of excessive head penetration which may cause excessive media wear.
- j. Access Track 0 and repeat steps d through i.

2. Read/Write Head Penetration (Side 1) Adjustment

To adjust the read/write head penetration on Side 1, proceed as follows:

- a. Set Diskette power on.
- b. Load scratch diskette into Side 1.
- c. Access Track 76 and load head Side 1.
- d. Write alternate 1's and 0's pattern.
- e. Monitor read data per Paragraph e of check procedure.
- f. While monitoring read data adjust head penetration via set screw (Figure 6-12). Adjust for maximum read data amplitude.
- g. Re-write and check for maximum amplitude.
- h. De-energize head load solenoid and observe attenuation in read amplitude. This should be at least 50%. If not, the indication is there is excessive read/write head penetration.
- i. Access Track 0 and repeat steps d through h.

Materials List, PTC Configuration

REV A	PERSCI INCORPORATED 9 EPT 4 - 83 MATERIAL LIST						
	TITLE ASSY, DUAL DISKETTE DRIVE				M/L NO. 200131-001		REV A
COMPILED BY:		DATE	CHECKED BY:	DATE	APPROVED BY:	DATE	RELEASE/CHANGE DATE
						9-12-77	9-12-77
NEXT ASSY.			1ST USED ON 270	DWG. SIZE NONE	SHEET <u>1</u> OF <u>1</u>		
ITEM NO.	DRAWING TITLE	DWG NO.	QTY	CODE	REMARKS	LAST REV	
	USE BASIC ASSY 200131-000 <i>BM</i>						
	LATEST REV AND ADD THE FOLLOWING:						
3	ASSY, DATA SEPARATOR <i>BM</i>	200157-001	1	A	000-001	E/A	
4	ASSY, P.C.B. DATA AND INTERFACE <i>BM</i>	200263-007	1	A	000 007	H/D	
6	ASSY, EJECT AND CARRIER <i>BM</i>	200219-001	1	A		D	
24	BRACKET, WRITE PROTECT <i>part 2</i> <i>disk head wires</i>	200189	1	D	SIDE 1	A	
SELECTIONS AND OPTIONS							
MODEL: 270							
HARD SECTOR, 32 SECTORS							
SINGLE DENSITY-PERSCI							
REMOTE EJECT: NONE							
WRITE PROTECT: NONE							

M/L NO. 200131-001

9 EPT 4 - 84
MATERIAL LIST

TITLE ASSY DUAL DISKETTE DRIVE	DWG NO. 200131-000	REV C	SHEET 1 OF 2
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PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS	REV.
1	ASSY CENTER AND UPPER DECK BM	200227	1		B
2	ASSY POSITIONER BM	200228	1		A
3	ASSY DATA SEPARATOR BM			SEE BUILD ML	
4	ASSY P.C.B. DATA AND INTERFACE BM			SEE BUILD ML	
5	BEZEL	200192-002	1		
6	ASSY EJECT AND CARRIER BM			SEE BUILD ML	
7	ASSY P.C.B. POSITION SERVO BM	200137	1		C
8	ASSY DATA BD PIVOT BM	200226	2		A
9	GUIDE HEAD CABLE	200260	1		
10	SCREW FL HD 82° SOC	100030-408	2	8-32 x 1/2	
11	SCREW SOC HD CAP	100003-416	1	8-32 x 1.00	
12	SCREW SOC HD CAP	100003-408	2	8-32 x 1/2	
13	SCREW BD HD SLOTTED	100002-203	4	4-40 x 3/16	
14	SCREW SOC HD CAP	100003-512	2	10-32 x 3/4	
15	SCREW BD HD SLOTTED	100002-204	7	4-40 x 1/4	
16	SCREW 82° FL HD SLOTTED	100029-408	4	8-32 x 1/2	
17	CLAMP CABLE	100005-003	2		
18	TIE WRAP	100036-007	2		
19	ASSY, WRITE PROTECT (SIDE 0) O			SEE BUILD ML	
20	BRACKET, COVER	200350	1		
21	COVER, SCALE	200311	1		
22	ASSY, WRITE PROTECT (SIDE 1) O			SEE BUILD ML	
23	TUBING, HEAT SHRINK	100095-006	AE		
24	BRACKET, WRITE PROTECT			SEE BUILD ML	
25	WASHER, FLAT REDUCED O.D.	100099-500	2	#10	
26	WASHER, SPLIT LOCK	100007-500	2	#10	
27	LABEL, IDENT	200085	1		
28	BAR, SUPPORT	200390	1		
29	SUPPORT MAGNET	200391	1		
30	SCREW SOC HD CAP	100003-610	2	1/4 x 5/8	
31	WASHER, SPLIT LOCK	100007-600	2	#1/4	
32	WASHER FLAT	100008-600	2	#1/4	
33	BRACKET, PLO ED	200172	1		

200131-000

9-29-77

MATERIAL LIST

TITLE ASSY. P.C.B. PHASED LOCKED
DOUBLE F DATA SEPARATOR

DWG NO
200157-000

REV
E

SHEET 2 OF 3

MOD 70/270/277

PERSCI, INC.

DWG NO.
200157-000

REV
E

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	PROCESSED BOARD	200155	1	REV D
2	SUBASSY, HARNESS	200398-005	1	P6
3				
4	IC LM311N	150600	1	U3
5	IC MC1458-P1	150602	1	U2
6	IC 7400	150603	2	U1, 8
7	IC 7474	150609	4	U4, 6, 7, 9
8	IC 7486	150611	1	U5
9	IC 74123	150612	1	U10
10	IC 7416	150621	1	U11
11				
12				
13				
14	TRANSISTOR 2N4400	150200	2	Q2, 6
15	TRANSISTOR 2N4402	150201	4	Q1, 4, 7, 8
16	TRANSISTOR 2N5460	150202	1	Q5
17	TRANSISTOR 2N2913	150203	1	Q3
18				
19				
20	DIODE 1N3064	150300	8	CR1,2,3,4,5,6,7,8
21	DIODE, ZENER 1N752A	150302	1	VR1
22	DIODE, ZENER 1N751A	150311	1	VR2
23				
24				
25	CAPACITOR, MICA 100 Pf	150102-101	3	C6, 10, 11
26	CAPACITOR, MYLAR 1000 Pf	150101-102	1	C9
27	CAPACITOR, MYLAR .0015 Uf	150101-152	1	C7
28	CAPACITOR, MYLAR .01 Uf	150101-103	1	C8
29	CAPACITOR, TANPL., 10% 1 Uf	150100-105	5	C1, 2, 3, 4, 5
30				
31				
32				
33	RESISTOR VAR., 20 TURN 2K	150003-202	1	R13

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MATERIAL LIST

REV

TITLE ASSY. P.C.B. PHASED LOCKED
DOUBLE F DATA SEPARATORDWG NO.
200157-000REV
E

SHEET 3 OF 3

PERSCI, INC.

DWG NO.

200157-000

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
34				
35	RESISTOR $\frac{1}{2}$ W 5% 1K	150002-102	1	R28
36				
37	RESISTOR $\frac{1}{4}$ W 5% 330	150000-331	1	R3
38	RESISTOR $\frac{1}{4}$ W 5% 750	150000-751	1	R15
39	RESISTOR $\frac{1}{4}$ W 5% 1K	150000-102	11	R2,4,5,6,12,14,16, R20,22,26,27
40	RESISTOR $\frac{1}{2}$ W 5% 1.5K	150000-152	1	R10
41	RESISTOR $\frac{1}{2}$ W 5% 3.3K	150000-332	2	R1, 17
42	RESISTOR $\frac{1}{2}$ W 5% 3.9K	150000-392	2	R23, 24
43	RESISTOR $\frac{1}{2}$ W 5% 5.1K	150000-512	1	R21
44	RESISTOR $\frac{1}{2}$ W 5% 5.6K	150000-562	1	R11
45	RESISTOR $\frac{1}{2}$ W 5% 10K	150000-103	1	R19
46	RESISTOR $\frac{1}{4}$ W 5% 15K	150000-153	1	R9
47	RESISTOR $\frac{1}{4}$ W 5% 22K	150000-223	2	R7, 18
48	RESISTOR $\frac{1}{4}$ W 5% 240K	150000-244	1	R8
49				
50				
51				
52	HOUSING, CONNECTOR, 10 Pin	100032-010	1	P6
53				
54				
55				
56	PIM, MALE	100046	5	TP1, 2, 3, 4, 5
57				
58	WIRE, INSUL., AWG 24			
59				
60				
61				
	SCHEMATIC	200115	REF	REV C
	ARTWORK	200156	REF	

MATERIAL LIST

REV
200263-01

TITLE
ASSEMBLY, PCB DATA AND INTERFACE

DWG NO.
200263-007

REV
0

SHEET 1 OF 1

MODEL 270 HARD SECTOR 32 SECTORS

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
	USE BASIC BD 200263-000			
	LATEST REVISION AND ADD			
	THE FOLLOWING:			
1	ASSY, SELECT MODULE	200288-003	1	U11
2				
3	CAPACITOR, TANTL., 10% 0.1UF	150100-104	1	C36
4	CAPACITOR, TANTL., 10% 1UF	150100-105	2	C40,41
5				
6	RESISTOR, 1/4 W., 5% 11K	150000-113	2	R88,94
7				
8	WIRE, INSULATED, AWG 24		A/R	JUMPER FROM A TO B ✓
				JUMPER FROM D TO E ✓
				JUMPER FROM F TO G ✓
				JUMPER FROM H TO J ✓
				JUMPER FROM H TO P ✓
				JUMPER FROM R TO S ✓
				JUMPER FROM W TO Y ✓
				JUMPER FROM AA TO AB ✓
				JUMPER FROM AD TO AF ✓
				JUMPER FROM AH TO AK ✓
				JUMPER FROM AL TO AM ✓
				JUMPER FROM AT TO AY ✓
				JUMPER FROM AU TO AW ✓
				JUMPER FROM BA TO BB ✓
				JUMPER FROM BD TO BE ✓
				JUMPER FROM BH TO BJ ✓
				JUMPER FROM BK TO BM ✓
				SECTOR "0" JUMPER 32 ✓
				SECTOR "1" JUMPER 32 ✓
	NOTE: JUMPER POINTS NOT LISTED			CHASSIS GND W1
	ARE OPEN (NOT USED)			

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MATE 9 EPT 4 - 90 T

 TITLE
 ASSEMBLY, PCB DATA AND INTERFACE

 DWG NO.
 200263-000

 REV
 H

SHEET 2 OF 6

MODEL 270 BASIC BOARD

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	BOARD, PROCESSED	200262	1	REV C
2				
3	BRACKET, DATA BD	200171	1	REV B
4	INSULATOR, DATA BD	200174	1	REV A
5				
6				
7				
8				
9				
10				
11	IC LM311N	150600	3	U18, 22, 61
12	IC MC1406L	150601	1	U55
13	IC MC1458C-P1	150602	2	U40, 51
14	IC 7400	150603	5	U15, 28, 53, 57, 60
15	IC 7404	150604	5	U20, 30, 38, 41, 4r
16	IC 7408	150605	4	U26, 29, 45, 50
17	IC 7432	150608	4	U19, 54, 56, 58
18	IC 7474	150609	6	U14, 24, 39, 46, 47, 52
19	IC 7486	150611	1	U21
20	IC 74123	150612	4	U10, 12, 25, 44
21	IC 74193	150614	2	U42, 43
22	IC 75451	150616	1	U17
23	IC 75452	150617	2	U31, 36
24	IC 75453	150618	9	U2, 3, 4, 5, 6, 7, 8, 23, 59
25	IC 72733	150619	2	U33, 35
26	IC 7416	150621	2	U13, 48
27	IC 7406	150622	1	U37
28	IC SN72306P	150646	2	U34, 32
29				
30	RESISTOR NETWORK 4.7K	150050	1	U9
31	RESISTOR NETWORK 220/330	150051	1	U1
32				
33				

TITLE ASSEMBLY, PCB DATA AND INTERFACE	DWG NO. 200263-000	REV H	SHEET 3 OF 6
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MODEL 270 BASIC BOARD **PERSCI, INC.**

DWG NO. 200263-C

REV H

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
34	TRANSISTOR 2N4400	150200	5	Q2,26,27,28,31
35	TRANSISTOR 2N4402	150201	25	Q3,4,5,6,7,8,9,10, 13,16,17,18,19,20, 21,22,23,24,25, 29,30,32,33,34,35
36	TRANSISTOR 2N5460	150202	4	Q11,12,14,15
37	TRANSISTOR 2N2913	150203	1	Q1
38	TRANSISTOR 2N706A	150207	4	Q36,37,38,39
39				
40				
41				
42	DIODE 1N3064	150300	16	CR3,4,5,6,7,8, 9,10,11,12,13,14, 15,16,17,18
43	DIODE, ZENER 1N752A	150302	1	VR1
44	DIODE, ZENER 1N759A	150313	2	VR2,4
45	DIODE, ZENER 1N751A	150311	1	VR3
46	INDUCTOR 200UH	150094	1	L1
47	CAPACITOR, MICA .001UF	150102-102	2	C58,59
48	CAPACITOR, MICA 220pf	150102-221	1	C14
49	CAPACITOR, MICA 100pf	150102-101	3	C1,50,51
50	CAPACITOR, MICA 510pf	150102-511	4	C21,26,46,49
51	CAPACITOR, MYLAR .001UF	150101-102	2	C3,4
52	CAPACITOR, CERAMIC .01UF	150103-103	15	C7,11,18,20,24,25, 28,30,34,37,38,43, 45,52,56
53	CAPACITOR, TANTL 10% 0.1UF	150100-104	3	C35,42,44
54	CAPACITOR, TANTL 10% 1UF	150100-105	23	C2,5,6,8,9,10,12, 13,15,16,17,19, 22, 23,27,29,33,39,47, 53,54,55,57

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TITLE
ASSEMBLY, PCB DATA AND INTERFACE

DWG NO.
200263-000

REV
H

SHEET 4 OF 6

MODEL 270 BASIC BOARD

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
55	CAPACITOR, TANTL 22UF	150100-226	1	- C48
56				
57				
58				
59	RESISTOR, VARIABLE 2K	150003-202	1	R154
60				
61	RESISTOR 1/2 W., 5% 10	150002-100	2	R121,126
62	RESISTOR 1/2 W., 5% 47	150002-470	2	R69,70
63	RESISTOR 1/2 W., 5% 68	150002-680	4	R104,105,106,107
64	RESISTOR 1/2 W., 5% 1K	150002-102	1	R169
65	RESISTOR, 1/2 W., 1% 1.50K	150001-1501	1	R81
66	RESISTOR 1/2 W., 1% 332	150001-3320	2	R13,14
67	RESISTOR 1/2 W., 1% 1.78K	150001-1781	1	R138
68	RESISTOR 1/2 W., 1% 3.01K	150001-3011	1	R78
69	RESISTOR 1/2 W., 1% 10K	150001-1002	5	R108,109,147,148,149
70	RESISTOR 1/2 W., 1% 24.9K	150001-2492	1	R152
71	RESISTOR 1/2 W., 1% 30.1K	150001-3012	1	R146
72	RESISTOR 1/2 W., 1% 4.64K	150001-4641	2	R86,87
73				
74	RESISTOR 1/2 W., 5% 10	150000-100	13	R3,10, 12,18,19, 33,34,37,38,41, 42,56,77
75	RESISTOR 1/2 W., 5% 47	150000-470	2	R26,27
76	RESISTOR 1/2 W., 5% 100	150000-101	13	R23,29,35,36,39, 40,82,83,84,85, 101,103,128
77				
78	RESISTOR 1/2 W., 5% 220	150000-221	7	R5,7,49,53,58, 120,125
79	RESISTOR 1/2 W., 5% 330	150000-331	13	R6,8,9,15,16,17, 59,65,66,67,68, 119,124

REV H
200263-
NO.

TITLE ASSEMBLY, PCB DATA AND INTERFACE	DWG NO. 200263-000	REV H	SHEET 5 OF 6
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MODEL 270 BASIC BOARD **PERSCI, INC.**

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
80	RESISTOR 1/4 W., 5% 510	150000-511	1	R111
81	RESISTOR 1/4 W., 5% 1K	150000-102	24	R1,2,48,52,64,71, 72,73,74,89,92,95,98, 112,114,117,118,122, 123,132,134,158,166, 170
82	RESISTOR 1/4 W., 5% 2K	150000-202	10	R22,24,28,30, 110,115,116,133, 137,139
83	RESISTOR 1/4 W., 5% 680	150000-681	1	R25
84	RESISTOR 1/4 W., 5% 3.9K	150000-392	4	R4,45,57,135
85	RESISTOR 1/4 W., 5% 4.7K	150000-472	11	R60,61,175, 130,136,155,159, 160,161,167,168
86	RESISTOR 1/4 W., 5% 5.1K	150000-512	1	R153
87	RESISTOR 1/4 W., 5% 6.8K	150000-682	5	R46,47,50,51,62
88	RESISTOR 1/4 W., 5% 10K	150000-103	23	R20,21,31,32,43,44, 54,55,79,131,151,156, 157,162,163,164,165, 171,172,173,174,90,96
89	RESISTOR 1/4 W., 5% 15K	150000-153	2	R100, 102
90	RESISTOR 1/4 W., 5% 18K	150000-183	1	R63
91	RESISTOR 1/4 W., 5% 20K	150000-203	2	R141,144
92	RESISTOR 1/4 W., 5% 22K	150000-223	3	R75,76,80
93	RESISTOR 1/4 W., 5% 30K	150000-303	3	R93,99,140
94				
95	RESISTOR 1/4 W., 5% 39K	150000-393	2	R143,145
96	RESISTOR 1/4 W., 5% 47K	150000-473	3	R150,176,177
97	RESISTOR 1/4 W., 5% 220K	150000-224	2	R91,97
98	RESISTOR 1/4 W., 5% 100K	150000-104	2	R113,129
99	RESISTOR 1/4 W., 5% 240K	150000-244	1	R142
100	RESISTOR 1/4 W., 5% 1MEG	150000-105	1	R127

REV D
 DWG NO. 200219-001

TITLE
 ASSY EJECT & CARRIER

DWG NO.
 200219-001

REV D
 SHEET 1 OF 3

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1				
2	PLATE CARRIER SIDE 0	200054	1	
3	RING EXT. "E" TYPE	100001-004	6	
4				
5	SHAFT CONE	200073	2	
6	SPRING, COMPRESSION CONE	200360	2	
7	WASHER SHIM	200081-001	2	
8	CONE THRUST	200355	2	
9				
10	FLANGE CONE	200326	2	
11	BEARING BALL FLANGED	100011-001	2	
12	NUT HEX	100015-100	2	#2
13	ASSY PHOTOSENSE	200274-002	2	
14	WASHER FLAT	100008-100	2	#2
15	SCREW SOC HD CAP	100003-104	2	2-56 X 1/4
16	CAM EJECT MTR SIDE 1	200220	1	
17	SPRING, CONE	200359	2	
18	FOAM PRESSURE	200103	4	
19	PLATE CARRIER SIDE 1	200166	1	
20	SCREW BD HD SLOTTED	100002-203	12	4-40 X 3/16
21	BRACKET CIRCUIT BD	200167-002	1	
22	GUIDE DISKETTE	200047-002	2	
23	GUIDE DISKETTE	200047-001	2	
24	SWITCH MOM. PUSH	100026	2	
25	PIN ROLL	100006-408	2	
26	RING EXT. "E" TYPE	100001-002	2	
27	BEARING BALL	100029-002	2	
28	ASSY, CRANK CAM	200035-001	1	
29	ASSY, CRANK CAM	200035-002	1	
30	BEARING OILITE	1000027	2	
31	BLOCK CARRIER PIVOT	200202-001	2	
32	SCREW SOC HD CAP	100003-206	8	4-40 X 3/8
33	SCREW BD HD SLOTTED	100002-206	10	4-40 X 3/8

MATE 9 EPT 4 - 96 T

TITLE
ASSY EJECT AND CARRIER

DWG NO.
200219-001

P.V.
D

SHEET 2 OF 3

PERSCI, INC.

200219-001

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
34	ARM SUPPORT DUAL	200194	2	
35	SPRING, TENSION	100022-002	4	
36	PIN ROLL	100006-116	2	
37	SPRING COMPRESSION	100021-003	2	
38	SCREW BD HD SLOTTED	100002-216	4	4-40 X 1.00
39	BLOCK CARRIER PIVOT	200202-002	2	
40	SCREW BD HD SLOTTED	100002-410	4	8-32 X 5/8
41	BRACKET LOAD SWITCH	200147	1	
42	SWITCH MICRO (LEVER)	100019	2	
43	SCREW BD HD SLOTTED	100002-208	4	4-40 X 1/2
44	SCREW BD HD SLOTTED	100002-204	2	4-40 X 1/4
45				SEE OTHER DASH NO. ML'S
46	BLOCK PIVOT	200043	4	
47	SWITCH MICRO	100028	4	
48	CAM EJECT MTR SIDE O	200058	1	
49	BRACKET EJECT MTR	200289	2	
50	PLATE SIDE LOWER DECK	200148	1	
51				SEE OTHER DASH NO. ML'S
52	SUBASSY, GEAR MOTOR	200394-001	1	
53	BRACKET CIRCUIT BD	200167-001	1	
54	SCREW SET HEX SOC	100004-405	2	6-32 X 5/16
55	SUBASSY, GEAR MOTOR	200394-002	1	
56	PIN ROLL	100006-112	2	
57	TAPE ADHESIVE TEFLON	100059	A/R	
58	SCREW SET HEX SOCKET	100004-403	2	
59	SCREW SET HEX SOCKET	100005-414	1	4-40 X 7/8
60	ADHESIVE TAPE	100012	A/R	
61	LEVER		A/R	
62				
63	WIRE, 24 AWG	U.L. 100037-024	A/R	
64				
65				
66				

TITLE ASSY CENTER AND UPPERDECK	DWG NO. 200227	REV B	SHEET <u>1</u> OF <u>2</u>
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PERSCI, INC.

200227

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	ASSY. SPINDLE MOTOR	200218	1	
2	ASSY. DISKETTE SPINDLE	200217	1	
3	ASSY, HD. ENG. SOL (SIDE 0)	200214	1	
4	ASSY, HD. ENG. SOL (SIDE 1)	200216	1	
5	ASSY, SPINDLE SENSOR	200213-002	1	
6	ASSY, LED (SIDE 0)	200221	1	
7	ASSY, LED (SIDE 1)	200222	1	
8				
9				
10	ASSY F.C.E. SPINDLE SERVO	200134	1	
11				
12	SPEC BELT SPINDLE MTR.	200042	1	
13	GUIDE DISKETTE	200047-001	2	
14	GUIDE DISKETTE	200047-002	2	
15	STOP DISKETTE SIDE 0	200182	1	
16	STOP DISKETTE SIDE 1	200183	1	
17	PLATE CENTER DECK	200149	1	
18	PLATE SIDE UPPER DECK	200170	1	
19				
20	BRACKET LIFTER PIVOT	200164	1	
21	LIFTER PRES ARM	200150	1	
22	SHAFT LIFTER	200178	1	
23	SUPPORT DISKETTE REF.	200044	2	
24	SHAFT EJECT DUAL	200196	1	
25	CRANK EJECT	200007	2	
26	ACTUATOR EJECT	200006	2	
27	ARM EJECT	200059	2	
28	GUIDE EJECT ARM	200046-001	1	
29	GUIDE EJECT ARM	200046-002	1	
30	SPRING TORSION	200009	1	
31	SPRING TORSION	200169	1	
32	SPACER, PHENOLIC	200103-203	1	
33	SPACER ALUM. ROUND	200021-002	2	

MAT 9 EPT 4 - 99 ST

TITLE
ASSY CENTER AND UPPER DECK

DWG NO.
200227

REV
B

SHEET 2 OF 2

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
34	SPACER ALUM ROUND	200021-004	2	
35	WASHER, SHIM	200091-001	2	
36	STANDOFF, HEATSINK	200197	2	
37	COVER, CABLE SERVO	20016	1	
38	SPRING COMP	100021-002	3	
39	WASHER, FIBROUS	100051-001	3	
40	PIN ROLL	100006-104	2	1/16 DIA X 1/4
41	PIN ROLL	100006-116	2	1/16 DIA X 1
42	PIN ROLL	100006-408	2	1/8 DIA X 1/2
43	SCREW BD HD SLOTTED	100002-207	1	4-40 X 7/16
44	SCREW FL HD 82° SLOTTED	100039 214	2	4-40 X 7/8
45	SCREW BD HD SLOTTED	100002-108	3	2-56 X 1/2
46	SCREW BD HD SLOTTED	100002-203	13	4-40 X 3/16
47	SCREW BD HD SLOTTED	100002-204	8	4-40 X 1/4
48	SCREW BD HD SLOTTED	100002-214	4	4-40 X 7/8
49	SCREW BD HD SLOTTED	100002-406	5	8-32 X 3/8
50	SCREW BD HD SLOTTED	100002-424	2	8-32 X 1-1/2
51				
52	SCREW SET SOC HD	100004-204	1	4-40 X 1/4
53				
54	SCREW SOC HD CAP	100003-206	2	4-40 X 3/8
55				
56	SCREW SOC HD CAP	100003-408	2	8-32 X 1/2
57				
58				
59	CLAMP CABLE	100005-001	1	1/16 DIA
60				
61	RING EXT. RET "E" TYPE	100001-002	4	1/8 DIA
62				
63	TAPE ADHESIVE TEFLON	100059	A/R	
64				
65				
66				

TITLE
ASSY POSITIONER

DWG NO.
200228

REV
A

SHEET 1 OF 2

PERSCI, INC.

DWG NO.
200228

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	ASSY VOICE COIL	200024	1	
2	ASSY MAGNET	200023	1	
3	ASSY TRANSDUCER AMP	200079	1	
4				
5	ASSY TRANSDUCER	200068	1	
6	ASSY CARRIAGE SIDE 0	200270-001	1	
7	ASSY CARRIAGE SIDE 1	200269	1	
	CLAMP, COIL	200085	1	
9	ASSY SCALE	200272	1	
10	HOLDER PRES PAD	200244	2	
11	PAD PRESSURE	200087	2	
12	WASHER FELT	200126	1	
13	SUPPORT CARRIAGE & COIL	200181	1	
14	FRAME POSITIONER	200193	1	
15	ROD GUIDE	200017	2	
16	PLATE DEFLEXION	200254	1	
17	SUPPORT HEAD SIDE 1	200253	1	
18	SPACER HEAD SUPPORT	200255	1	
19	PIV PIVOT	200304	2	
20	ARM PRES. PAD	200033	2	
21	SPRING TORSION	200303	2	
22	RETAINER, FELT WASHER	200306	1	
23	"O" RING RUBBER	100061	1	
24	RING EXT "E" TYPE	100001-002	4	
25	SCREW SOC HD CAP	100003-312	1	6-32 X 3/4
26	SCREW SOC HD CAP	100003-308	2	6-32 X 1/2
27	SCREW SOC HD CAP	100003-208	5	4-40 X 1/2
28				
29	SCREW SET HEX SOC	100004-402	1	8-32 X 1/8
30	SCREW HEX SOC BT HD	100014-304	4	6-32 X 1/4
31	SCREW HEX SOC BT HD	100014-208	1	4-40 X 5/16
32	SCREW HEX SOC BT HD	100014-108	1	4-40 X 5/16
33	SCREW HEX SOC BT HD	100014-208	2	4-40 X 1/2

REV
 F

TITLE ASSY. P.C.B.
 LAMP AMPLIFIER

DWG NO.
 200080

REV
 F

SHEET 2 OF 3

PERSCI, INC.

DWG NO.
 200080

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	BOARD, PROCESSED	200089	1	REV C
2				
3				
4				
5	IC 1458	150602	3	U1, 2, 3
6				
7	TRANSISTOR 2N2222 A	150208	1	Q1
8				
9	DIODE, ZENER IN752 A	150302	1	VR1
10	CAPACITOR, MICA 100 PF	150102-101	3	C5,6,7
11	CAPACITOR, TANT. 1 Uf	150100-105	4	C1, 2, 3, 4
12				
13	RESISTOR, VAR 2K	150003-202	6	R3, 4, 5, 8, 10, 11
14				
15	RESISTOR $\frac{1}{2}$ W 5% 33	150002-330	1	R15
16	RESISTOR $\frac{1}{8}$ W 1% 1.00K	150001-1001	1	R6
17	RESISTOR $\frac{1}{8}$ W 1% 5.62K	150001-5621	1	R17
18				
19	RESISTOR $\frac{1}{4}$ W 5% 1K	150000-102	2	R14, 16
20	RESISTOR $\frac{1}{4}$ W 5% 4.7K	150000-472	1	R20
21	RESISTOR $\frac{1}{4}$ W 5% 10K	150000-103	1	R1
22	RESISTOR $\frac{1}{4}$ W 5% 51K	150000-513	1	R12
23	RESISTOR $\frac{1}{4}$ W 5% 560K	150000-564	4	R9, 11, 18, 13
24	RESISTOR $\frac{1}{4}$ W 5% 5.6MEG	150000-565	1	R7
25				
26				
27	PIN, MALE	100046	7	TP1, 2, 3, 4, 5, 6, 7
28	CONNECTOR, 5 Pin	100041-005	1	J13
29				
30				
31				
32				
33				

22

MATERIAL LIST

TITLE	ASSY. P.C.B. POSITIONER SERVO	DWG NO. 200137	REV C	SHEET 4 OF 5
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MODEL 270/277

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
67	SCREW, BINDING HD., 4-40	100002-207	4	
68	INSL & WASHER	150212	4	to be used with
69	WASHER, SHOULDER	100050-001	4	NJE-32
70	WASHER, FLAT	100008-200	4	
71	NUT	100015-200	4	
72				
73	SCREW, BINDING HD., SLOTTED	100002-307	4	
74	INSULATOR	150213	4	to be used with
75	WASHER, SHOULDER	100050-001	4	TIP 32 & RCA 32
76	WASHER, FLAT	100008-300	4	
77	NUT	100015-300	4	
78				
79	CONNECTOR 10 Pin	100041-010	1	J5
80	CONNECTOR 4 Pin	100041-004	1	J8
81	SUBASSY, HARNESS	200398-007	1	P8
82	SUBASSY, HARNESS	200398-008	1	P7
83				
84				
85				
86				
87				
88				
89				
90				
91				
92				
93				
94	WIRE, BUSS AWG 24		A/R	Use as jumper
95	WIRE, BUSS, #22		A/R	across R50
96				
97				
98				
99	GREASE, SILICON		A/R	55

200137

TITLE	ASSY. P.C.B. POSITIONER SERVO	DWG NO. 200137	REV C	SHEET 3 OF 5
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PERSCI, INC.

200137

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
34	RESISTOR, VAR 2K	150003-202	1	R33
35				
36	RESISTOR, 3W 5% 1	150008-010	2	R77,78
37				
38	RESISTOR, 1/4W 1% 1K	150001-1001	12	R54,55,56,57,58,59,60,61,62,63,64,65
39	RESISTOR, 1/4W 1% 10K	150001-1002	7	R13,14,15,28,29,52,53
40	RESISTOR, 1/4W 1% 80.6K	150001-8062	1	R48
41				
42	RESISTOR, 1/4W 5% 100	150000-101	1	R69
43	RESISTOR, 1/4W 5% 200	150000-201	2	R2,4
44	RESISTOR, 1/4W 5% 510	150000-511	1	R47
45	RESISTOR, 1/4W 5% 750	150000-751	1	R42
46	RESISTOR, 1/4W 5% 1K	150000-102	14	R5,8,9,16,18,23,27,35,39,41,45,72,74,43
47	RESISTOR, 1/4W 5% 1.2K	150000-122	1	R46
48	RESISTOR, 1/4W 5% 2K	150000-202	1	R38
49	RESISTOR, 1/4W 5% 3.3K	150000-332	2	R67,71
50	RESISTOR, 1/4W 5% 3.9K	150000-392	2	R1,3
51	RESISTOR, 1/4W 5% 4.7K	150000-472	1	R34
52	RESISTOR, 1/4W 5% 5.1K	150000-512	3	R12,20,75
53	RESISTOR, 1/4W 5% 10K	150000-103	7	R6,10,11,30,31,51,73
54	RESISTOR, 1/4W 5% 20K	150000-203	1	R37
55	RESISTOR, 1/4W 5% 22K	150000-223	3	R17,24,26
56	RESISTOR, 1/4W 5% 39K	150000-393	1	R68
57	RESISTOR, 1/4W 5% 51K	150000-513	1	R7
58	RESISTOR, 1/4W 5% 100K	150000-104	8	R21,32,36,40,44,66,70,49
59				
60				
61	RESISTOR, 1/4W 5% 390K	150000-394	1	R19
62	RESISTOR, 1/4W 5% 3.9MEG	150000-395	1	R76
63	RESISTOR, 1/4W 5% 1MEG	150000-105	2	R22,25
64				
65				
66				56

REV

DWG NO.
200137

TITLE		DWG NO.	REV	SHEET OF
ASSY. P.C.B. POSITIONER SERVO		200137	C	5
MODEL 270/277		PERSCI, INC.		
ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	BOARD, PROCESSED	200152	1	REV C
2	HEAT SINK	200162	1	
3				
4	IC 7400	150603	2	U4, 5
5	IC 7404	150604	1	U3
6	IC 7432	150608	1	U7
7	IC LM311N	150600	6	U1,2,8,9,10,12
8	IC MC14580-F1	150602	5	U11,13,15,16,17
9	IC 75451	150616	1	U14
10	IC AH5012	150620	1	U6
11				
12	TRANSISTOR 2N4400	150200	3	Q1, 3, 9
13	TRANSISTOR 2N4402	150201	4	Q4,10,11,16
14	TRANSISTOR 2N5460	150202	1	Q2
15	TRANSISTOR MJE-32, IIF-30, R2-2	150204	4	Q12,13,14,15
16	TRANSISTOR 2N2222A	150208	2	Q5,7
17	TRANSISTOR 2N2907A	150209	2	Q6,8
18				
19				
20	DIODE 1N3064	150300	4	CR1,2,3,4,
21	DIODE, ZENER 1N755A	150301	1	VR1
22				
23	CAPACITOR, mica 510 Pf	150102-511	1	C2
24	CAPACITOR, mylar .001 Uf	150101-102	1	C4
25	CAPACITOR, mylar .0015 Uf	150101-152	1	C8
26	CAPACITOR, CER .01 Uf	150103-103	3	C3,5,6,
27	CAPACITOR, mylar .002 Uf	150101-203	1	C1
28	CAPACITOR, tantalum 10u	150100-105	6	C9,10,11,12,13,14
29	CAPACITOR, mylar 1 Uf	150104-105	1	C7
30				
31				
32				
33				

TITLE	ASSY., P.C.B. SPINDLE SERVO	DWG NO.	200134	REV	F	SHEET	2	OF	4
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MODEL	270/277	PERSCI, INC.							
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200134

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	BOARD, PROCESSED	200135	1	REV D
2	SUBASSY, HARNESS	200398-006	1	P5
3	SUBASSY, HARNESS	200399	1	P4
4	HEAT SINK	200160	1	
5				
6				
7				
8	IC LM311N	150600	1	U6
9	IC MC1458-P1	150602	2	U5, 7
10	IC 7400	150603	1	U1
11	IC 7430	150607	1	U4
12	IC 74193	150614	2	U2, 3
13	IC 7486	150611	1	U8
14				
15				
16				
17	TRANSISTOR 2N4400	150200	3	Q3, 6, 7
18	TRANSISTOR 2N4402	150201	2	Q1, 2
19	TRANSISTOR TIP-32, RCA-32, MJE-32	150204	1	Q4
20	TRANSISTOR 2N3771	150205	1	Q5
21				
22				
23	DIODE 1N3064	150300	2	CR1, 3
24	DIODE 1N4003	150301	2	CR2, 4
25	DIODE, ZENER 1N751A	150311	1	VR1
26	CAPACITOR, MYLAR .001UF	150101-102	1	C17
27	CAPACITOR, Mica 100 Pf	150102-101	1	C13
28	CAPACITOR, Mylar 1000Pf	150101-102	1	C11
29	CAPACITOR, Mylar 6800Pf	150101-682	1	C14
30	CAPACITOR, CERAMIC .01 UF	150103-103	1	C15
31	CAPACITOR, TANT. 10% 0.1 UF	150100-104	1	C8
32	CAPACITOR, Mylar 10% 0.1 Uf	150101-104	2	C5, 8
33	CAPACITOR, TANT. 10% 1 Uf	150100-105	7	C1, 2, 3, 4, 7, 9, 12

TITLE		ASSY., P.C.B. SPINDLE SERVO		DWG NO. 200134		REV F	SHEET 3 OF 4
PERSCI, INC.							
ITEM NO.	DRAWING TITLE			DWG NO.	QTY	REMARKS	
34	CAPACITOR, Mylar 5% 1 Uf			150104-105	2	C6, 10	
35							
36	RESISTOR 1/4W 5% 150			150002-151	1	R27	
37	RESISTOR 1/4W 5% 1K			150002-102	1	R26	
38	RESISTOR 2W 5% 15			150004-150	1	R15	
39							
40	RESISTOR 1/4W 1% 1K			150001-1001	1	R4	
41	RESISTOR 1/4W 1% 1.1K			150001-1101	1	R5	
42	RESISTOR 1/4W .1% 40K			150009-4002	2	R13, 14	
43							
44	RESISTOR 1/4W 5% 47			150000-470	1	R24	
45	RESISTOR 1/4W 5% 100			150000-101	2	R25, 28	
46	RESISTOR 1/4W 5% 510			150000-511	2	R12, 21	
47	RESISTOR 1/4W 5% 1K			150000-102	4	P 17, 18, 19, 22	
48	RESISTOR 1/4W 5% 10K			150000-103	5	R6, 8, 10, 11, 20	
49	RESISTOR 1/4W 5% 51K			150000-513	2	R3, 9	
50	RESISTOR 1/4W 5% 100K			150000-104	2	R7, 16	
51	RESISTOR 1/4W 5% 300K			150000-304	1	R16	
52	RESISTOR 1/4W 5% 560K			150000-564	1	R1	
53	RESISTOR 1/4W 5% 220K			150000-224	1	R23	
54							
55							
56							
57							
58	CONNECTOR, ANGLE 2 Pin			100042-002	1	J1	
59	CONNECTOR, ANGLE 4 Pin			100040-004	1	J2	
60							
61							
62							
63							
64							
65							
66							

DWG NO. 200134

TITLE
 ASSY CARRIER

DWG NO.
 200004

REV
 C

SHEET 1 OF 1

PERSCI, INC.

200004

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	PLATE CARRIER	200054	1	
2	CONE, TMC 1ST	200325	1	
3	FLANGE, CONE	200326	1	
4	SHAFT CONE	200073	1	
5	SPRING, COIL	200319	1	
6	SPRING EXTENSION	100022-002	2	
7	BEARING FLANGED	100011-001	1	
8	SPRING COMPRESSION CONE	100011-001	1	
9	WASHER SHIM	200001-001	1	
10				
11	FOAM PRESSURE	200103	2	
12				
13				
14				
15	RING EXT "E" RET	100001-004	3	
16				
17				
18				
19				
20	TAPE ADHESIVE TEFLON	100059	A/R	
21				
22				
23				
24				
25				
26				
27				
28				
29				

9 EPT 4 - 115

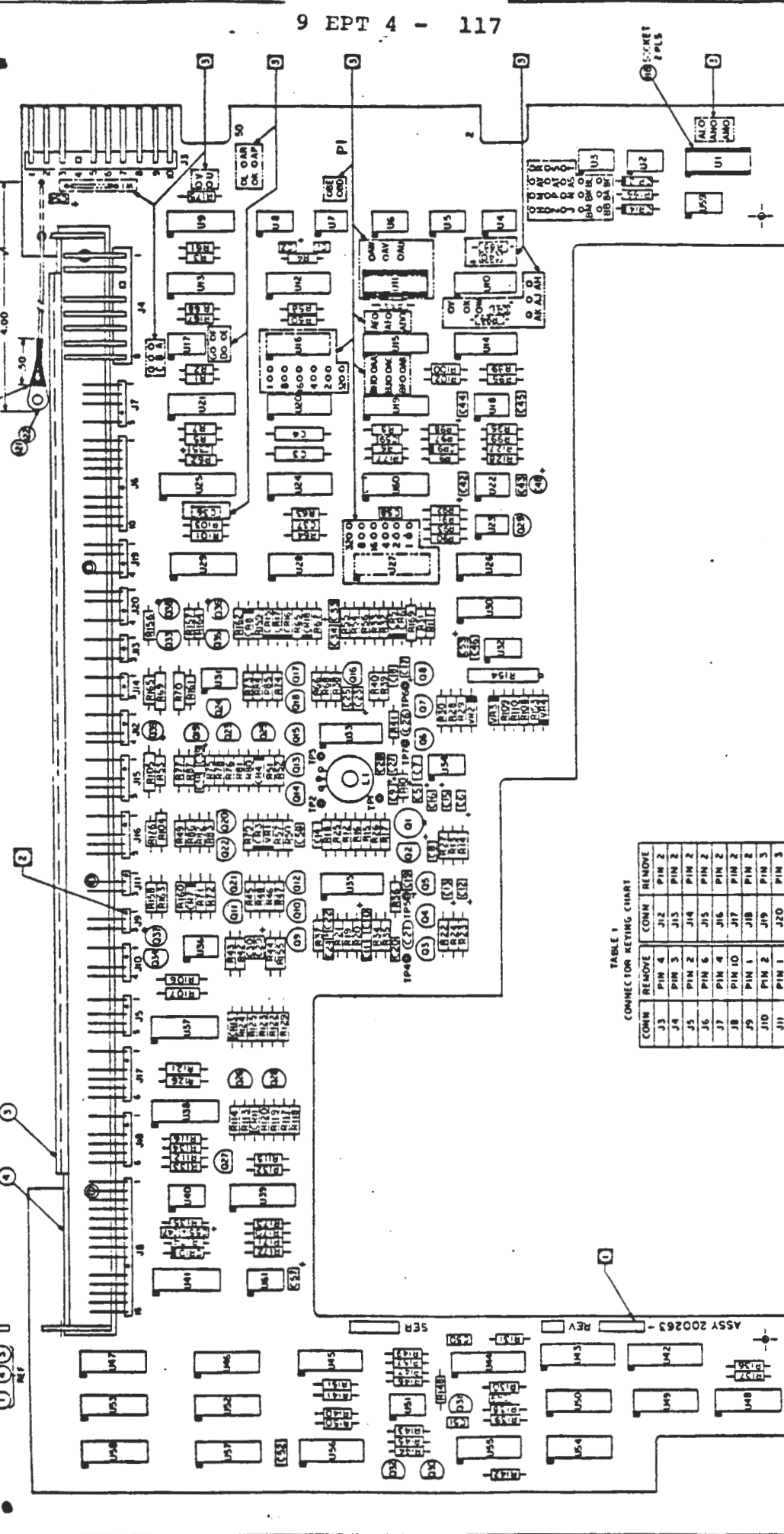
PerSci Documents, Drives to Serial No. 10,000

PerSci DRIVE-ASSEMBLY DRAWINGS
(Supplement P/N 733012)

CONTENTS

Assembly, Data and Interface PCB
Assembly, Positioner Servo
Assembly, Spindle Servo
Assembly, Phased Locked Double F Data Separator
Assembly, Lamp Amplifier PCB
Assembly, Dual Diskette Drive
Assembly, Center and Upper Deck
Assembly, Positioner
Assembly, Eject & Carrier
PERSCI PARTS LIST (Supplement 733013)
PerSci Selected Parts
PerSci Material Lists

REV	DATE	APPR	DESCRIPTION
1	10/24/77
2	10/24/77
3	10/24/77
4	10/24/77
5	10/24/77
6	10/24/77
7	10/24/77
8	10/24/77
9	10/24/77
10	10/24/77



PERSCI, INC.

PERSCI

ASSEMBLY, PCB DATA & INTERFACE
MODEL 270 SCALE 1:1
SHEET 1 OF 1 4-70263

- 4. SCHEMATIC REF 200284
- 5. FOR VIA COMP. VALUES AND JUMPER LOCATIONS SEE TABULATED M.
- 6. REMOVE CONNECTOR PINS AS SPECIFIED ON TABLE 1, PRIOR TO CONNECTOR INSTALLATION.
- 7. MARK DASH VERSION, REVISION AND SERIAL NUMBER 12 HIGH. BLACK CHARACTERS IN AREA SHOWN, UNLESS OTHERWISE SPECIFIED.

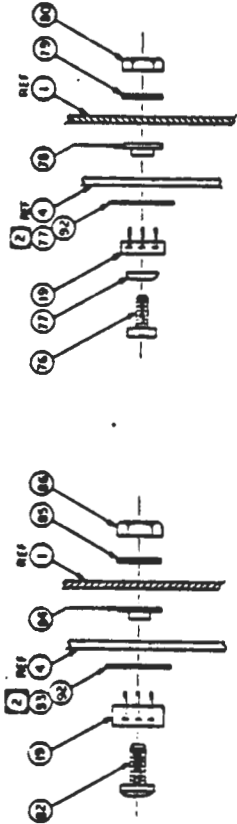
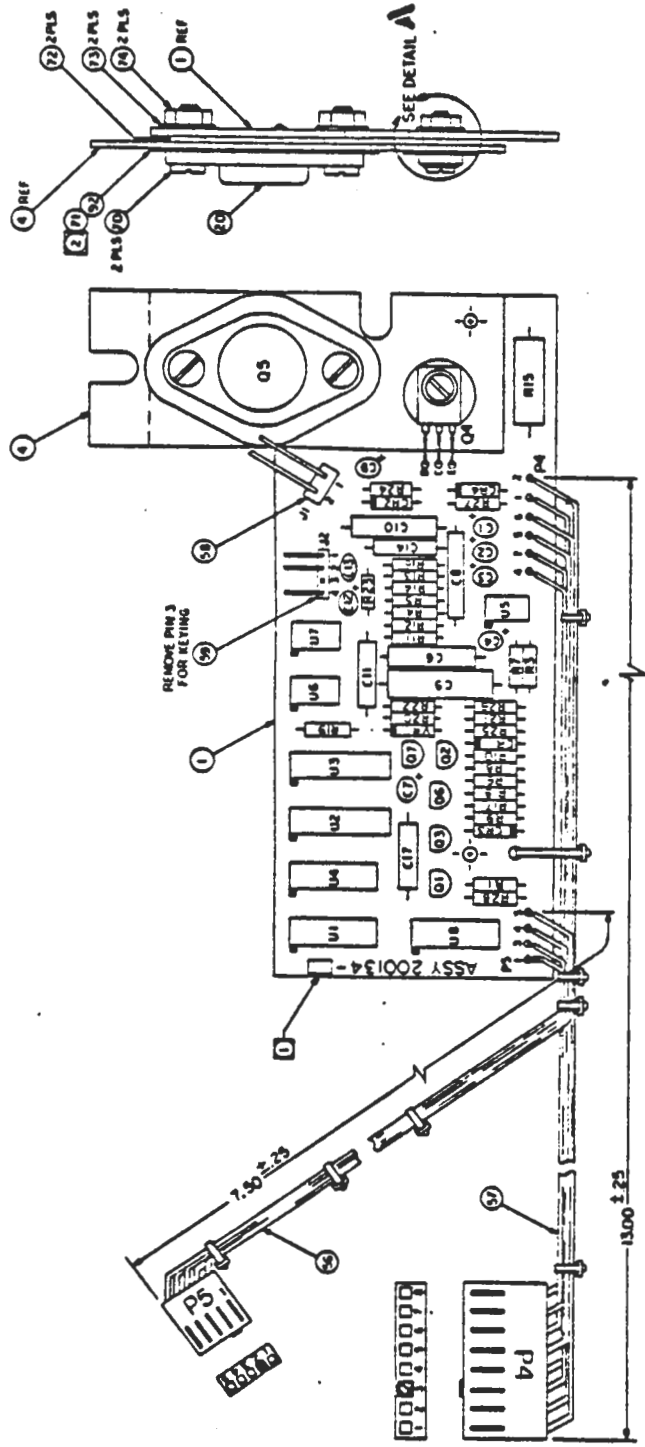
TABLE 1
CONNECTOR REWING CHART

CONN	REMOVE	CONN	REMOVE
J3	PIN 4	J12	PIN 2
J4	PIN 3	J13	PIN 2
J5	PIN 2	J14	PIN 2
J6	PIN 6	J15	PIN 2
J7	PIN 4	J16	PIN 2
J8	PIN 10	J17	PIN 2
J9	PIN 1	J18	PIN 2
J10	PIN 2	J19	PIN 3
J11	PIN 1	J20	PIN 3

ASSEMBLY, PCB DATA & INTERFACE
MODEL 270 SCALE 1:1
SHEET 1 OF 1 4-70263

REV	DESCRIPTIONS
1	INITIAL REV
2	REVISED DRAWING NEW LAYOUT
3	REVISED DRAWING NEW LAYOUT
4	REVISED DRAWING NEW LAYOUT
5	REVISED DRAWING NEW LAYOUT
6	REVISED DRAWING NEW LAYOUT
7	REVISED DRAWING NEW LAYOUT
8	REVISED DRAWING NEW LAYOUT
9	REVISED DRAWING NEW LAYOUT
10	REVISED DRAWING NEW LAYOUT

9 EPT 4 - 119



3 SCHEMATIC REF 200133.
 2 APPLY SILICON GREASE ON BOTH SIDES OF MICA INSULATOR.
 1 MARK REVISION LEVELS 12 HIGH WHITE CHARACTERS IN APPROX AREA SHOWN UNLESS OTHERWISE SPECIFIED:

PERSCI, INC.

PERASSY 200227

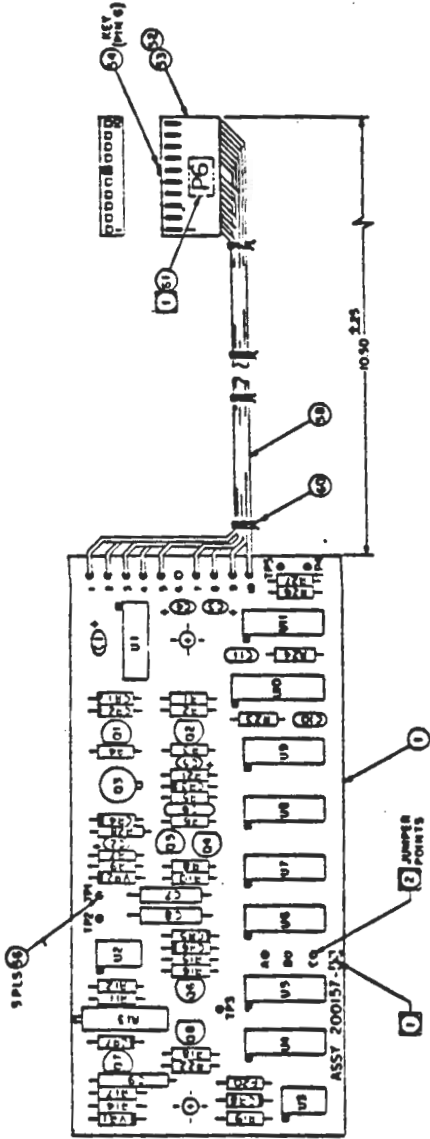
ASSEMBLY PCB, SPINDLE SERVO

MODEL 270/277 PART 1 200134F

3

1	ASSEMBLY DRAWING	REV. 1	DATE: 1/1/74
2	ASSEMBLY	REV. 1	DATE: 1/1/74

9 EPT 4 - 120



3. SCHEMATIC REF 200115.
 ① FOR JUMPER LOCATIONS SEE W/L DASH VERSIONS
 ② MARK REF. DESIGNATIONS ON REVISION LEVEL
 ③ 12 MICH BLACK/WHITE CHARACTERS IN APPROPRIATE AREA SHOWN.
 UNLESS OTHERWISE SPECIFIED:

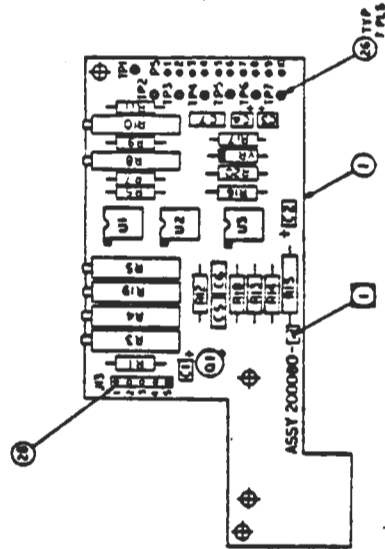
PERSCI, INC.

ASSY. PCB, PHASED LOGIC, E F

MODEL 270272

REV. 1.1 2-0157 C

REV	REVISIONS
A	ENGINE BELL
B	ASSEMBLY
C	ECO 7
D	ECO 62 MFG BELL
E	ECO 76
F	ECO 88



2 SCHEMATIC REF 200096

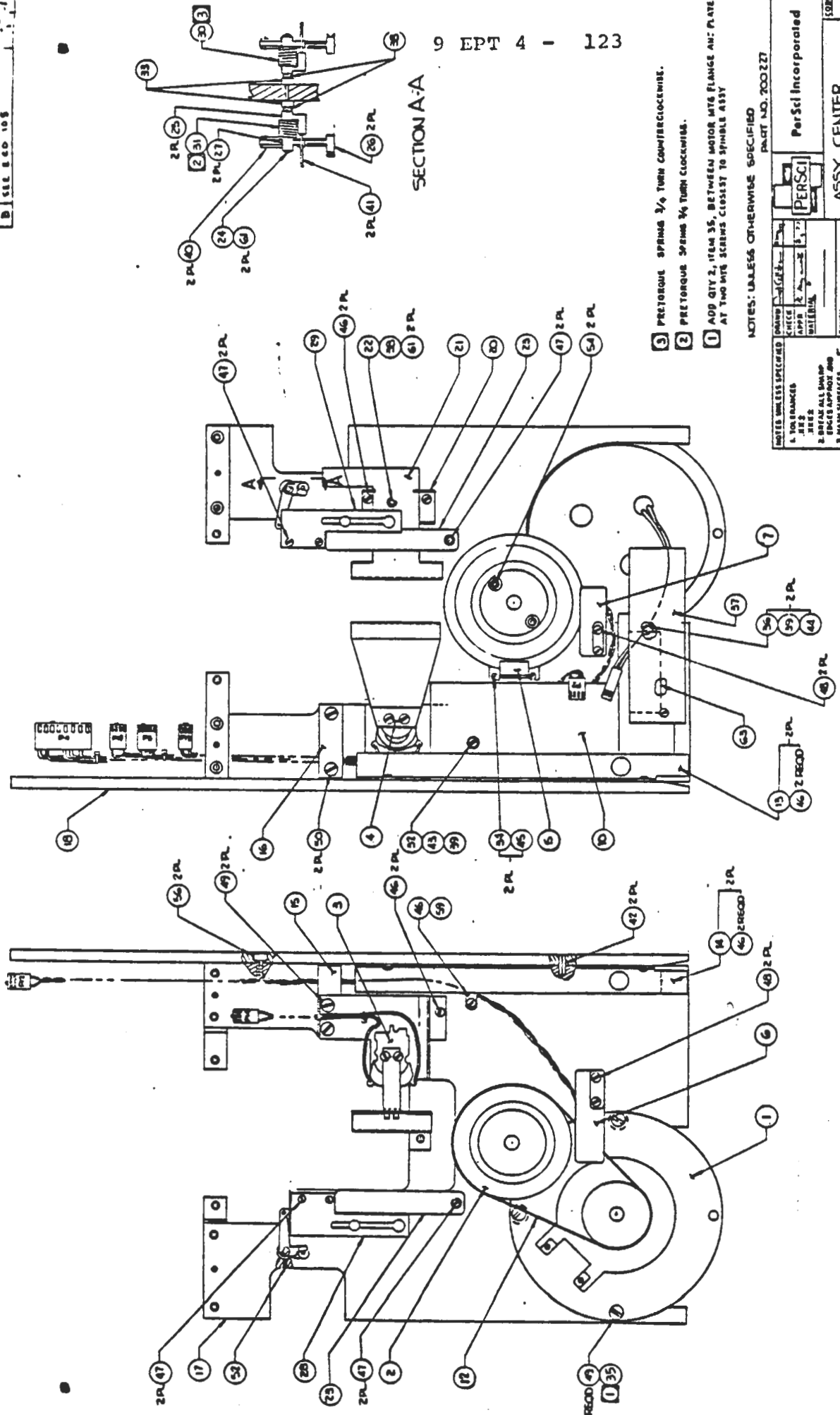
1 MARK REF DESIGNATIONS OR REVISION LEVEL
 .12 INCH BLACK/WHITE CHARACTERS IN APPOSITE
 AREA SHOWN.
 UNLESS OTHERWISE SPECIFIED:

PERSCI, INC.	
PERSCI	
PER ASSY	
- 200079	
ASSEMBLY PCB LAMP AMPLIFIER	
MODEL 70270277	SCALE 1:1
	SHEET NO 3
	20-0801E

REV	DESCRIPTION	DATE
A	EXCISE RELEASE	10/11/51
B	SEE E.C.D. 105	

9 EPT 4 - 123

SECTION A-A

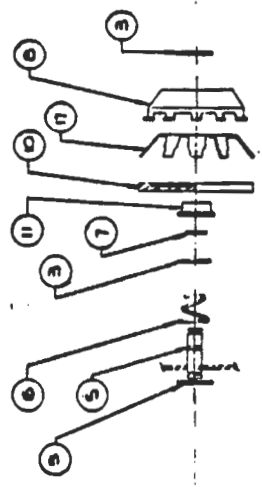
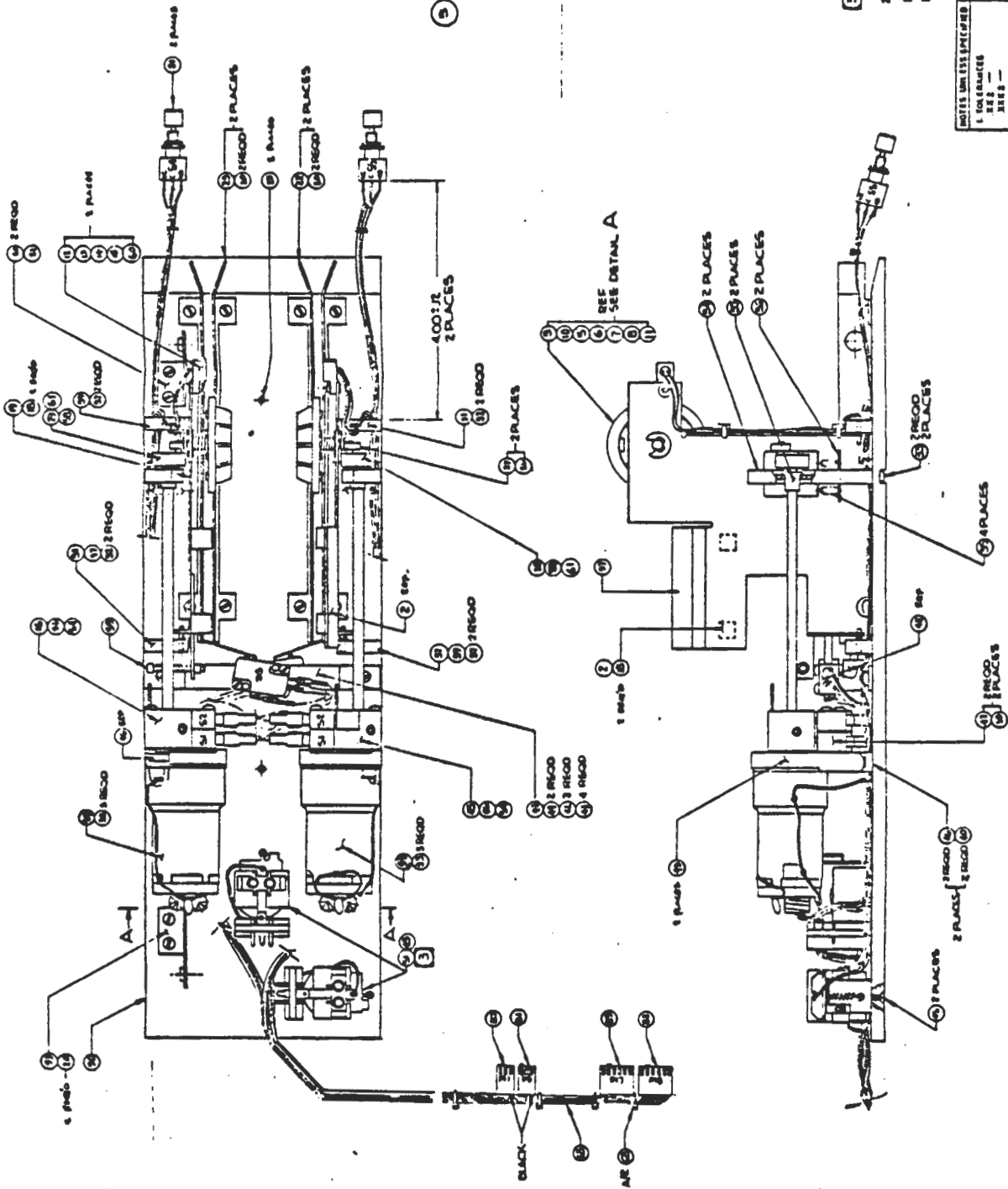


- 1 PRETORQUE SPRING 3/4 TURN COUNTERCLOCKWISE.
- 2 PRETORQUE SPRING 3/4 TURN CLOCKWISE.
- 3 ADD QTY 2, ITEM 35, BETWEEN MOTOR M76 FLANGE AND PLATE AT TWO M76 SCREWS CLOSEST TO SPINDLE ASSY

NOTES: UNLESS OTHERWISE SPECIFIED
 PERSCIL PART NO. 700227

UNLESS OTHERWISE SPECIFIED	PERSCIL	PerSci Incorporated
1. FOR DIMENSIONS	SEE DRAWING	
2. ALL DIMENSIONS APPROXIMATE		
3. HOLE LOCATIONS APPROXIMATE		
4. ALL DIMENSIONS IN INCHES		
DATE	11/1/51	DATE
DESIGNED BY	217	DATE
HECKED BY	200151	DATE
PART NO. 700227		
ASSY. CENTER AND UPPERDECK		
WORK ORDER NO.	200227	
REV.	D	
REVISED BY		
REVISED DATE		
SHEET 1 OF 1		

REVISIONS		DATE	BY
A	EXASR RELEASE		
B	DEVISEL		
C	REC'D NO. 95		
D	SEE Ltr. 10.5		



- 1. THESE RELAYS ARE FOR REMOTE SELECT OPTIONS. SEE -005, -008 & -009 WIRE LISTS FOR QTY REQ.
 - 2. FOR SCHEMATIC SEE 200233, 200234 & 200243.
 - 3. FOR WIRE LIST SEE 200065.
- NOTES: UNLESS OTHERWISE SPECIFIED

PART NO 200219-10		PerSci Incorporated	
DESIGN	DATE	REV	QTY
CHECKED	APPROVED	DATE	
MATERIALS		ASST. MGR. & CLERK	
FINISH		NO. OF PLACES	1
MATERIAL		NO. OF PLACES	1
FINISH		NO. OF PLACES	1
MATERIAL		NO. OF PLACES	1
FINISH		NO. OF PLACES	1

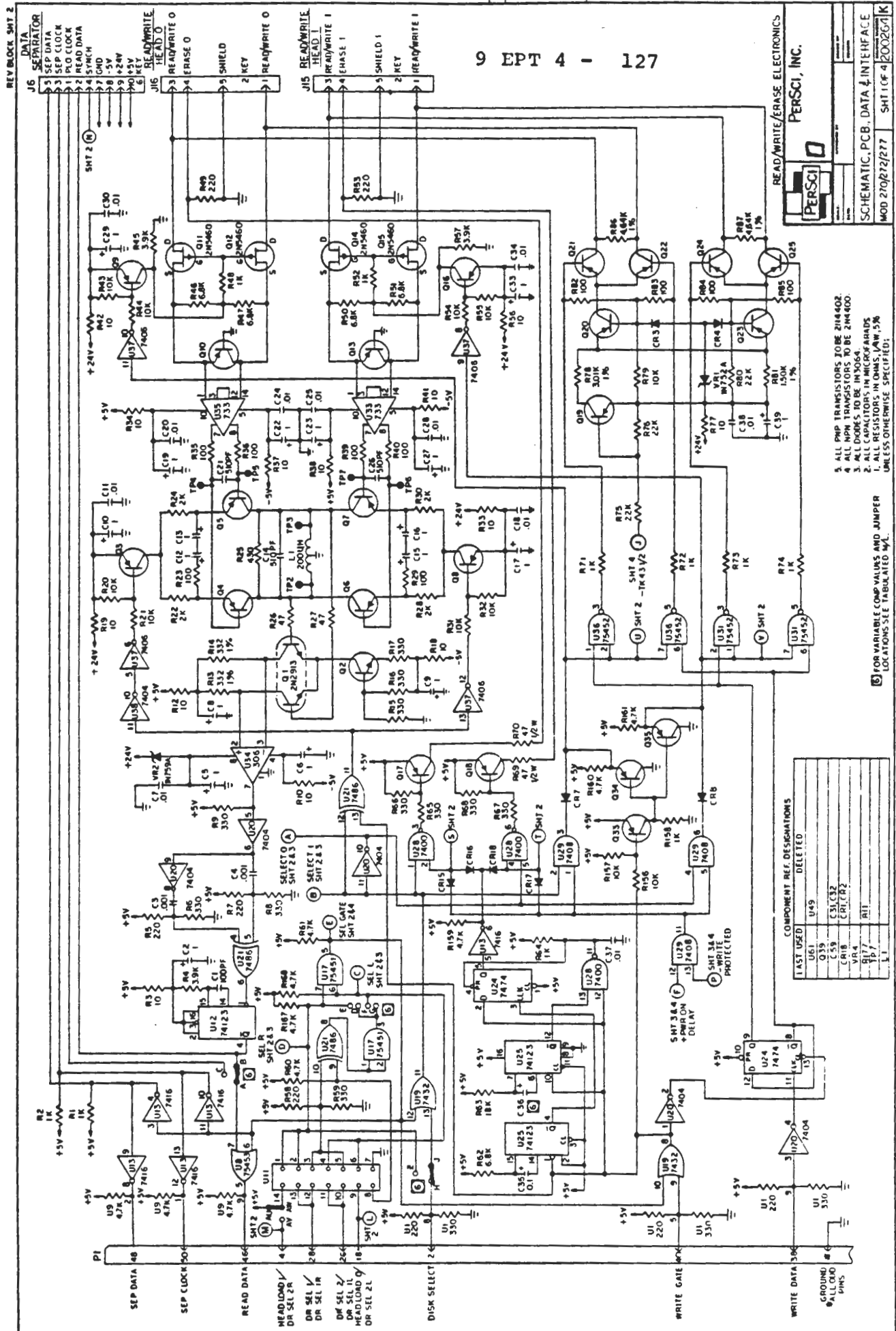
PerSci Diskette Drive Schematics
(Supplement 733011)

There are three sets of schematics in this section. Each set corresponds to drives within a given series of serial numbers:

- 5000 to 10,000
- 2500 to 5,000
- Prior to 2,500

Schematic, Data and Interface PCB, Sheet 1 of 4
Sheet 2 of 4
Sheet 3 of 4
Sheet 4 of 4

- Schematic, Positioner Servo PCB
- Schematic, Spindle Servo PCB
- Schematic, Phase Locked Double F Data Separator
- Schematic, Lamp Amplifier PCB
- Schematic, LED Assembly, Side 0
- Schematic, LED Assembly, Side 1
- Schematic, Phototransistor Assembly, Side 0
- Schematic, Phototransistor Assembly, Side 1
- Schematic, Spindle Motor Assembly
- Schematic, Eject Motor Assembly
- Schematic, Head Load Assembly, Side 0
- Schematic, Head Load Assembly, Side 1
- Schematic, Positioner Motor
- Schematic, Read/Write Head Assembly, Side 0
- Schematic, Read/Write Head Assembly, Side 1



REV BLOCK SMT 2

DATA SEPARATOR

SEP DATA
SEP CLOCK
PLO CLOCK
READ DATA
SYNCH
IGND
+5V
+24V
+24V
+24V

J15 HEADWRITE HEAD 0
3 READWRITE 0
4 ERASE 0
5 SHIELD
2 KEY
1 HEADWRITE 0

J15 HEADWRITE HEAD 1
3 READWRITE 1
4 ERASE 1
5 SHIELD
2 KEY
1 HEADWRITE 1

READ/WRITE/ERASE ELECTRONICS

PERSCI, INC.

PERSCI

SCHEMATIC, PCB, DATA & INTERFACE

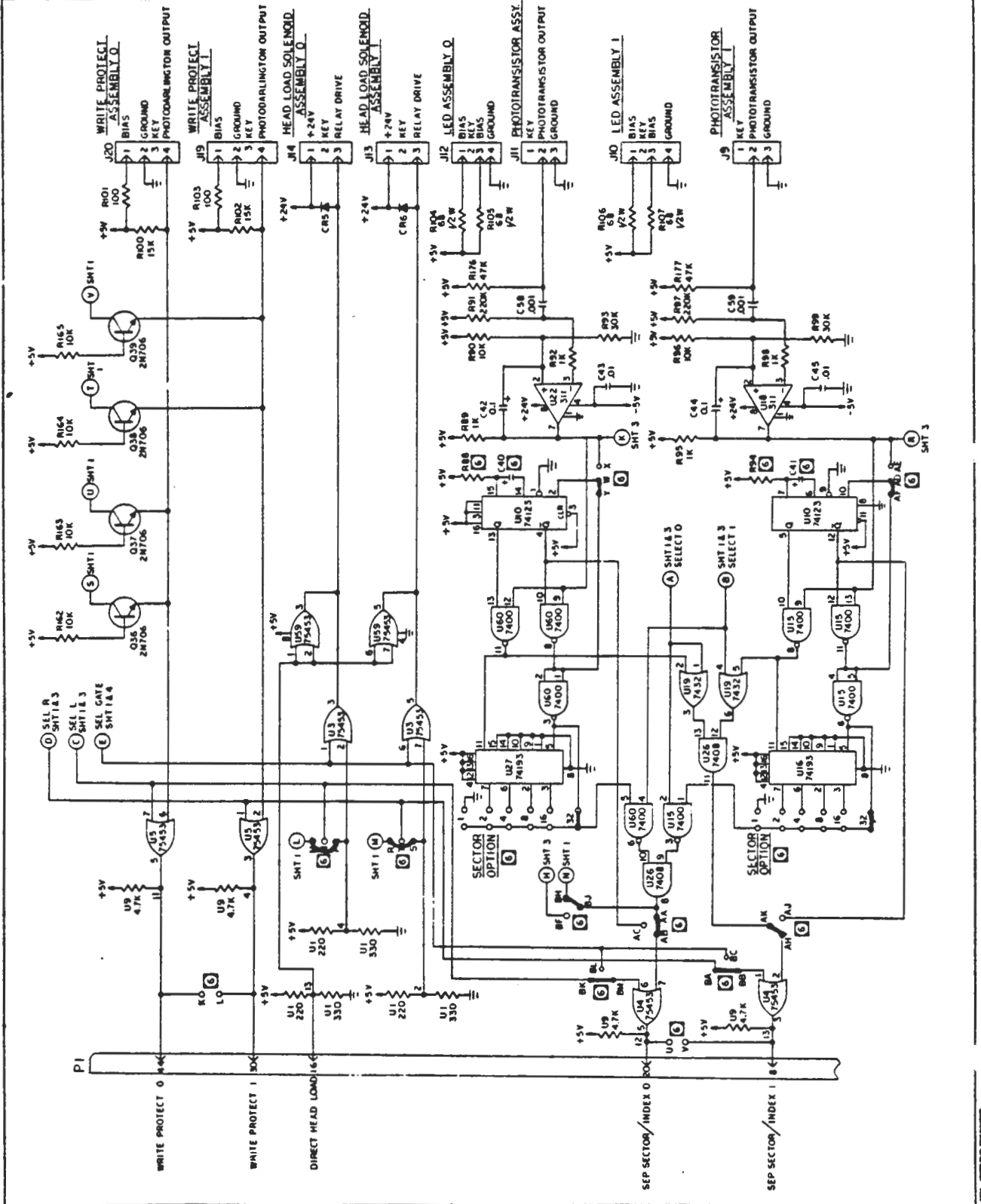
MOD 270727/277 SHT 1 OF 4 200264 K

1. ALL PNP TRANSISTORS TO BE 2N4402.
 2. ALL NPN TRANSISTORS TO BE 2N4400.
 3. ALL DIODES TO BE IN3064.
 4. ALL CAPACITORS IN MICROFARADS.
 5. ALL RESISTORS IN OHMS, μ M, OR K.
- UNLESS OTHERWISE SPECIFIED:

FOR VARIABLE COMP VALUES AND JUMPER LOCATIONS SEE TABULATED M.L.

COMPONENT REF. DESIGNATIONS	DELETED
U61	U49
Q39	Q39
C31, C32	C59
CR18, CR2	CR18, CR2
VR4	VR4
TP7	TP7
L1	L1

REV	DESCRIPTION	DATE	BY
A	MFG REL	1/75	
B	ECO #12	1/75	
C	ECO #13	1/75	
D	ECO #45	1/75	
E	ECO #57	1/75	
F	ECO #59	1/75	
G	ECO #134	1/75	
H	ECO #154	1/75	
J	ECO #156	1/75	
K	ECO #188	1/75	



WRITE PROTECT, H.LOAD, INDEX

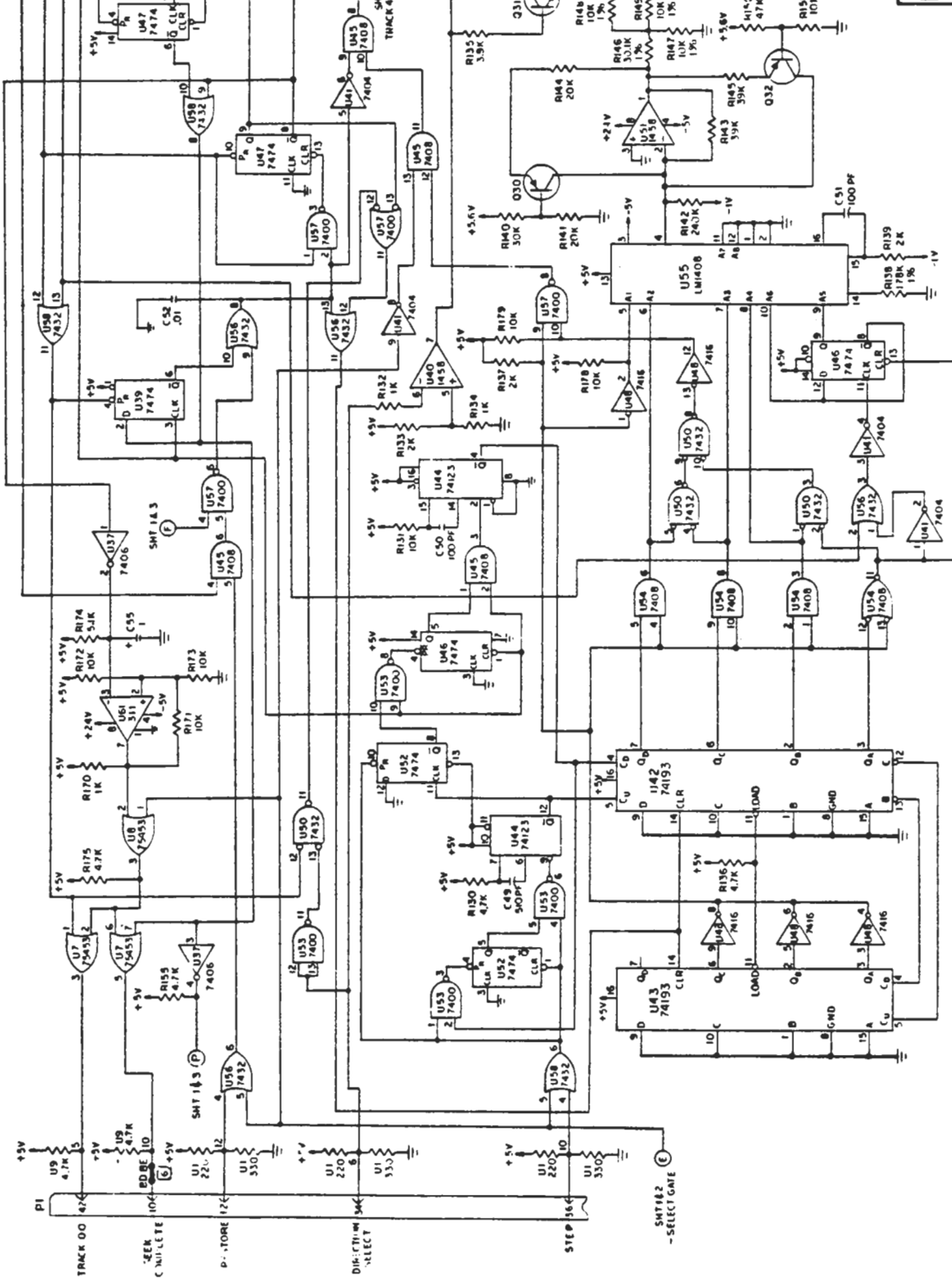
PERSCI, INC.



SCHEMATIC, PCB, DATA & INTERFACE
 MOO 27q/2/277 SMT 2 of 4 200264K

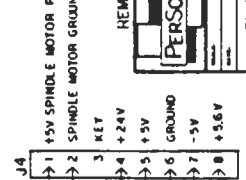
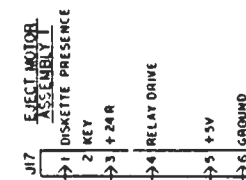
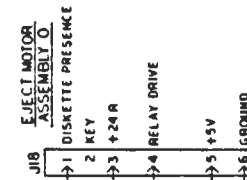
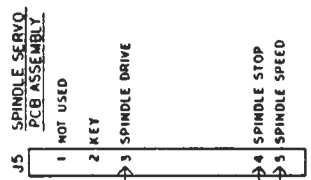
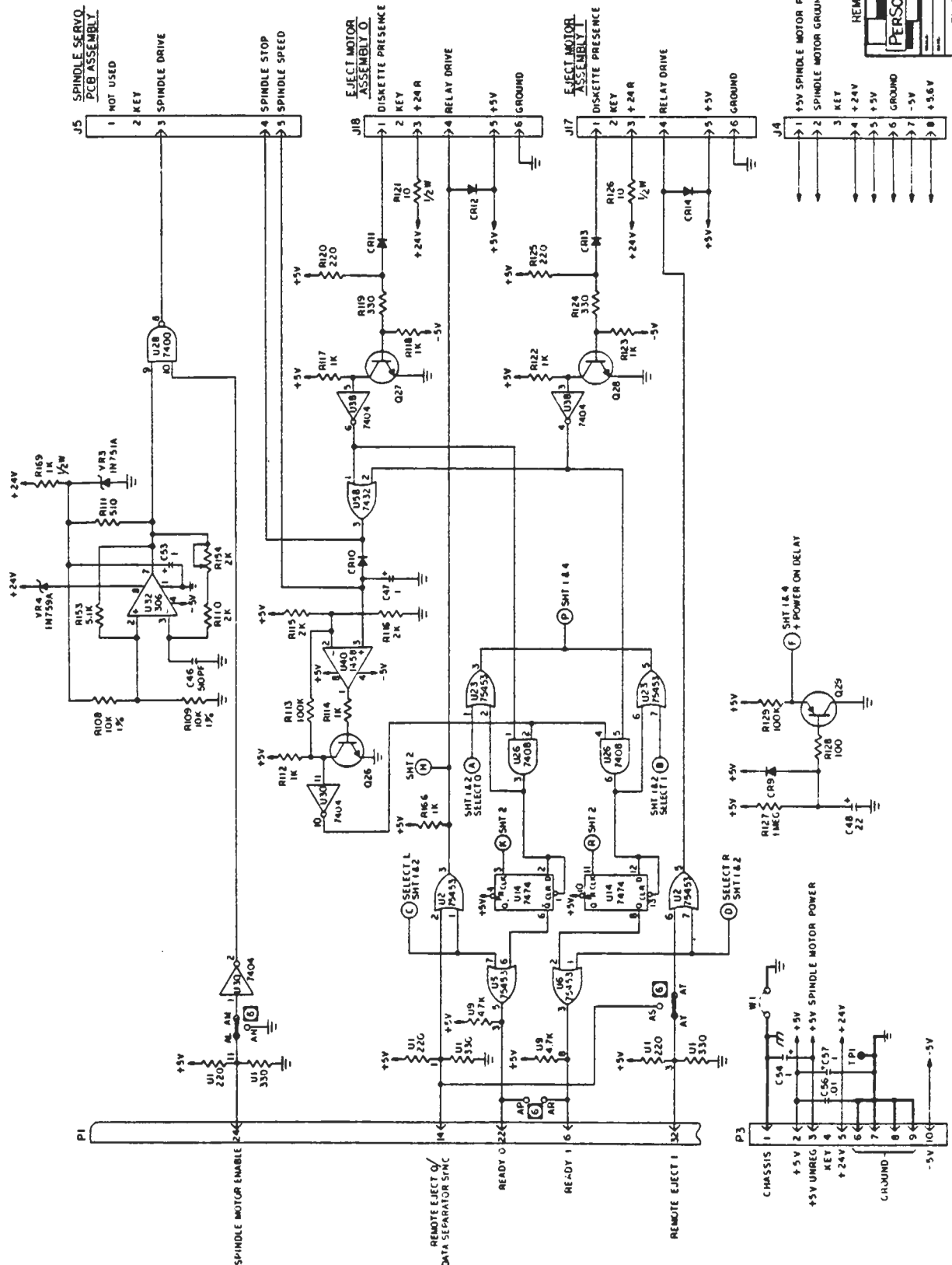
POSITIONER SERVO PCB ASSEMBLY

9 TRACK 00
3 HALF TRACKS
2 DETENT PULSES
2 SEEK COMPLETE
7 TRACKS
-1V
6 HOLD (H)
1 FIND TRACK 00(-)
5 FIND TRACK 00(H)
4 SEEK(H)
3 TRACK 43 1/2
+5.6V
11 DIRECTION
10 KEY
3 VELOCITY FUNCTION



POSITIONER CONTROL CIRCUITS

 SCHEMATIC PCB DATA INTERFACE
 MOD 270/272/277 SHT 4084 200261K



PERSCI, INC.

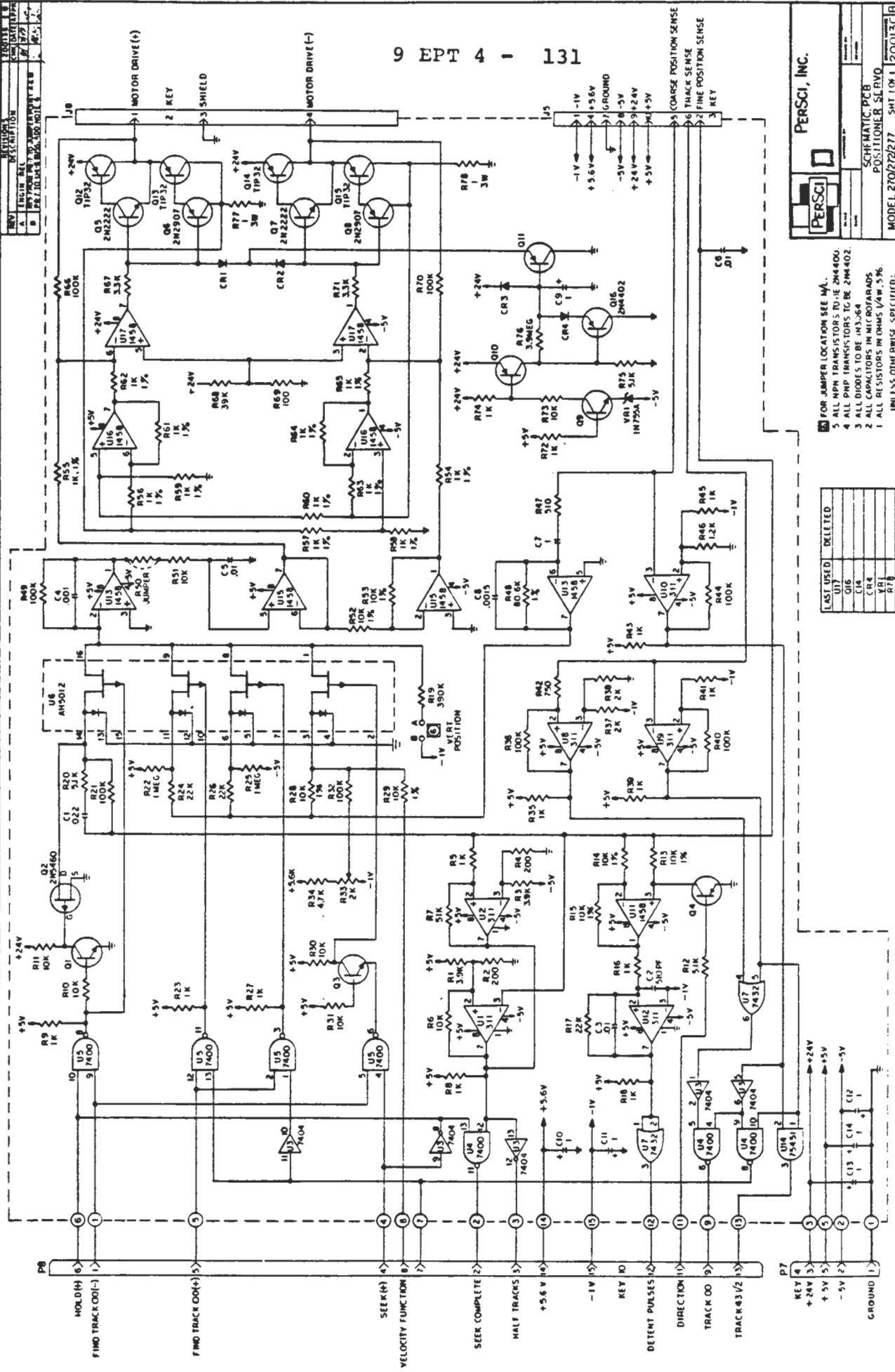
SCHEMATIC, PCB, DATA INTERFACE

MOD. 270/272/277

SHT 1 of 4

20026-1K

REV	DESCRIPTION	DATE	BY
A	REVISED TO ADD MOTOR DRIVE	11/77	...
B	REVISED TO ADD TRACK SENSE	11/77	...



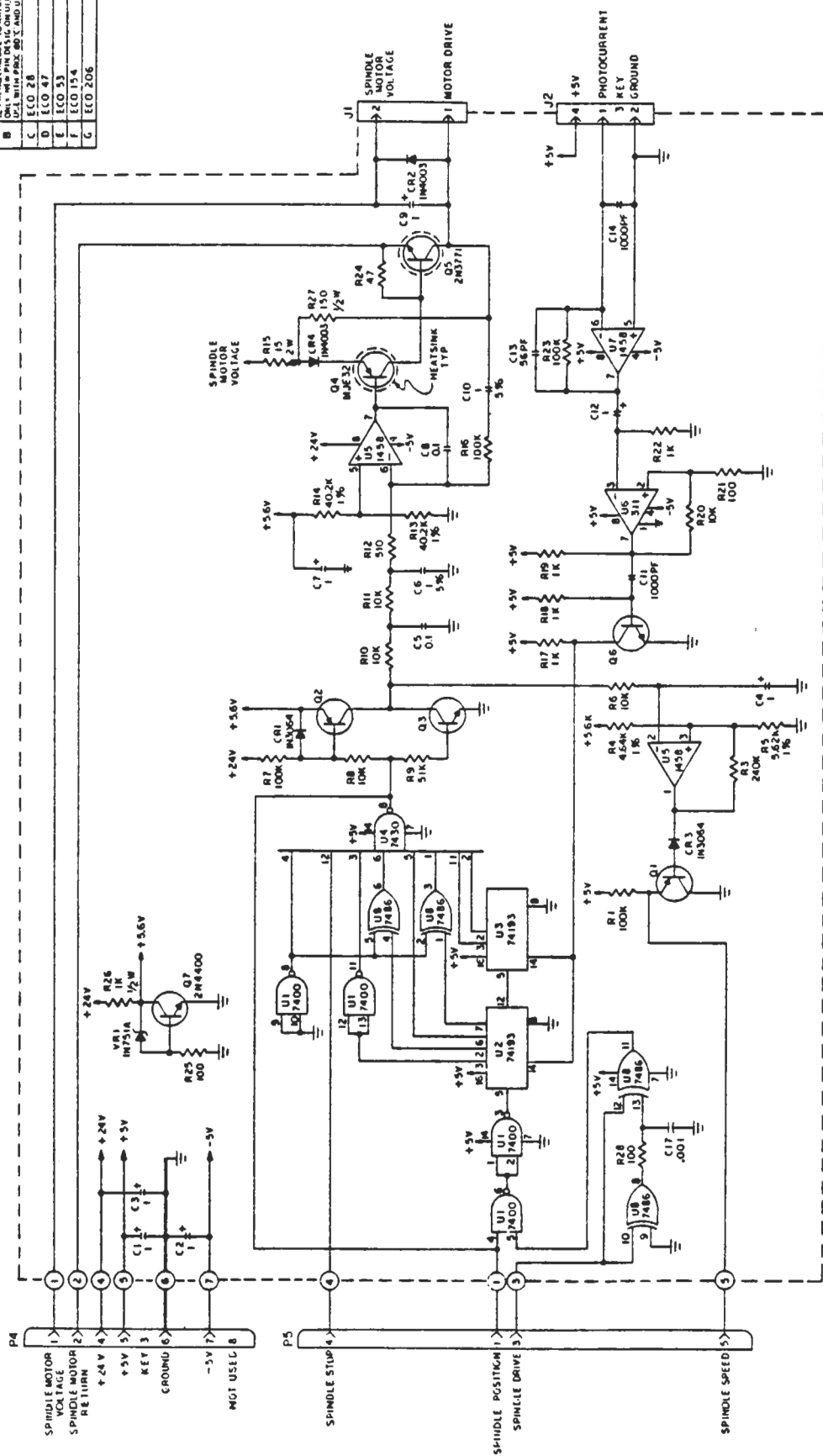
- FOR JUMPER LOCATION SEE M.A.
 5 ALL NPN TRANSISTORS TO BE 2N4400.
 4 ALL PNP TRANSISTORS TO BE 2N4402.
 3 ALL DIODES TO BE 1N4364.
 2 ALL CAPACITORS TO BE MICROFARADS
 1 ALL RESISTORS IN OHMS 1/4W .5%

LAST USED	DELETED
U17	
Q16	
C14	
CR4	
VR1	
R78	

PERSCI, INC.

SCHMATIC PCB
 POSITIONER SERVVO
 MODEL 27027277 SMT 10K 1 20013GB

REV	REVISIONS	DATE
A	ENGINE REL	200133 G
B	16 PIN MICRO TO APPROX 100 PIN DUAL IN LINE	
C	ECO 28	
D	ECO 47	
E	ECO 53	
F	ECO 154	
G	ECO 206	



REF DESIGNATIONS DELETED

U1	U7
U2	U8
U3	U9
U4	U10
U5	U11
U6	U12
U7	U13
U8	U14
U9	U15
U10	U16
U11	U17
U12	U18
U13	U19
U14	U20
U15	U21
U16	U22
U17	U23
U18	U24
U19	U25
U20	U26
U21	U27
U22	U28
U23	U29
U24	U30
U25	U31
U26	U32
U27	U33
U28	U34
U29	U35
U30	U36
U31	U37
U32	U38
U33	U39
U34	U40
U35	U41
U36	U42
U37	U43
U38	U44
U39	U45
U40	U46
U41	U47
U42	U48
U43	U49
U44	U50
U45	U51
U46	U52
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U80	U86
U81	U87
U82	U88
U83	U89
U84	U90
U85	U91
U86	U92
U87	U93
U88	U94
U89	U95
U90	U96
U91	U97
U92	U98
U93	U99
U94	U100

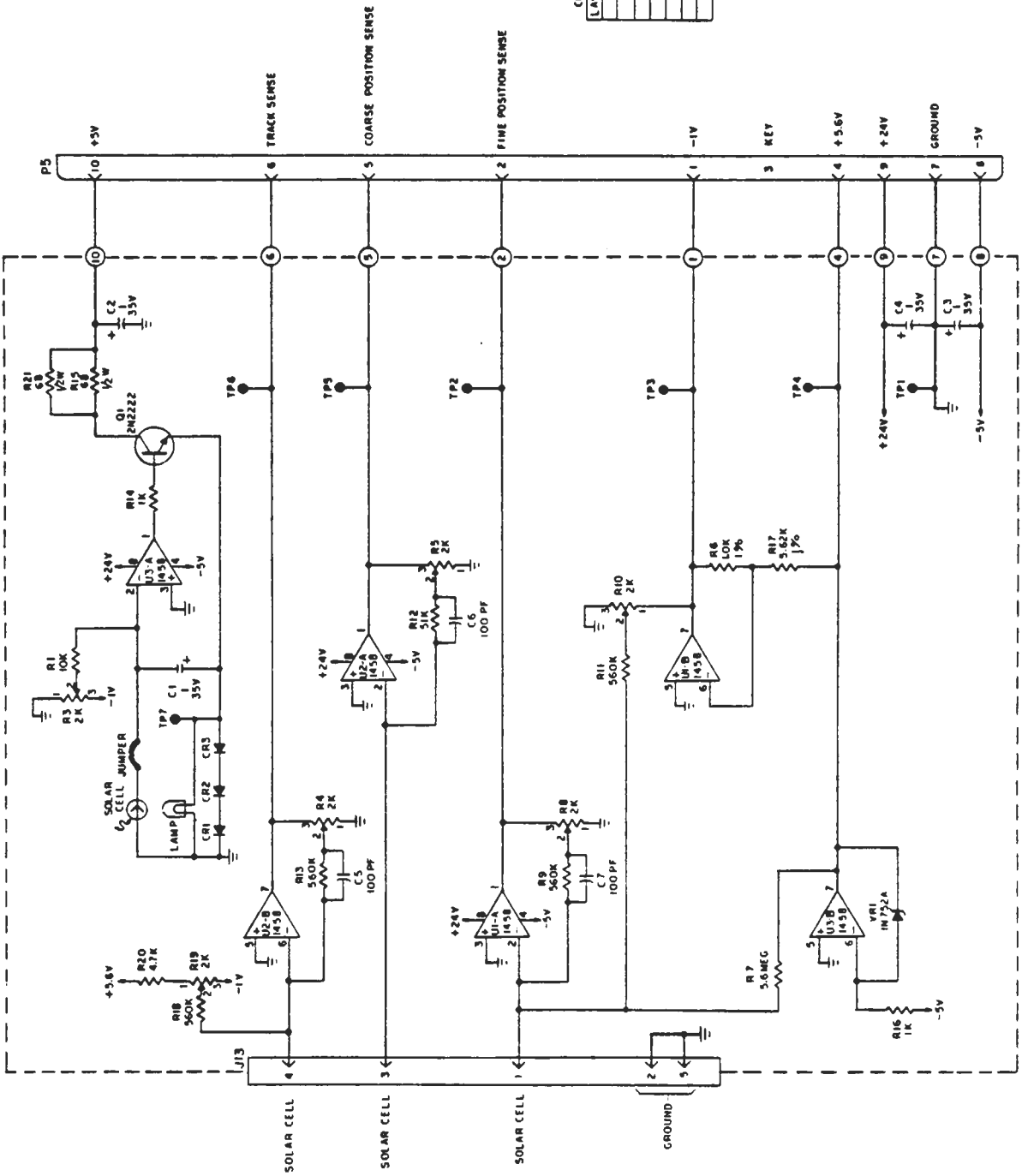
- 4 ALL PNP TRANSISTORS TO BE 2N4402
 - 3 ALL NPN TRANSISTORS TO BE 2N4400
 - 2 ALL CAPACITOR VALUES IN MICROFARADS
 - 1 ALL RESISTOR VALUES IN OHMS, 1/4W, 5%
- UNLESS OTHERWISE SPECIFIED:

PERSCI, INC.

SCHEMATIC, PCB, SPINDLE SERVO


MOD 270/272/277 SW 1 OF 1 200133 G

REV	REVISIONS	DATE	BY
A	ENGINE REL		
B	ADD R14, R19, R20		
C	ECO 63 MFG REL		
D	SEE ECO 77		
E	ECO 119		



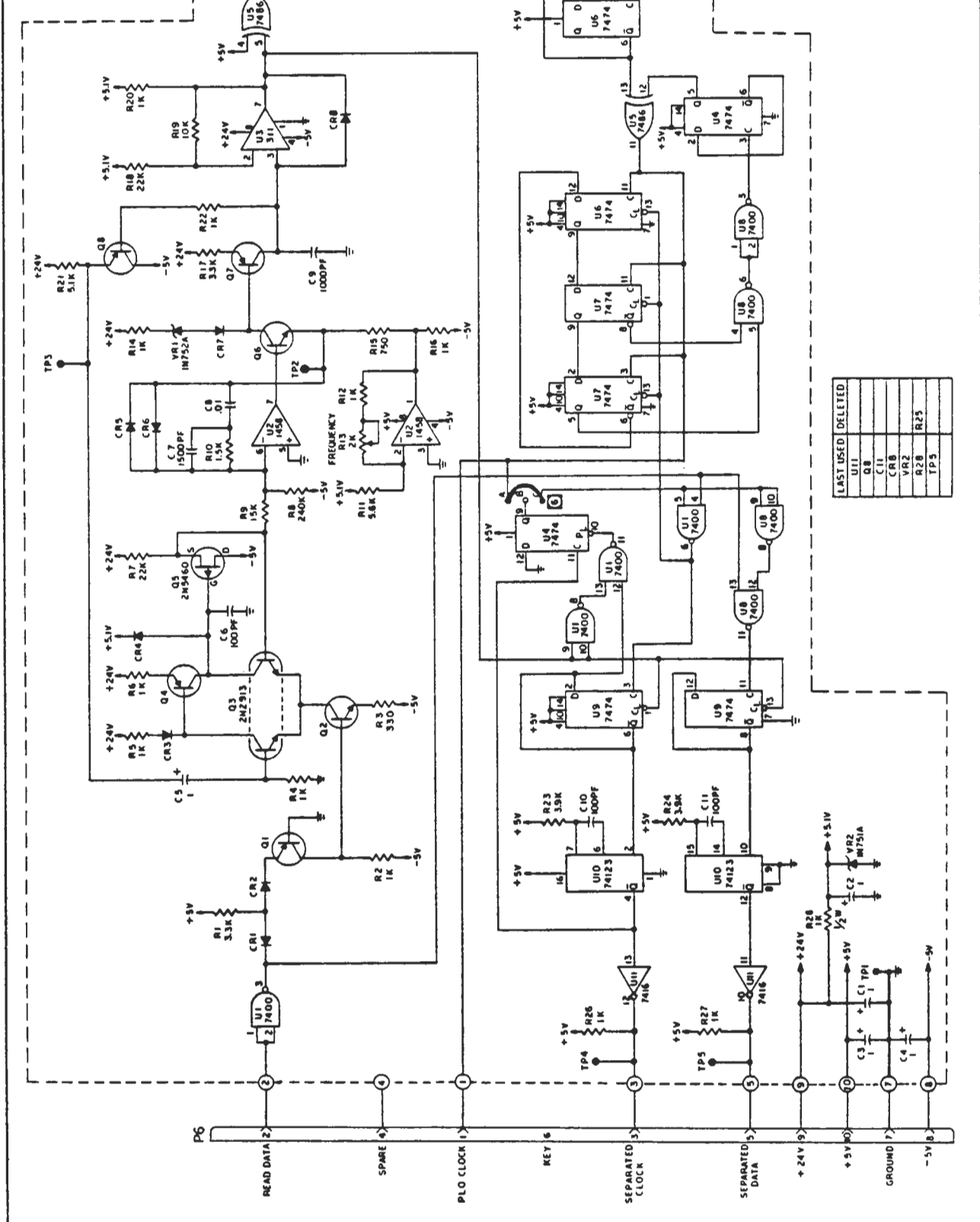
COMP REF DESIGNATIONS	LAST USED	DELETED
U3		
Q1		
CR3		
C7		
R21		R2
TP7		
VRI		

3 ALL DIMOS TO BE M4003.
 2 ALL CAPACITOR VALUES IN MICROFARADS.
 1 ALL RESISTOR VALUES IN OHMS, 1/4W, 5%
 UNLESS OTHERWISE SPECIFIED;

PERSCI  **PERSCI, INC.**

SCHEMATIC, PCB, LAMP AMPLIFIER
 MOD 270/272/277 SHT 10/1 200096

REV	DESCRIPTIONS	DATE	BY
A	ENGINE REL	7-1-74	J
B	AND ORIGINAL APPROVALS	7-1-74	J
C	AND ORIGINAL APPROVALS	7-1-74	J

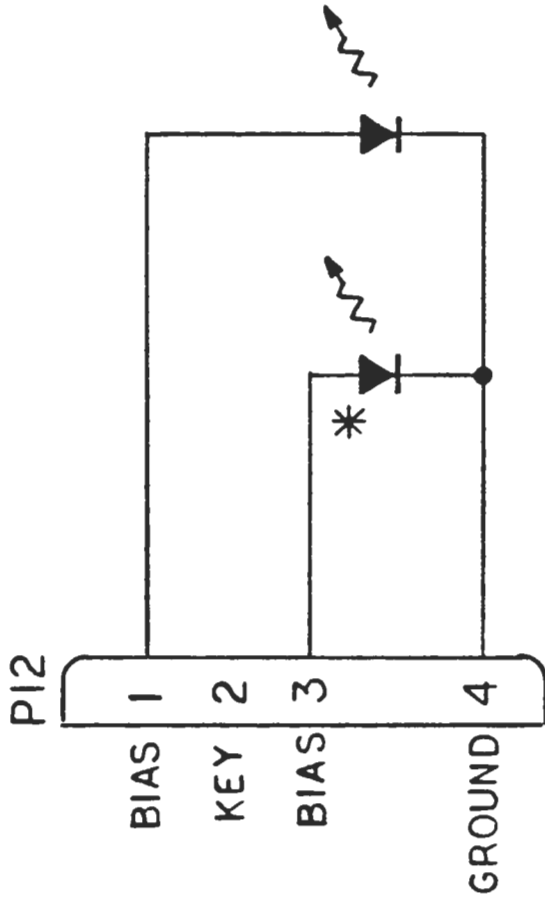


- FOR JUMPER LOCATIONS SEE TABULATED #1
 5 ALL PNP TRANSISTORS TO BE 2N4402.
 4 ALL NPN TRANSISTORS TO BE 2N4400.
 3 ALL DIODES TO BE 1N3064
 2 ALL CAPACITORS IN MICROFARADS
 1 ALL RESISTORS IN OHMS Ω W. 5%
 UNLESS OTHERWISE SPECIFIED:

LAST USED DELETED	
U11	
Q8	
C11	
VR2	
CR8	
R28	
R25	
TP5	



SCHEMATIC	PHASE LOCKED DOUBLE F DATA SEPARATOR
MOD 270/272/277	SMT 1 OF 1 200115 C



* NOTE
 SECOND LED OPTIONAL FOR
 DUAL INDEX OPTION DRIVE.



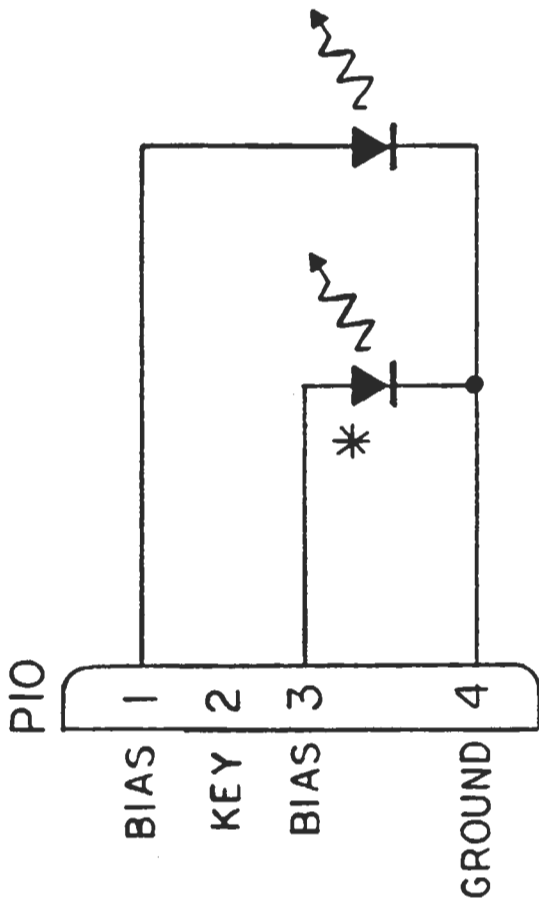
PERSCI, INC.

SCHEMATIC
 LED ASSEMBLY
 SIDE 0

270/272/277 SHT10F1

200241 B

9 EPT 4 - 136



* NOTE;
 SECOND LED OPTIONAL FOR
 DUAL INDEX OPTION DRIVE.



PERSCI, INC.

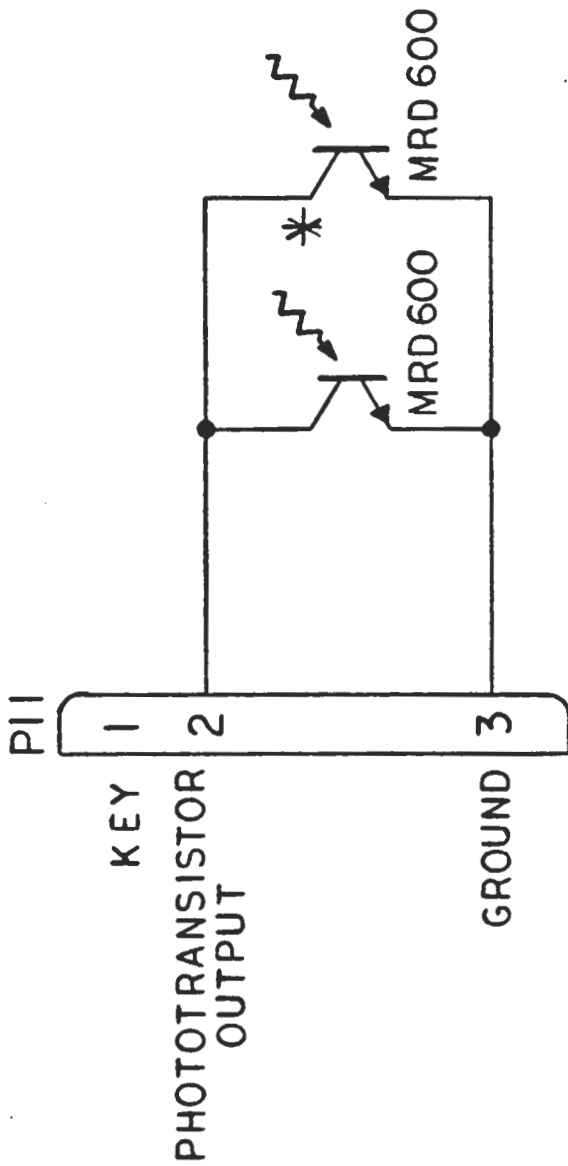
SCHEMATIC
 LED ASSEMBLY
 SIDE 1

27C 72/277

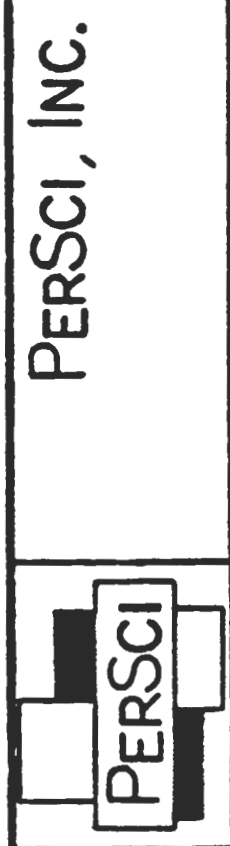
SHT10CF1

20024C

B



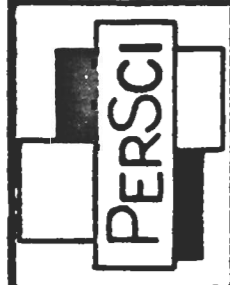
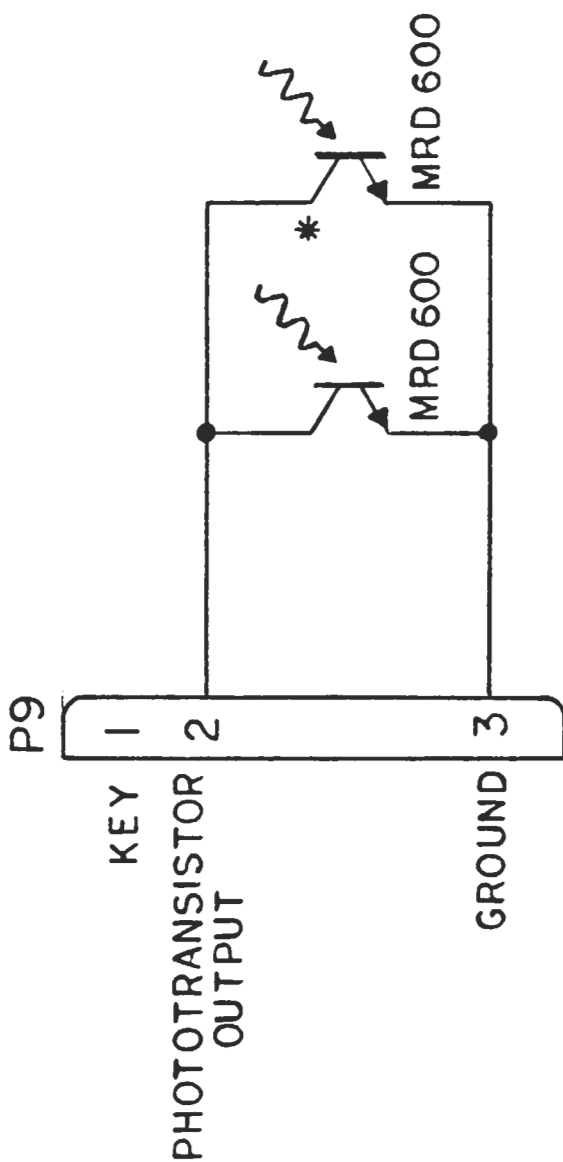
* NOTE
 SECOND PHOTOTRANSISTOR
 OPTIONAL FOR DUAL INDEX
 OPTION.



PERSCI, INC.

SCHEMATIC
 PHOTOTRANSISTOR ASSEMBLY
 SIDE Ø

270/272/277 SHT 1 OF 1 200234 B



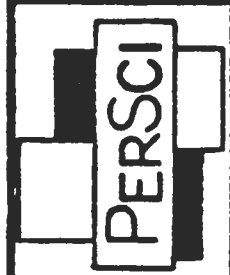
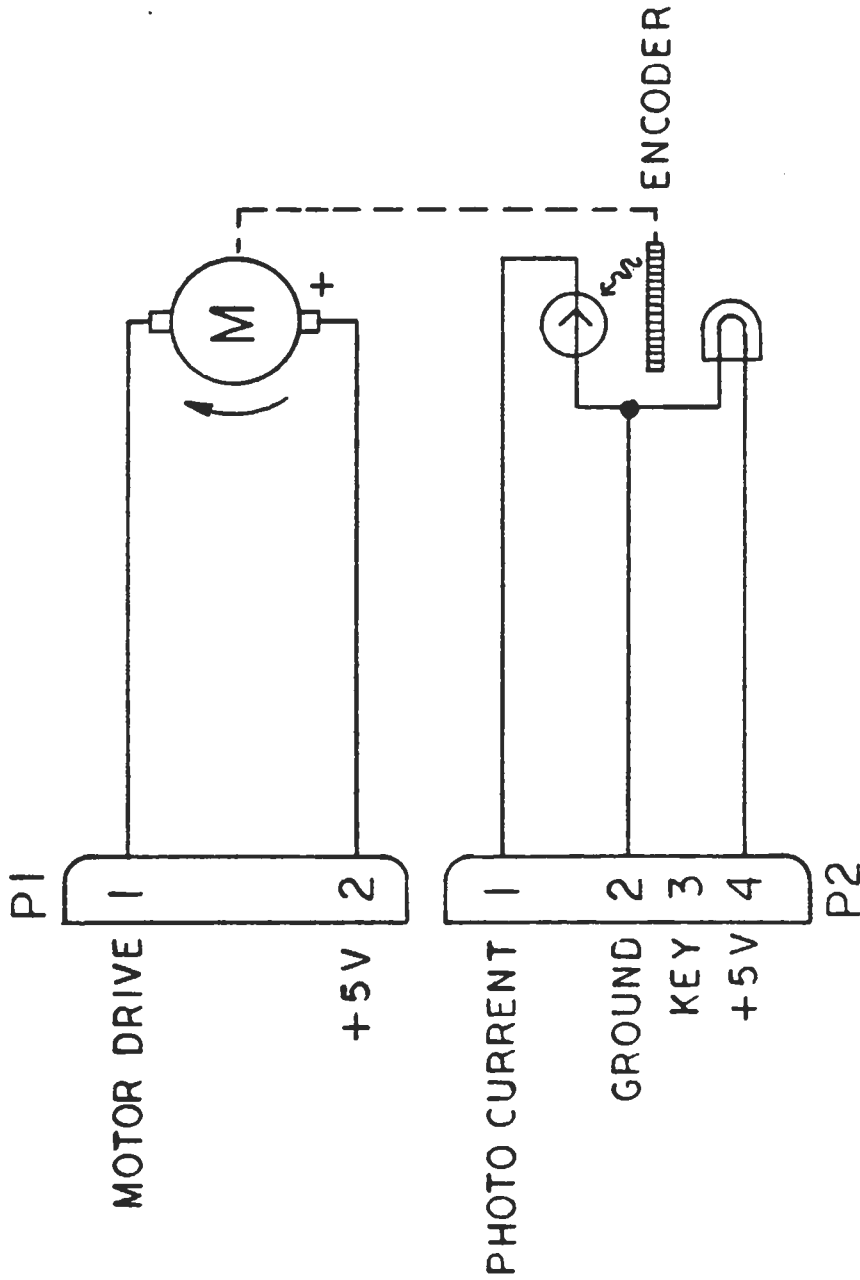
PERSCI, INC.

SCHEMATIC
PHOTOTRANSISTOR ASSEMBLY
SIDE 1

NOTE
SECOND PHOTOTRANSISTOR
OPTIONAL FOR DUAL INDEX
OPTION.

27C '272/277 SHT 10F1

200233 B



PERSCI, INC.

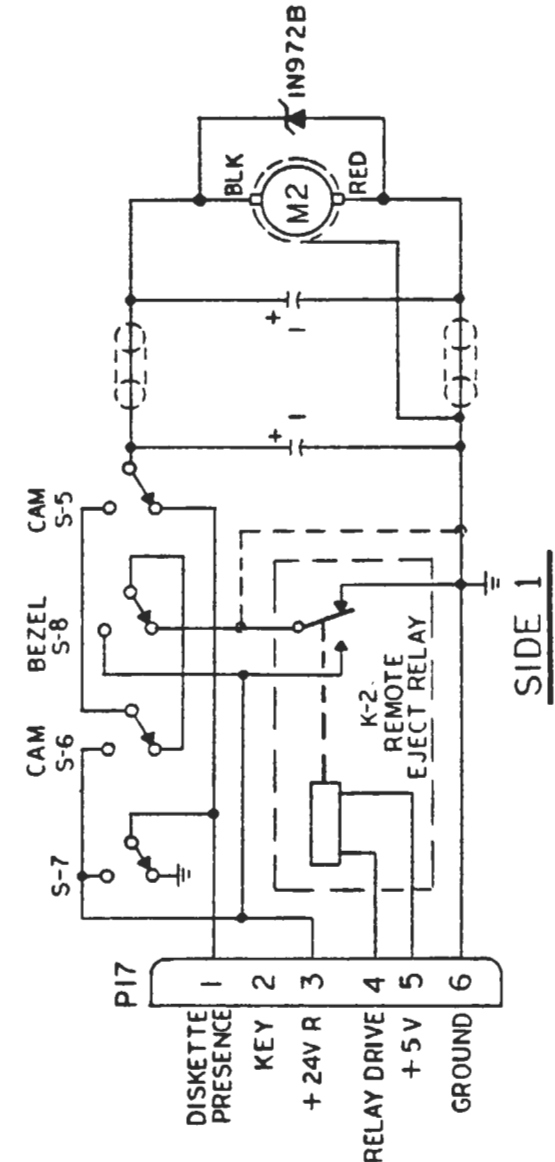
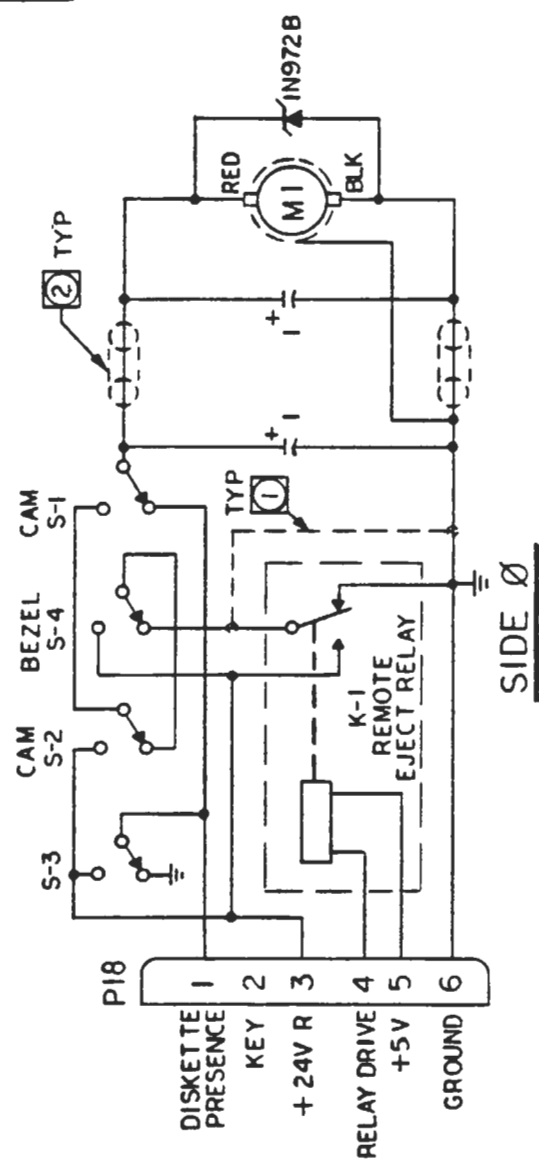
SCHEMATIC
SPINDLE MOTOR ASSEMBLY

270/272/277 SHT 1 OF 1


200239

A

REVISIONS		200243	B
REV.	DESCRIPTION	CHK.	DATE
A	MFG RELEASE	[Signature]	1/1/74
B	ECO 109	[Signature]	1/1/74



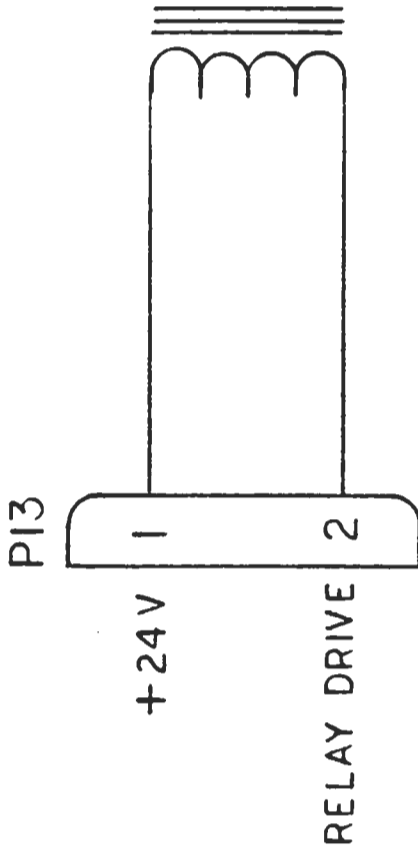
- NOTES:
- ③ ALL SWITCHES SHOWN NORMALLY CLOSED.
 - ② FERRITE BEAD PERSCI 100031.
 - ① OPTIONAL WIRING WITHOUT RELAY.



PERSCI, INC.

SCHEMATIC
EJECT MOTOR ASSEMBLY

270/272/277 SHT 10F1 200243 B



PERSCI, INC.



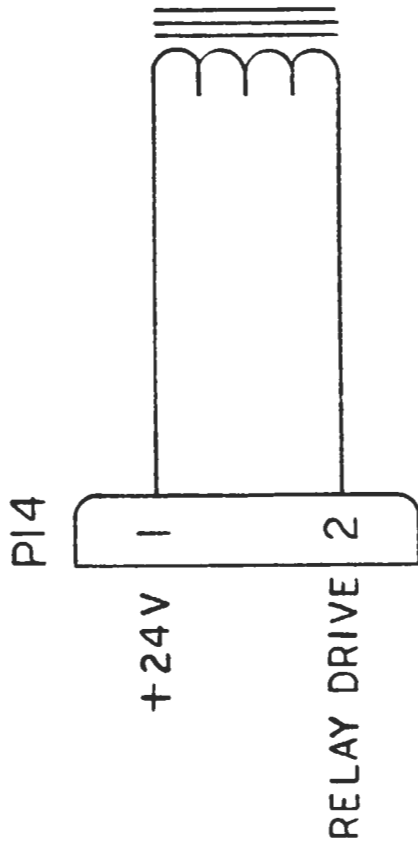
SCHEMATIC
HEAD LOAD ASSEMBLY
SIDE 1

270/272/277

SHT 1 OF 1

200238

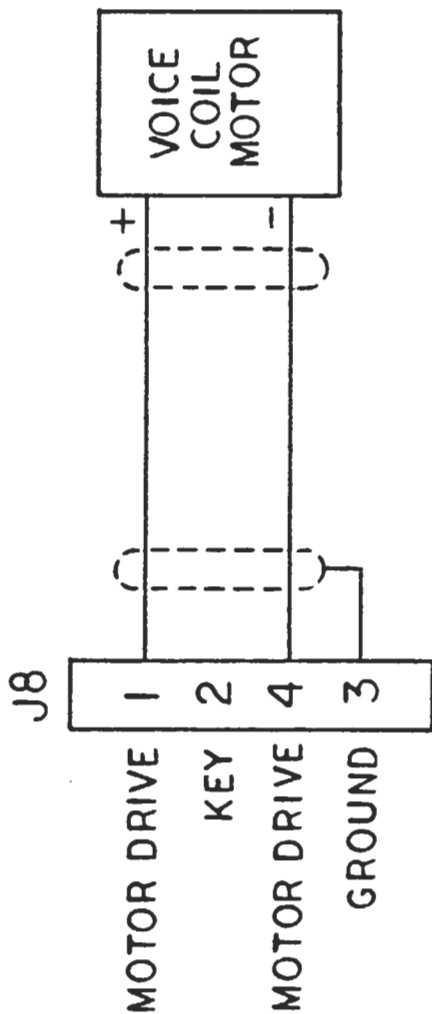
A



PERSCI, INC.

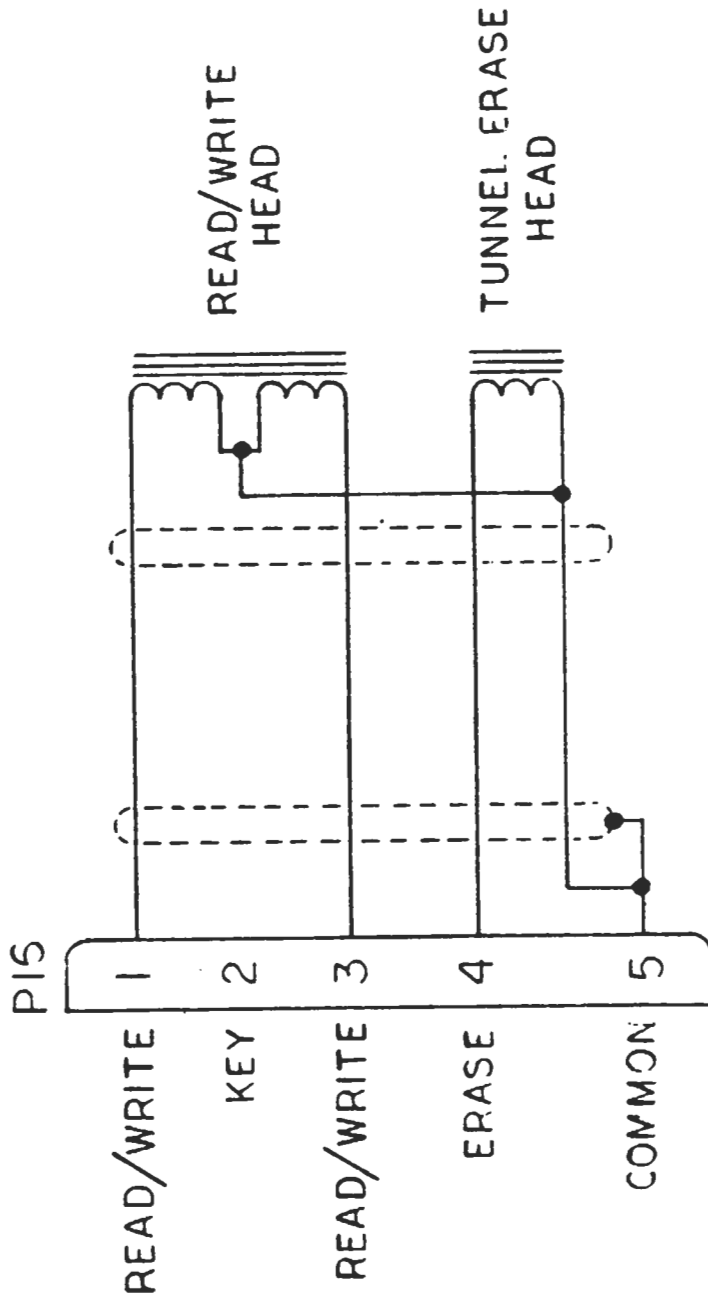
SCHEMATIC
HEAD LOAD ASSEMBLY
SIDE 0

270/272/277	SHT 1 OF 1	200237	A
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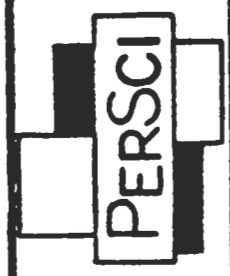


SCHEMATIC
POSITIONER MOTOR

270/272/277	SHT 1 OF 1	200242	A
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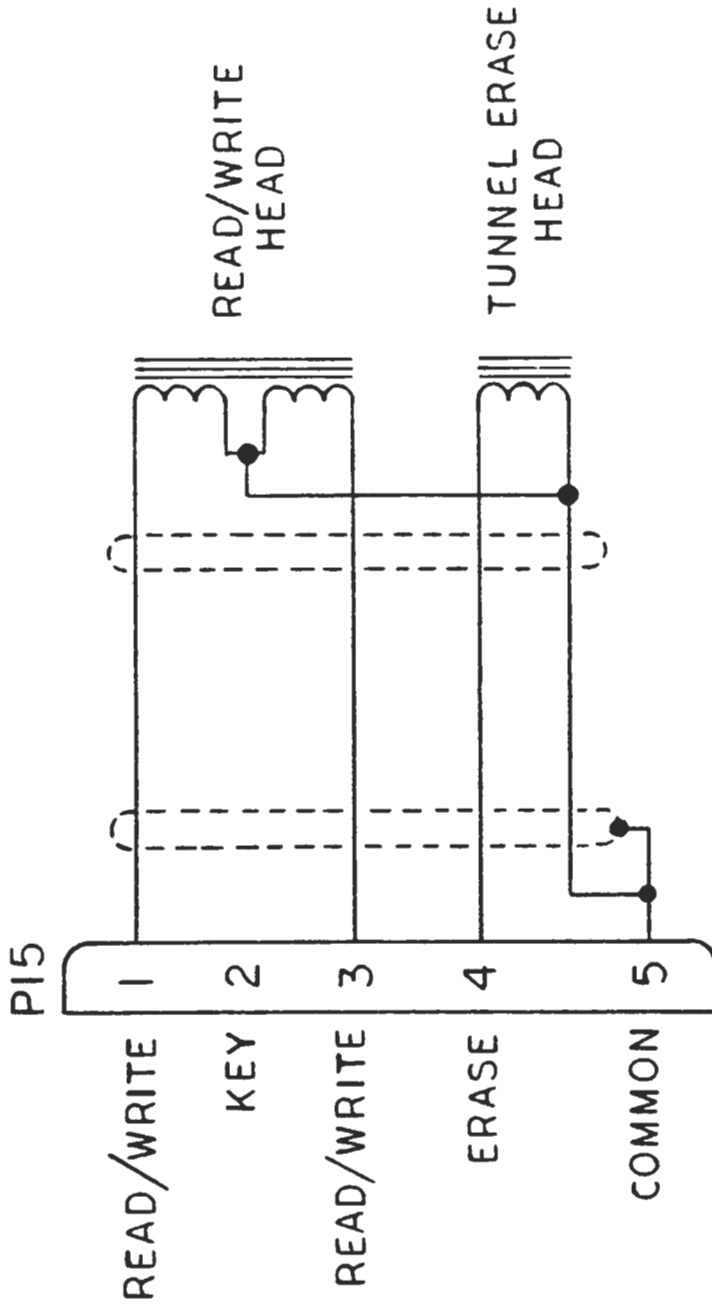


PERSCI, INC.



SCHEMATIC
 READ/WRITE HEAD ASSEMBLY
 SIDE 0

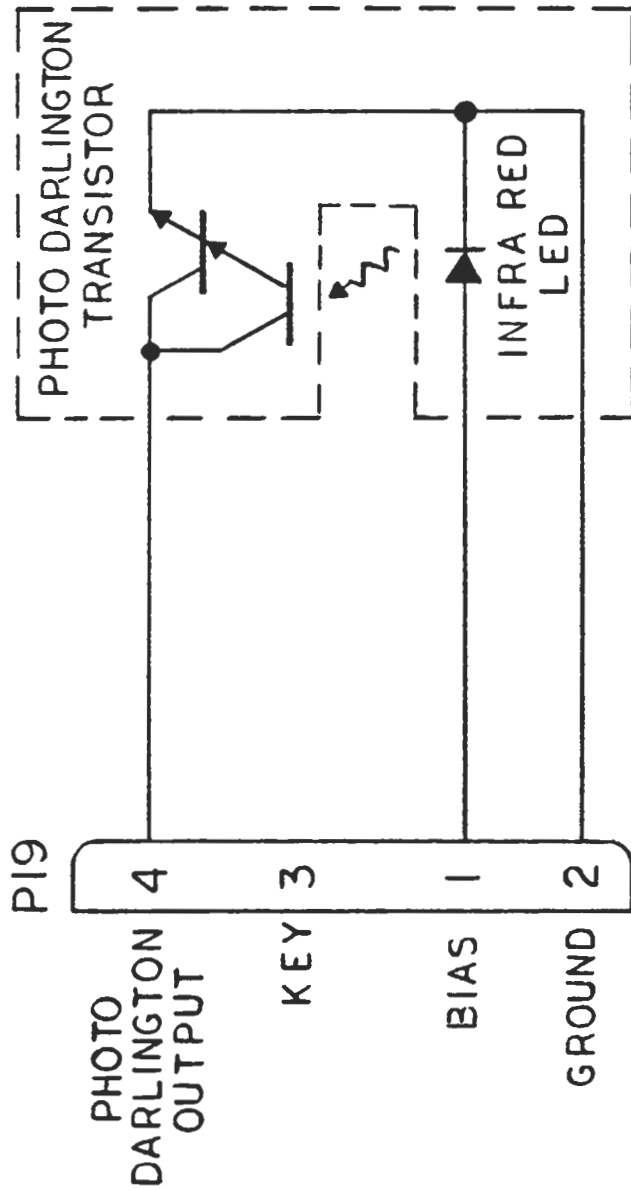
270/272/277	SHT 1 OF 1	200235	A
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PERSCI, INC.

SCHEMATIC
 READ/WRITE HEAD ASSEMBLY
 SIDE 1

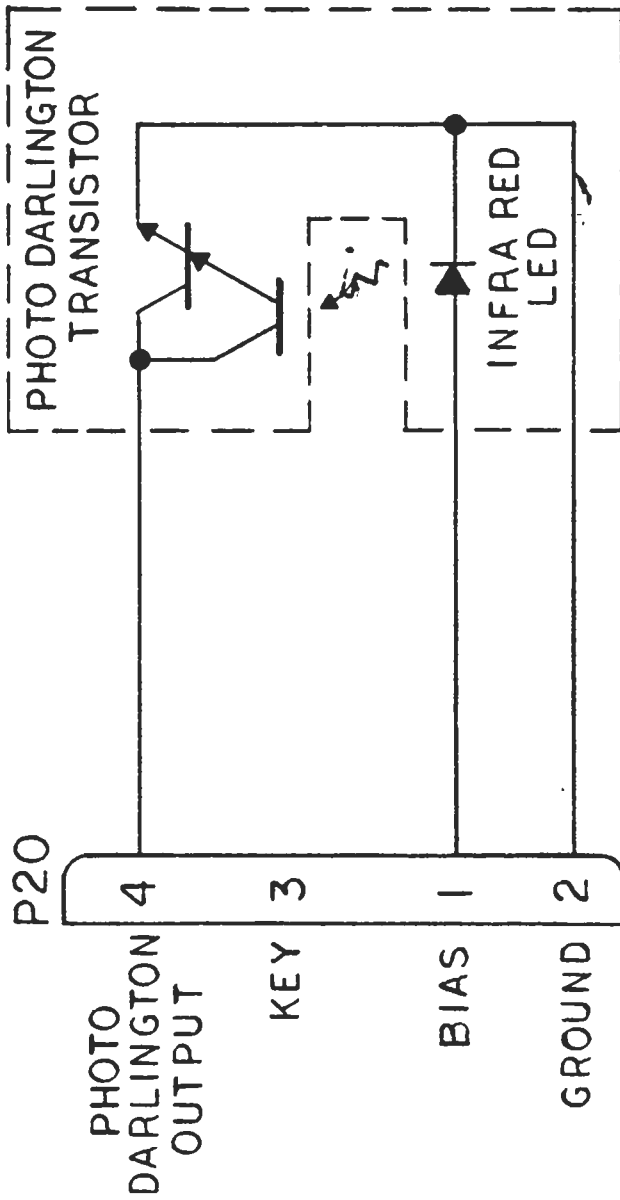
270/277	SHT 10F1	200236	A
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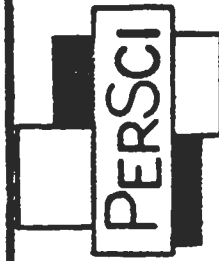
PERSCI, INC.

SCHEMATIC
WRITE PROTECT MODULE
SIDE 1

270' 7-1/277	SHT 10F1	200232	A
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PERSCI, INC.



SCHMATIC
WRITE PROTECT MODULE
SIDE 0

270/272/277

SHT 1 OF 1

200231

A

THE SCHEMATICS IN THIS SECTION REFER TO
PerSci DRIVES WITH SERIAL NUMBER:
2500 - 5000 (approximately)

REV	DESCRIPTION	DATE	UNIT APPROVED
A	MFG REL		
B	ECO #12		
C	ECO #13		
D	ECO #43		
E	ECO #57		
F	ECO #59		

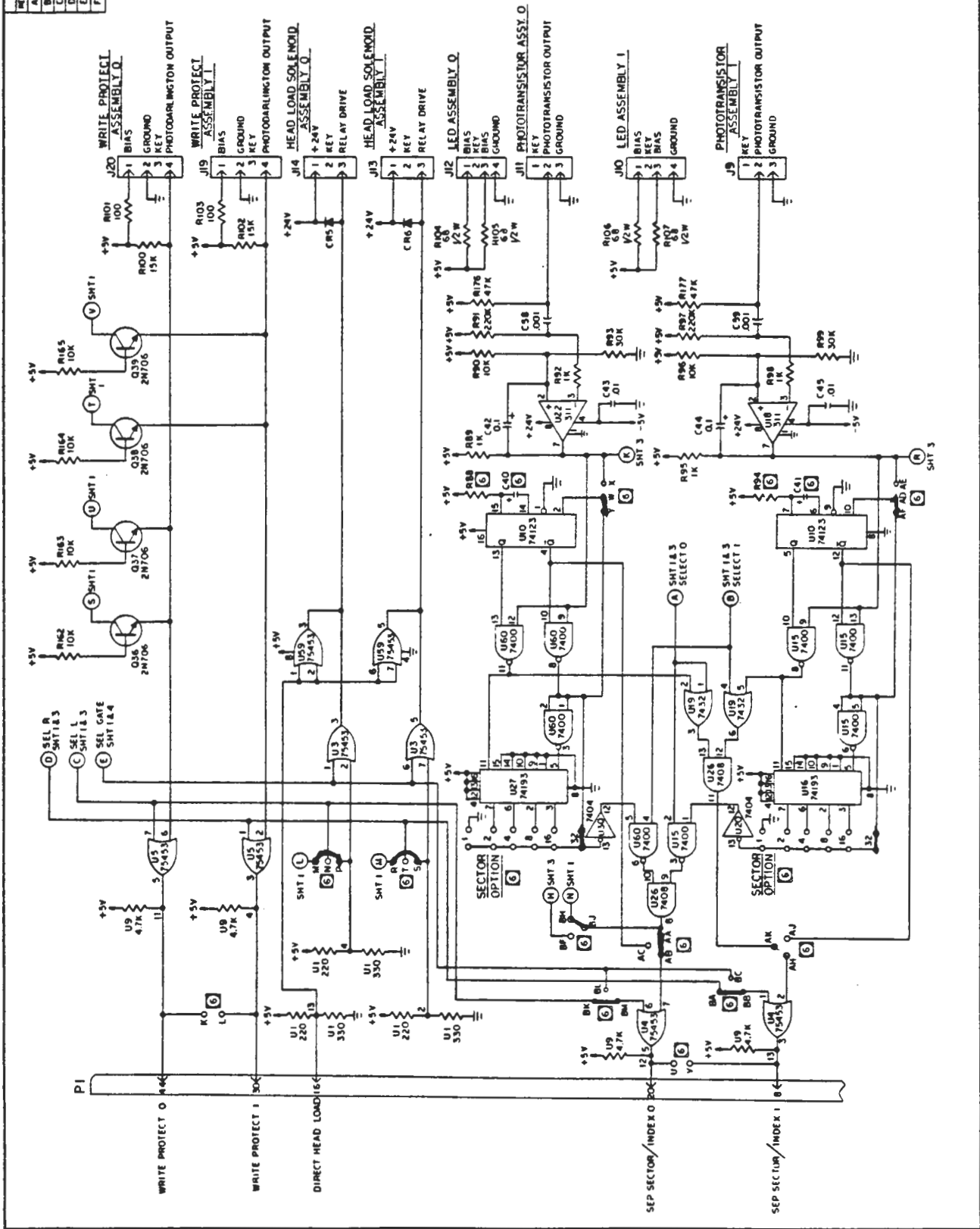
WRITE PROTECT. H.LOAD. INDEX.

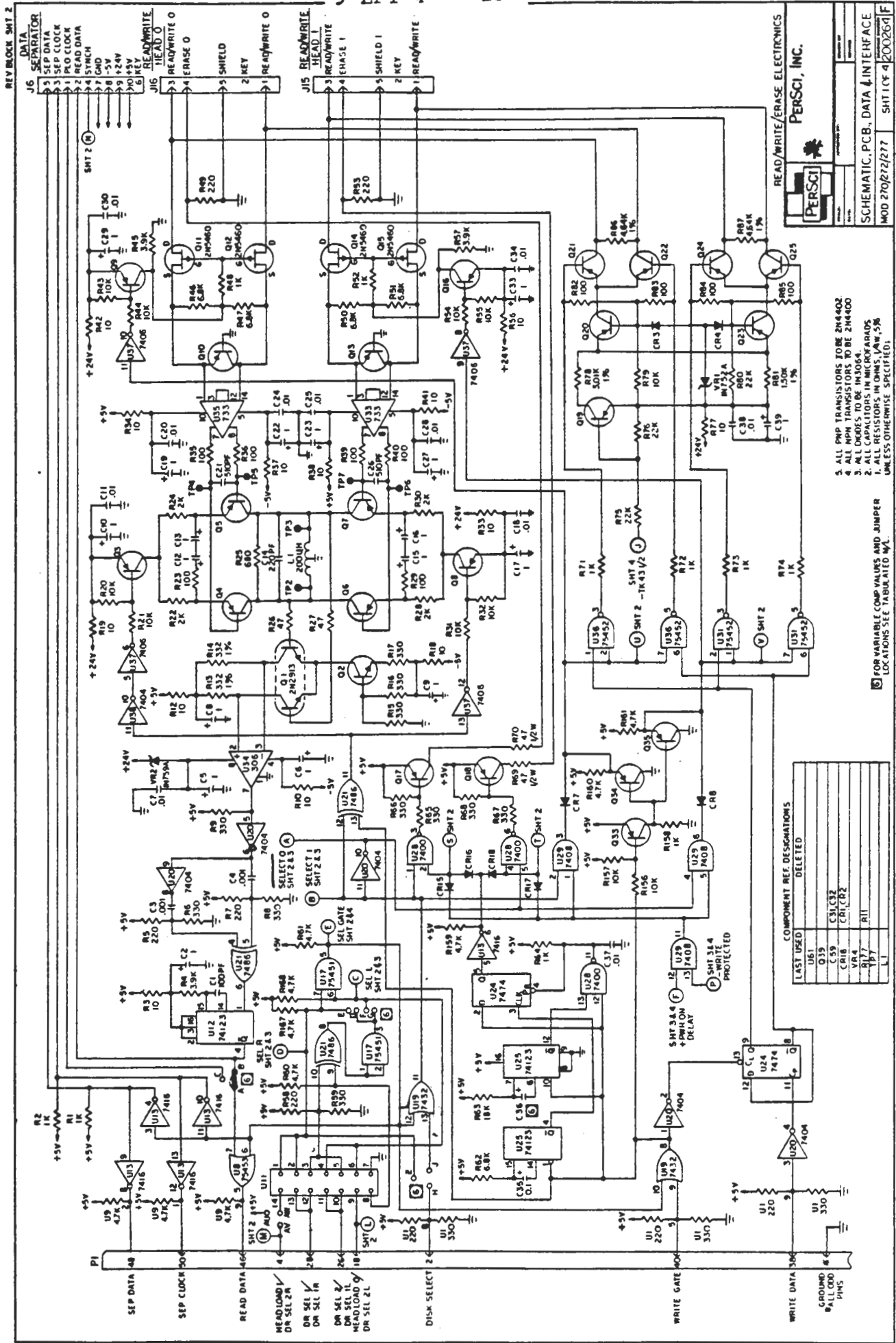
PERSCI

PERSCI, INC.

SCHEMATIC, P.C.B. DATA & INTERFACE

MOD 27q/27z/277 SHT 2 OF 4 200264F





REV BLOCK SMT 2

DATA SEPARATOR
 1 SEP DATA
 2 SEP CLOCK
 3 PLO CLOCK
 4 READ DATA
 5 SYNC
 6 -5V
 7 +24V
 8 +5V
 9 KEY
 10 KEY

HEADWRITE HEAD 0
 1 HEADWRITE 0
 2 SHIELD
 3 KEY
 4 HEADWRITE 0

HEADWRITE HEAD 1
 1 HEADWRITE 1
 2 SHIELD 1
 3 KEY
 4 HEADWRITE 1

READ/WRITE/ERASE ELECTRONICS

PERSCI

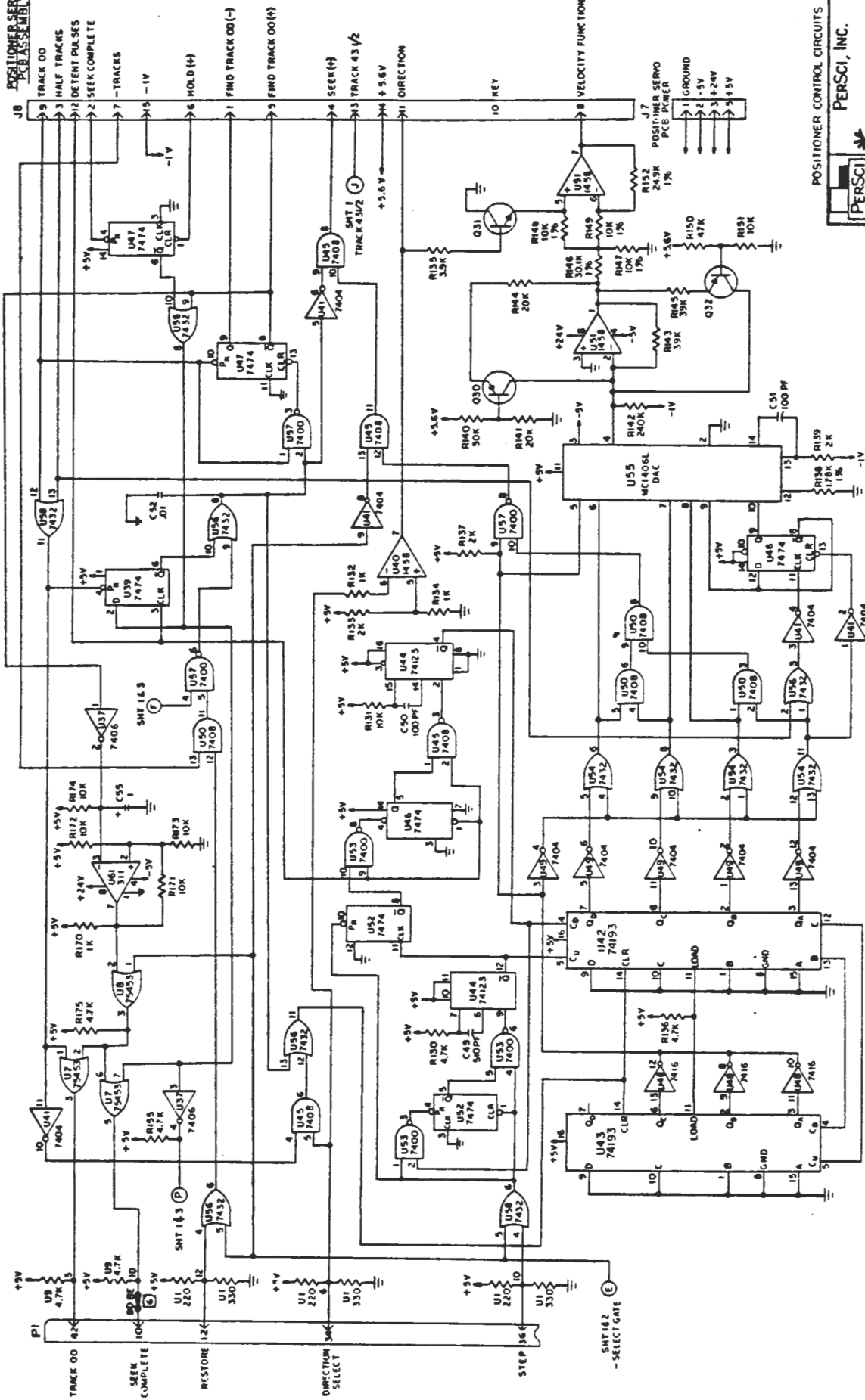
SCHEMATIC PCB DATA INTERFACE
 MOD 270272/277 SMT 1 OF 4 2002691F

- 3. ALL PNP TRANSISTORS TO BE 2N4402.
- 4. ALL PNP TRANSISTORS TO BE 2N4402.
- 5. ALL CAPACITORS IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
- 6. FOR VARIABLE COMP VALUES AND JUMPER LOCATIONS SEE TABULATED WL.

COMPONENT REF DESIGNATIONS

LAST USED	DELETED
U61	
Q39	CS1C32
C59	CR1C2
CR8	VR4
VR4	RI1
RI7	
LI	

POSITIONER SERVO PCB ASSEMBLY



POSITIONER CONTROL CIRCUITS

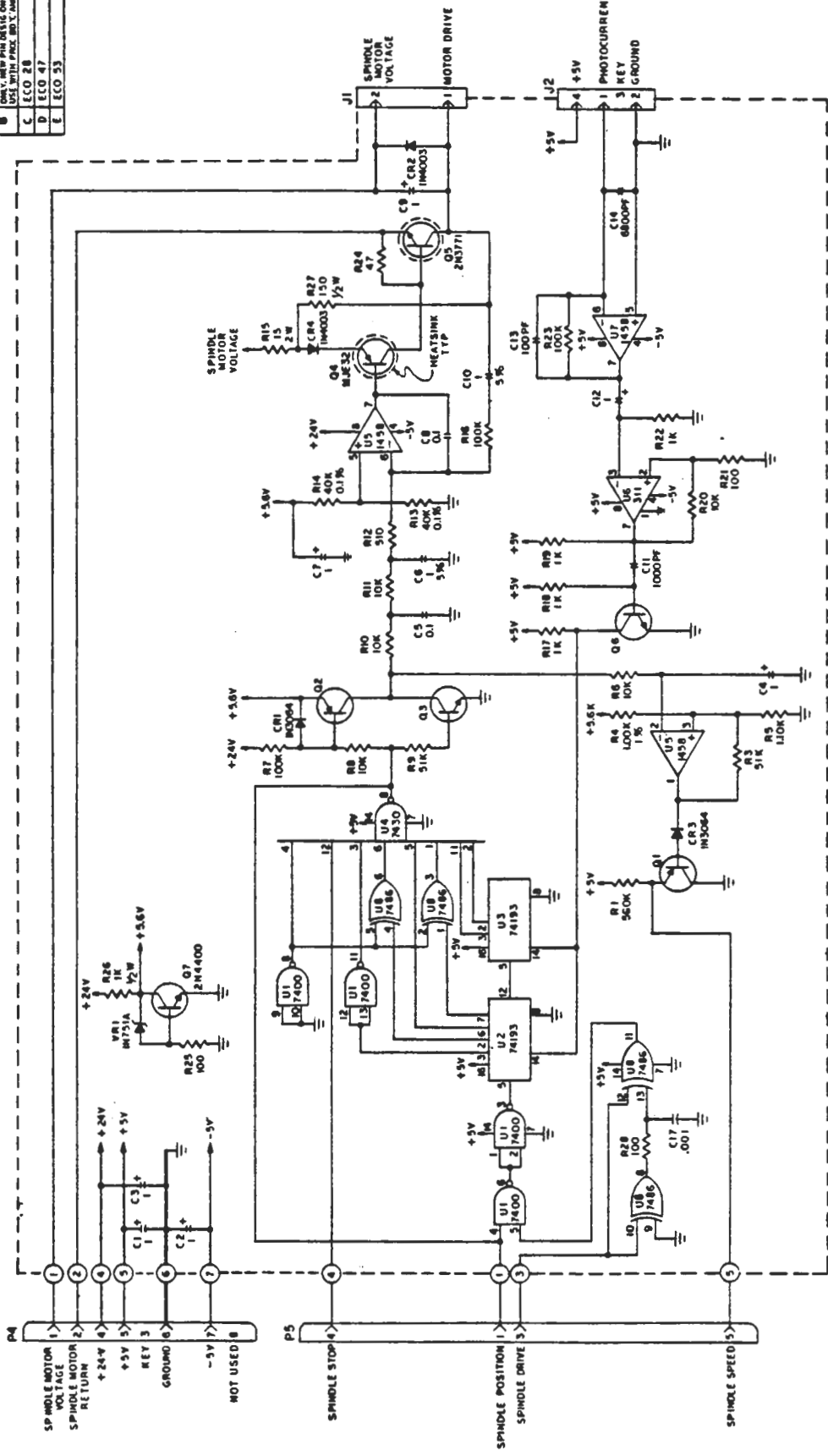


PERSCI, INC.

SCHEMATIC PCB DATA INTERFACE

MOD 270/272/277 SHT 4 of 4 2002G-1F

REV	DATE	DESCRIPTION
A	7/94	ENGINE DEL
B	11/77	IC PWR REGULATOR TO APPROXIMATE 200mA
C	11/77	USE WITH PWR. REG. AND UP
D	11/77	ECO 28
E	11/77	ECO 47
F	11/77	ECO 53



PERSCI

SCHEMATIC, PCB, SPINDLE SERVO

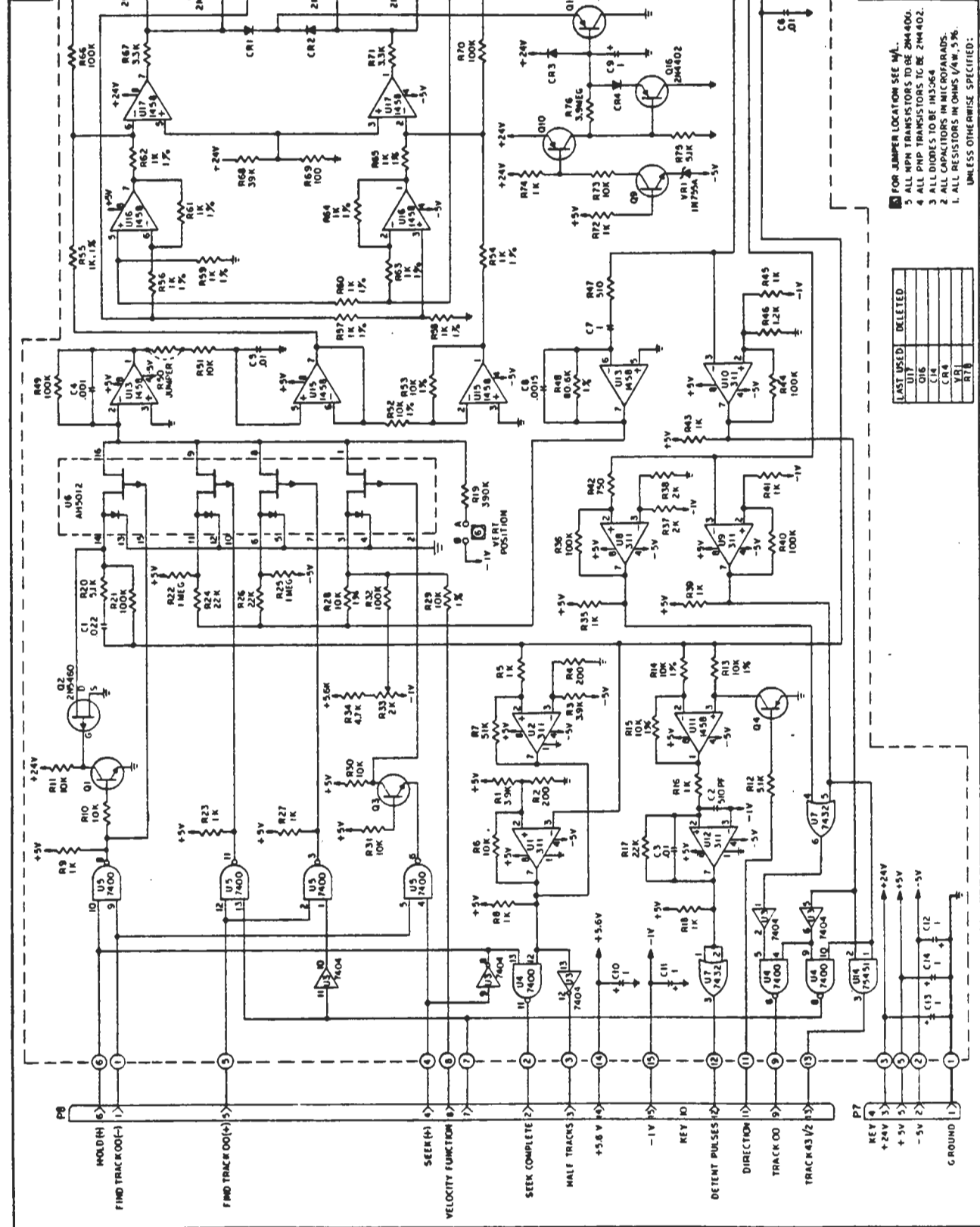
MOD 270/272/277 SMT LOT 1 200133 E

- 4 ALL PNP TRANSISTORS TO BE 2N4402.
 - 3 ALL NPN TRANSISTORS TO BE 2N4400
 - 2 ALL CAPACITOR VALUES IN MICROFARADS
 - 1. ALL RESISTOR VALUES IN OHMS, 1/4W, 5%.
- UNLESS OTHERWISE SPECIFIED;

REF DESIGNATIONS

LAST USED	DELETED
U1	
Q7	
CR4	
C17	C15, C16
R28	R2
Y.R1	

REV	DESCRIPTION	DATE	BY
1	REVISED PER INSTRUMENT	07/77	J.A.
2	REVISED PER INSTRUMENT	07/77	J.A.
3	REVISED PER INSTRUMENT	07/77	J.A.
4	REVISED PER INSTRUMENT	07/77	J.A.
5	REVISED PER INSTRUMENT	07/77	J.A.
6	REVISED PER INSTRUMENT	07/77	J.A.
7	REVISED PER INSTRUMENT	07/77	J.A.
8	REVISED PER INSTRUMENT	07/77	J.A.
9	REVISED PER INSTRUMENT	07/77	J.A.
10	REVISED PER INSTRUMENT	07/77	J.A.
11	REVISED PER INSTRUMENT	07/77	J.A.
12	REVISED PER INSTRUMENT	07/77	J.A.
13	REVISED PER INSTRUMENT	07/77	J.A.
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15	REVISED PER INSTRUMENT	07/77	J.A.
16	REVISED PER INSTRUMENT	07/77	J.A.
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19	REVISED PER INSTRUMENT	07/77	J.A.
20	REVISED PER INSTRUMENT	07/77	J.A.
21	REVISED PER INSTRUMENT	07/77	J.A.
22	REVISED PER INSTRUMENT	07/77	J.A.
23	REVISED PER INSTRUMENT	07/77	J.A.
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30	REVISED PER INSTRUMENT	07/77	J.A.
31	REVISED PER INSTRUMENT	07/77	J.A.
32	REVISED PER INSTRUMENT	07/77	J.A.
33	REVISED PER INSTRUMENT	07/77	J.A.
34	REVISED PER INSTRUMENT	07/77	J.A.
35	REVISED PER INSTRUMENT	07/77	J.A.
36	REVISED PER INSTRUMENT	07/77	J.A.
37	REVISED PER INSTRUMENT	07/77	J.A.
38	REVISED PER INSTRUMENT	07/77	J.A.
39	REVISED PER INSTRUMENT	07/77	J.A.
40	REVISED PER INSTRUMENT	07/77	J.A.
41	REVISED PER INSTRUMENT	07/77	J.A.
42	REVISED PER INSTRUMENT	07/77	J.A.
43	REVISED PER INSTRUMENT	07/77	J.A.
44	REVISED PER INSTRUMENT	07/77	J.A.
45	REVISED PER INSTRUMENT	07/77	J.A.
46	REVISED PER INSTRUMENT	07/77	J.A.
47	REVISED PER INSTRUMENT	07/77	J.A.
48	REVISED PER INSTRUMENT	07/77	J.A.
49	REVISED PER INSTRUMENT	07/77	J.A.
50	REVISED PER INSTRUMENT	07/77	J.A.
51	REVISED PER INSTRUMENT	07/77	J.A.
52	REVISED PER INSTRUMENT	07/77	J.A.
53	REVISED PER INSTRUMENT	07/77	J.A.
54	REVISED PER INSTRUMENT	07/77	J.A.
55	REVISED PER INSTRUMENT	07/77	J.A.
56	REVISED PER INSTRUMENT	07/77	J.A.
57	REVISED PER INSTRUMENT	07/77	J.A.
58	REVISED PER INSTRUMENT	07/77	J.A.
59	REVISED PER INSTRUMENT	07/77	J.A.
60	REVISED PER INSTRUMENT	07/77	J.A.
61	REVISED PER INSTRUMENT	07/77	J.A.
62	REVISED PER INSTRUMENT	07/77	J.A.
63	REVISED PER INSTRUMENT	07/77	J.A.
64	REVISED PER INSTRUMENT	07/77	J.A.
65	REVISED PER INSTRUMENT	07/77	J.A.
66	REVISED PER INSTRUMENT	07/77	J.A.
67	REVISED PER INSTRUMENT	07/77	J.A.
68	REVISED PER INSTRUMENT	07/77	J.A.
69	REVISED PER INSTRUMENT	07/77	J.A.
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72	REVISED PER INSTRUMENT	07/77	J.A.
73	REVISED PER INSTRUMENT	07/77	J.A.
74	REVISED PER INSTRUMENT	07/77	J.A.
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76	REVISED PER INSTRUMENT	07/77	J.A.
77	REVISED PER INSTRUMENT	07/77	J.A.
78	REVISED PER INSTRUMENT	07/77	J.A.
79	REVISED PER INSTRUMENT	07/77	J.A.
80	REVISED PER INSTRUMENT	07/77	J.A.
81	REVISED PER INSTRUMENT	07/77	J.A.
82	REVISED PER INSTRUMENT	07/77	J.A.
83	REVISED PER INSTRUMENT	07/77	J.A.
84	REVISED PER INSTRUMENT	07/77	J.A.
85	REVISED PER INSTRUMENT	07/77	J.A.
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90	REVISED PER INSTRUMENT	07/77	J.A.
91	REVISED PER INSTRUMENT	07/77	J.A.
92	REVISED PER INSTRUMENT	07/77	J.A.
93	REVISED PER INSTRUMENT	07/77	J.A.
94	REVISED PER INSTRUMENT	07/77	J.A.
95	REVISED PER INSTRUMENT	07/77	J.A.
96	REVISED PER INSTRUMENT	07/77	J.A.
97	REVISED PER INSTRUMENT	07/77	J.A.
98	REVISED PER INSTRUMENT	07/77	J.A.
99	REVISED PER INSTRUMENT	07/77	J.A.
100	REVISED PER INSTRUMENT	07/77	J.A.



- FOR JUMPER LOCATION SEE W/L.
- 5 ALL NPN TRANSISTORS TO BE 2N4400.
 - 4 ALL PNP TRANSISTORS TO BE 2N4402.
 - 3 ALL DIODES TO BE 1N3064
 - 2 ALL CAPACITORS IN MICROFARADS.
 - 1 ALL RESISTORS IN OHMS 1/4W, 5%.
- UNLESS OTHERWISE SPECIFIED:

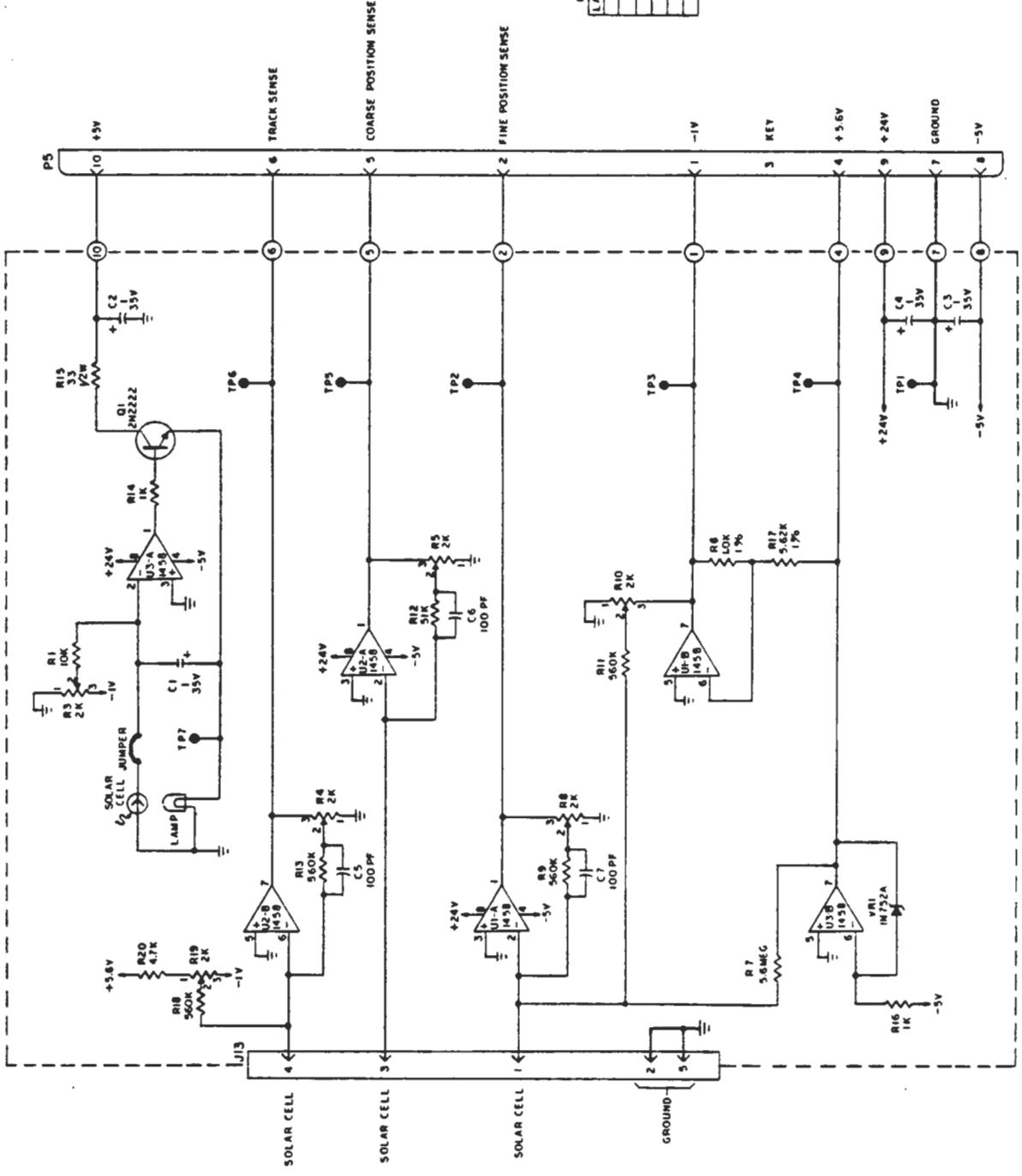
LAST USED	DELETED
U17	
U16	
C14	
C14	
CR4	
VR1	
VR1	
VR1	
VR1	

PERSCI, INC.

MODEL 270/272/277 SMT 1 OF 1 200130B

SCHMATIC: PCB POSITIONER SERVO

REVISIONS		200086 D
REV	DESCRIPTION	DATE
A	ENGIN REL	
B	ADD R10 P5 20	
C	ECO 63' MFG. REL	
D	SEE ECO 77	



COMP. REF. DESIGNATIONS

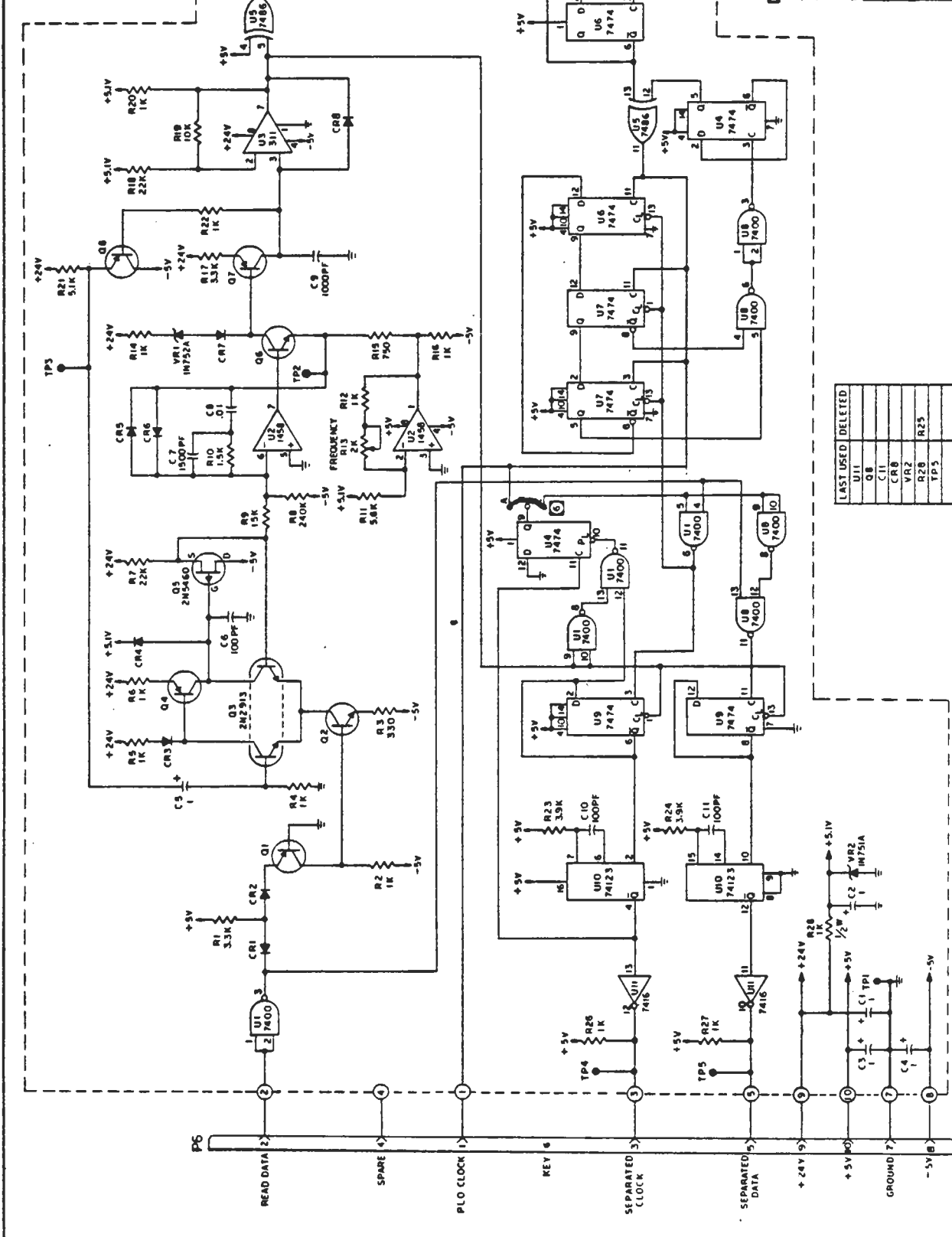
LAST USED	DELETED
U3	
Q1	
C7	
R20	
TP7	

2 ALL CAPACITOR VALUES IN MIKROFARADS
 1 ALL RESISTOR VALUES IN OHMS, 1/4W, 5%
 UNLESS OTHERWISE SPECIFIED;

PERSCI, INC.

SCHMATIC, PCB, LAMP AMPLIFIER
 MOD 270/272/277 SHT 10F1 200096D

REV	REVISIONS	DATE	BY
A	ENGINE REL	7/17/74	JL
B	AND APPROVAL APPROVAL	8/1/74	JL
C	AND APPROVAL APPROVAL	8/1/74	JL



- 1. FOR JUMPER LOCATIONS SEE TABULATED M.L.
- 2. ALL PNP TRANSISTORS TO BE 2N4402.
- 3. ALL NPN TRANSISTORS TO BE 2N4400.
- 4. ALL DIODES TO BE 1N3064.
- 5. ALL CAPACITORS IN MICROFARADS.
- 6. UNLESS OTHERWISE SPECIFIED:

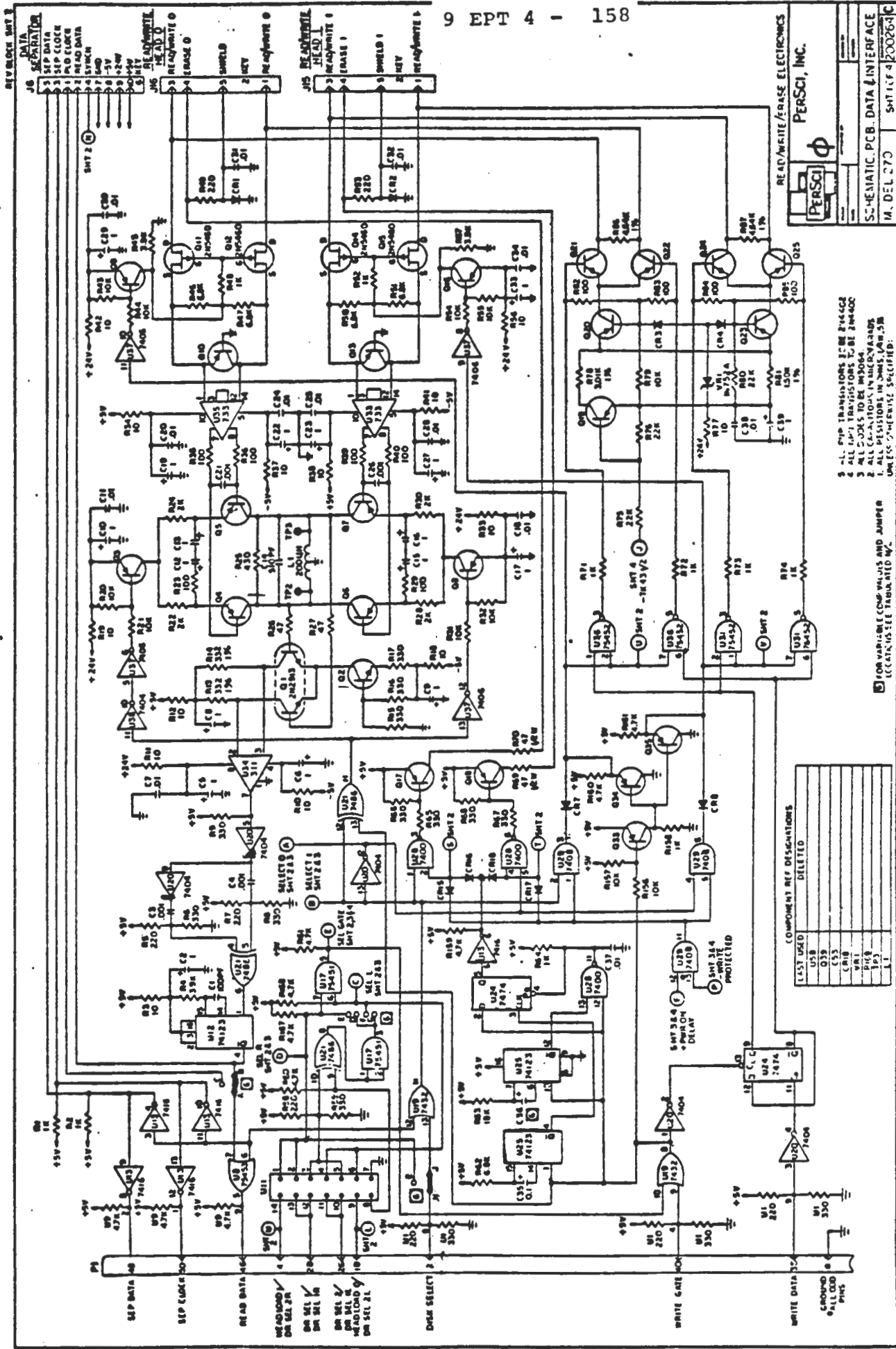
PERSCI, INC.

SCHEMATIC PHASE LOCKED DOUBLE DATA SEPARATOR

MOD 270127/271 SMT 1 OF 1 20015 C

LAST USED	DELETED
U11	
Q8	
C11	
VR2	
R28	
R25	
TP5	

THE SCHEMATICS IN THIS SECTION APPLY TO
PerSci DRIVES WITH SERIAL NUMBERS
PRIOR TO 2500 (approximately)



- 1. ALL PNP TRANSISTORS TO BE 2N4304
- 2. ALL NPN TRANSISTORS TO BE 2N4400
- 3. ALL LOGIC TO BE 7400A
- 4. ALL CAPACITORS IN MICROFARADS
- 5. ALL RESISTORS IN OHMS, UNLESS OTHERWISE SPECIFIED.

FOR VARIABLE COMPONENT VALUES AND JUMPER LOCATIONS SEE TABULATED M/C

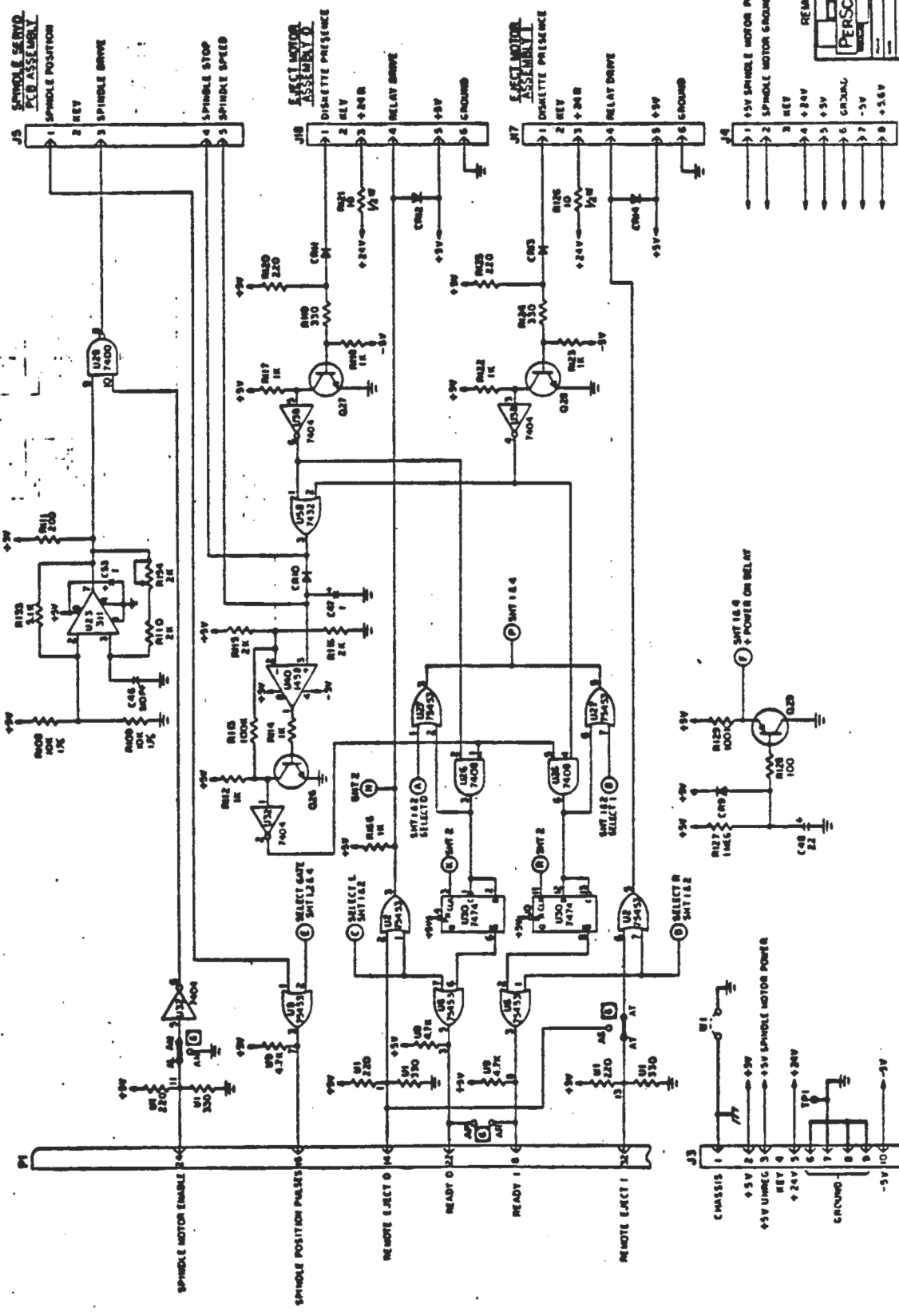
COMPONENT REF DESIGNATIONS	DELETED
U28	
Q29	
C33	
CR8	
VR1	
VR2	
VR3	
VR4	
VR5	
VR6	
VR7	
VR8	
VR9	
VR10	
VR11	
VR12	
VR13	
VR14	
VR15	
VR16	
VR17	
VR18	
VR19	
VR20	
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VR81	
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VR84	
VR85	
VR86	
VR87	
VR88	
VR89	
VR90	
VR91	
VR92	
VR93	
VR94	
VR95	
VR96	
VR97	
VR98	
VR99	
VR100	

PERSCI, INC.

READ/WRITE/ERASE ELECTRONICS

S-CHEMATIC PCB DATA INTERFACE

M. DEL 270 SMT 1/2 200264C



PERSCI

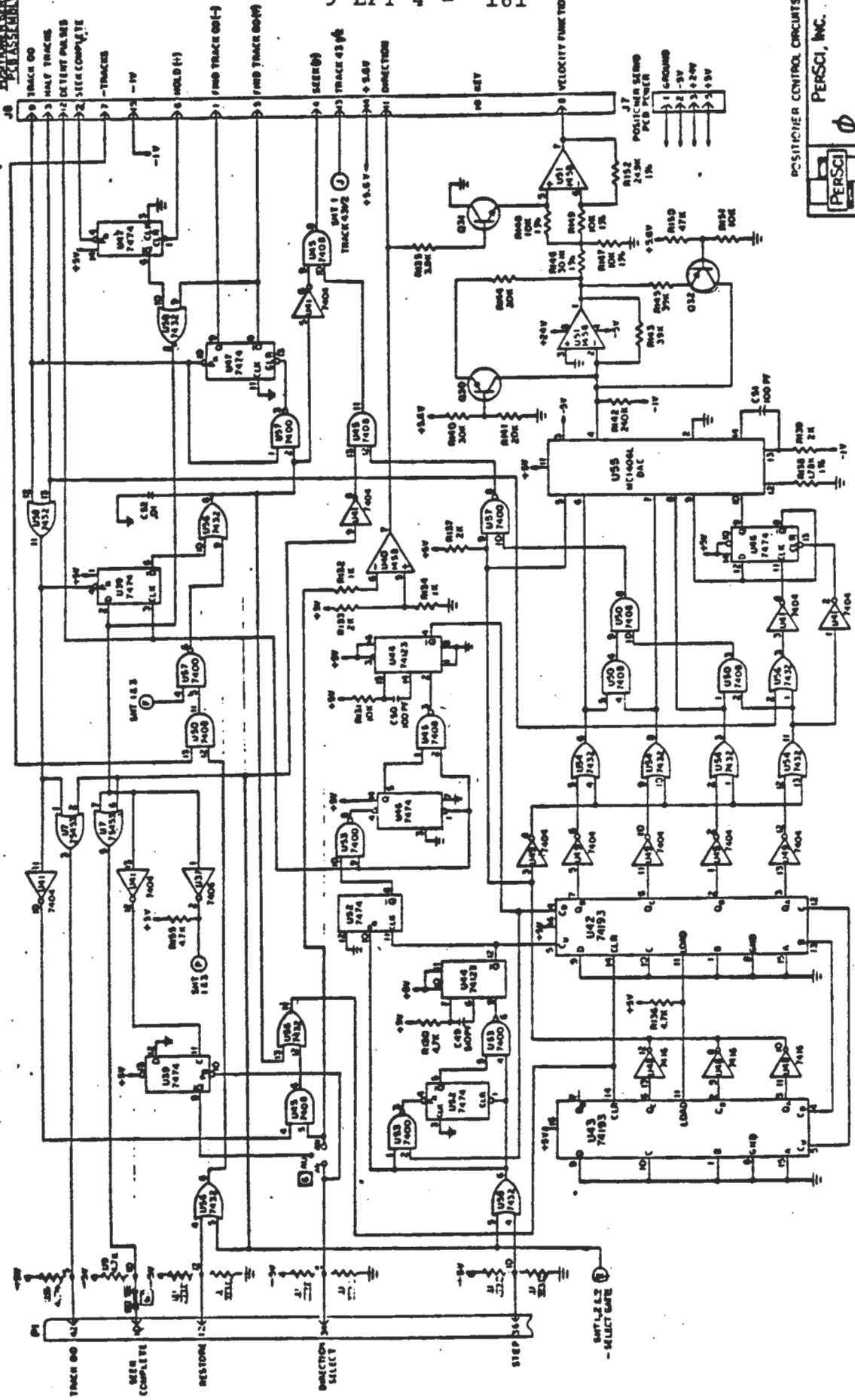
REMOTE EJECT, READY, SPINDLE

PERSCI, INC.

SCHEMATIC, P.C.B. DATA & INTERFACE

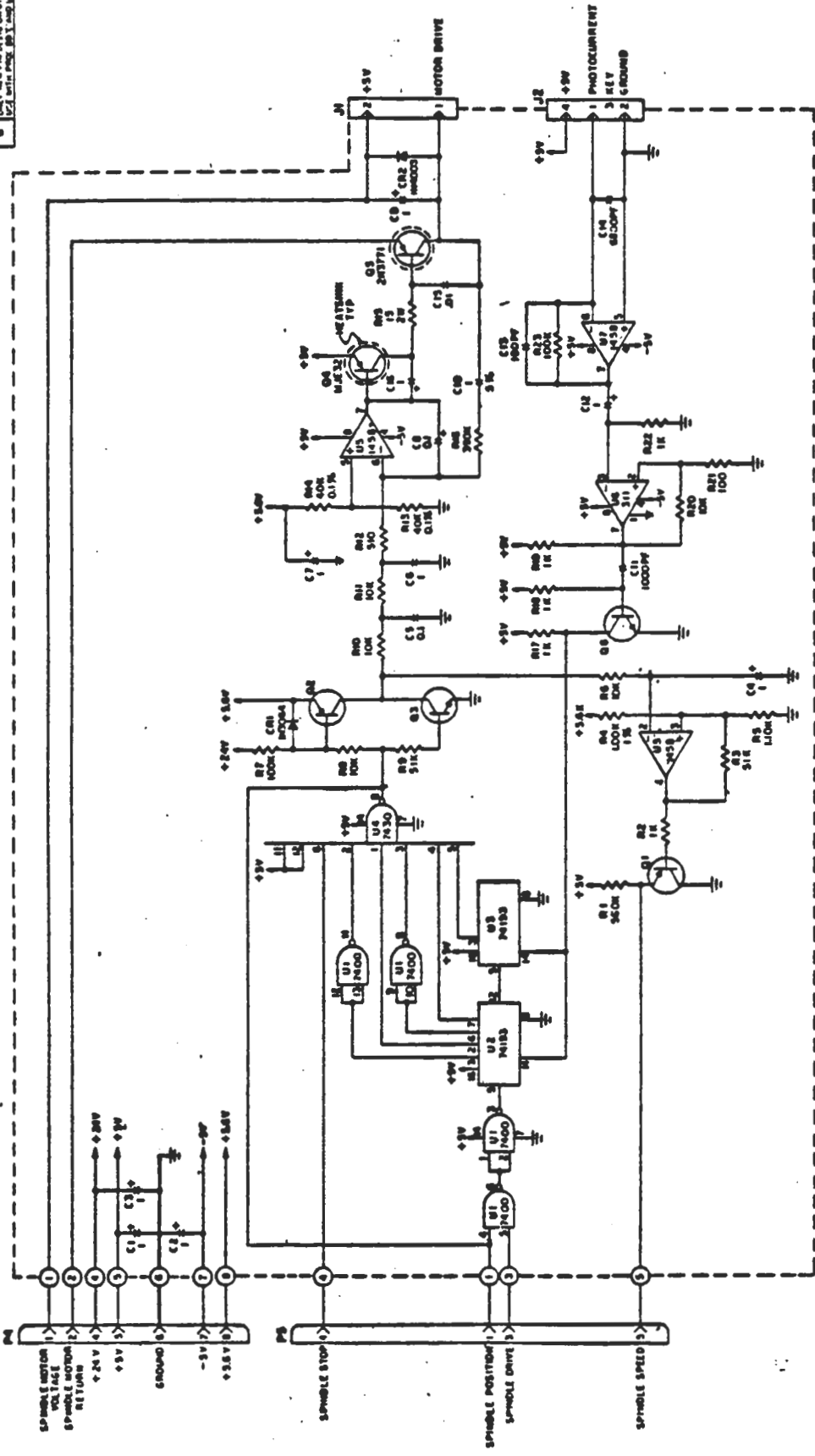
MOG 270 SMT 3 OF 4 2002CAC

POSITIONER SERVO
PC BOARD



POSITIONER CONTROL CIRCUITS
PERSCI
 PERSCI, INC.
 SCHEMATIC, P.C.E. DATA & INTERFACE
 M. S. 270
 SMT 4094
 200264C

REV	DESCRIPTION	DATE
1	INITIAL DESIGN	10/15/68
2	REVISION	11/10/68
3	REVISION	12/15/68
4	REVISION	1/15/69
5	REVISION	2/15/69
6	REVISION	3/15/69
7	REVISION	4/15/69
8	REVISION	5/15/69
9	REVISION	6/15/69
10	REVISION	7/15/69
11	REVISION	8/15/69
12	REVISION	9/15/69
13	REVISION	10/15/69
14	REVISION	11/15/69
15	REVISION	12/15/69



REF DESIGNATIONS

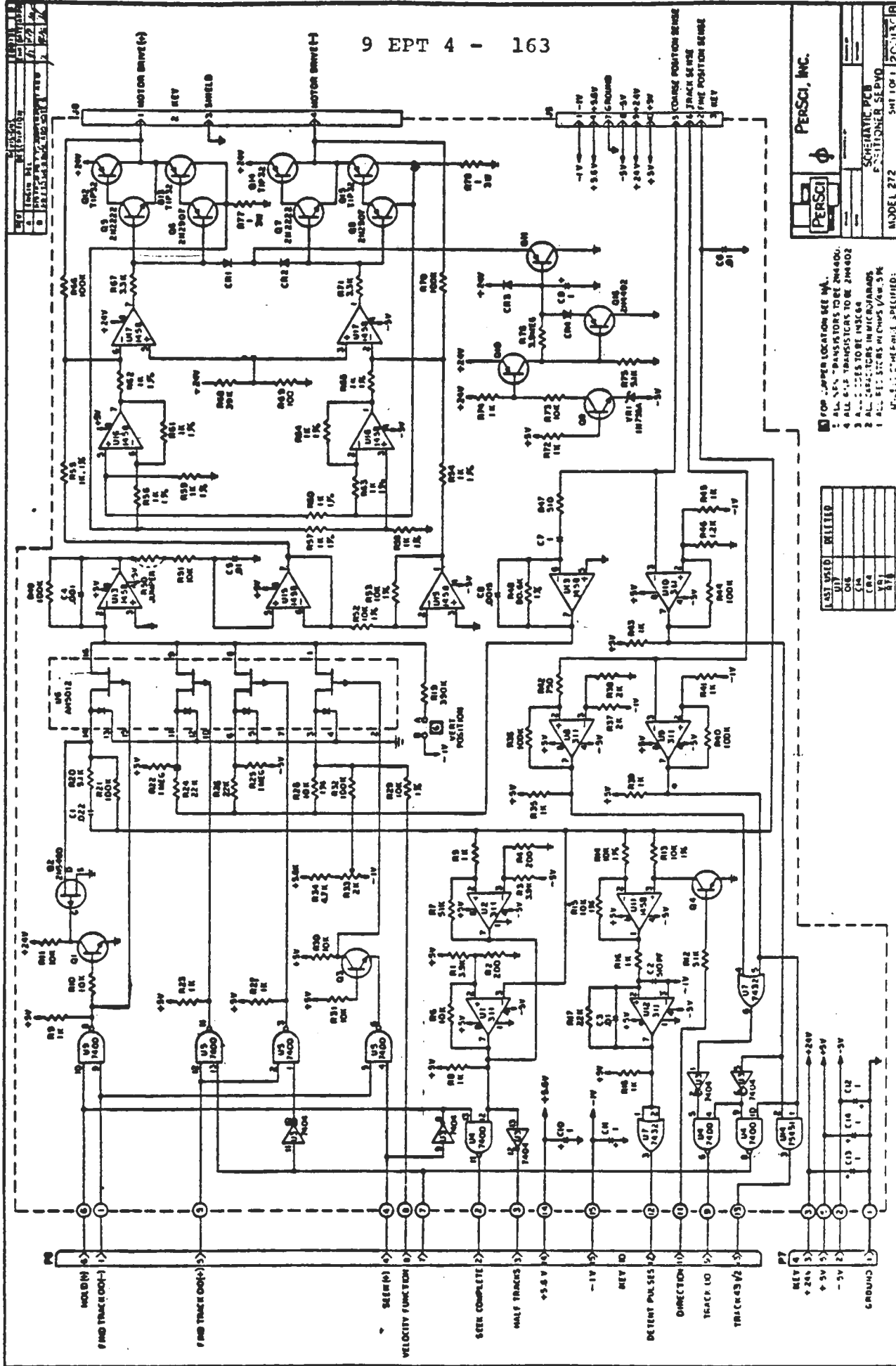
U1	74100
U2	74100
U3	74100
U4	74100
U5	74100
R1	100K
R2	10K
R3	10K
R4	10K
R5	10K
R6	10K
R7	100K
R8	10K
R9	10K
R10	10K
R11	10K
R12	10K
R13	10K
R14	10K
R15	10K
R16	10K
R17	10K

- 4 ALL PNP TRANSISTORS TO BE 2N4002
 - 3 ALL NPN TRANSISTORS TO BE 2N4000
 - 2 ALL CAPACITOR VALUES IN MICROFARADS
 - 1 ALL RESISTOR VALUES IN OHMS, (K=1K, M=1M)
- UNLESS OTHERWISE SPECIFIED

PERSCI, INC.

SCHEMATIC, PCE SPINDLE SERVO

MODEL 272 3 of 101 20G133 B



PERSCI, INC.

SCHEMATIC PCB
FUNCTIONER SEW

MODEL 272

REV 101

PCN1318

- 1. ALL NEW TRANSISTORS TO BE 2N4002
- 2. ALL NEW RESISTORS TO BE 1/4W
- 3. ALL NEW CAPACITORS TO BE 50V
- 4. ALL NEW DIODES TO BE 1N4001
- 5. ALL NEW IC'S TO BE IN MICRO SMD
- 6. ALL NEW IC'S TO BE IN MICRO SMD

LAST USED	WILLIPI
U17	
U16	
U15	
U14	
U13	
U12	
U11	
U10	
U9	
U8	
U7	
U6	
U5	
U4	
U3	
U2	
U1	

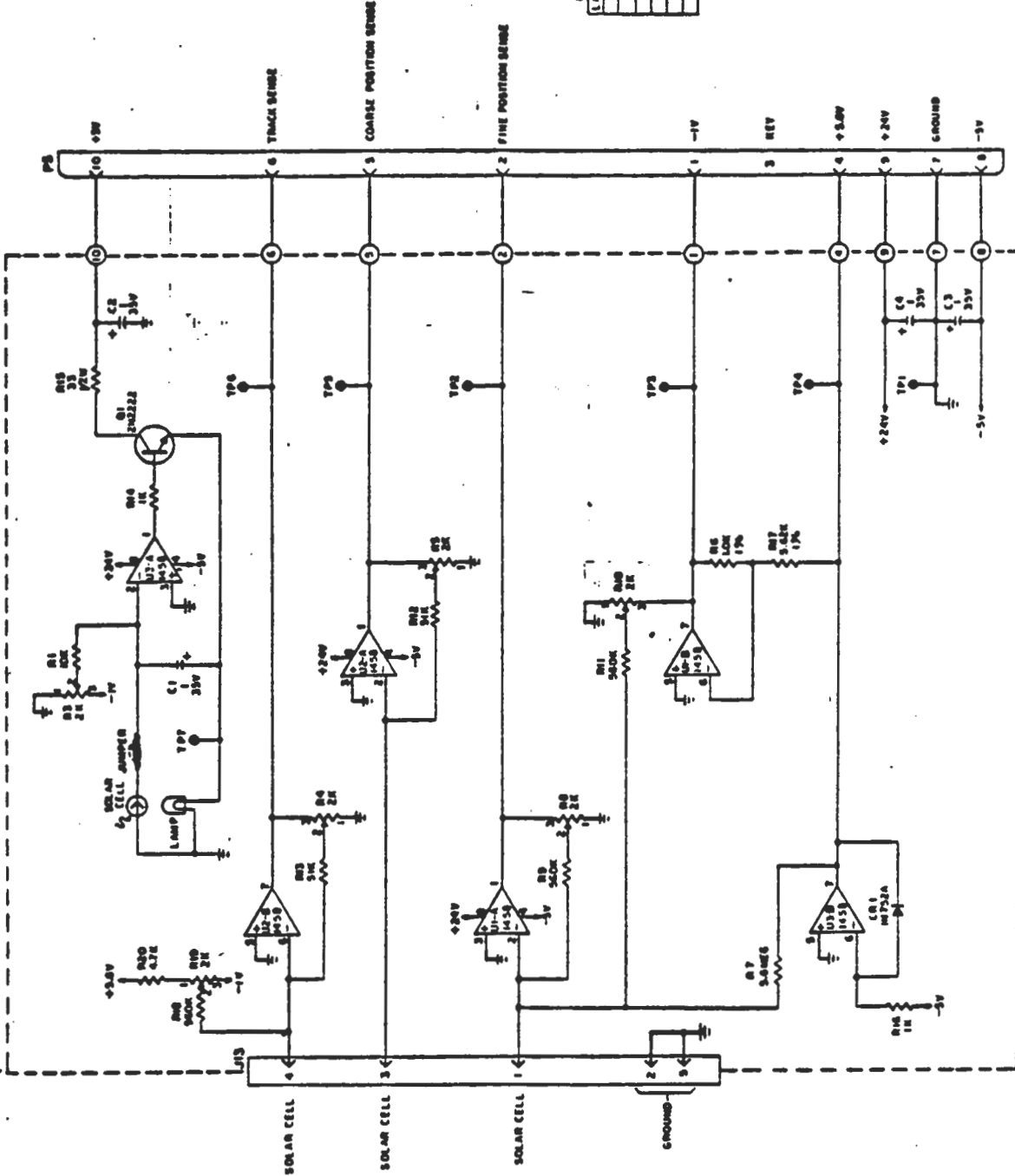
REV	DESCRIPTION	DATE
A	ENGINEER BILL	10/1/77
B	ADD PARTS LIST	10/1/77

COMP REF DESIGNATIONS	DELETED
U3	
U1	
CR1	
CS	
R20	
R2	
TP7	

2 ALL CAPACITOR VALUES IN MICROGRADS.
 1 ALL RESISTOR VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.

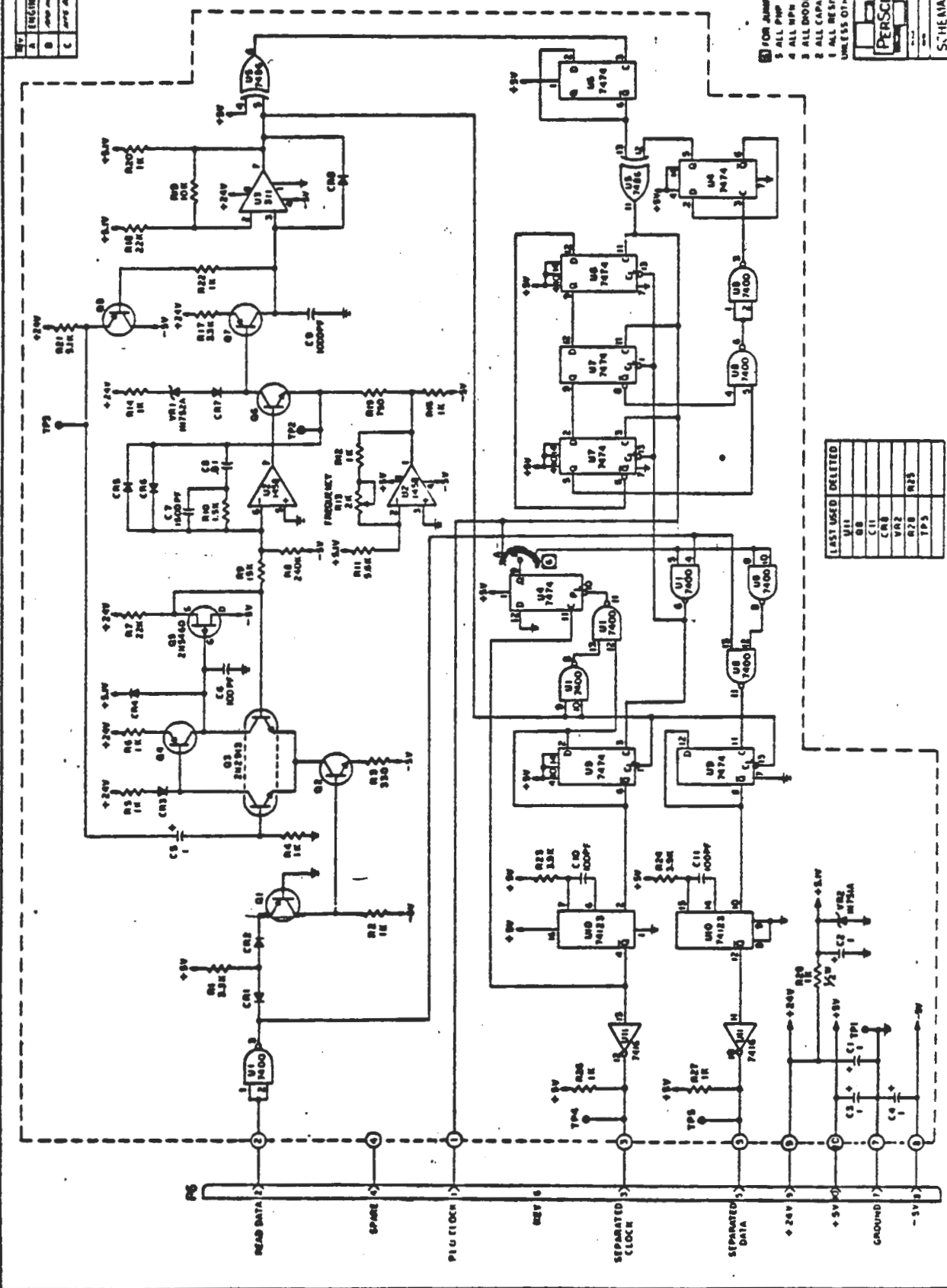
PERSCI, INC.

SCHEMATIC PCB LAMP AMPLIFIER
 MODEL 70/272 SMT-CF1 20050



PROC. 80 B

REV	DESCRIPTION	DATE	BY
1	INITIAL	7-17-64	J.P.
2	ENGINEER	7-17-64	J.P.
3	PHYSICIAN APPROVED	7-17-64	J.P.
4	PHYSICIAN APPROVED	7-17-64	J.P.
5	PHYSICIAN APPROVED	7-17-64	J.P.



- FOR JUMPER LOCATIONS SEE TABULATED W/L.
- ALL PNP TRANSISTORS TO BE 2N4402.
- ALL NPN TRANSISTORS TO BE 2N4402.
- ALL DIODES TO BE 1N304S.
- ALL CAPACITORS IN MICROFARADS.
- ALL RESISTORS IN OHMS UNLESS OTHERWISE SPECIFIED.

PERSCI, INC.

PHASE LOCKED DOUBLE DATA SEPARATOR

MCD 70/272 SMT 1 OF 1 200015

LAST USED	DELETED
U11	
U12	
U13	
U14	
U15	
U16	
U17	
U18	
U19	
U20	
U21	
U22	
U23	
U24	
U25	
U26	
U27	
U28	
U29	
U30	
U31	
U32	
U33	
U34	
U35	
U36	
U37	
U38	
U39	
U40	

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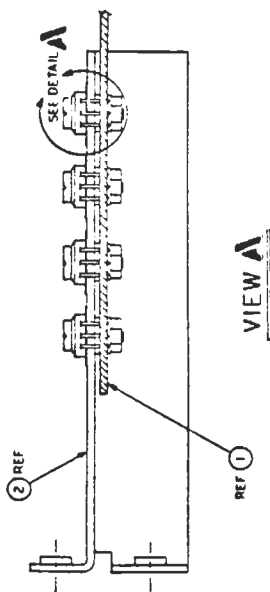
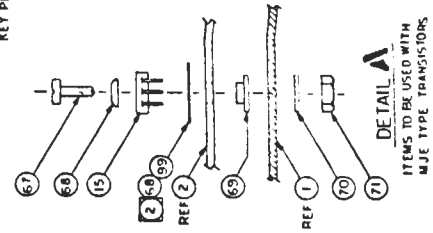
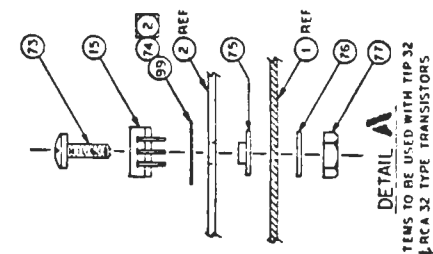
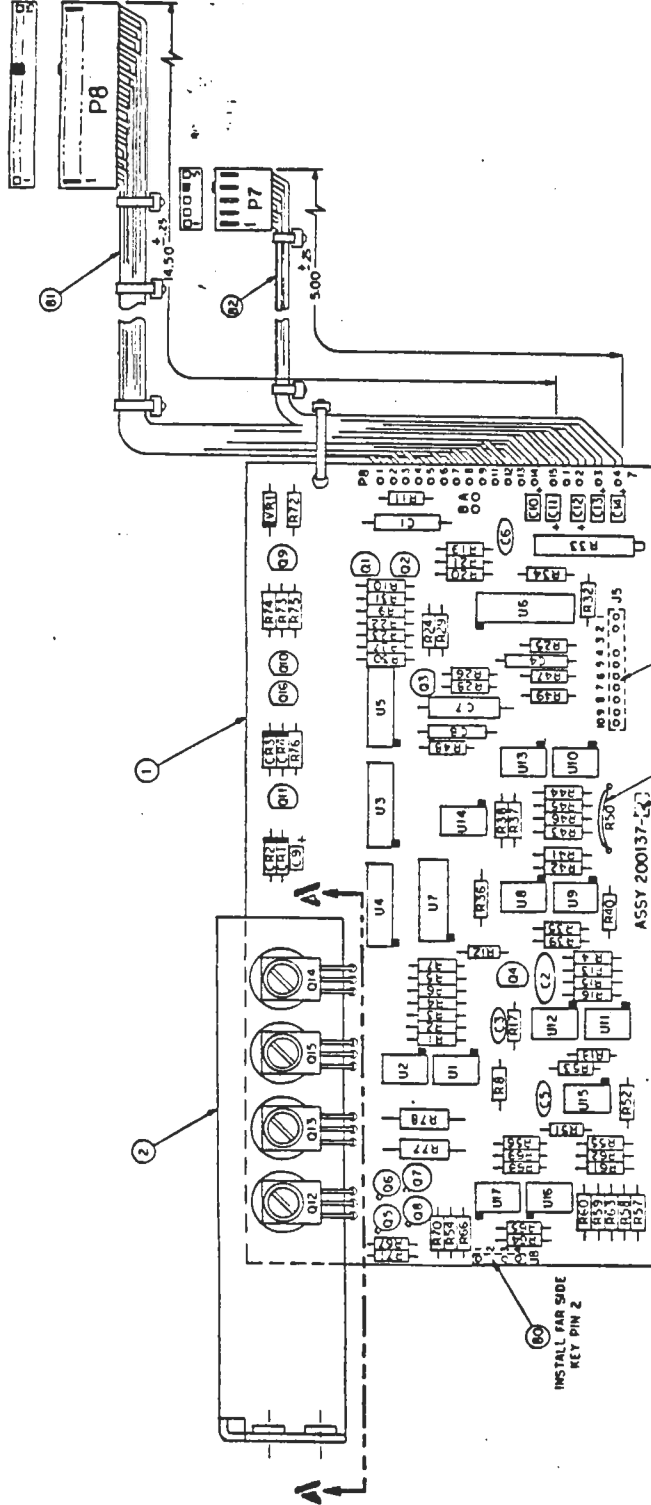
9 EPT 4 - 166
CONTENTS (Continued)

SECTION 8, DRAWINGS

DRIVE-ASSEMBLY DRAWINGS

FIGURE	PAGE
8-15	Assembly, Data and Interface PCB
8-16	Assembly, Positioner Servo
8-17	Assembly, Spindle Servo
8-18	Assembly, Phased Locked Double F Data Separator
8-19	Assembly, Lamp Amplifier PCB
8-20	Schematic, Data and Interface PCB, Sheet 1 of 4 Sheet 2 of 4 Sheet 3 of 4 Sheet 4 of 4
8-21	Schematic, Positioner Servo PCB
8-22	Schematic, Spindle Servo PCB
8-23	Schematic, Phase Locked Double F Data Separator
8-24	Schematic, Lamp Amplifier PCB
8-25	Schematic, LED Assembly, Side 0
8-26	Schematic, LED Assembly, Side 1
8-27	Schematic, Phototransistor Assembly, Side 0
8-28	Schematic, Phototransistor Assembly, Side 1
8-29	Schematic, Spindle Motor Assembly
8-30	Schematic, Eject Motor Assembly
8-31	Schematic, Head Load Assembly, Side 0
8-32	Schematic, Head Load Assembly, Side 1
8-33	Schematic, Positioner Motor
8-34	Schematic, Read/Write Head Assembly, Side 0
8-35	Schematic, Read/Write Head Assembly, Side 1

REV	REVISIONS	DATE
A	ENGINE REL	11/15/52
B	ADDED JUMPER POINT A P	11/15/52
C	ECO 93	11/15/52



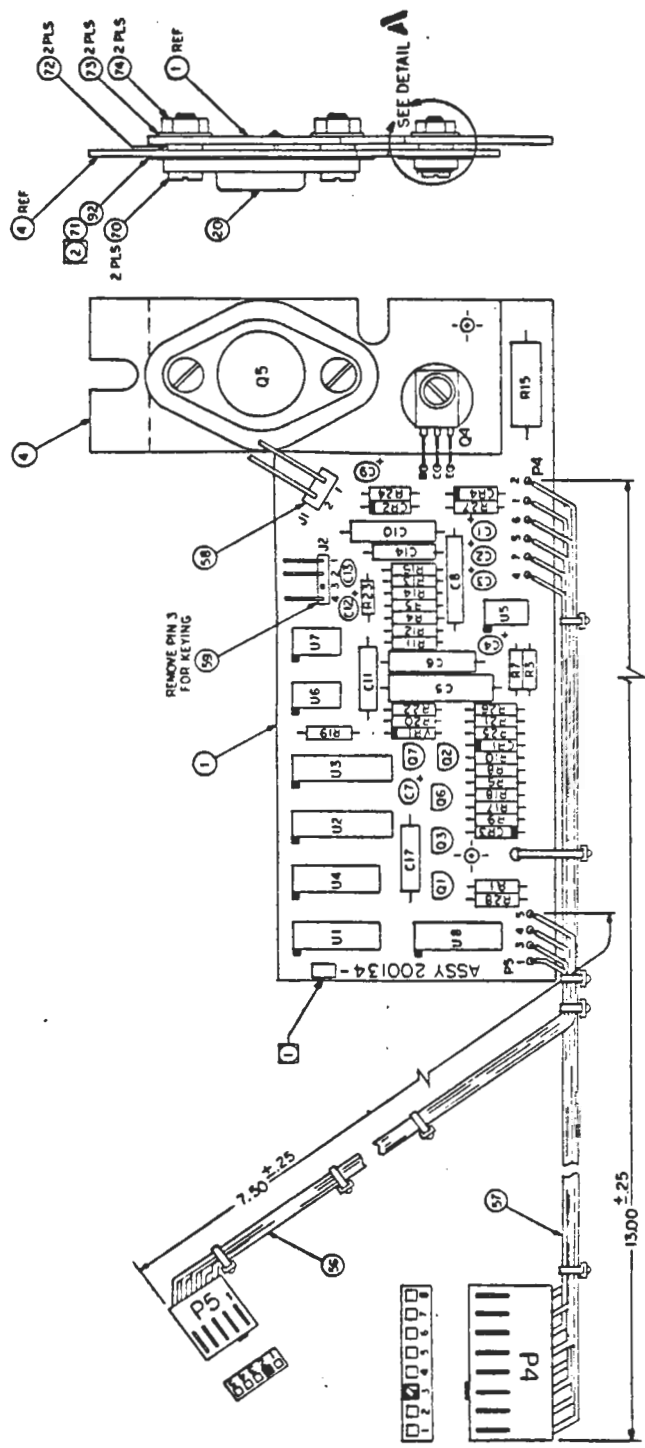
3. SCHEMATIC REF 200136.
 2. APPLY SILICON GREASE ON BOTH SIDES OF MICA INSULATOR.
 0. MARK REF DESIGNATIONS OR REVISION LEVEL IN HIGH BLACK/WHITE CHARACTERS IN APPROX AREA SHOWN UNLESS OTHERWISE SPECIFIED

PERSCI, INC.

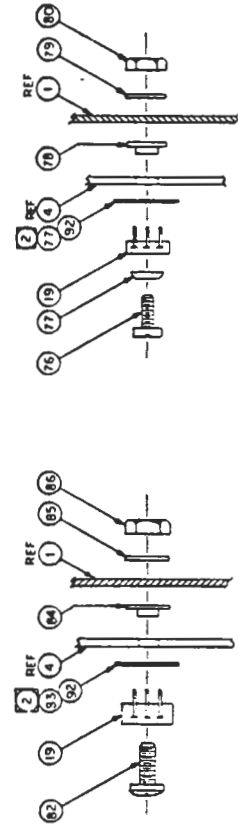
WET ASSY
 200131
 ASSEMBLY, PCB, POSITIONER SERVO

REV	DESCRIPTIONS	DATE
A	LENGTH REL	1/14/64
B	REVISED ADDRESS-NEW LAYOUT	1/14/64
C	1.00 X	1/14/64
D	1.00 X	1/14/64
E	1.00 X	1/14/64
F	1.00 X	1/14/64

9 EPT 4 - 168



- 3 SCHEMATIC REF 200133.
- 2 APPLY SILICON GREASE ON BOTH SIDES OF MICA INSULATOR.
- 1 MARK REVISION LEVEL IN HIGH WHITE CHARACTERS IN APPROX AREA SHOWN, UNLESS OTHERWISE SPECIFIED:



PERSCI, INC.

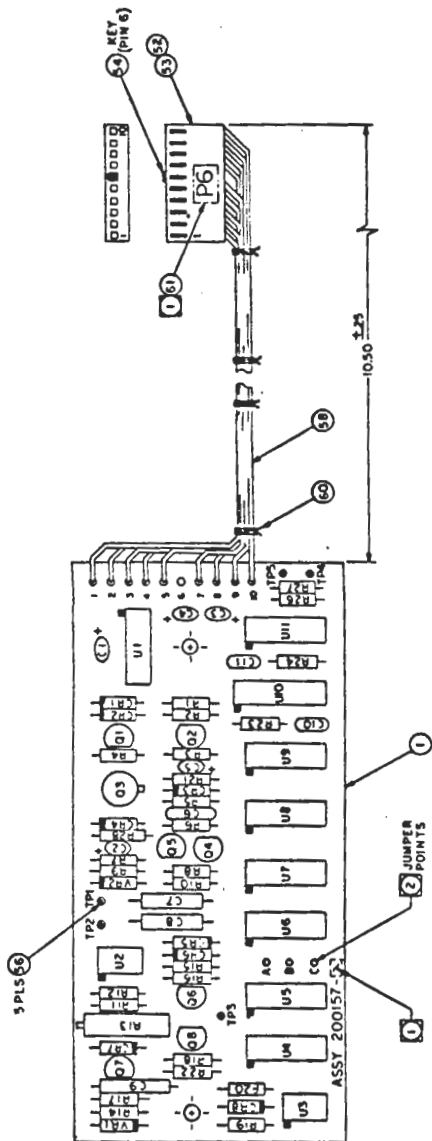
PERSCI

NET ASST 200227

ASSEMBLY, PCB, SPINDLE SERVO

MODEL 270/277 SCALE 2:1 PART OF 4 200134 F

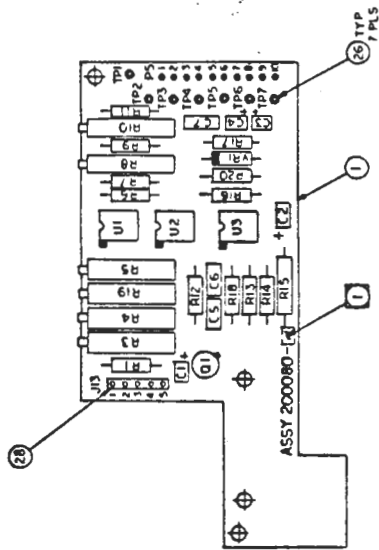
A	ENGIN REL	11-5	
B	ADD ORIGINAL DESIGNER'S SIGNATURE	11-5	
C	DATE REC. AND OTHER APPROVALS	11-5	



3 SCHEMATIC REF 200115.
 2 FOR JUMPER LOCATIONS SEE W/L DASH VERSIONS
 1 MARK REF. DESIGNATIONS OR REVISION LEVEL
 IN BLACK OR WHITE CHARACTERS IN APPRO-
 PRIATE LOCATIONS UNLESS OTHERWISE SPECIFIED:

PERSCI, INC.	
PERSCI	
PHASED LOCKED LOOP	2
ASSY. PCB.	2
MODEL 270272	2

REV	REVISIONS	DESCRIPTION
A	ENGIN REL	
B	ADD'D INPT'D	
C	ECO 7	
D	ECO 62	MFG REL
E	ECO 76	
F	ECO 88	



2. SCHEMATIC REF. 200096.

① MARK REF. DESIGNATIONS OR REVISION LEVEL
 .12 HIGH BLACK/WHITE CHARACTERS IN A 10-BOX
 AREA SHOWN.
 UNLESS OTHERWISE SPECIFIED:

PERSCI, INC.

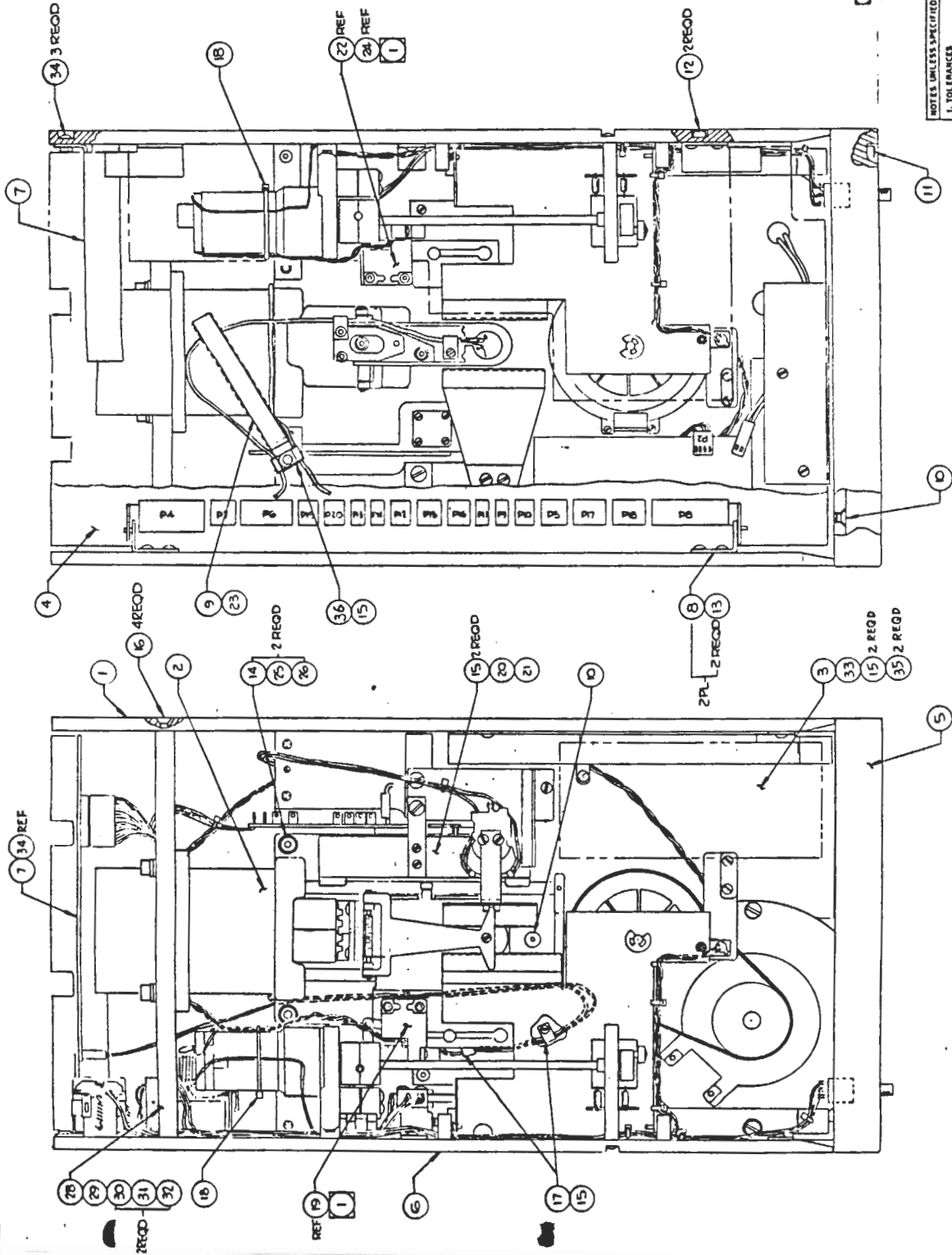
NEXT ASSY.
 -200079

ASSEMBLY PCB LAMP AMPLIFIER

MODEL 70720

SCALE 7:1
 SHEET 1 OF 3 200080E

REV	DESCRIPTION	DATE	BY
A	ENGR. CHANGE	11/17/74	
B	SEE ECD 99	11/17/74	
C	SEE ECD 104	11/17/74	



ITEMS 19 & 22 ARE WRITE PROTECT OPTIONAL ASSEMBLIES SHOWN INSTALLED. INSTALL ITEM 24 WHEN ITEM 22 IS NOT REQUIRED.
 NOTES: UNLESS OTHERWISE SPECIFIED PART NO. 200131-1XX

NOTES UNLESS SPECIFIED		CHECK		DATE	
1. TOLERANCES	XX ±	DESIGN	DATE	APPROV.	DATE
2. BREAK ALL SHARP EDGES APPROX. .010		APP'R			
3. MASK SURFACES		MATERIAL			
4. ALL DIMS IN INCHES		FINISH			
		MODEL NO.	277	SCALE	1/A D
		RELT ASSY		NO. OF SCALE	100
				WEIGHT	200131
					C
					SHEET OF 1

PERSCI
 PerSci Incorporated
 ASSY, DUAL DISKETTE DRIVE

PERSCI PARTS

The parts listed in this section are PerSci Parts for the Model 270 Dual Density Drive 200131-001.

The prices quoted were received from PerSci on 1/17/79. All parts listed here should be ordered direct from PerSci. Their terms are C.O.D.

Dealers who order parts on their business letterhead can receive parts in accordance with the OEM price schedule included.

Any parts ordered from PerSci should say for Drive Part Number 20013122-001 so that parts are compatible with the drive we use in the Helios II Disk System.

You may order your parts from:

PerSci Inc.
Attention: Customer Service Department
12210 Nebraska Avenue
West Los Angeles, California 90025
Telephone (213) 820-3766
Telex 687444

**Model 270
PerSci Parts**

<u>PART NO.</u>	<u>DESCRIPTION</u>	<u>OEM PRICE</u>	<u>LIST PRICE</u>
100011-003	Spindle Hub Bearings	5.00	6.50
100019	Micro-Sw.(Disk Presence)	3.00	5.00
100026	Momentary-Sw.(Eject)	5.00	7.00
100028	Micro-Switch(Cam)	2.00	3.00
150090-001	Diskette	10.00	10.00
150090-007	Alignment Diskette	45.00	45.00
200042	Belt,Spindle Motor	3.00	5.00
200068	Transducer Assy. (Mask)	25.00	33.00
200079	Lamp Amplifier Board	35.00	46.00
200087-002	Pressure Pad (Gray)	.50	.65
200134	Spindle Servo Board	50.00	65.00
200137	Positioner Servo Board	70.00	100.00
200213-002	Spindle Servo	15.00	20.00
200214	Head Load Assy. Side 0	15.00	20.00
200216	Head Load Assy. Side 1	10.00	15.00
200218	Spindle Motor	90.00	120.00
200221	LED Assy. Side 0	10.00	13.00
200222	LED Assy. Side 1	10.00	13.00
200223-002	Write Protect Assy. Side 0	18.00	24.00
200224	Write Protect Assy. Side 1	18.00	24.00
200228	Positioner Assy. Complete	295.00	400.00
200247-002	Lamp Assy. Positioner	4.00	5.00
200258	Data Separator (Dual Density)	45.00	60.00
200263-001	Data & Interface Board	105.00	250.00
200269	Head & Carriage Assy. Side 0	50.00	70.00
200270-001	Head & Carriage Assy. Side 1	60.00	80.00
200272	Scale Assy.	25.00	33.00
200274-002	Photosense Assy. (Index)	5.00	10.00
200308-001	Solar Cell Assy.	2.70	3.50
200310	Bezel	9.00	12.00
200394-001	Eject Motor Assy. Side 0	50.00	65.00
200394-002	Eject Motor Assy. Side 1	50.00	65.00
200432	Cone Assy.	9.00	12.00
200441	Card Insert (Head Restraint)	1.00	1.30
200458	Holder, Pressure Pad	2.00	2.60
200594	Cam Support	2.00	2.50
200631-001	Eject Arm Side 1	1.65	2.00
200631-002	Eject Arm Side 0	1.65	2.00

The following replacement parts are available on a limited basis from the Processor Technology factory at the following price schedule. Please order parts from the Customer Service Department by the part number listed in the table.

**Processor Technology Spare Parts
PerSci Model 270 Diskette Drive**

PART NO.	DESCRIPTION	PRICE EA
100013-02	Mini Lamp, Positioner	3.75
100019	Micro-Sw. (Disk Presence)	7.50
100026	Momentary-Sw. (Eject)	12.50
150090-007	Alignment Diskette	45.00
200042	Belt, Spindle Motor	7.50
200079	Lamp Amplifier Board	87.50
200087-002	Pressure Pad (Gray)	1.25
200134	Spindle Servo Board	125.00
200218	Spindle Motor	137.50
200247-002	Lamp Assy. Positioner	10.00
200157-001	Assy, PCB, Data Separator	87.50
200263-007	Data & Interface Board	375.00
200272	Scale Assy.	62.50
200432	Cone Assy.	22.50
200458	Holder, Pressure Pad	5.00
200058	Cam, Eject (specify 0 or 1)	3.63
200131-001	270 Dual Drive	1295.00 *
150600	LM 311 IC	2.50
150602	MC 1454C-PI IC	5.75
150603	7400 IC	3.50
150604	7404 IC	3.50
150605	7408 IC	3.00
150607	7430 IC	6.25
150608	7432 IC	3.50
150609	7474 IC	4.25
150618	75453 IC	2.50
150619	LM 733 IC	3.25
150200	2N4400 Transistor	1.50
150201	2N4402 Transistor	1.50
150202	2N5460 Transistor	5.25
200059	Arm, Eject (old style)	3.50
200631-001	Arm, Eject (unit 1)	4.13
200631-002	Arm, Eject (unit 0)	4.13
200060	Holder, Lamp	4.50
200194	Assy, Support With Bearings	5.63
200220	Cam, Eject Motor (side 1)	3.75

* Limited availability

REV C.		MAT 9 EPT 4 - 178 T		DWG NO. 200131-000		REV C		SHEET 1 OF 2	
TITLE		ASSY DUAL DISKETTE DRIVE		PERSCI, INC.					
ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS					
1	ASSY CENTER AND UPPER DECK BM	200227	1						
2	ASSY POSITIONER BM	200228	1						
3	ASSY DATA SEPARATOR BM			SEE BUILD ML					
4	ASSY P.C.B. DATA AND INTERFACE BM			SEE BUILD ML					
5	BEZEL	200192-002	1						
6	ASSY EJECT AND CARRIER BM			SEE BUILD ML					
7	ASSY P.C.B. POSITION SERVO BM	200137	1						
8	ASSY DATA BD PIVOT BM	200226	2						
9	GUIDE HEAD CABLE	200260	1						
10	SCREW FL HD 82° SOC	100030-408	2	8-32 x 1/2					
11	SCREW SOC HD CAP	100003-416	1	8-32 x 1.00					
12	SCREW SOC HD CAP	100003-408	2	8-32 x 1/2					
13	SCREW BD HD SLOTTED	100002-203	4	4-40 x 3/16					
14	SCREW SOC HD CAP	100003-512	2	10-32 x 3/4					
15	SCREW BD HD SLOTTED	100002-204	7	4-40 x 1/4					
16	SCREW 82° FL HD SLOTTED	100029-408	4	8-32 x 1/2					
17	CLAMP CABLE	100005-003	2						
18	TIE WRAP	100033-007	2						
19	ASSY, WRITE PROTECT (SIDE 0) O			SEE BUILD ML					
20	BRACKET, COVER	200350	1						
21	COVER, SCALE	200311	1						
22	ASSY, WRITE PROTECT (SIDE 1) O			SEE BUILD ML					
23	TUBING, HEAT SHRINK	100095-006	AE						
24	BRACKET, WRITE PROTECT			SEE BUILD ML					
25	WASHER, FLAT REDUCED O.D.	100099-500	2	#10					
26	WASHER, SPLIT LOCK	100007-500	2	#10					
27	LABEL, IDENT	200088	1						
28	BAE, SUPPORT	200390	1						
29	SUPPORT MAGNET	200391	1						
30	SCREW SOC HD CAP	100003-610	2	1/4 x 5/8					
31	WASHER, SPLIT LOCK	100007-600	2	#1/4					
32	WASHER, FLAT	100008-600	2	#1/4					
33	BRACKET, PLO ED	200172	1						

TITLE	ASSY., P.C.B. SPINDLE SERVO	DWG NO. 200134	REV F	SHEET 3 OF 4
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PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
34	CAPACITOR, Mylar 5% 1 Uf	150104-105	2	C6, 10
35				
36	RESISTOR 1/4W 5% 150	150002-151	1	R27
37	RESISTOR 1/4W 5% 1K	150002-102	1	R26
38	RESISTOR 2W 5% 15	150004-150	1	R15
39				
40	RESISTOR 1/4W 1% 1K	150001-1001	1	R4
41	RESISTOR 1/4W 1% 1.1K	150001-1101	1	R5
42	RESISTOR 1/4W .1% 40K	150009-4002	2	R13, 14
43				
44	RESISTOR 1/4W 5% 47	150000-470	1	R24
45	RESISTOR 1/4W 5% 100	150000-101	2	R25, 28
46	RESISTOR 1/4W 5% 510	150000-511	2	R12, 21
47	RESISTOR 1/4W 5% 1K	150000-102	4	P 17,18,19,22
48	RESISTOR 1/4W 5% 10K	150000-103	5	R6,8,10,11,20
49	RESISTOR 1/4W 5% 51K	150000-513	2	R3, 9
50	RESISTOR 1/4W 5% 100K	150000-104	2	R7, 16
51	RESISTOR 1/4W 5% 390K	150000-394	1	R16
52	RESISTOR 1/4W 5% 560K	150000-564	1	R1
53	RESISTOR 1/4W 5% 220K	150000-224	1	R23
54				
55				
56				
57				
58	CONNECTOR, ANGLE 2 Pin	100042-002	1	J1
59	CONNECTOR, ANGLE 4 Pin	100040-004	1	J2
60				
61				
62				
63				
64				
65				
66				

200134

REV E
 DWG NO. 200157-000

MA' 9 EPT 4 - 180 BT

TITLE ASSY. P.C.B. PHASED LOCKED DOUBLE P DATA SEPARATOR
 DWG NO. 200157-000
 REV E SHEET 2 OF 3

MOD 70/270/277

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	PROCESSED BOARD	200155	1	REV D
2	SUBASSY, HARNESS	200398-005	1	P6
3				
4	IC LN311N	150600	1	U3
5	IC MC1458-P1	150602	1	U2
6	IC 7400	150603	2	U1, 8
7	IC 7474	150609	4	U4, 6, 7, 9
8	IC 7486	150611	1	U5
9	IC 74123	150612	1	U10
10	IC 7416	150621	1	U11
11				
12				
13				
14	TRANSISTOR 2N4400	150200	2	Q2, 6
15	TRANSISTOR 2N4402	150201	4	Q1, 4, 7, 8
16	TRANSISTOR 2N5460	150202	1	Q5
17	TRANSISTOR 2N2913	150203	1	Q3
18				
19				
20	DIODE 1N3064	150300	8	CR1,2,3,4,5,6,7,8
21	DIODE, ZENER 1N752A	150302	1	VR1
22	DIODE, ZENER 1N751A	150311	1	VR2
23				
24				
25	CAPACITOR, MICA 100 Pf	150102-101	3	C6, 10, 11
26	CAPACITOR, MYLAR 1000 Pf	150101-102	1	C9
27	CAPACITOR, MYLAR .0015 Uf	150101-152	1	C7
28	CAPACITOR, MYLAR .01 Uf	150101-103	1	C8
29	CAPACITOR, TANPL., 10% 1 Uf	150100-105	5	C1, 2, 3, 4, 5
30				
31				
32				
33	RESISTOR VAR., 20 TURN 2K	150003-202	1	R13

TITLE	ASSY. P.C.B. POSITIONER SERVO	DWG NO. 200137	REV C	SHEET 3 OF 5
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PERSCI, INC.

200137

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
34	RESISTOR, VAR 2K	150003-202	1	R33
35				
36	RESISTOR, 3W 5% 1	150008-010	2	R77,78
37				
38	RESISTOR, 1/4W 1% 1K	150001-1001	12	R54,55,56,57,58,59,60,61,62,63,64,65
39	RESISTOR, 1/4W 1% 10K	150001-1002	7	R13,14,15,28,29,52,53
40	RESISTOR, 1/4W 1% 80.6K	150001-8062	1	R48
41				
42	RESISTOR, 1/4W 5% 100	150000-101	1	R69
43	RESISTOR, 1/4W 5% 200	150000-201	2	R2,4
44	RESISTOR, 1/4W 5% 510	150000-511	1	R47
45	RESISTOR, 1/4W 5% 750	150000-751	1	R42
46	RESISTOR, 1/4W 5% 1K	150000-102	14	R5,8,9,16,18,23,27,35,39,41,45,72,74,43
47	RESISTOR, 1/4W 5% 1.2K	150000-122	1	R46
48	RESISTOR, 1/4W 5% 2K	150000-202	1	R38
49	RESISTOR, 1/4W 5% 3.3K	150000-332	2	R67,71
50	RESISTOR, 1/4W 5% 3.9K	150000-392	2	R1,3
51	RESISTOR, 1/4W 5% 4.7K	150000-472	1	R34
52	RESISTOR, 1/4W 5% 5.1K	150000-512	3	R12,20,75
53	RESISTOR, 1/4W 5% 10K	150000-103	7	R6,10,11,30,31,51,73
54	RESISTOR, 1/4W 5% 20K	150000-203	1	R37
55	RESISTOR, 1/4W 5% 22K	150000-223	3	R17,24,26
56	RESISTOR, 1/4W 5% 39K	150000-393	1	R68
57	RESISTOR, 1/4W 5% 51K	150000-513	1	R7
58	RESISTOR, 1/4W 5% 100K	150000-104	8	R21,32,36,40,44,66,70,49
59				
60				
61	RESISTOR, 1/4W 5% 390K	150000-394	1	R19
62	RESISTOR, 1/4W 5% 3.9MEG	150000-395	1	R76
63	RESISTOR, 1/4W 5% 1MEG	150000-105	2	R22,25
64				
65				
66				

DWG NO. 2002.000

TITLE ASSEMBLY, PCB DATA AND INTERF 9 EPT 4 - 184 G NO. 200263-000

REV H SHEET 2 OF 6

MODEL 270 BASIC BOARD

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	BOARD, PROCESSED	200262	1	REV C
2				
3	BRACKET, DATA BD	200171	1	REV B
4	INSULATOR, DATA BD	200174	1	REV A
5				
6				
7				
8				
9				
10				
11	IC LM311N	150600	3	U18, 22, 61
12	IC MC1406L	150601	1	U55
13	IC MC1458C-P1	150602	2	U40, 51
14	IC 7400	150603	5	U15, 28, 53, 57, 60
15	IC 7404	150604	5	U20, 30, 38, 41, 49
16	IC 7408	150605	4	U26, 29, 45, 50
17	IC 7432	150608	4	U19, 54, 56, 58
18	IC 7474	150609	6	U14, 24, 39, 46, 47, 52
19	IC 7486	150611	1	U21
20	IC 74123	150612	4	U10, 12, 25, 44
21	IC 74193	150614	2	U42, 43
22	IC 75451	150616	1	U17
23	IC 75452	150617	2	U31, 36
24	IC 75453	150618	9	U2, 3, 4, 5, 6, 7, 8, 23, 59
25	IC 72733	150619	2	U33, 35
26	IC 7416	150621	2	U13, 48
27	IC 7406	150622	1	U37
28	IC SN72306P	150646	2	U34, 32
29				
30	RESISTOR NETWORK 4.7K	150050	1	U9
31	RESISTOR NETWORK 220/330	150051	1	U1
32				
33				

REV H
DWG NO 200263-000

TITLE ASSEMBLY, PCB DATA AND INTERFERENCE 9. EPT 4 - 186 DWG NO. 200263-000 REV H SHEET 4 OF 6

MODEL 270 BASIC BOARD PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
55	CAPACITOR, TANTL 22UF	150100-226	1	C48
56				
57				
58				
59	RESISTOR, VARIABLE 2K	150003-202	1	R154
60				
61	RESISTOR 1/2 W., 5% 10	150002-100	2	R121,126
62	RESISTOR 1/2 W., 5% 47	150002-470	2	R69,70
63	RESISTOR 1/2 W., 5% 68	150002-680	4	R104,105,106,107
64	RESISTOR 1/2 W., 5% 1K	150002-102	1	R169
65	RESISTOR, 1/2 W., 1% 1.50K	150001-1501	1	R81
66	RESISTOR 1/2 W., 1% 332	150001-3320	2	R13,14
67	RESISTOR 1/2 W., 1% 1.78K	150001-1781	1	R138
68	RESISTOR 1/2 W., 1% 3.01K	150001-3011	1	R78
69	RESISTOR 1/2 W., 1% 10K	150001-1002	5	R108,109,147,148,149
70	RESISTOR 1/2 W., 1% 24.9K	150001-2492	1	R152
71	RESISTOR 1/2 W., 1% 30.1K	150001-3012	1	R146
72	RESISTOR 1/2 W., 1% 4.64K	150001-4641	2	R86,87
73				
74	RESISTOR 1/2 W., 5% 10	150000-100	13	R3,10, 12,18,19, 33,34,37,38,41, 42,56,77
75	RESISTOR 1/2 W., 5% 47	150000-470	2	R26,27
76	RESISTOR 1/2 W., 5% 100	150000-101	13	R23,29,35,36,39, 40,82,83,84,85, 101,103,128
77				
78	RESISTOR 1/2 W., 5% 220	150000-221	7	R5,7,49,53,58, 120,125
79	RESISTOR 1/2 W., 5% 330	150000-331	13	R6,8,9,15,16,17, 59,65,66,67,68, 119,124

MATERIAL LIST

REV F
DWG NO. 200080

TITLE ASSY. P.C.B. LAMP AMPLIFIER 9 EPT 4 - 187 00080
 IWG NO. 00080
 REV F SHEET 2 OF

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	BOARD, PROCESSED	200089	1	REV C
2				
3				
4				
5	IC 1458	150602	3	U1, 2, 3
6				
7	TRANSISTOR 2N2222 A	150208	1	Q1
8				
9	DIODE, ZENER IN752 A	150302	1	VR1
10	CAPACITOR, MICA 100 PF	150102-101	3	C5,6,7
11	CAPACITOR, TANT. 1 UF	150100-105	4	C1, 2, 3, 4
12				
13	RESISTOR, VAR 2K	150003-202	6	R3, 4, 5, 8, 10,
14				
15	RESISTOR 1/2W 5% 33	150002-330	1	R15
16	RESISTOR 1/8W 1% 1.00K	150001-1001	1	R6
17	RESISTOR 1/8W 1% 5.62K	150001-5621	1	R17
18				
19	RESISTOR 1/4W 5% 1K	150000-102	2	R14, 16
20	RESISTOR 1/4W 5% 4.7K	150000-472	1	R20
21	RESISTOR 1/4W 5% 10K	150000-103	1	R1
22	RESISTOR 1/4W 5% 51K	150000-513	1	R12
23	RESISTOR 1/4W 5% 560K	150000-564	4	R9, 11, 18, 13
24	RESISTOR 1/4W 5% 5.6MEG	150000-565	1	R7
25				
26				
27	PIN, MALE	100046	7	TP1,2,3,4,5,6,7
28	CONNECTOR, 5 Pin	100041-005	1	J13
29				
30				
31				
32				
33				

MATERIAL LIST

TITLE ASSY POSITIONER	9 EPT 4 - 189	DWG NO. 200228	REV A	SHEET 1 OF 2
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PERSCI, INC.

DWG NO. 200228

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	ASSY VOICE COIL	200024	1	
2	ASSY MAGNET	200023	1	
3	ASSY TRANSDUCER AMP	200079	1	
4				
5	ASSY TRANSDUCER	200068	1	
6	ASSY CARRIAGE SIDE 0	200270-001	1	
7	ASSY CARRIAGE SIDE 1	200269	1	
	CLAMP, CABLE	200085	1	
9	ASSY SCALE	200272	1	
10	HOLDER PRES PAD	200244	2	
11	PAD PRESSURE	200087	2	
12	WASHER FELT	200126	1	
13	SUPPORT CARRIAGE & COIL	200181	1	
14	FRAME POSITIONER	200193	1	
15	ROD GUIDE	200017	2	
16	PLATE DEFLEXION	200254	1	
17	SUPPORT HEAD SIDE 1	200253	1	
18	SPACER HEAD SUPPORT	200255	1	
19	PIN PIVOT	200304	2	
20	ARM PRES. PAD	200033	2	
21	SPRING TORSION	200303	2	
22	RETAINER. FELT WASHER	200306	1	
23	"O" RING RUBBER	100061	1	
24	RING EXT "E" TYPE	100001-002	4	
25	SCREW SOC HD CAP	100003-312	1	6-32 X 3/4
26	SCREW SOC HD CAP	100003-306	2	6-32 X 1/2
27	SCREW SOC HD CAP	100003-205	2	4-40 X 1/2
28				
29	SCREW SET HEX SOC	100004-402	1	8-32 X 1/8
30	SCREW HEX SOC BT HD	100014-304	4	6-32 X 1/4
31	SCREW HEX SOC BT HD	100014-202	1	4-40 X 3/16
32	SCREW HEX SOC BT HD	100014-105	1	4-40 X 5/16
33	SCREW HEX SOC BT HD	100014-208	2	4-40 X 1/2

200219-001

TITLE ASSY EJECT AND CARRIER 9 EPT 4 - 190	DWG NO. 200219-001	P-V D	SHEET 2 OF 3
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PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
34	ARM SUPPORT DUAL	200194	2	
35	SPRING, TENSION	100022-002	4	
36	PIN ROLL	100006-116	2	
37	SPRING COMPRESSION	100021-003	2	
38	SCREW BD HD SLOTTED	100002-216	4	4-40 X 1.00
39	BLOCK CARRIER PIVOT	200202-002	2	
40	SCREW BD HD SLOTTED	100002-410	4	8-32 X 5/8
41	BRACKET LOAD SWITCH	200147	1	
42	SWITCH MICRO (LEVER)	100019	2	
43	SCREW BD HD SLOTTED	100002-208	4	4-40 X 1/2
44	SCREW BD HD SLOTTED	100002-204	2	4-40 X 1/4
45				SEE OTHER DASH NO. ML'S
46	BLOCK PIVOT	200043	4	
47	SWITCH MICRO	100028	4	
48	CAM EJECT MTR SIDE O.	200058	1	
49	BRACKET EJECT MTR	200289	2	
50	PLATE SIDE LOWER DECK	200148	1	
51				SEE OTHER DASH NO. ML'S
52	SUBASSY, GEAR MOTOR	200394-001	1	
53	BRACKET CIRCUIT BD	200167-001	1	
54	SCREW SET HEX SOC	100004-405	2	6-32 X 5/16
55	SUBASSY, GEAR MOTOR	200394-002	1	
56	PIN ROLL	100006-112	2	
57	TAPE ADHESIVE TEFLON	100059	A/R	
58	SCREW SET HEX SOCKET	100004-403	2	
59	SCREW SET HEX SOCKET	100005-414	1	4-40 X 7/8
60	ADHESIVE TAPE	100002	A/R	
61	LEVER		1	
62				
63	WIRE, 24 AWG	U.L. 100037-024	A/R	
64				
65				
66				

REV B
 DWG NO. 200227

MAY 9 EPT 4 - 191 BT

TITLE ASSY CENTER AND UPPERDECK
 DWG NO. 200227
 REV B SHEET 1 OF 2

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	ASSY, SPINDLE MOTOR	200218	1	
2	ASSY, DISKETTE SPINDLE	200217	1	
3	ASSY, HD. ENG. SOL (SIDE 0)	200214	1	
4	ASSY, HD. ENG. SOL (SIDE 1)	200216	1	
5	ASSY, SPINDLE SENSOR	200213-002	1	
6	ASSY, LED (SIDE 0)	200221	1	
7	ASSY, LED (SIDE 1)	200222	1	
8				
9				
10	ASSY, F.C.E. SPINDLE SERVO	200134	1	
11				
12	SPEC BELT SPINDLE MTR.	200042	1	
13	GUIDE DISKETTE	200047-001	2	
14	GUIDE DISKETTE	200047-002	2	
15	STOP DISKETTE SIDE 0	200182	1	
16	STOP DISKETTE SIDE 1	200183	1	
17	PLATE CENTER DECK	200149	1	
18	PLATE SIDE UPPER DECK	200170	1	
19				
20	BRACKET LIFTER PIVOT	200164	1	
21	LIFTER PRES ARM	200150	1	
22	SHAFT LIFTER	200178	1	
23	SUPPORT DISKETTE REF.	200047	2	
24	SHAFT EJECT DUAL	200196	1	
25	CRANK EJECT	200007	2	
26	ACTUATOR EJECT	200006	2	
27	ARM EJECT	200059	2	
28	GUIDE EJECT ARM	200046-001	1	
29	GUIDE EJECT ARM	200046-002	1	
30	SPRING TORSION	200009	1	
31	SPRING TORSION	200169	1	
32	SPACER, PHENOLIC	200103-203	1	
33	SPACER ALUM. ROUND	200021-002	2	

MATERIAL LIST

TITLE ASSY CENTER AND UPPERDECK 9 EPT 4 - 192 DWG NO. 200227 REV B SHEET 1 OF 2

PERSCI, INC.

REV B
DWG NO. 200227

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	ASSY, SPINDLE MOTOR	200218	1	
2	ASSY, DISKETTE SPINDLE	200217	1	
3	ASSY, HD. ENG. SOL (SIDE 0)	200214	1	
4	ASSY, HD. ENG. SOL (SIDE 1)	200216	1	
5	ASSY, SPINDLE SENSOR	200213-002	1	
6	ASSY, LED (SIDE 0)	200221	1	
7	ASSY, LED (SIDE 1)	200222	1	
8				
9				
10	ASSY, F.C.E., SPINDLE SERVO	200134	1	
11				
12	SPEC BELT SPINDLE MTR.	200042	1	
13	GUIDE DISKETTE	200047-001	2	
14	GUIDE DISKETTE	200047-002	2	
15	STOP DISKETTE SIDE 0	200182	1	
16	STOP DISKETTE SIDE 1	200183	1	
17	PLATE CENTER DECK	200149	1	
18	PLATE SIDE UPPER DECK	200170	1	
19				
20	BRACKET LIFTER PIVOT	200164	1	
21	LIFTER PRES ARM	200150	1	
22	SHAFT LIFTER	200178	1	
23	SUPPORT DISKETTE REF.	200184	2	
24	SHAFT EJECT DUAL	200196	1	
25	CRANK EJECT	200007	2	
26	ACTUATOR EJECT	200006	2	
27	ARM EJECT	200059	2	
28	GUIDE EJECT ARM	200046-001	1	
29	GUIDE EJECT ARM	200046-002	1	
30	SPRING TORSION	200009	1	
31	SPRING TORSION	200169	1	
32	SPACER, PHENOLIC	200103-203	1	
33	SPACER ALUM. ROUND	200021-002	2	

9.21-

MATERIAL LIST

TITLE: ASSY EJECT AND CARRIER 9 EPT 4 - 193 DWG NO. 200219-001 P-V D SHEET 2 OF 3

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
34	ARM SUPPORT DUAL	200194	2	
35	SPRING, TENSION	100022-002	4	
36	PIN ROLL	100006-116	2	
37	SPRING COMPRESSION	100021-003	2	
38	SCREW BD HD SLOTTED	100002-216	4	4-40 X 1.00
39	BLOCK CARRIER PIVOT	200202-002	2	
40	SCREW BD HD SLOTTED	100002-410	4	8-32 X 5/8
41	BRACKET LOAD SWITCH	200147	1	
42	SWITCH MICRO (LEVER)	100019	2	
43	SCREW BD HD SLOTTED	100002-208	4	4-40 X 1/2
44	SCREW BD HD SLOTTED	100002-204	2	4-40 X 1/4
45				SEE OTHER DASH NO. ML'S
46	BLOCK PIVOT	200043	4	
47	SWITCH MICRO	100028	4	
48	CAM EJECT MTR SIDE O.	200058	1	
49	BRACKET EJECT MTR	200289	2	
50	PLATE SIDE LOWER DECK	200148	1	
51				SEE OTHER DASH NO. ML'S
52	SUBASSY, GEAR MOTOR	200394-001	1	
53	BRACKET CIRCUIT BD	200167-001	1	
54	SCREW SET HEX SOC	100004-405	2	6-32 X 5/16
55	SUBASSY, GEAR MOTOR	200394-002	1	
56	PIN ROLL	100006-112	2	
57	TAPE ADHESIVE TEFLON	100059	A/R	
58	SCREW SET HEX SOCKET	100004-403	2	
59	SCREW SET HEX SOCKET	100004-404	1	4-40 X 7/8
60	ADHESIVE TAPE	100012	A/R	
61	LEVER		1	
62				
63	WIRE, 24 AWG	U.L. 100037-024	A/R	
64				
65				
66				

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	ASSY VOICE COIL	200024	1	
2	ASSY MAGNET	200023	1	
3	ASSY TRANSDUCER AMP	200079	1	
4				
5	ASSY TRANSDUCER	200068	1	
6	ASSY CARRIAGE SIDE 0	200270-001	1	
7	ASSY CARRIAGE SIDE 1	200269	1	
	CLAMP, CABLE	200085	1	
9	ASSY SCALE	200272	1	
10	HOLDER PRES PAD	200244	2	
11	PAD PRESSURE	200087	2	
12	WASHER FELT	200126	1	
13	SUPPORT CARRIAGE & COIL	200181	1	
14	FRAME POSITIONER	200193	1	
15	ROD GUIDE	200017	2	
16	PLATE DEFLEXION	200254	1	
17	SUPPORT HEAD SIDE 1	200253	1	
18	SPACER HEAD SUPPORT	200255	1	
19	PIV PIVOT	200304	2	
20	ARM PRES. PAD	200033	2	
21	SPRING TORSION	200303	2	
22	RETAINER, FELT WASHER	200306	1	
23	"O" RING RUBBER	100061	1	
24	RING EXT "E" TYPE	100001-002	4	
25	SCREW SOC HD CAP	100003-312	1	6-32 X 3/4
26	SCREW SOC HD CAP	100003-301	2	6-32 X 1/2
27	SCREW SOC HD CAP	100003-305	2	4-40 X 1/2
28				
29	SCREW SET HEX SOC	100004-402	1	8-32 X 1/8
30	SCREW HEX SOC BT HD	100014-304	4	6-32 X 1/4
31	SCREW HEX SOC BT HD	100014-203	1	4-40 X 5/16
32	SCREW HEX SOC BT HD	100014-205	1	4-40 X 5/16
33	SCREW HEX SOC BT HD	100014-208	2	4-40 X 1/2

REV
FDWG NO.
200080

LIST

TITLE ASSY. P.C.B.
LAMP AMPLIFIER

9 EPT 4 - 196

DWG NO.
200080REV
F

SHEET 2 OF

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	BOARD, PROCESSED	200089	1	REV C
2				
3				
4				
5	IC 1458	150602	3	U1, 2, 3
6				
7	TRANSISTOR 2N2222 A	150208	1	Q1
8				
9	DIODE, ZENER IN752 A	150302	1	VR1
10	CAPACITOR, MICA 100 PF	150102-101	3	C5,6,7
11	CAPACITOR, TANT. 1 UF	150100-105	4	C1, 2, 3, 4
12				
13	RESISTOR, VAR 2K	150003-202	6	R3, 4, 5, 8, 10,
14				
15	RESISTOR $\frac{1}{2}$ W 5% 33	150002-330	1	R15
16	RESISTOR $\frac{1}{8}$ W 1% 1.00K	150001-1001	1	R6
17	RESISTOR $\frac{1}{8}$ W 1% 5.62K	150001-5621	1	R17
18				
19	RESISTOR $\frac{1}{4}$ W 5% 1K	150000-102	2	R14, 16
20	RESISTOR $\frac{1}{4}$ W 5% 4.7K	150000-472	1	R20
21	RESISTOR $\frac{1}{4}$ W 5% 10K	150000-103	1	R1
22	RESISTOR $\frac{1}{4}$ W 5% 51K	150000-513	1	R12
23	RESISTOR $\frac{1}{4}$ W 5% 560K	150000-564	4	R9, 11, 18, 13
24	RESISTOR $\frac{1}{4}$ W 5% 5.6MEG	150000-565	1	R7
25				
26				
27	PIN, MALE	100046	7	TP1,2,3,4,5,6,7
28	CONNECTOR, 5 Pin	100041-005	1	J13
29				
30				
31				
32				
33				

REV H
DWG NO. 200263

COMPONENT LIST

TITLE		9 EPT 4 - 197		DWG NO.	REV	SHEET 4 OF 4
ASSEMBLY, PCB DATA AND INTERFACE				200263-000	H	
MODEL 270 BASIC BOARD				PERSCI, INC.		
ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS		
55	CAPACITOR, TANTL 22UF	150100-226	1	C48		
56						
57						
58						
59	RESISTOR, VARIABLE 2K	150003-202	1	R154		
60						
61	RESISTOR 1/2 W., 5% 10	150002-100	2	R121,126		
62	RESISTOR 1/2 W., 5% 47	150002-470	2	R69,70		
63	RESISTOR 1/2 W., 5% 68	150002-680	4	R104,105,106,107		
64	RESISTOR 1/2 W., 5% 1K	150002-102	1	R169		
65	RESISTOR, 1/2 W., 1% 1.50K	150001-1501	1	R81		
66	RESISTOR 1/2 W., 1% 332	150001-3320	2	R13,14		
67	RESISTOR 1/2 W., 1% 1.78K	150001-1781	1	R138		
68	RESISTOR 1/2 W., 1% 3.01K	150001-3011	1	R78		
69	RESISTOR 1/2 W., 1% 10K	150001-1002	5	R108,109,147,148,149		
70	RESISTOR 1/2 W., 1% 24.9K	150001-2492	1	R152		
71	RESISTOR 1/2 W., 1% 30.1K	150001-3012	1	R146		
72	RESISTOR 1/2 W., 1% 4.64K	150001-4641	2	R86,87		
73						
74	RESISTOR 1/2 W., 5% 10	150000-100	13	R3,10, 12,18,19, 33,34,37,38,41, 42,56,77		
75	RESISTOR 1/2 W., 5% 47	150000-470	2	R26,27		
76	RESISTOR 1/2 W., 5% 100	150000-101	13	R23,29,35,36,39, 40,82,83,84,85, 101,103,128		
77						
78	RESISTOR 1/2 W., 5% 220	150000-221	7	R5,7,49,53,58, 120,125		
79	RESISTOR 1/2 W., 5% 330	150000-331	13	R6,8,9,15,16,17, 59,65,66,67,68, 119,124		

REV H
DWG NO. 200269 EPT 4 - 199
TITLE
ASSEMBLY, PCB DATA AND INTERFACEDWG NO.
200263-000REV
H

SHEET 2 OF 6

MODEL 270 BASIC BOARD

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	BOARD, PROCESSED	200262	1	REV C
2				
3	BRACKET, DATA BD	200171	1	REV B
4	INSULATOR, DATA BD	200174	1	REV A
5				
6				
7				
8				
9				
10				
11	IC LM311N	150600	3	U18, 22, 61
12	IC MC1406L	150601	1	U55
13	IC MC1458C-P1	150602	2	U40, 51
14	IC 7400	150603	5	U15, 28, 53, 57, 60
15	IC 7404	150604	5	U20, 30, 38, 41, 49
16	IC 7408	150605	4	U26, 29, 45, 50
17	IC 7432	150608	4	U19, 54, 56, 58
18	IC 7474	150609	6	U14, 24, 39, 46, 47, 52
19	IC 7486	150611	1	U21
20	IC 74123	150612	4	U10, 12, 25, 44
21	IC 74193	150614	2	U42, 43
22	IC 75451	150616	1	U17
23	IC 75452	150617	2	U31, 36
24	IC 75453	150618	9	U2, 3, 4, 5, 6, 7, 8, 23, 59
25	IC 72733	150619	2	U33, 35
26	IC 7416	150621	2	U13, 48
27	IC 7406	150622	1	U37
28	IC SN72306P	150646	2	U34, 32
29				
30	RESISTOR NETWORK 4.7K	150050	1	U9
31	RESISTOR NETWORK 220/330	150051	1	U1
32				
33				

MATERIAL LIST

DWG NO. 200137

TITLE ASSY. P.C.B. 9 EPT 4 - 200 POSITIONER SERVO	DWG NO. 200137	REV C	SHEET 3 OF 5
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PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
34	RESISTOR, VAR 2K	150003-202	1	R33
35				
36	RESISTOR, 3W 5% 1	150008-010	2	R77,78
37				
38	RESISTOR, 1/4W 1% 1K	150001-1001	12	R54,55,56,57,58,59,60,61,62,63,64,65
39	RESISTOR, 1/4W 1% 10K	150001-1002	7	R13,14,15,28,29,52,53
40	RESISTOR, 1/4W 1% 80.6K	150001-8062	1	R48
41				
42	RESISTOR, 1/4W 5% 100	150000-101	1	R69
43	RESISTOR, 1/4W 5% 200	150000-201	2	R2,4
44	RESISTOR, 1/4W 5% 510	150000-511	1	R47
45	RESISTOR, 1/4W 5% 750	150000-751	1	R42
46	RESISTOR, 1/4W 5% 1K	150000-102	14	R5,8,9,16,18,23,27,35,39,41,45,72,74,43
47	RESISTOR, 1/4W 5% 1.2K	150000-122	1	R46
48	RESISTOR, 1/4W 5% 2K	150000-202	1	R38
49	RESISTOR, 1/4W 5% 3.3K	150000-332	2	R67,71
50	RESISTOR, 1/4W 5% 3.9K	150000-392	2	R1,3
51	RESISTOR, 1/4W 5% 4.7K	150000-472	1	R34
52	RESISTOR, 1/4W 5% 5.1K	150000-512	3	R12,20,75
53	RESISTOR, 1/4W 5% 10K	150000-103	7	R6,10,11,30,31,51,73
54	RESISTOR, 1/4W 5% 20K	150000-203	1	R37
55	RESISTOR, 1/4W 5% 22K	150000-223	3	R17,24,26
56	RESISTOR, 1/4W 5% 39K	150000-393	1	R68
57	RESISTOR, 1/4W 5% 51K	150000-513	1	R7
58	RESISTOR, 1/4W 5% 100K	150000-104	8	R21,32,36,40,44,66,70,49
59				
60				
61	RESISTOR, 1/4W 5% 390K	150000-394	1	R19
62	RESISTOR, 1/4W 5% 3.9MEG	150000-395	1	R76
63	RESISTOR, 1/4W 5% 1MEG	150000-105	2	R22,25
64				
65				
66				

REV E
DWG NO. 200157-000

TITLE ASSY. P.C.B. PHASED LOCKED DOUBLE F DATA SEPARATOR DWG NO 200157-000 REV E SHEET 2 OF 3

MOD 70/270/277

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	PROCESSED BOARD	200155	1	REV D
2	SUBASSY, HARNESS	200398-005	1	P6
3				
4	IC LM311N	150600	1	U3
5	IC MC1458-P1	150602	1	U2
6	IC 7400	150603	2	U1, 8
7	IC 7474	150609	4	U4, 6, 7, 9
8	IC 7486	150611	1	U5
9	IC 74123	150612	1	U10
10	IC 7416	150621	1	U11
11				
12				
13				
14	TRANSISTOR 2N4400	150200	2	Q2, 6
15	TRANSISTOR 2N4402	150201	4	Q1, 4, 7, 8
16	TRANSISTOR 2N5460	150202	1	Q5
17	TRANSISTOR 2N2913	150203	1	Q3
18				
19				
20	DIODE 1N3064	150300	8	CR1, 2, 3, 4, 5, 6, 7, 8
21	DIODE, ZENER 1N752A	150302	1	VR1
22	DIODE, ZENER 1N751A	150311	1	VR2
23				
24				
25	CAPACITOR, MICA 100 Pf	150102-101	3	C6, 10, 11
26	CAPACITOR, MYLAR 1000 Pf	150101-102	1	C9
27	CAPACITOR, MYLAR .0015 Uf	150101-152	1	C7
28	CAPACITOR, MYLAR .01 Uf	150101-103	1	C8
29	CAPACITOR, TANPL., 10% 1 Uf	150100-105	5	C1, 2, 3, 4, 5
30				
31				
32				
33	RESISTOR VAR., 20 TURN 2K	150003-202	1	R13

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
34	CAPACITOR, Mylar 5% 1 uf	150104-105	2	C6, 10
35				
36	RESISTOR $\frac{1}{2}$ W 5% 150	150002-151	1	R27
37	RESISTOR $\frac{1}{2}$ W 5% 1K	150002-102	1	R26
38	RESISTOR 2W 5% 15	150004-150	1	R15
39				
40	RESISTOR $\frac{1}{2}$ W 1% 1K	150001-1001	1	R4
41	RESISTOR $\frac{1}{2}$ W 1% 1.1K	150001-1101	1	R5
42	RESISTOR $\frac{1}{2}$ W .1% 40K	150009-4002	2	R13, 14
43				
44	RESISTOR $\frac{1}{2}$ W 5% 47	150000-470	1	R24
45	RESISTOR $\frac{1}{2}$ W 5% 100	150000-101	2	R25, 28
46	RESISTOR $\frac{1}{2}$ W 5% 510	150000-511	2	R12, 21
47	RESISTOR $\frac{1}{2}$ W 5% 1K	150000-102	4	P 17,18,19,22
48	RESISTOR $\frac{1}{2}$ W 5% 10K	150000-103	5	R6,8,10,11,20
49	RESISTOR $\frac{1}{2}$ W 5% 51K	150000-513	2	R3, 9
50	RESISTOR $\frac{1}{2}$ W 5% 100K	150000-104	2	R7, 16
51	RESISTOR $\frac{1}{2}$W 5% 300K	150000-304	1	R16
52	RESISTOR $\frac{1}{2}$ W 5% 560K	150000-564	1	R1
53	RESISTOR $\frac{1}{2}$ W 5% 220K	150000-224	1	R23
54				
55				
56				
57				
58	CONNECTOR, ANGLE 2 Pin	100042-002	1	J1
59	CONNECTOR, ANGLE 4 Pin	100040-004	1	J2
60				
61				
62				
63				
64				
65				
66				

REV C.
DWG NO. 200131

9-20-77

LIST

TITLE 9 EPT 4 - 205 DWG NO. 200131-000 REV C SHEET 1 OF 2
ASSY DUAL DISKETTE DRIVE

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS	RE
1	ASSY CENTER AND UPPER DECK BM	200227	1		BM
2	ASSY POSITIONER BM	200228	1		A
3	ASSY DATA SEPARATOR BM			SEE BUILD ML	
4	ASSY P.C.B. DATA AND INTERFACE BM			SEE BUILD ML	
5	BEZEL	200192-002	1		
6	ASSY EJECT AND CARRIER BM			SEE BUILD ML	
7	ASSY P.C.B. POSITION SERVO BM	200137	1		C
8	ASSY DATA BD PIVOT BM	200226	2		A
9	GUIDE HEAD CABLE	200260	1		
10	SCREW FL HD 82° SOC	100030-408	2	8-32 x 1/2	
11	SCREW SOC HD CAP	100003-416	1	8-32 x 1.00	
12	SCREW SOC HD CAP	100003-408	2	8-32 x 1/2	
13	SCREW BD HD SLOTTED	100002-203	4	4-40 x 3/16	
14	SCREW SOC HD CAP	100003-512	2	10-32 x 3/4	
15	SCREW BD HD SLOTTED	100002-204	7	4-40 x 1/4	
16	SCREW 82° FL HD SLOTTED	100029-408	4	8-32 x 1/2	
17	CLAMP CABLE	100005-003	2		
18	TIE WRAP	100036-007	2		
19	ASSY, WRITE PROTECT (SIDE 0) O			SEE BUILD ML	
20	BRACKET, COVER	200330	1		
21	COVER, SCALE	200311	1		
22	ASSY, WRITE PROTECT (SIDE 1) O			SEE BUILD ML	
23	TUBING, HEAT SHRINK	100095-006	AE		
24	BRACKET, WRITE PROTECT			SEE BUILD ML	
25	WASHER, FLAT REDUCED O.D.	100099-500	2	#10	
26	WASHER, SPLIT LOCK	100007-500	2	#10	
27	LABEL, IDENT	200088	1		
28	BAE, SUPPORT	200390	1		
29	SUPPORT MAGNET	200391	1		
30	SCREW SOC HD CAP	100003-610	2	1/4 x 5/8	
31	WASHER, SPLIT LOCK	100007-600	2	#1/4	
32	WASHER, FLAT	100008-600	2	#1/4	
33	BRACKET, PLO ED	200172	1		

REV A
M/L NO. 200131-0

PERSCI INCORPORATED 733012 MATERIAL LIST

TITLE ASSY, DUAL DISKETTE DRIVE				9 EPT 4 - 207		M/L NO. 200131-001		REV A
COMPILED BY:		DATE	CHECKED BY:		DATE	APPROVED BY:		DATE
						ALH 9-12-77		9-12-77
NEXT ASSY.			1ST USED ON 270		DWG SIZE NONE		SHEET 1 OF 1	

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	CODE	REMARKS	LAST REV
	USE BASIC ASSY 200131-000	B/M				
	LATEST REV AND ADD THE FOLLOWING:					
3	ASSY, DATA SEPARATOR	B/M 200157-001	1	A	000-001	E/A
4	ASSY, P.C.B. DATA AND INTERFACE	B/M 200263-007	1	A	000-007	H/D
6	ASSY, EJECT AND CARRIER	B/M 200219-001	1	A		D
24	BRACKET, WRITE PROTECT	200189	1	D	SIDE 1	A
	<i>side of head wires</i>					
	SELECTIONS AND OPTIONS					
	MODEL: 270					
	HARD SECTOR, 32 SECTORS					
	SINGLE DENSITY-PERSCI					
	REMOTE EJECT: NONE					
	WRITE PROTECT: NONE					

CODE: D = DETAIL PART WITH NO M/L A = ASSEMBLY WITH M/L
 R = REFERENCE DOCUMENT S = SHIP SEPARATE

MATERIAL LIST

TITLE ASSY DUAL DISKETTE DRIVE 9 EPT 4 - 208 WG NO. 200131-000 REV C SHEET 1 OF 2

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS	
1	ASSY CENTER AND UPPER DECK BM	200227	1		B
2	ASSY POSITIONER BM	200228	1		A
3	ASSY DATA SEPARATOR BM			SEE BUILD ML	
4	ASSY P.C.B. DATA AND INTERFACE BM			SEE BUILD ML	
5	BEZEL	200192-002	1		
6	ASSY EJECT AND CARRIER BM			SEE BUILD ML	
7	ASSY P.C.B. POSITION SERVO BM	200137	1		C
8	ASSY DATA BD PIVOT BM	200226	2		A
9	GUIDE HEAD CABLE	200260	1		
10	SCREW FL HD 82° SOC	100030-408	2	8-32 X 1/2	
11	SCREW SOC HD CAP	100003-416	1	8-32 X 1.00	
12	SCREW SOC HD CAP	100003-408	2	8-32 X 1/2	
13	SCREW BD HD SLOTTED	100002-203	4	4-40 X 3/16	
14	SCREW SOC HD CAP	100003-512	2	10-32 X 3/4	
15	SCREW BD HD SLOTTED	100002-204	7	4-40 X 1/4	
16	SCREW 82° FL HD SLOTTED	100029-408	4	8-32 X 1/2	
17	CLAMP CABLE	100005-003	2		
18	TIE WRAP	100036-007	2		
19	ASSY, WRITE PROTECT (SIDE 0) O			SEE BUILD ML	
20	BRACKET, COVER	200330	1		
21	COVER, SCALE	200311	1		
22	ASSY, WRITE PROTECT (SIDE 1) O			SEE BUILD ML	
23	TUBING, HEAT SHRINK	100095-006	AE		
24	BRACKET, WRITE PROTECT			SEE BUILD ML	
25	WASHER, FLAT REDUCED O.D.	100099-500	2	#10	
26	WASHER, SPLIT LOCK	100007-500	2	#10	
27	LABEL, IDENT	200088	1		
28	BAR, SUPPORT	200390	1		
29	SUPPORT MAGNET	200391	1		
30	SCREW SOC HD CAP	100003-610	2	1/4 X 5/8	
31	WASHER, SPLIT LOCK	100007-600	2	#1/4	
32	WASHER, FLAT	100003-600	2	#1/4	
33	BRACKET, PLO ED	200172	1		

TITLE ASSY. P.C.B. PHASED LOCKED
DOUBLE F DATA SEPARATOR

DWG NO
200157-000

REV
E

SHEET 2 OF 3

MOD 70/270/277

PERSCI, INC.

ITEM NO.	DRAWING TITLE		DWG NO.	QTY	REMARKS
1	PROCESSED BOARD		200155	1	REV D
2	SUBASSY, HARNESS		200398-005	1	P6
3					
4	IC	LM311N	150600	1	U3
5	IC	MC1458-P1	150602	1	U2
6	IC	7400	150603	2	U1, 8
7	IC	7474	150609	4	U4, 6, 7, 9
8	IC	7486	150611	1	U5
9	IC	74123	150612	1	U10
10	IC	7416	150621	1	U11
11					
12					
13					
14	TRANSISTOR	2N4400	150200	2	Q2, 6
15	TRANSISTOR	2N4402	150201	4	Q1, 4, 7, 8
16	TRANSISTOR	2N5460	150202	1	Q5
17	TRANSISTOR	2N2913	150203	1	Q3
18					
19					
20	DIODE	1N3064	150300	8	CR1,2,3,4,5,6,7,8
21	DIODE, ZENER	1N752A	150302	1	VR1
22	DIODE, ZENER	1N751A	150311	1	VR2
23					
24					
25	CAPACITOR, MICA	100 Pf	150102-101	3	C6, 10, 11
26	CAPACITOR, MYLAR	1000 Pf	150101-102	1	C9
27	CAPACITOR, MYLAR	.0015 Uf	150101-152	1	C7
28	CAPACITOR, MYLAR	.01 Uf	150101-103	1	C8
29	CAPACITOR, TANPL., 10%	1 Uf	150100-105	5	C1, 2, 3, 4, 5
30					
31					
32					
33	RESISTOR VAR., 20 TURN	2K	150003-202	1	R13

200157-000

E

TITLE ASSY. P.C.B. PHASED LOCKED
DOUBLE F DATA SEPARATOR

DWG NO.
200157-000

REV
E

SHEET 3 OF 3

PERSCI, INC.

DWG NO. 200157-000

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
34				
35	RESISTOR 1/2W 5% 1K	150002-102	1	R28
36				
37	RESISTOR 1/4W 5% 330	150000-331	1	R3
38	RESISTOR 1/4W 5% 750	150000-751	1	R15
39	RESISTOR 1/4W 5% 1K	150000-102	11	R2,4,5,6,12,14,16, R20,22,26,27
40	RESISTOR 1/2W 5% 1.5K	150000-152	1	R10
41	RESISTOR 1/2W 5% 3.3K	150000-332	2	R1, 17
42	RESISTOR 1/2W 5% 3.9K	150000-392	2	R23, 24
43	RESISTOR 1/2W 5% 5.1K	150000-512	1	R21
44	RESISTOR 1/2W 5% 5.6K	150000-562	1	R11
45	RESISTOR 1/2W 5% 10K	150000-103	1	R19
46	RESISTOR 1/4W 5% 15K	150000-153	1	R9
47	RESISTOR 1/4W 5% 22K	150000-223	2	R7, 18
48	RESISTOR 1/4W 5% 240K	150000-244	1	R8
49				
50				
51				
52	HOUSJNG, CONNECTOR; 10 Pin	100032-010	1	P6
53				
54				
55				
56	PIN, MALE	100046	5	TP1, 2, 3, 4, 5
57				
58	WIRE, INSUL., AWG 24			
59				
60				
61				
	SCHEMATIC	200115	REF	REV C
	ARTWORK	200156	REF	

TITLE
ASSEMBLY, PCB DATA AND INTERFACE

DWG NO.
200263-007

REV
0

SHEET 1 OF 1

MODEL 270 HARD SECTOR 32 SECTORS

PERSCI, INC.

200263 7

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
	USE BASIC BD 200263-000			
	LATEST REVISION AND ADD			
	THE FOLLOWING:			
1	ASSY, SELECT MODULE	200288-003	1	U11
2				
3	CAPACITOR, TANTL., 10% 0.1UF	150100-104	1	C36
4	CAPACITOR, TANTL., 10% 1UF	150100-105	2	C40,41
5				
6	RESISTOR, 1/2 W., 5% 11K	150000-113	2	R88,94
7				
8	WIRE, INSULATED, AWG 24		A/R	JUMPER FROM A TO B ✓
				JUMPER FROM D TO E ✓
				JUMPER FROM F TO G ✓
				JUMPER FROM H TO J ✓
				JUMPER FROM I TO P ✓
				JUMPER FROM R TO S ✓
				JUMPER FROM W TO Y ✓
				JUMPER FROM AA TO AB ✓
				JUMPER FROM AD TO AF ✓
				JUMPER FROM AH TO AK ✓
				JUMPER FROM AL TO AM ✓
				JUMPER FROM AT TO AY ✓
				JUMPER FROM AU TO AV ✓
				JUMPER FROM BA TO BB ✓
				JUMPER FROM BD TO BE ✓
				JUMPER FROM BH TO BJ ✓
				JUMPER FROM BK TO BM ✓
				SECTOR "0" JUMPER 32 ✓
				SECTOR "1" JUMPER 32 ✓
	NOTE: JUMPER POINTS NOT LISTED			CHASSIS GND W1 ✓
	ARE OPEN (NOT USED)			

H

20026 700

MATERIAL LIST

TITLE ASSEMBLY, PCB DATA AND IN	9 EPT 4 - 214	DWG NO. 200263-000	REV H	SHEET 2 OF 6
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MODEL 270 BASIC BOARD

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	BOARD, PROCESSED	200262	1	REV C
2				
3	BRACKET, DATA BD	200171	1	REV B
4	INSULATOR, DATA BD	200174	1	REV A
5				
6				
7				
8				
9				
10				
11	IC LM311N	150600	3	U18, 22, 61
12	IC MC1406L	150601	1	U55
13	IC MC1458C-P1	150602	2	U40, 51
14	IC 7400	150603	5	U15, 28, 53, 57, 60
15	IC 7404	150604	5	U20, 30, 38, 41, 49
16	IC 7408	150605	4	U26, 29, 45, 50
17	IC 7432	150608	4	U19, 54, 56, 58
18	IC 7474	150609	6	U14, 24, 39, 46, 47, 52
19	IC 7486	150611	1	U21
20	IC 74123	150612	4	U10, 12, 25, 44
21	IC 74193	150614	2	U42, 43
22	IC 75451	150616	1	U17
23	IC 75452	150617	2	U31, 36
24	IC 75453	150618	9	U2, 3, 4, 5, 6, 7, 8, 23, 59
25	IC 72733	150619	2	U33, 35
26	IC 7416	150621	2	U13, 48
27	IC 7406	150622	1	U37
28	IC SN72306P	150646	2	U34, 32
29				
30	RESISTOR NETWORK 4.7K	150050	1	U9
31	RESISTOR NETWORK 220/330	150051	1	U1
32				
33				

MATERIAL LIST

TITLE ASSEMBLY, PCB DATA AND INTERFACE	9 EPT 4 - 215	DWG NO. 200263-000	REV H	SHEET 3 OF 6
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MODEL 270 BASIC BOARD	PERSCI, INC.
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200263 IN

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
34	TRANSISTOR 2N4400	150200	5	Q2,26,27,28,31
35	TRANSISTOR 2N4402	150201	25	Q3,4,5,6,7,8,9,10, 13,16,17,18,19,20, 21,22,23,24,25, 29,30,32,33,34,35
36	TRANSISTOR 2N5460	150202	4	Q11,12,14,15
37	TRANSISTOR 2N2913	150203	1	Q1
38	TRANSISTOR 2N706A	150207	4	Q36,37,38,39
39				
40				
41				
42	DIODE 1N3064	150300	16	CR3,4,5,6,7,8, 9,10,11,12,13,14, 15,16,17,18
43	DIODE, ZENER 1N752A	150302	1	VR1
44	DIODE, ZENER 1N759A	150313	2	VR2,4
45	DIODE, ZENER 1N751A	150311	1	VR3
46	INDUCTOR 200UH	150094	1	L1
47	CAPACITOR, MICA .001UF	150102-102	2	C58,59
48	CAPACITOR, MICA 220pf	150102-221	1	C14
49	CAPACITOR, MICA 100pf	150102-101	3	C1,50,51
50	CAPACITOR, MICA 510pf	150102-511	4	C21,26,46,49
51	CAPACITOR, MYLAR .001UF	150101-102	2	C3,4
52	CAPACITOR, CERAMIC .01UF	150103-103	15	C7,11,18,20,24,25, 28,30,34,37,38,43, 45,52,56
53	CAPACITOR, TANTL 10% 0.1UF	150100-104	3	C35,42,44
54	CAPACITOR, TANTL 10% 1UF	150100-105	23	C2,5,6,8,9,10,12, 13,15,16,17,19, 22, 23,27,29,33,39,47, 53,54,55,57

MATERIAL LIST

TITLE
ASSEMBLY, PCB DATA AND INTERFACE

9 EPT 4 - 216)WG NO.
200263-000

REV

H

SHEET 4 OF 6

MODEL 270 BASIC BOARD

PERSCI, INC.

20026 100

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
55	CAPACITOR, TANTL 22UF	150100-226	1	C48
56				
57				
58				
59	RESISTOR, VARIABLE 2K	150003-202	1	R154
60				
61	RESISTOR 1/2 W., 5% 10	150002-100	2	R121,126
62	RESISTOR 1/2 W., 5% 47	150002-470	2	R69,70
63	RESISTOR 1/2 W., 5% 68	150002-680	4	R104,105,106,107
64	RESISTOR 1/2 W., 5% 1K	150002-102	1	R169
65	RESISTOR, 1/2 W., 1% 1.50K	150001-1501	1	R81
66	RESISTOR 1/2 W., 1% 332	150001-3320	2	R13,14
67	RESISTOR 1/2 W., 1% 1.78K	150001-1781	1	R138
68	RESISTOR 1/2 W., 1% 3.01K	150001-3011	1	R78
69	RESISTOR 1/2 W., 1% 10K	150001-1002	5	R108,109,147,148,1
70	RESISTOR 1/2 W., 1% 24.9K	150001-2492	1	R152
71	RESISTOR 1/2 W., 1% 30.1K	150001-3012	1	R146
72	RESISTOR 1/2 W., 1% 4.64K	150001-4641	2	R86,87
73				
74	RESISTOR 1/2 W., 5% 10	150000-100	13	R3,10, 12,18,19, 33,34,37,38,41, 42,56,77
75	RESISTOR 1/2 W., 5% 47	150000-470	2	R26,27
76	RESISTOR 1/2 W., 5% 100	150000-101	13	R23,29,35,36,39, 40,82,83,84,85, 101,103,128
77				
78	RESISTOR 1/2 W., 5% 220	150000-221	7	R5,7,49,53,58, 120,125
79	RESISTOR 1/2 W., 5% 330	150000-331	13	R6,8,9,15,16,17, 59,65,66,67,68, 119,124

MATERIAL LIST

TITLE ASSEMBLY, PCB DATA AND INTERFACE 9 EPT 4 - 217 DWG NO. 200263-000 REV H SHEET 5 OF 6

MODEL 270 BASIC BOARD

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
80	RESISTOR 1/2 W., 5% 510	150000-511	1	R111
81	RESISTOR 1/2 W., 5% 1K	150000-102	24	R1,2,48,52,64,71, 72,73,74,89,92,95,98, 112,114,117,118,122, 123,132,134,158,166, 170
82	RESISTOR 1/2 W., 5% 2K	150000-202	10	R22,24,28,30, 110,115,116,133, 137,139
83	RESISTOR 1/2 W., 5% 680	150000-681	1	R25
84	RESISTOR 1/2 W., 5% 3.9K	150000-392	4	R4,45,57,135
85	RESISTOR 1/2 W., 5% 4.7K	150000-472	11	R60,61,175, 130,136,155,159, 160,161,167,168
86	RESISTOR 1/2 W., 5% 5.1K	150000-512	1	R153
87	RESISTOR 1/2 W., 5% 6.8K	150000-682	5	R46,47,50,51,62
88	RESISTOR 1/2 W., 5% 10K	150000-103	23	R20,21,31,32,43,44, 54,55,79,131,151,156, 157,162,163,164,165, 171,172,173,174,90,96
89	RESISTOR 1/2 W., 5% 15K	150000-153	2	R100, 102
90	RESISTOR 1/2 W., 5% 18K	150000-183	1	R63
91	RESISTOR 1/2 W., 5% 20K	150000-203	2	R141,144
92	RESISTOR 1/2 W., 5% 22K	150000-223	3	R75,76,80
93	RESISTOR 1/2 W., 5% 30K	150000-303	3	R93,99,140
94				
95	RESISTOR 1/2 W., 5% 39K	150000-393	2	R143,145
96	RESISTOR 1/2 W., 5% 47K	150000-473	3	R150,176,177
97	RESISTOR 1/2 W., 5% 220K	150000-224	2	R91,97
98	RESISTOR 1/2 W., 5% 100K	150000-104	2	R113,129
99	RESISTOR 1/2 W., 5% 240K	150000-244	1	R142
100	RESISTOR 1/2 W., 5% 1MEG	150000-105	1	R127

200263-000

MATERIAL LIST

TITLE
ASSY EJECT & CARRIER

9 EPT 4 - 219

DWG NO.
200219-001

REV
D

SHEET 1 OF 3

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1				
2	PLATE CARRIER SIDE 0	200054	1	
3	RING EXT. "E" TYPE	100001-004	6	
4				
5	SHAFT CONE	200073	2	
6	SPRING, COMPRESSION CONE	200360	2	
7	WASHER SHIM	200081-001	2	
8	CONE THRUST	200325	2	
9				
10	FLANGE CONE	200326	2	
11	BEARING BALL FLANGED	100011-001	2	
12	NUT HEX	100015-100	2	#2
13	ASSY PHOTOSENSE	200274-002	2	
14	WASHER FLAT	100008-100	2	#2
15	SCREW SOC HD CAP	100003-104	2	2-56 X 1/4
16	CAM EJECT MTR SIDE 1	200220	1	
17	SPRING, CONE	200359	2	
18	FOAM PRESSURE	200103	4	
19	PLATE CARRIER SIDE 1	200166	1	
20	SCREW BD HD SLOTTED	100002-203	12	4-40 X 3/16
21	BRACKET CIRCUIT BD	200167-002	1	
22	GUIDE DISKETTE	200047-002	2	
23	GUIDE DISKETTE	200047-001	2	
24	SWITCH MOM. PUSH	100026	2	
25	PIN ROLL	100006-408	2	
26	RING EXT. "E" TYPE	100001-002	2	
27	BEARING BALL	100029-002	2	
28	ASSY, CRANK CAM	200035-001	1	
29	ASSY, CRANK CAM	200035-002	1	
30	BEARING OILITE	1000027	2	
31	BLOCK CARRIER PIVOT	200202-001	2	
32	SCREW SOC HD CAP	100003-206	8	4-40 X 3/8
33	SCREW BD HD SLOTTED	100002-206	10	4-40 X 3/8

200219

9.2.1.77

MATERIAL LIST

TITLE
ASSY EJECT AND CARRIER 9 EPT 4 - 220

DWG NO.
200219-001

P-V
D

SHEET 2 **OF** 3

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
34	ARM SUPPORT DUAL	200194	2	
35	SPRING, TENSION	100022-002	4	
36	PIN ROLL	100006-116	2	
37	SPRING COMPRESSION	100021-003	2	
38	SCREW BD HD SLOTTED	100002-216	4	4-40 X 1.00
39	BLOCK CARRIER PIVOT	200202-002	2	
40	SCREW BD HD SLOTTED	100002-410	4	8-32 X 5/8
41	BRACKET LOAD SWITCH	200147	1	
42	SWITCH MICRO (LEVER)	100019	2	
43	SCREW BD HD SLOTTED	100002-208	4	4-40 X 1/2
44	SCREW BD HD SLOTTED	100002-204	2	4-40 X 1/4
45				SEE OTHER DASH NO. ML'S
46	BLOCK PIVOT	200043	4	
47	SWITCH MICRO	100028	4	
48	CAM EJECT MTR SIDE O	200058	1	
49	BRACKET EJECT MTR	200289	2	
50	PLATE SIDE LOWER DECK	200148	1	
51				SEE OTHER DASH NO. ML'S
52	SUBASSY, GEAR MOTOR	200394-001	1	
53	BRACKET CIRCUIT BD	200167-001	1	
54	SCREW SET HEX SOC	100004-405	2	6-32 X 5/16
55	SUBASSY, GEAR MOTOR	200394-002	1	
56	PIN ROLL	100006-112	2	
57	TAPE ADHESIVE TEFLON	100059	A/R	
58	SCREW SET HEX SOCKET	100004-403	2	
59	SCREW SET HEX SOCKET	100005-414	1	4-40 X 7/8
60	ADHESIVE TAPE	100012	A/R	1-1/2
61	LEVER		1	
62				
63	WIRE, 24 AWG	U.L. 100037-024	A/R	
64				
65				
66				

MATERIAL LIST

TITLE ASSY CENTER AND UPPERDECK 9 EPT 4 - 222 DWG NO 200227 REV B SHEET 1 OF 2

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	ASSY, SPINDLE MOTOR	200218	1	
2	ASSY, DISKETTE SPINDLE	200217	1	
3	ASSY, HD. ENG. SOL (SIDE 0)	200214	1	
4	ASSY, HD. ENG. SOL (SIDE 1)	200216	1	
5	ASSY, SPINDLE SENSOR	200213-002	1	
6	ASSY, LED (SIDE 0)	200221	1	
7	ASSY, LED (SIDE 1)	200222	1	
8				
9				
10	ASSY F.C.E. SPINDLE SERVO	200134	1	
11				
12	SPEC BELT SPINDLE MTR.	200042	1	
13	GUIDE DISKETTE	200047-001	2	
14	GUIDE DISKETTE	200047-002	2	
15	STOP DISKETTE SIDE 0	200182	1	
16	STOP DISKETTE SIDE 1	200183	1	
17	PLATE CENTER DECK	200149	1	
18	PLATE SIDE UPPER DECK	200170	1	
19				
20	BRACKET LIFTER PIVOT	200164	1	
21	LIFTER PRES ARM	200150	1	
22	SHAFT LIFTER	200178	1	
23	SUPPORT DISKETTE REF.	200047	2	
24	SHAFT EJECT DUAL	200196	1	
25	CRANK EJECT	200007	2	
26	ACTUATOR EJECT	200006	2	
27	ARM EJECT	200059	2	
28	GUIDE EJECT ARM	200046-001	1	
29	GUIDE EJECT ARM	200046-002	1	
30	SPRING TORSION	200009	1	
31	SPRING TORSION	200169	1	
32	SPACER, PHENOLIC	200103-203	1	
33	SPACER ALUM. ROUND	200021-002	2	

200227

7.21-

MATERIAL LIST

TITLE ASSY CENTER AND UPPER DEC. 9 EPT 4 - 223 DWG NO. 200227

REV
B

SHEET 2 OF 2

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
34	SPACER ALUM ROUND	200021-004	2	
35	WASHER, SHIM	200091-001	2	
36	STANDOFF, HEATSINK	200197	2	
37	COVER, SPOOL SERVO	200161	1	
38	SPRING COMP	100021-002	3	
39	WASHER, PHENOLIC	100051-001	3	
40	PIN ROLL	100006-104	2	1/16 DIA X 1/4
41	PIN ROLL	100006-116	2	1/16 DIA X 1
42	PIN ROLL	100006-408	2	1/8 DIA X 1/2
43	SCREW BD HD SLOTTED	100002-207	1	4-40 X 7/16
44	SCREW FL HD 82° SLOTTED	100039 214	2	4-40 X 7/8
45	SCREW BD HD SLOTTED	100002-108	3	2-56 X 1/2
46	SCREW BD HD SLOTTED	100002-203	13	4-40 X 3/16
47	SCREW BD HD SLOTTED	100002-204	8	4-40 X 1/4
48	SCREW BD HD SLOTTED	100002-214	4	4-40 X 7/8
49	SCREW BD HD SLOTTED	100002-406	5	8-32 X 3/8
50	SCREW BD HD SLOTTED	100002-424	2	8-32 X 1-1/2
51				
52	SCREW SET SOC HD	100004-204	1	4-40 X 1/4
53				
54	SCREW SOC HD CAP	100003-206	2	4-40 X 3/8
55				
56	SCREW SOC HD CAP	100003-408	2	8-32 X 1/2
57				
58				
59	CLAMP CABLE	100005-001	1	1/16 DIA
60				
61	RING EXT. RET "E" TYPE	100001-002	4	1/8 DIA
62				
63	TAPE ADHESIVE TEFLON	100059	A/R	
64				
65				
66				

B
200

MATERIAL LIST

TITLE
ASSY POSITIONER

9 EPT 4 - 224

DWG NO.
200228

REV
A

SHEET 1 OF 2

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	ASSY VOICE COIL	200024	1	
2	ASSY MAGNET	200023	1	
3	ASSY TRANSDUCER AMP	200079	1	
4				
5	ASSY TRANSDUCER	200068	1	
6	ASSY CARRIAGE SIDE 0	200270-001	1	
7	ASSY CARRIAGE SIDE 1	200269	1	
	CLAMP, COLE	200085	1	
9	ASSY SCALE	200272	1	
10	HOLDER PRES PAD	200244	2	
11	PAD PRESSURE	200087	2	
12	WASHER FELT	200126	1	
13	SUPPORT CARRIAGE & COIL	200181	1	
14	FRAME POSITIONER	200193	1	
15	ROD GUIDE	200017	2	
16	PLATE DEFLEXION	200254	1	
17	SUPPORT HEAD SIDE 1	200253	1	
18	SPACER HEAD SUPPORT	200255	1	
19	PIN PIVOT	200304	2	
20	ARM PRES. PAD	200033	2	
21	SPRING TORSION	200303	2	
22	RETAINER. FELT WASHER	200306	1	
23	"O" RING RUBBER	100061	1	
24	RING EXT "E" TYPE	100001-002	4	
25	SCREW SOC HD CAP	100003-312	1	6-32 X 3/4
26	SCREW SOC HD CAP	100003-308	2	6-32 X 1/2
27	SCREW SOC HD CAP	100003-205	2	4-40 X 1/2
28				
29	SCREW SET HEX SOC	100004-402	1	8-32 X 1/8
30	SCREW HEX SOC BT HD	100014-304	4	6-32 X 1/4
31	SCREW HEX SOC BT HD	100014-203	1	4-40 X 3/16
32	SCREW HEX SOC BT HD	100014-205	1	4-40 X 1/2
33	SCREW HEX SOC BT HD	100014-208	2	4-40 X 1/2

27002

REV
F

MATERIAL LIST

TITLE ASSY. P.C.B.⁹ EPT 4 - 226
LAMP AMPLIFIERDWG NO.
200080REV
F

SHEET 2 OF 3

PERSCI, INC.

DWG NO.
200080

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	BOARD, PROCESSED	200089	1	REV C
2				
3				
4				
5	IC 1458	150602	3	U1, 2, 3
6				
7	TRANSISTOR 2N2222 A	150208	1	Q1
8				
9	DIODE, ZENER IN752 A	150302	1	VR1
10	CAPACITOR, MICA 100 PF	150102-101	3	C5,6,7
11	CAPACITOR, TANT. 1 UF	150100-105	4	C1, 2, 3, 4
12				
13	RESISTOR, VAR 2K	150003-202	6	R3, 4, 5, 8, 10,
14				
15	RESISTOR $\frac{1}{2}$ W 5% 33	150002-330	1	R15
16	RESISTOR $\frac{1}{8}$ W 1% 1.00K	150001-1001	1	R6
17	RESISTOR $\frac{1}{8}$ W 1% 5.62K	150001-5621	1	R17
18				
19	RESISTOR $\frac{1}{4}$ W 5% 1K	150000-102	2	R14, 16
20	RESISTOR $\frac{1}{4}$ W 5% 4.7K	150000-472	1	R20
21	RESISTOR $\frac{1}{4}$ W 5% 10K	150000-103	1	R1
22	RESISTOR $\frac{1}{4}$ W 5% 51K	150000-513	1	R12
23	RESISTOR $\frac{1}{4}$ W 5% 560K	150000-564	4	R9, 11, 18, 13
24	RESISTOR $\frac{1}{4}$ W 5% 5.6MEG	150000-565	1	R7
25				
26				
27	PIN, MALE	100046	7	TP1,2,3,4,5,6,7
28	CONNECTOR, 5 Pin	100041-005	1	J13
29				
30				
31				
32				
33				

MATERIAL LIST

TITLE ASSY. P.C.Eg EPT 4 - 229 POSITIONER SERVO	DWG NO. 200137	REV C	SHEET 4 OF 5
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MODEL 270/277

PERSCI, INC.

200137

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
67	SCREW, BINDING HD., 4-40	100002-207	4	} to be used with MJE-32
68	INSL & WASHER	150212	4	
69	WASHER, SHOULDER	100050-001	4	
70	WASHER, FLAT	100008-200	4	
71	NUT	100015-200	4	
72				
73	SCREW, BINDING HD., SLOTTED	100002-307	4	} to be used with TIP 32 & RCA 32
74	INSULATOR	150213	4	
75	WASHER, SHOULDER	100050-001	4	
76	WASHER, FLAT	100008-300	4	
77	NUT	100015-300	4	
78				
79	CONNECTOR 10 Pin	100041-010	1	J5
80	CONNECTOR 4 Pin	100041-004	1	J8
81	SUBASSY, HARNESS	200398-007	1	P8
82	SUBASSY, HARNESS	200398-008	1	P7
83				
84				
85				
86				
87				
88				
89				
90				
91				
92				
93				
94	WIRE, BUSS AWG 24		A/R	} Use as jumper across R50
95	SILICON, TEFION, #22		A/R	
96				
97				
98				
99	GREASE, SILICON		A/R	

MATERIAL LIST

TITLE	ASSY. P.C.B. 9 EPT 4 - 230 POSITIONER SERVO	DWG NO.	200137	REV	C	SHEET	3 OF 5
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PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
34	RESISTOR, VAR 2K	150003-202	1	R33
35				
36	RESISTOR, 3W 5% 1	150008-010	2	R77,78
37				
38	RESISTOR, 1/4W 1% 1K	150001-1001	12	R54,55,56,57,58,59,60,61,62,63,64,65
39	RESISTOR, 1/4W 1% 10K	150001-1002	7	R13,14,15,28,29,52,53
40	RESISTOR, 1/4W 1% 80.6K	150001-8062	1	R48
41				
42	RESISTOR, 1/2W 5% 100	150000-101	1	R69
43	RESISTOR, 1/2W 5% 200	150000-201	2	R2,4
44	RESISTOR, 1/2W 5% 510	150000-511	1	R47
45	RESISTOR, 1/2W 5% 750	150000-751	1	R42
46	RESISTOR, 1/2W 5% 1K	150000-102	14	R5,8,9,16,18,23,27,35,39,41,45,72,74,43
47	RESISTOR, 1/2W 5% 1.2K	150000-122	1	R46
48	RESISTOR, 1/2W 5% 2K	150000-202	1	R38
49	RESISTOR, 1/2W 5% 3.3K	150000-332	2	R67,71
50	RESISTOR, 1/2W 5% 3.9K	150000-392	2	R1,3
51	RESISTOR, 1/2W 5% 4.7K	150000-472	1	R34
52	RESISTOR, 1/2W 5% 5.1K	150000-512	3	R12,20,75
53	RESISTOR, 1/2W 5% 10K	150000-103	7	R6,10,11,30,31,51,73
54	RESISTOR, 1/2W 5% 20K	150000-203	1	R37
55	RESISTOR, 1/2W 5% 22K	150000-223	3	R17,24,26
56	RESISTOR, 1/2W 5% 39K	150000-393	1	R68
57	RESISTOR, 1/2W 5% 51K	150000-513	1	R7
58	RESISTOR, 1/2W 5% 100K	150000-104	8	R21,32,36,40,44,66,70,49
59				
60				
61	RESISTOR, 1/2W 5% 390K	150000-394	1	R19
62	RESISTOR, 1/2W 5% 3.9MEG	150000-395	1	R76
63	RESISTOR, 1/2W 5% 1MEG	150000-105	2	R22,25
64				
65				
66				

200137

MATERIAL LIST

TITLE ASSY. P.C.B. 9 EPT 4 - 231 POSITIONER SERVO	DWG NO. 200137	REV C	SHEET 2 OF 5
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MODEL 270/277

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	BOARD, PROCESSED	200152	1	REV C
2	HEAT SINK	200162	1	
3				
4	IC 7400	150603	2	U4, 5
5	IC 7404	150604	1	U3
6	IC 7432	150608	1	U7
7	IC LM311N	150600	6	U1,2,8,9,10,12
8	IC MC14580-P1	150602	5	U11,13,15,16,17
9	IC 75451	150616	1	U14
10	IC AH5012	150620	1	U6
11				
12	TRANSISTOR 2N4400	150200	3	Q1, 3, 9
13	TRANSISTOR 2N4402	150201	4	Q4,10,11,16
14	TRANSISTOR 2N5460	150202	1	Q2
15	TRANSISTOR MJE-32, TIF-32, R ₂	150204	4	Q12,13,14,15
16	TRANSISTOR 2N2222A	150208	2	Q5,7
17	TRANSISTOR 2N2907A	150209	2	Q6,8
18				
19				
20	DIODE 1N3064	150300	4	CR1,2,3,4,
21	DIODE, ZENER 1N755A	150301	1	VR1
22				
23	CAPACITOR, mica 510 Pf	150102-511	1	C2
24	CAPACITOR, mylar .001 Uf	150101-102	1	C4
25	CAPACITOR, mylar .0015 Uf	150101-152	1	C8
26	CAPACITOR, CER .01 Uf	150103-103	3	C3,5,6,
27	CAPACITOR, mylar .022 Uf	150101-222	1	C1
28	CAPACITOR, tantalum 1Uf	150100-105	6	C9,10,11,12,13,14
29	CAPACITOR, mylar 1 Uf	150104-105	1	C7
30				
31				
32				
33				

200137

REV F
DWG NO. 200134

MATERIAL LIST

TITLE ASSY., P.C.B 9 EPT 4 - 233WG NO. 200134
SPINDLE SERVO

REV F SHEET 2 OF 4

MODEL 270/277

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	BOARD, PROCESSED	200135	1	REV D
2	SUBASSY, HARNESS	200398-006	1	P5
3	SUBASSY, HARNESS	200399	1	P4
4	HEAT SINK	200160	1	
5				
6				
7				
8	IC LM311N	150600	1	U6
9	IC MC1458-P1	150602	2	U5, 7
10	IC 7400	150603	1	U1
11	IC 7430	150607	1	U4
12	IC 74193	150614	2	U2, 3
13	IC 7486	150611	1	U8
14				
15				
16				
17	TRANSISTOR 2N4400	150200	3	Q3, 6, 7
18	TRANSISTOR 2N4402	150201	2	Q1, 2
19	TRANSISTOR TIP-32, RCA-32, NJE-32	150204	1	Q4
20	TRANSISTOR 2N3771	150205	1	Q5
21				
22				
23	DIODE 1N3064	150300	2	CR1, 3
24	DIODE 1N4003	150301	2	CR2, 4
25	DIODE, ZENER 1N751A	150311	1	VR1
26	CAPACITOR, MYLAR .001UF	150101-102	1	C17
27	CAPACITOR, Mica 100 Pf	150102-101	1	C13
28	CAPACITOR, Mylar 1000Pf	150101-102	1	C11
29	CAPACITOR, Mylar 6800Pf	150101-682	1	C14
30	CAPACITOR, CERAMIC .01 UF	150100-100	1	C15
31	CAPACITOR, TANT. 10% 0.1 UF	150100-100	1	C15
32	CAPACITOR, Mylar 10% 0.1 Uf	150101-104	2	C5, 8
33	CAPACITOR, TANT. 10% 1 Uf	150100-105	7	C1, 2, 3, 4, 7, 9, 12

MATERIAL LIST

TITLE ASSY., P.C.B 9 EPT 4 - 2341WG NO. SPINDLE SERVO	200134	REV F	SHEET 3 OF 4
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PERSCI, INC.

200134

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
34	CAPACITOR, Mylar 5% 1 Uf	150104-105	2	C6, 10
35				
36	RESISTOR 1/2W 5% 150	150002-151	1	R27
37	RESISTOR 1/2W 5% 1K	150002-102	1	R26
38	RESISTOR 2W 5% 15	150004-150	1	R15
39				
40	RESISTOR 1/2W 1% 1K	150001-1001	1	R4
41	RESISTOR 1/2W 1% 1.1K	150001-1101	1	R5
42	RESISTOR 1/2W .1% 40K	150009-4002	2	R13, 14
43				
44	RESISTOR 1/2W 5% 47	150000-470	1	R24
45	RESISTOR 1/2W 5% 100	150000-101	2	R25, 28
46	RESISTOR 1/2W 5% 510	150000-511	2	R12, 21
47	RESISTOR 1/2W 5% 1K	150000-102	4	P 17, 18, 19, 22
48	RESISTOR 1/2W 5% 10K	150000-103	5	R6, 8, 10, 11, 20
49	RESISTOR 1/2W 5% 51K	150000-513	2	R3, 9
50	RESISTOR 1/2W 5% 100K	150000-104	2	R7, 16
51	RESISTOR 1/2W 5% 300K	150000-304	1	R16
52	RESISTOR 1/2W 5% 560K	150000-564	1	R1
53	RESISTOR 1/2W 5% 220K	150000-224	1	R23
54				
55				
56				
57				
58	CONNECTOR, ANGLE 2 Pin	100042-002	1	J1
59	CONNECTOR, ANGLE 4 Pin	100040-004	1	J2
60				
61				
62				
63				
64				
65				
66				

MATERIAL LIST

TITLE ASSY., P.C.E 9 EPT 4 - 235
SPINDLE SERVO

DWG NO.
200134

REV
F

SHEET 4 **OF** 4

PERSCI, INC.

200134

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
67				
68				
69				
70	SCREW, BINDING HD 4-40	100002-307	2	} T0-3 Use
71	INSULATOR, MICA	150211	1	
72	WASHER, SHOULDER	100050-001	2	
73	WASHER, FLAT	100008-300	2	
74	NUT	100015-300	2	
75				
76	SCREW, BINDING HD	100002-207	1	} Use with MJE 32
77	INSULATOR, MICA & WASHER	150212	1	
78	WASHER, SHOULDER	100050-001	1	
79	WASHER, FLAT	100008-200	1	
80	NUT	100015-200	1	
81				
82	SCREW, BINDING HD	100002-306	1	} Use with RCA 32 and TIP 32
83	INSULATOR, MICA	150213	1	
84	WASHER, SHOULDER	100050-001	1	
85	WASHER, FLAT	100008-300	1	
86	NUT	100015-300	1	
87				
88				
89				
90				
91				
92	GREASE, SILICON		A/R	
	SCHEMATIC	200133	REF	REV Z
	ARTWORK	200151	REF	REV C

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PerSci Documents, Drives to Serial No. 10,000 and Later

**PERSCI DOCUMENTS FOR
DRIVES WITH SERIAL NO. 10670 AND LATER**



**PCB Assemblies
Logic & Schematic Diagram
Diskette Drive
Models 270/272/277**

PREFACE

This manual of schematics and electrical assemblies has been compiled to match the configuration of the serial numbered drive at the time of shipment. In case of initial mismatch or replacement, assemblies not matching the documentation contained herein, a formal request for replacement must be made.

In making requests for matching documentation, please indicate the assembly number, the assembly dash number, and the revision letter.

TABLE OF CONTENTSLOGIC AND SCHEMATIC DIAGRAMS
PCB ASSEMBLY AND MATERIAL LISTS

<u>TITLE</u>	<u>DRAWING/MATERIAL LIST NUMBER, REVISION</u>
1. Transducer Amp - Assembly	200079 <u>H</u> Sht 1 of 1
Transducer Amp - M/L	200079-001 <u>H</u> Sht 1 of 1
Transducer Amp - M/L	200079-002 <u>B</u> Sht 1 of 1
2. Lamp Amplifier - Assembly	200080 <u>J</u> Sht 1 of 1
Lamp Amplifier - M/L	200080 <u>J</u> Sht 1 & 2
Lamp Amplifier - Schematic	200096 <u>G</u> Sht 1 of 1
3. Spindle Servo - Assembly	200134 <u>J</u> Sht 1 of 1
Spindle Servo - M/L List	200134 <u>J</u> Sht 1, 2, & 3
Spindle Servo - Schematic	200133 <u>G</u> Sht 1 of 1
4. Positioner Servo - Assembly	200137 <u>F</u> Sht 1 of 1
Positioner Servo - M/L	200137 <u>F</u> Sht 1 thru 4
Positioner Servo - Schematic	200136 <u>D</u> Sht 1 of 1
5. Data Separator - Assembly	<u>200157 E</u> Sht 1 of <u>1</u>
Data Separator - M/L	<u>" -000 E</u> Sht <u>1 & 2</u>
Data Separator - M/L	<u>" -001 A</u>
Data Separator - Schematic	<u>200115 C</u> Sht 1 of 1
6. Write Protect, Side 0 - Schematic	200231A Sht 1 of 1
7. Write Protect, Side 1 - Schematic	200232A Sht 1 of 1
8. Phototransistor, Side 1 - Schematic	200233C Sht 1 of 1
9. Phototransistor, Side 0 - Schematic	200234C Sht 1 of 1
10. Read/Write Head, Side 0 - Schematic	200235A Sht 1 of 1
11. Read/Write Head, Side 1 - Schematic	200236A Sht 1 of 1
12. Head Load Assembly, Side 0 - Schematic	200237A Sht 1 of 1
13. Head Load Assembly, Side 1 - Schematic	200238A Sht 1 of 1

TABLE OF CONTENTS (Continued)

14. Spindle Motor Assembly - Schematic	200239B Sht 1 of 1
15. LED Assembly, Side 1 - Schematic	200240B Sht 1 of 1
16. LED Assembly, Side 0 - Schematic	200241B Sht 1 of 1
17. Positioner Motor - Schematic	200242B Sht 1 of 1
18. Eject Motor Assembly - Schematic (Line out one Schematic No.)	200243B Sht 1 of 1 200742A
19. Data and Interface - Assembly	200263 <u>S</u> Sht 1 of 1
Data and Interface - M/L	200263-000 <u>S</u> Sht 1 thru 5
Data and Interface - M/L	200263- <u>007</u> Sht 1 <u>OF</u> <u>1</u>
Data and Interface - Schematic	200264 <u>M</u> Sht 1 thru 4

SPECIAL DOCUMENTATION (LIST AND/OR LINE OUT)

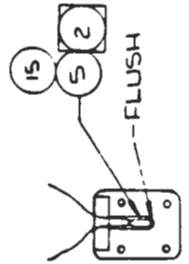
NONE

~~AS LISTED~~

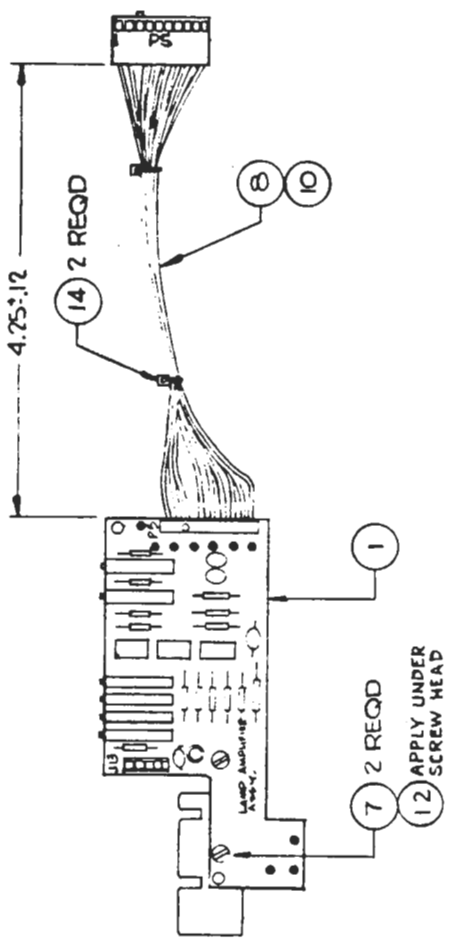
TABLATION CHART

ASSY NO	ITEM 5 (P/N)	USED ON
200079-001	100013-003	270/277
200079-002	100013-005	70/270/277

REV	DESCRIPTION	200079 H
A	ENGR RELEASE	
B	REVISED	8-77 J.L.A.
C	SEE E.C.O. III	8-77 J.L.A.
D	ITEM 5 P/N: 100013-003	8-77 J.L.A.
E	SEE E.C.O. 137	8-77 J.L.A.
F	ECO 171	8-77 J.L.A.
G	ECO 228	8-77 J.L.A.
H	270/277 TO USE SEE ECO 298	8-77 J.L.A.

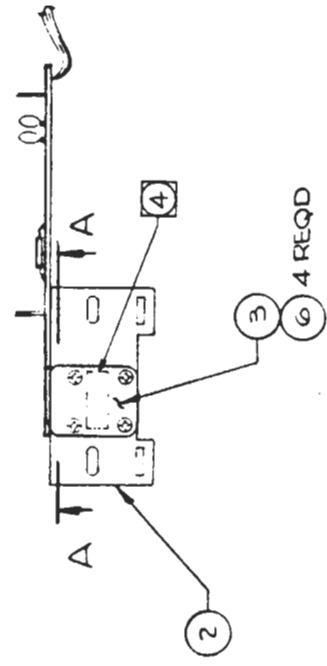


DETAIL OF ITEM 5
INSTALLATION



VIEW A-A

ORIENTATION OF ITEM 4

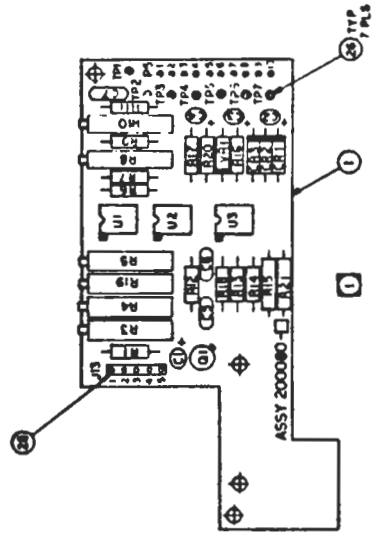


- 4 MARK DASH NO. WITH WHITE EPOXY INK.
 - 3. FOR SCHEMATIC SEE 200096.
 - 2 BOND ITEM 5 INTO GROOVE OF ITEM 3, USING ITEM 15.
 - 1. FOR WIRE LIST SEE 200186.
- NOTES: UNLESS OTHERWISE SPECIFIED

PART NO. 200079-XXX

NOTES UNLESS SPECIFIED 1. TOLERANCES .XX ± .XXX ± 2. BREAK ALL SHARP EDGES APPROX .010 3. MACH. SURFACES ✓ 4. ALL DIMS IN INCHES.	DRAWN: [Signature] CHECKED: [Signature] APPR: [Signature] MATERIAL:	FINISH:	MODEL NO. 70 277	SCALE 1/1 SIZE C	WEIGHT	SHEET 1 OF 1
	PERSCI ASSY., TRANSDUCE IZ AMP.	CODE 200079 (CHAINTED)	H	H	H	H

REV	REVISIONS	DATE	BY
A	ORIGIN REL		
B	WAGO BRIDGE		
C	ECO 7		
D	ECO 12		
E	ECO 76		
F	ECO 88		
G	ECO 178		
H	ECO 228		
J	ECO 294		



2. SCHEMATIC: REF 200086.
 O MARKER DESIGNATIONS OR REVISION LEVEL
 12 HIGH BLACK/WHITE CHARACTERS IN APPR. 4
 AREA SHOWN.
 UNLESS OTHERWISE SPECIFIED:

PERSCI
 PERSCI, INC.
 2000 79
 ASSEMBLY PCB AND AMPLIFIER
 MODEL 7070/277

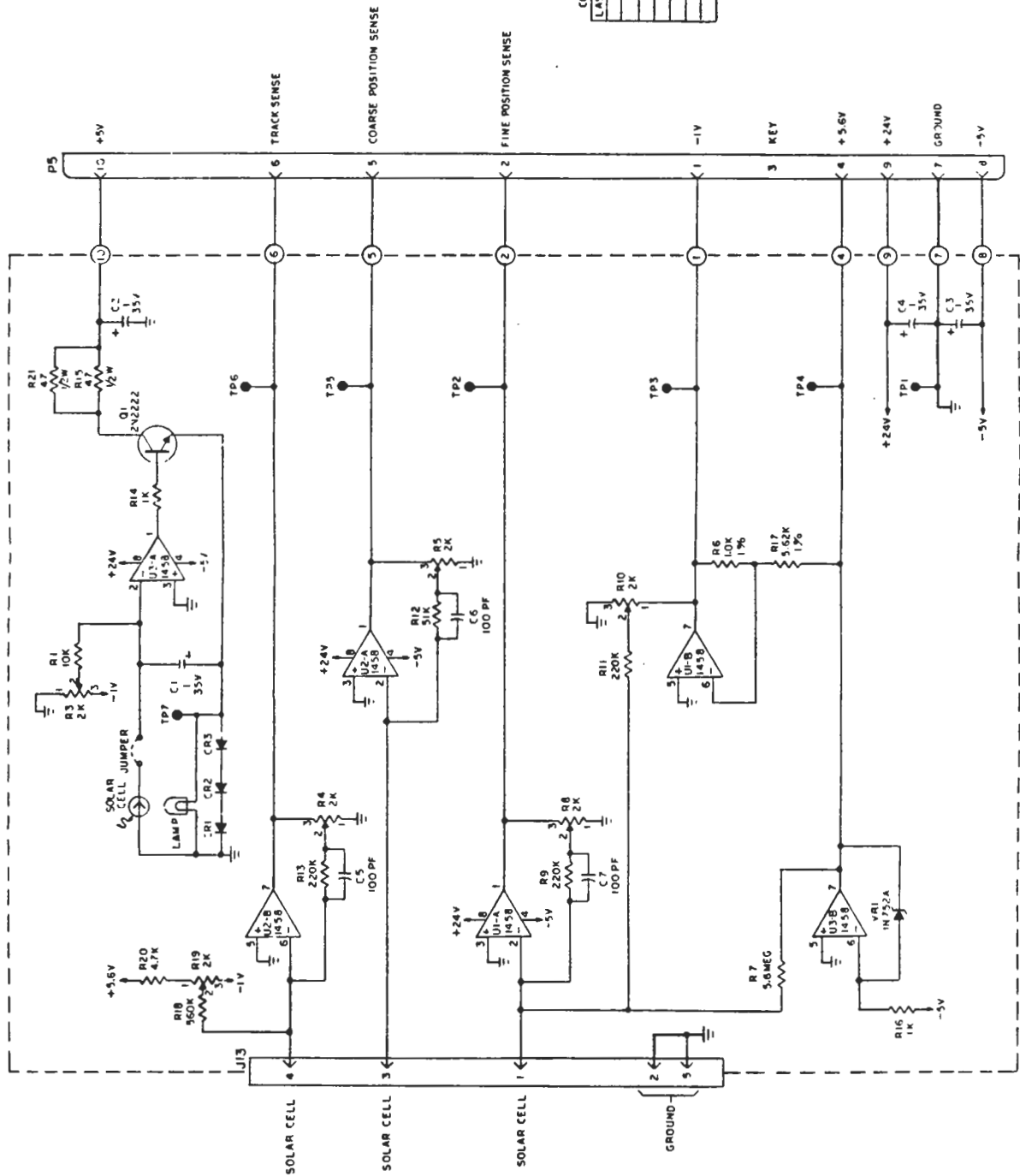
ML

MATERIAL LIST

REV J		TITLE		DWG NO.		REV		SHEET 1 OF 2	
		ASSY. P.C.B. LAMP AMPLIFIER		200080		↓			
		PERSCI, INC.							
ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS					
1	BOARD, PROCESSED	200089	1	REV 0					
2									
3									
4									
5	IC 1458	150602	3	U1, 2, 3					
6									
7	TRANSISTOR 2N2222 A	150208	1	Q1					
8	DIODE IN4003	150301	3	CR1,2,3					
9	DIODE, ZENER IN752 A	150302	1	VR1					
10	CAPACITOR, MICA 100 PF	150102-101	3	C5,6,7					
11	CAPACITOR, TANT. 1 UF	150100-105	4	C1, 2, 3, 4					
12									
13	RESISTOR, VAR 2K	150003-202	6	R3, 4, 5, 8, 10, 19					
14									
15	RESISTOR $\frac{1}{2}$ W 5% 47	150002-470	2	R15,21					
16	RESISTOR $\frac{1}{8}$ W 1% 1.00K	150001-1001	1	R6					
17	RESISTOR $\frac{1}{8}$ W 1% 5.62K	150001-5621	1	R17					
18									
19	RESISTOR $\frac{1}{2}$ W 5% 1K	150000-102	2	R14, 16					
20	RESISTOR $\frac{1}{2}$ W 5% 4.7K	150000-472	1	R20					
21	RESISTOR $\frac{1}{2}$ W 5% 10K	150000-103	1	R1					
22	RESISTOR $\frac{1}{2}$ W 5% 51K	150000-513	1	R12					
23	RESISTOR $\frac{1}{2}$ W 5% 560K	150000-564	1	R18					
24	RESISTOR $\frac{1}{2}$ W 5% 5.6MEG	150000-565	1	R7					
25	RESISTOR $\frac{1}{4}$ W, 5% 220K	150000-224	3	R9,11,13					
26									
27	PIN, MALE	100046	7	TP1,2,3,4,5,6,7					
28	CONNECTOR, 5 Pin	100041-005	1	J13					
29									
30									
31									
32									
33									

DWG NO.
200080

REV.	REVISIONS
A	EMPHASIS
B	ADD R18, R120
C	ECO 63 MFG. RE.
D	SEE ECO 77
E	ECO 179
F	ECO 227
G	ECO 294



COMP. REF. DESIGNATIONS

LAST USED	DELETED
U3	
Q1	
CR3	
C7	
R21	R2
TP7	
VRI	

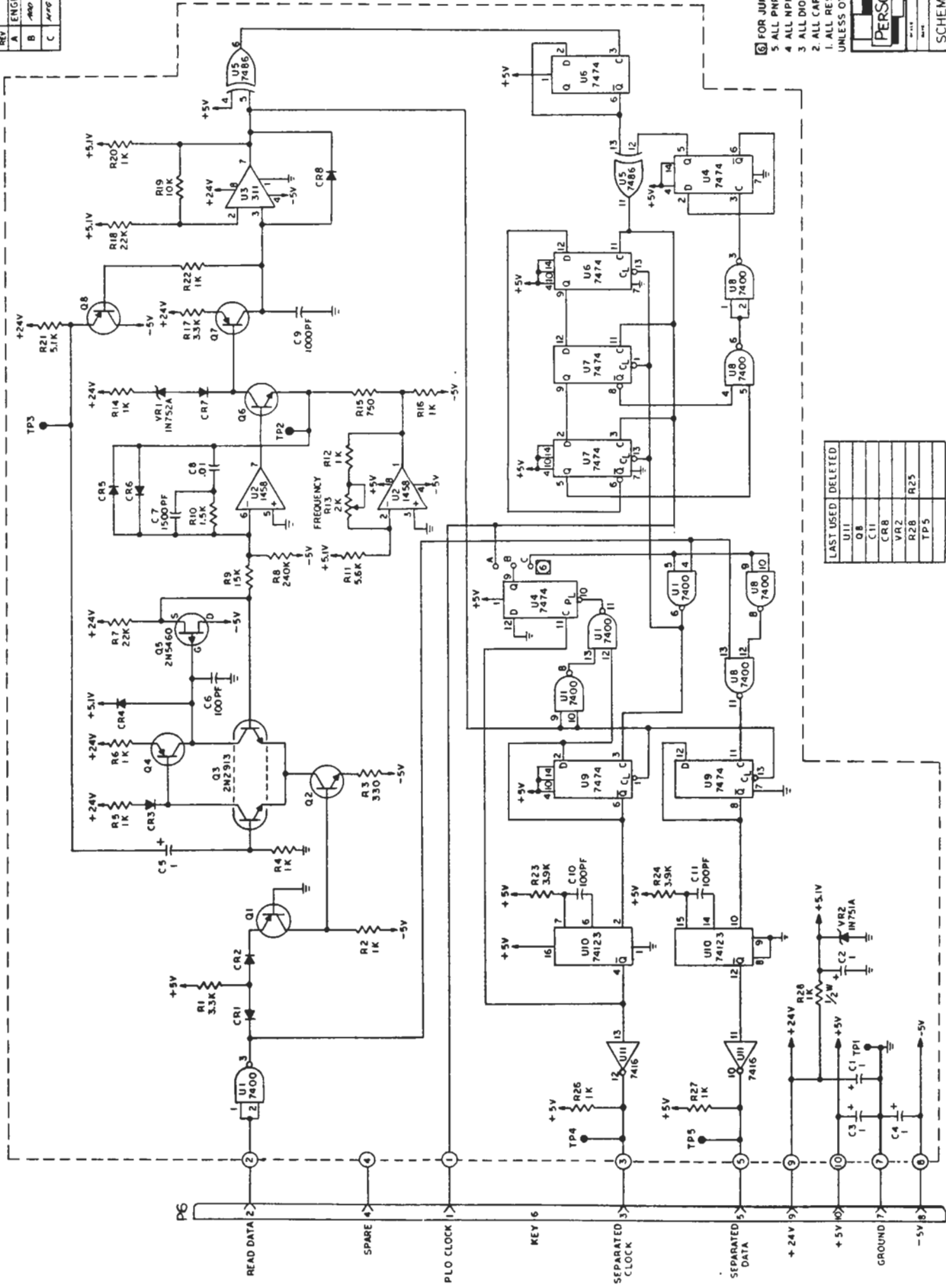
3 ALL DIODES TO BE IN4003.
 2 ALL CAPACITOR VALUES IN MICROFARADS.
 1 ALL RESISTOR VALUES IN OHMS, 10^3 , 10^4 , 10^5 ,
 UNLESS OTHERWISE SPECIFIED:

PERSCI, INC.

PERSCI
 1000 W. 10th St., Suite 100
 Phoenix, Arizona 85001
 (602) 252-2121

SCHEMATIC PCB LAYOUT AMPLIFIER
 MOD 2750/2/251 54T 251 251 G

REV	REVISIONS	DATE	BY
A	ENGINE REL	1/17/71	JL
B	AND INITIAL APPROVALS	1/21/71	JL
C	AND INITIAL APPROVALS	1/21/71	JL



- ① FOR JUMPER LOCATIONS SEE TABULATED W/L.
- 5 ALL PNP TRANSISTORS TO BE 2N4402.
- 4 ALL NPN TRANSISTORS TO BE 2N4400.
- 3 ALL DIODES TO BE IN 3064.
- 2 ALL CAPACITORS IN MICROFARADS.
- 1 ALL RESISTORS IN OHMS /W. 5% UNLESS OTHERWISE SPECIFIED:

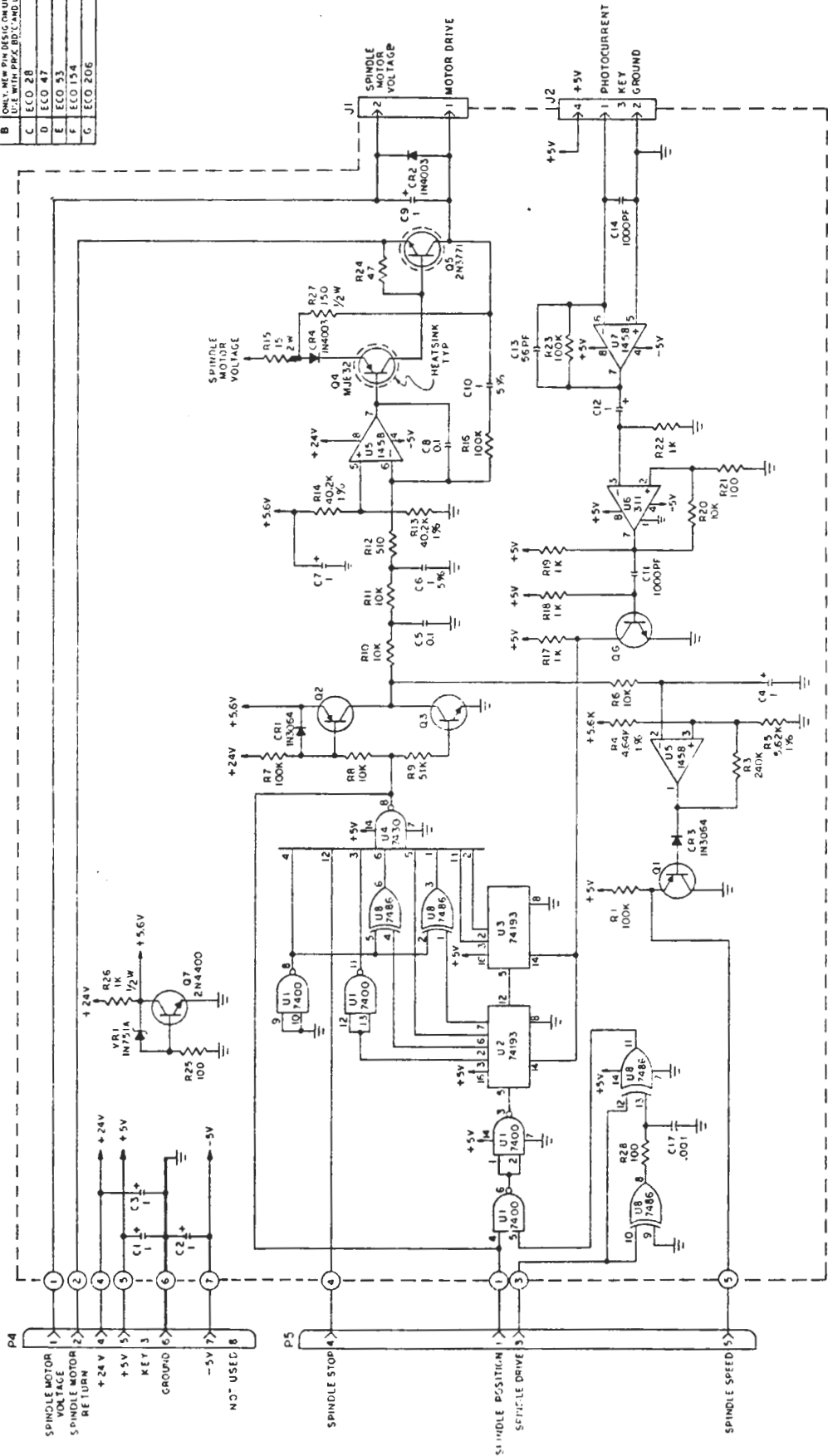
PERSCI, INC.

PHASE LOCKED DOUBLE F
DATA SEPARATOR

MOD 2700/272/277 SMT 1 OF 1 200115 C

LAST USED	DELETED
U11	
Q8	
C11	
CR8	
VR2	
R28	
TP5	

REV	DESCRIPTION	DATE	BY
A	ENGINEERING	1/15/77	J.P.
B	INDIVIDUAL TO ARTWORK	1/15/77	J.P.
C	ECO 28	1/15/77	J.P.
D	ECO 47	1/15/77	J.P.
E	ECO 53	1/15/77	J.P.
F	ECO 134	1/15/77	J.P.
G	ECO 206	1/15/77	J.P.



REF DESIGNATIONS	LAST USED	DELETED
U8		
Q4		
C17		
U5, C16		
R2		
R21		

- 4 ALL PNP TRANSISTORS TO BE 2N4402.
 - 3 ALL NPN TRANSISTORS TO BE 2N4400.
 - 2 ALL CAPACITOR VALUES IN MICROFARADS
 - 1 ALL RESISTOR VALUES IN OHMS, 1/4W, 5%.
- UNLESS OTHERWISE SPECIFIED:

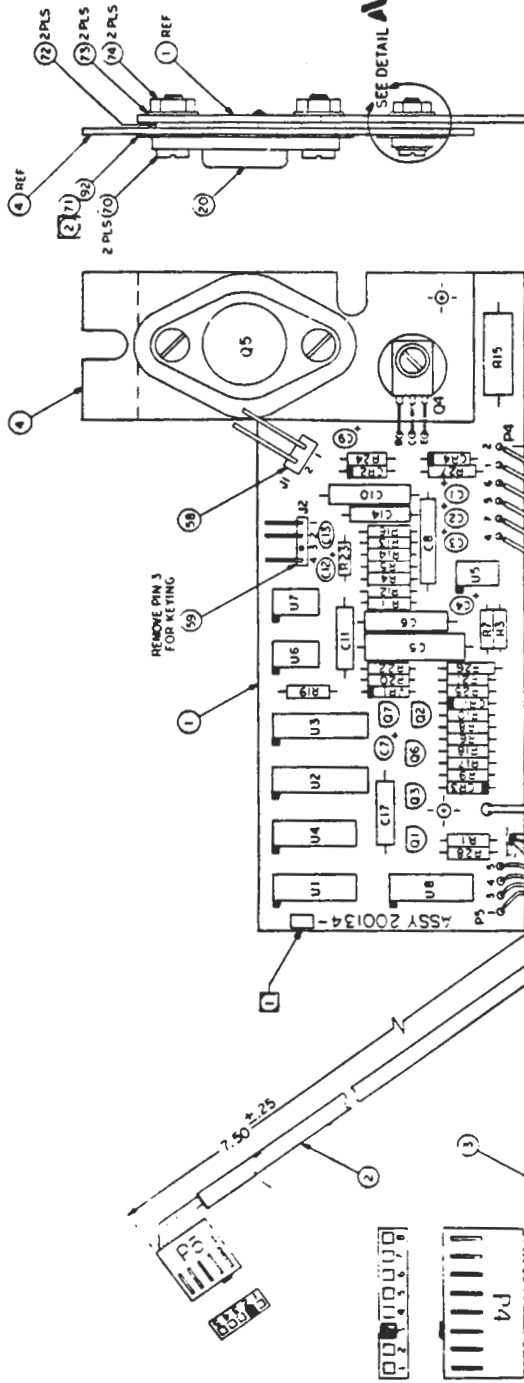
PERSCI, INC.

SCHEMATIC, PCB, SPINDLE SERVO

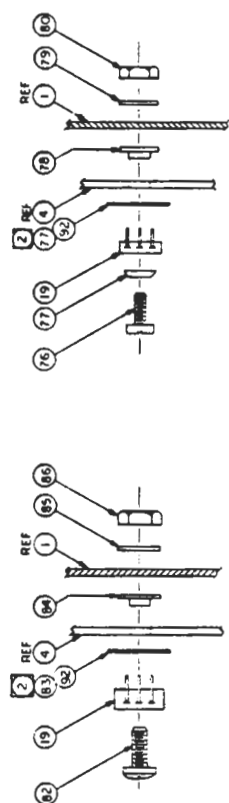
MOD 270/272/277 5MT 1 OF 1 200133 G

200133 G

REV	DESCRIPTION	200134	DATE
A	ENGINE REL		
B	INITIAL HARDWARE NEW LAYOUT		
C	E.O. 24		
D	E.O. 46		
E	E.O. 52		
F	E.O. 89		
G	E.O. 155		
H	E.O. 205		
J	E.O. 269		



- 1 SOLDER SHIELD TO PCB GROUND PLANE.
 - 2 SCHEMATIC REF 200133.
 - 3 APPLY SILICON GREASE ON BOTH SIDES OF MICA INSULATOR.
 - 4 MARK REVISION LEVEL 12 HIGH WHITE CHARACTERS IN APPROX AREA AS SHOWN.
- UNLESS OTHERWISE SPECIFIED:



DETAIL A
ITEMS TO BE USED WITH
MJE 32 TYPE TRANSISTORS

DETAIL B
ITEMS TO BE USED WITH TIP 32
PCA 32 TYPE TRANSISTORS

200134 J

ML

PERSCI, INC.

NEXT ASSY
200227

A S C F MELT, PCB, SPINDLE SERVO

MOUFL 270/27

REV 2
1.06.1
200134 J

MATERIAL LIST

REV J
DWG NO. 200134

TITLE		DWG NO.	REV	SHEET 1 OF 3
ASSY., P.C.B. SPINDLE SERVO		200134	J	
MODEL 270/277		PERSCI, INC.		
ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	BOARD, PROCESSED	200135	1	REV E.
2	SUBASSY, HARNESS	200400-004	1	P5
3	SUBASSY, HARNESS	200399	1	P4
4	HEAT SINK	200160	1	
5				
6				
7				
8	IC LM311N	150600	1	U6
9	IC MC1458-P1	150602	2	U5, 7
10	IC 7400	150603	1	U1
11	IC 7430	150607	1	U4
12	IC 74193	150614	2	U2, 3
13	IC 7486	150611	1	U8
14				
15				
16				
17	TRANSISTOR 2N4400	150200	3	Q3, 6, 7
18	TRANSISTOR 2N4402	150201	2	Q1, 2
19	TRANSISTOR TIP-32, RCA-32, MJE-32	150204	1	Q4
20	TRANSISTOR 2N3771	150205	1	Q5
21				
22				
23	DIODE 1N3064	150300	2	CR1, 3
24	DIODE 1N4003	150301	2	CR2, 4
25	DIODE, ZENER 1N751A	150311	1	VR1
26	CAPACITOR, MYLAR .001UF	150101-102	1	C17
27	CAPACITOR, Mica 56 PF	150102-560	1	C13
28	CAPACITOR, Mylar 1000PF	150101-102	2	C11, 14
29	CAPACITOR, Mylar 1000PF	150101-102	1	C11
30	CAPACITOR, CERAMIC .01 UF	150102-102	1	C15
31	CAPACITOR, TANT. 10% 0.1 UF	150100-101	1	C4
32	CAPACITOR, Mylar 10% 0.1 UF	150101-104	2	C5, 8
33	CAPACITOR, TANT. 10% 1 UF	150100-105	7	C1, 2, 3, 4, 7, 9, 12

MATERIAL LIST

REV J
DWG NO. 200134

TITLE	ASSY., P.C.B. SPINDLE SERVO	DWG NO.	200134	REV	J	SHEET 2 OF
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PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
34	CAPACITOR, Mylar 5% 1 UF	150104-105	2	C6, 10
35				
36	RESISTOR 1/4W 5% 150	150002-151	1	R27
37	RESISTOR 1/4W 5% 1K	150002-102	1	R26
38	RESISTOR 2W 5% 15	150004-150	1	R15
39				
40	RESISTOR 1/2W 1% 4.64K	150001-4641	1	R4
41	RESISTOR 1/2W 1% 5.62K	150001-5621	1	R5
42	RESISTOR 1/2W 1% 40.2K	150001-40.2	2	R13, 14
43				
44	RESISTOR 1/4W 5% 47	150000-470	1	R24
45	RESISTOR 1/2W 5% 100	150000-101	2	R25, 28
46	RESISTOR 1/2W 5% 510	150000-511	2	R12, 21
47	RESISTOR 1/2W 5% 1K	150000-102	4	R 17,18,19,22
48	RESISTOR 1/2W 5% 10K	150000-103	5	R6,8,10,11,20
49	RESISTOR 1/2W 5% 51K	150000-513	1	R9
50	RESISTOR 1/2W 5% 100K	150000-104	3	R1,7,16
51	RESISTOR 1/2W 5% 390K	150000-394	1	R16
52	RESISTOR 1/2W 5% 560K	150000-564	1	R1
53	RESISTOR 1/4W 5% 220K	150000-224	1	R23
54	RESISTOR 1/4W 5% 240K	150000-244	1	R3
55				
56				
57				
58	CONNECTOR, ANGLE 2 Pin	100042-002	1	J1
59	CONNECTOR, ANGLE 4 Pin	100040-004	1	J2
60				
61				
62				
63				
64				
65				
66				

9 EPT 4 - 257
MATERIAL LIST

REV J
 DWG NO. 200134

TITLE **ASSY., P.C.B. SPINDLE SERVO** DWG NO. **200134** REV **J** SHEET **3** OF **3**

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
67				
68				
69				
70	SCREW, BINDING HD 4-40	100002-308	2	} TO-9 Use
71	INSULATOR, MICA	150211	1	
72	WASHER, SHOULDER	100050-001	2	
73	WASHER, FLAT	100008-300	2	
74	NUT	100015-300	2	}
75				
76	SCREW, BINDING HD	100002-207	1	} Use with MJE 32
77	INSULATOR, MICA & WASHER	150212	1	
78	WASHER, SHOULDER	100050-001	1	
79	WASHER, FLAT	100008-200	1	
80	NUT	100015-200	1	}
81				
82	SCREW, BINDING HD	100002-306	1	} Use with RCA 32 and TIP 32
83	INSULATOR, MICA	150213	1	
84	WASHER, SHOULDER	100050-001	1	
85	WASHER, FLAT	100008-300	1	
86	NUT	100015-300	1	}
87				
88	TIE, CABLE	100086-003	6	
89				
90				
91				
92	GREASE, SILICON	100165	A/R	
	SCHEMATIC	200133	REP	REV C
	ARTWORK	200151	REP	REV D

MATERIAL LIST

TITLE		DWG NO.	REV	SHEET
ASSY. P.C.B. POSITIONER SERVO		200137	F	1 OF 4
MODEL 270/277		PERSCI, INC.		
QTY	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	BOARD, PROCESSED	200152	1	REV E
2	HEAT SINK	200162	1	
3				
4	IC 7400	150603	2	U4, 5
5	IC 7404	150604	1	U3
6	IC 7432	150608	1	U7
7	IC LM311N	150600	6	U1, 2, 8, 9, 10, 12
8	IC MC1458C-P1	150602	5	U11, 13, 15, 16, 17
9	IC 75451	150616	1	U14
10	IC AH5012	150620	1	U6
11				
12	TRANSISTOR 2N4400	150200	3	Q1, 3, 9
13	TRANSISTOR 2N4402	150201	4	Q4, 10, 11, 16
14	TRANSISTOR 2N5460	150202	1	Q2
15	TRANSISTOR MJE-32, TIP-32, RC	150204	4	Q12, 13, 14, 15
16	TRANSISTOR 2N2222A	150208	2	Q5, 7
17	TRANSISTOR 2N2907A	150209	2	Q6, 8
18				
19				
20	DIODE 1N3064	150300	4	CR1, 2, 3, 4,
21	DIODE, ZENER 1N755A	150303	1	VR1
22				
23	CAPACITOR, mica 510 Pf	150102-511	1	C2
24	CAPACITOR, mylar .001 Uf	150101-102	1	C4
25	CAPACITOR, mylar .0015 Uf	150101-152	1	C8
26	CAPACITOR, CER .01 Uf	150103-103	3	C3, 5, 6,
27	CAPACITOR, mylar .022 Uf	150101-223	1	C1
28	CAPACITOR, tantalum 1Uf	150100-105	6	C9, 10, 11, 12, 13, 14
29	CAPACITOR, mylar 1 Uf	150104-105	1	C7
30				
31				
32				
33				

REV
FDWG NO.
200137

MATERIAL LIST

REV
F

DWG NO.
200137

TITLE	ASSY. P.C.B. POSITIONER SERVO	DWG NO. 200137	REV F	SHEET 2 OF 4
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PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
34	RESISTOR, VAR 2K	150003-202	1	R33
35				
36	RESISTOR, 3W 5% 1	150008-010	2	R77,78
37				
38	RESISTOR, 1/2W 1% 1K	150001-1001	12	R34, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65
39	RESISTOR, 1/2W 1% 10K	150001-1002	7	R13, 14, 15, 28, 29, 52, 53
40	RESISTOR, 1/2W 1% 80.6K	150001-8062	1	R48
41				
42	RESISTOR, 1/2W 5% 100	150000-101	1	R69
43	RESISTOR, 1/2W 5% 200	150000-201	2	R2,4
44	RESISTOR, 1/2W 5% 510	150000-511	1	R47
45	RESISTOR, 1/2W 5% 750	150000-751	1	R42
46	RESISTOR, 1/2W 5% 1K	150000-102	14	R3, 8, 9, 10, 18, 23, 27, 35, 39, 61, 65, 72, 74, 75
47	RESISTOR, 1/2W 5% 1.2K	150000-122	1	R46
48	RESISTOR, 1/2W 5% 2K	150000-202	1	R38
49	RESISTOR, 1/2W 5% 3.3K	150000-332	2	R67,71
50	RESISTOR, 1/2W 5% 3.9K	150000-392	2	R1,3
51	RESISTOR, 1/2W 5% 4.7K	150000-472	1	R34
52	RESISTOR, 1/2W 5% 5.1K	150000-512	3	R12,20,75
53	RESISTOR, 1/2W 5% 10K	150000-103	7	R6, 10, 11, 30, 31, 51, 73
54	RESISTOR, 1/2W 5% 20K	150000-203	1	R37
55	RESISTOR, 1/2W 5% 22K	150000-223	3	R17,24,26
56	RESISTOR, 1/2W 5% 39K	150000-393	1	R68
57	RESISTOR, 1/2W 5% 51K	150000-513	1	R7
58	RESISTOR, 1/2W 5% 100K	150000-104	8	R2, 36, 40, 44, 66, 74
59				
60				
61	RESISTOR, 1/2W 5% 390K	150000-394	1	R19
62	RESISTOR, 1/2W 5% 3.9MEG	150000-395	1	R76
63	RESISTOR, 1/2W 5% 1MEG	150000-105	2	R22,25
64				
65				
66				

MATERIAL LIST

TITLE	ASSY. P.C.B. POSITIONER SERVO	DWG NO. 200137	REV F	SHEET 3 OF 4
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MODEL 270/277

PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
67	SCREW, BINDING HD., 4-40	100002-207	4	
68	INSL & WASHER	150212	4	to be used with
69	WASHER, SHOULDER	100050-001	4	MJE-32
70	WASHER, FLAT	100008-200	4	
71	NUT	100015-200	4	
72				
73	SCREW, BINDING HD., SLOTTED	100002-307	4	
74	INSULATOR	150213	4	to be used with
75	WASHER, SHOULDER	100050-001	4	TIP 32 & RCA 32
76	WASHER, FLAT	100008-300	4	
77	NUT	100015-300	4	
78				
79	CONNECTOR 10 Pin	100041-010	2	J5
80	CONNECTOR 4 Pin	100041-004	1	J8
81	SUBASSY, HARNESS	200398-007	1	P8
82	SUBASSY, HARNESS	200398-008	1	P7
83				
84	WIRE INSUL, AWG 24	100037-024	A/R	
85	TERMINAL, CONN	100159-003	2	P21
86				
87	HOUSING, SINGLE ROW	100154-002	1	P21
88				
89				
90				
91				
92				
93				
94	WIRE, BUSS AWG 24	100052-024	A/R	Use as jumper
95	SLEWING, TEFLON, #22	100135-022	A/R	across R30
96				
97				
98				
99	GREASE, SILICON	100165	A/R	

 REV F
 DWG NO. 200137

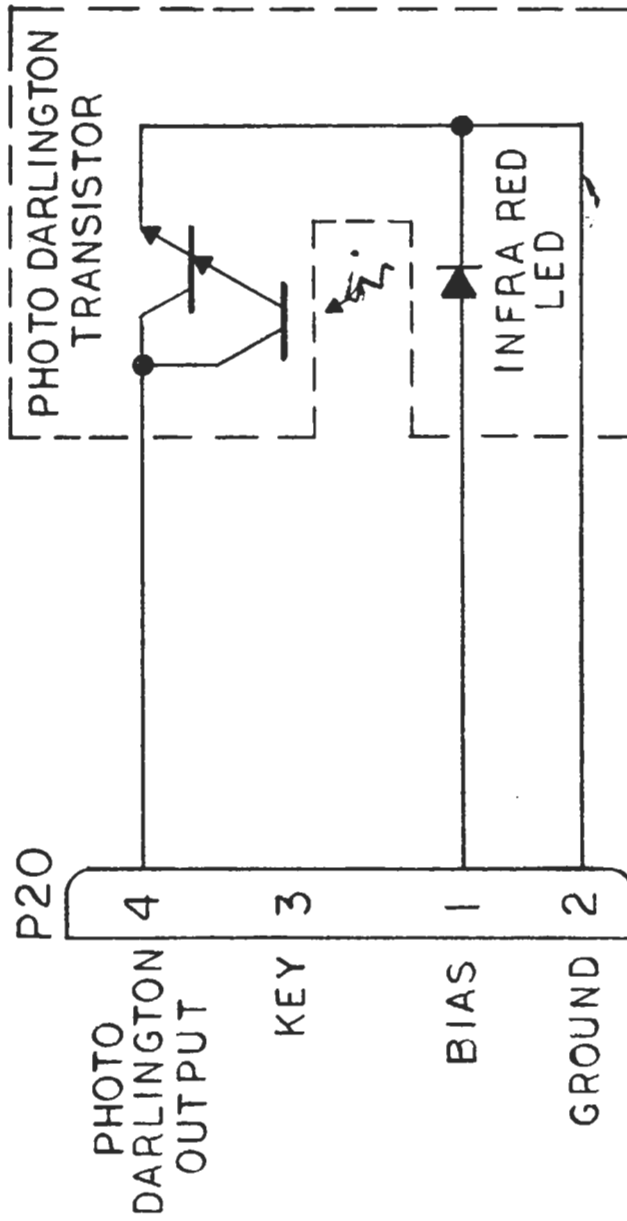
MATERIAL LIST

REV
E
DWG NO.
200157-000

TITLE		ASSY. P.C.B. PHASED LOCKED DOUBLE F DATA SEPARATOR		DWG NO	200157-000	REV	E	SHEET 1 OF 2
MOD 70/270/277				PERSCI, INC.				
ITEM NO.	DRAWING TITLE		DWG NO.	QTY	REMARKS			
1	PROCESSED BOARD		200155	1	REV D			
2	SUBASSY, HARNESS		200398-005	1	P6			
3								
4	IC	LM311N	150600	1	U3			
5	IC	MC1458-P1	150602	1	U2			
6	IC	7400	150603	2	U1, 8			
7	IC	7474	150609	4	U4, 6, 7, 9			
8	IC	7486	150611	1	U5			
9	IC	74123	150612	1	U10			
10	IC	7416	150621	1	U11			
11								
12								
13								
14	TRANSISTOR	2N4400	150200	2	Q2, 6			
15	TRANSISTOR	2N4402	150201	4	Q1, 4, 7, 8			
16	TRANSISTOR	2N5460	150202	1	Q5			
17	TRANSISTOR	2N2913	150203	1	Q3			
18								
19								
20	DIODE	1N3064	150300	8	CR1, 2, 3, 4, 5, 6, 7, 8			
21	DIODE, ZENER	1N752A	150302	1	VR1			
22	DIODE, ZENER	1N751A	150311	1	VR2			
23								
24								
25	CAPACITOR, MICA	100 Pf	150102-101	3	C6, 10, 11			
26	CAPACITOR, MYLAR	1000 Pf	150101-102	1	C9			
27	CAPACITOR, MYLAR	.0015 Uf	150101-152	1	C7			
28	CAPACITOR, MYLAR	.01 Uf	150101-103	1	C8			
29	CAPACITOR, TANTL., 10%	1 Uf	150100-105	5	C1, 2, 3, 4, 5			
30								
31								
32								
33	RESISTOR VAR., 20 TURN	2K	150003-202	1	R13			

MATERIAL LIST							
TITLE ASSY. P.C.B. PHASED LOCKED DOUBLE F DATA SEPARATOR				DWG NO. 200157-000		REV E	SHEET 2 OF 2
PERSCI, INC.							
ITEM NO.	DRAWING TITLE			DWG NO.	QTY	REMARKS	
34							
35	RESISTOR	$\frac{1}{2}W$	5% 1K	150002-102	1	R28	
36							
37	RESISTOR	$\frac{1}{2}W$	5% 330	150000-331	1	R3	
38	RESISTOR	$\frac{1}{2}W$	5% 750	150000-751	1	R15	
39	RESISTOR	$\frac{1}{2}W$	5% 1K	150000-102	11	R2,4,5,6,12,14,16, R20,22,26,27	
40	RESISTOR	$\frac{1}{2}W$	5% 1.5K	150000-152	1	R10	
41	RESISTOR	$\frac{1}{2}W$	5% 3.3K	150000-332	2	R1, 17	
42	RESISTOR	$\frac{1}{2}W$	5% 3.9K	150000-392	2	R23, 24	
43	RESISTOR	$\frac{1}{2}W$	5% 5.1K	150000-512	1	R21	
44	RESISTOR	$\frac{1}{2}W$	5% 5.6K	150000-562	1	R11	
45	RESISTOR	$\frac{1}{2}W$	5% 10K	150000-103	1	R19	
46	RESISTOR	$\frac{1}{2}W$	5% 15K	150000-153	1	R9	
47	RESISTOR	$\frac{1}{2}W$	5% 22K	150000-223	2	R7, 18	
48	RESISTOR	$\frac{1}{2}W$	5% 240K	150000-244	1	R8	
49							
50							
51							
52	HOUSING, CONNECTOR, 10 Pin			100032-010	1	P6	
53							
54							
55							
56	PIM, MALE			100046	5	TP1, 2, 3, 4, 5	
57							
58	WIRE, INSUL., AWG 24						
59							
60							
61							
	SCHEMATIC			200115	REF	REV C	
	ARTWORK			200156	REF		

 REV
E
 DWG NO.
200157-000



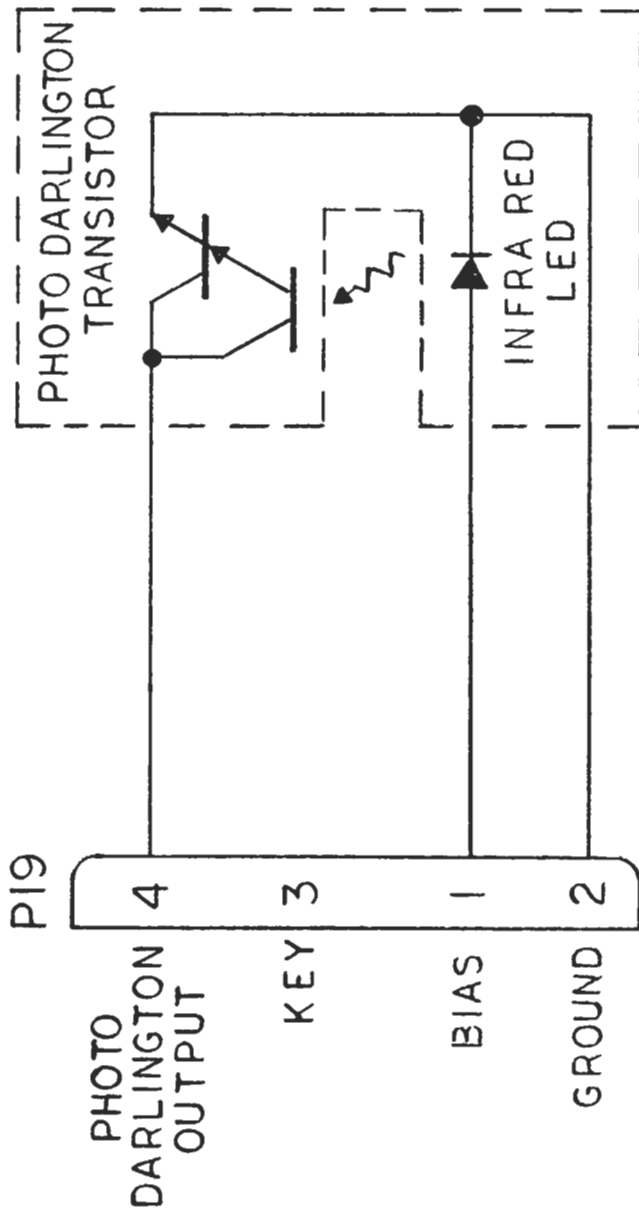
PERSCI, INC.

SCHEMATIC
WRITE PROTECT MODULE
SIDE 0

270/272/277 SHT 1 OF 1

200231

A



PERSCI, INC.

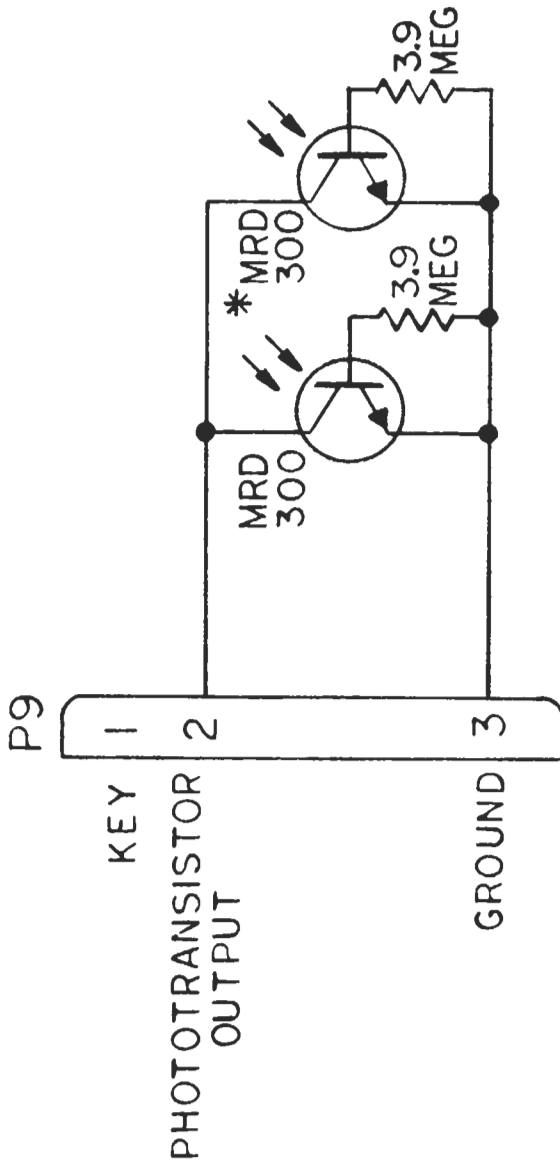
SCHEMATIC
WRITE PROTECT MODULE
SIDE 1

270/272/277

SHT 1 OF 1

200232

A



* NOTE
 SECOND PHOTOTRANSISTOR
 OPTIONAL FOR DUAL INDEX
 OPTION.

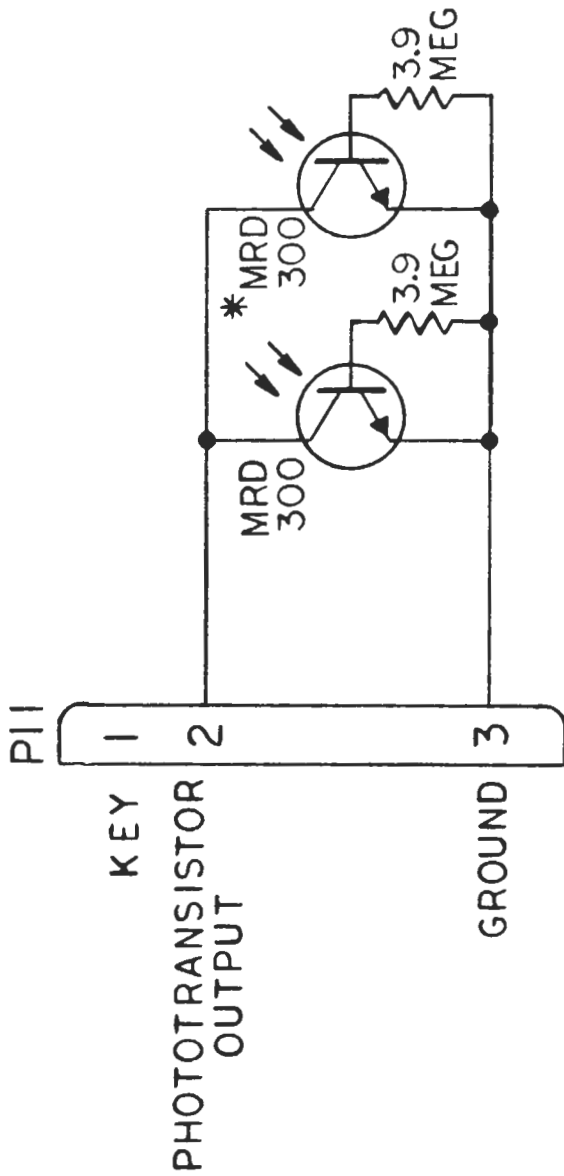


PERSCI, INC.

SCHEMATIC
 PHOTOTRANSISTOR ASSEMBLY
 SIDE 1

270/272/277 SHT 1 OF 1

200233 C

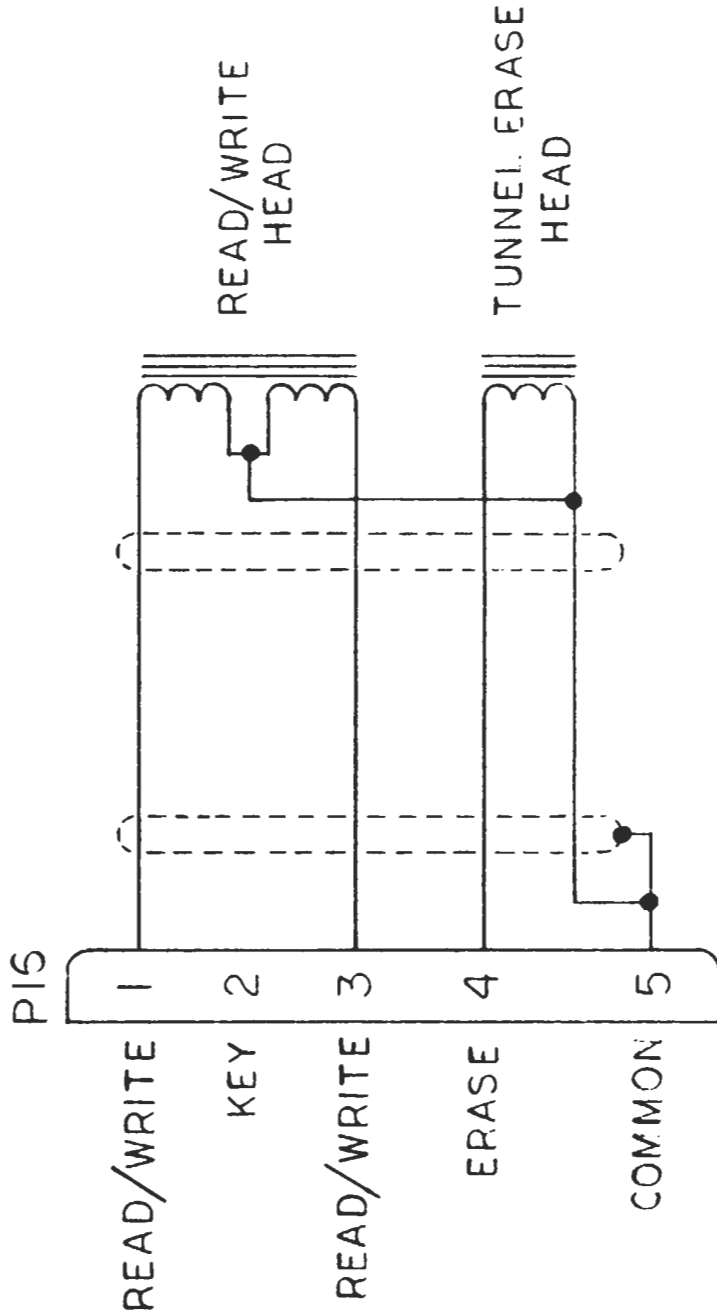


PERSCI, INC.

* NOTE
SECOND PHOTOTRANSISTOR
OPTIONAL FOR DUAL INDEX
OPTION.

SCHEMATIC
PHOTOTRANSISTOR ASSEMBLY
SIDE Ø

270/272/277 SHT 1 OF 1 200234 C



PERSCI, INC.

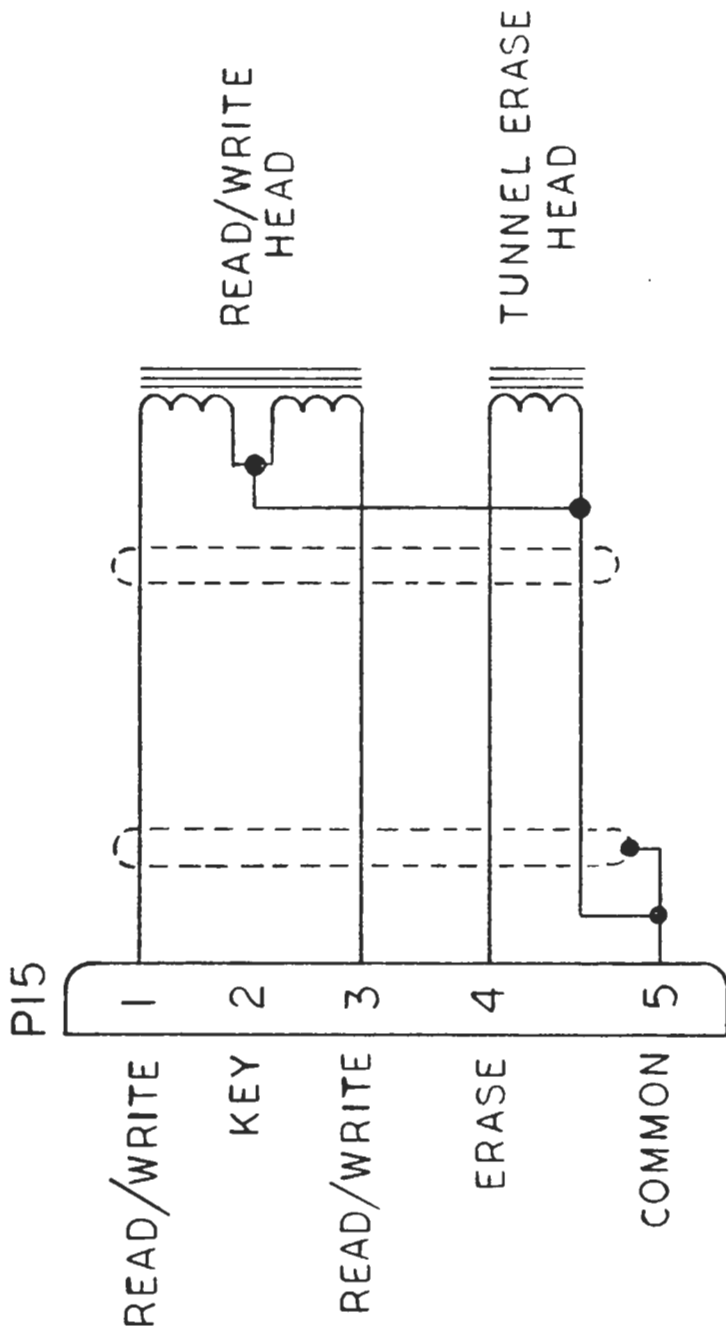
SCHEMATIC
 READ/WRITE HEAD ASSEMBLY
 SIDE 0

270/272/277

SHT 1 OF 1

200235

A



PERSCI, INC.

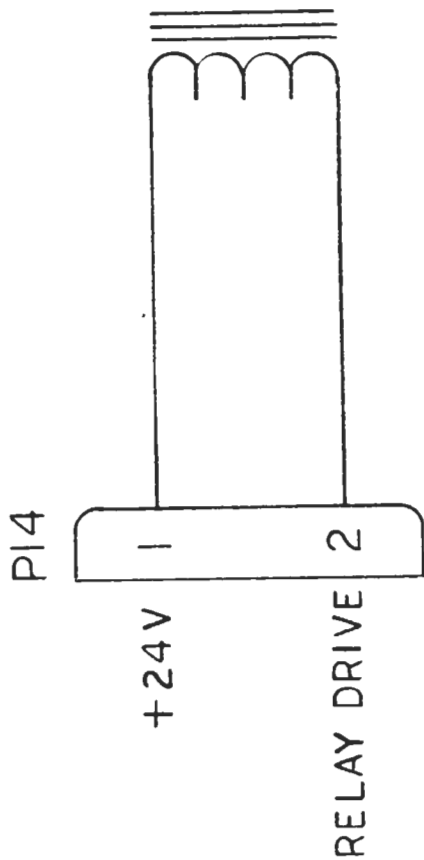
SCHEMATIC
 READ/WRITE HEAD ASSEMBLY
 SIDE 1

270/272/277

SHT 1 OF 1

200236

A



PERSCI, INC.

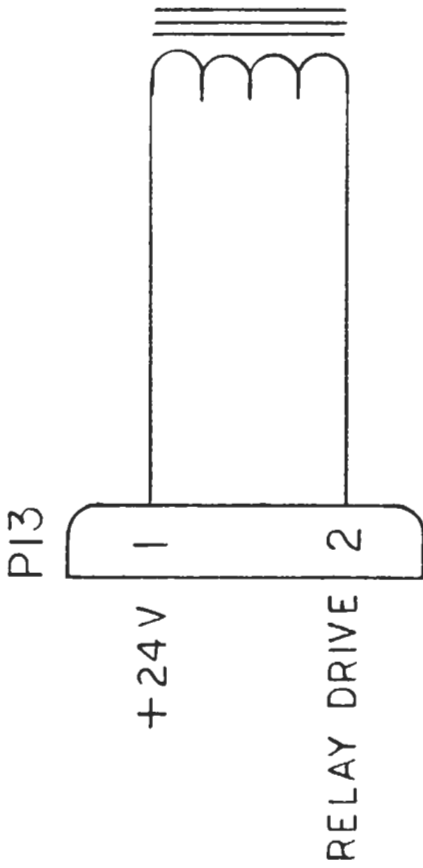
SCHEMATIC
HEAD LOAD ASSEMBLY
SIDE 0

270/272/277

SHT 1 OF 1

200237

A



PERSCI, INC.

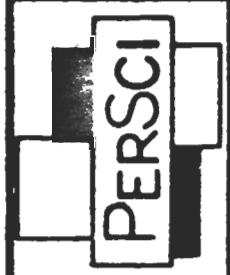
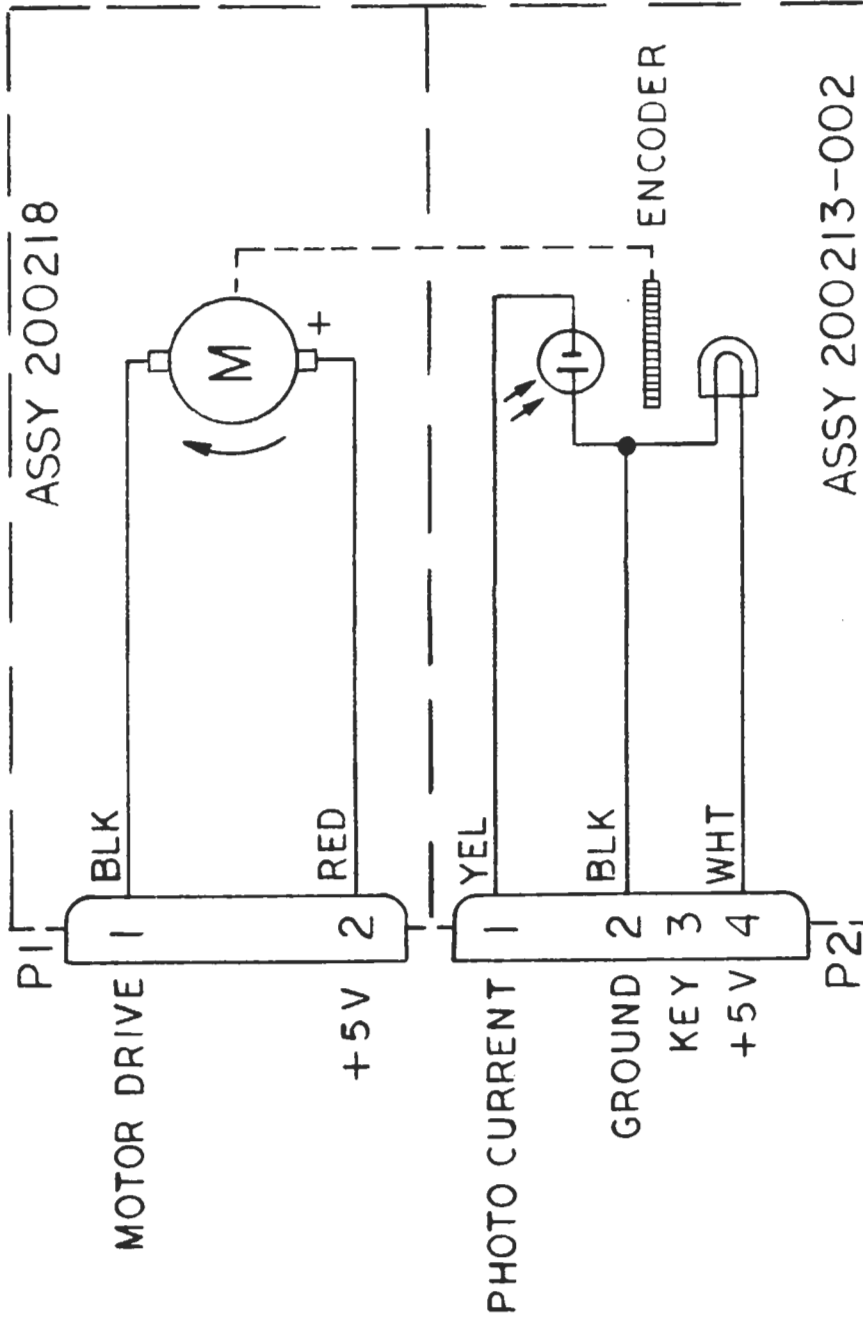
SCHEMATIC
HEAD LOAD ASSEMBLY
SIDE 1

270/272/277

SHT 1 OF 1

200238

A

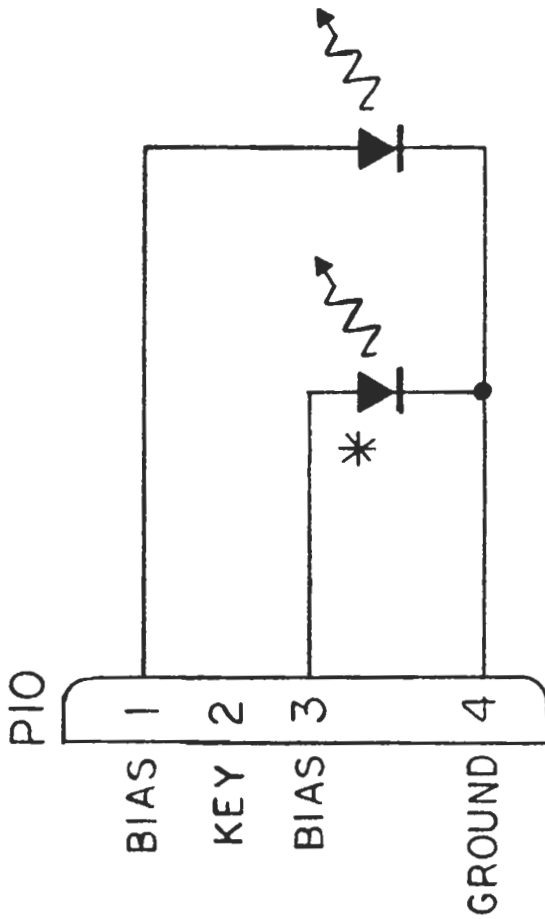


PERSCI, INC.

SCHEMATIC
SPINDLE MOTOR ASSEMBLY

270/272/277 SHT 1 OF 1

200239 | B



*NOTE;
SECOND LED OPTIONAL FOR
DUAL INDEX OPTION DRIVE.



PERSCI, INC.

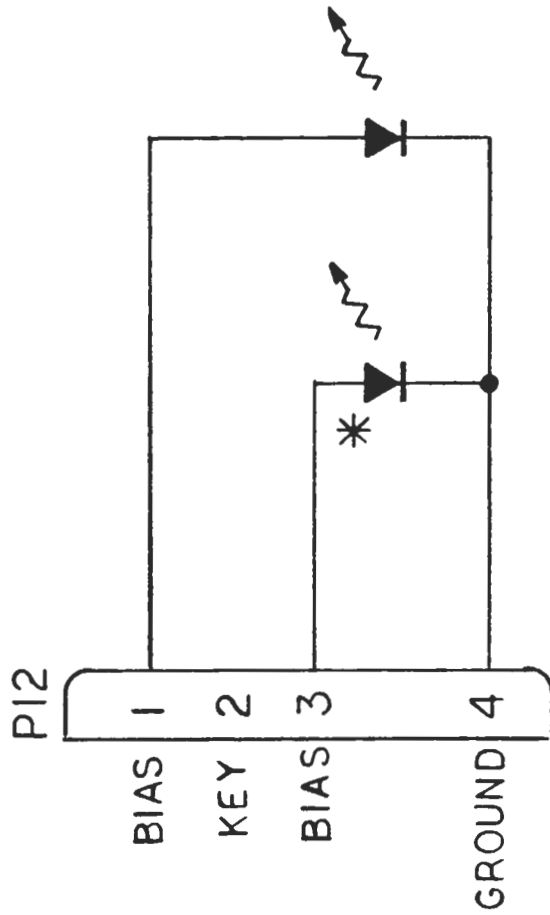
SCHEMATIC
LED ASSEMBLY
SIDE 1

270/272/277

SHT10FI

200240

B



* NOTE
 SECOND LED OPTIONAL FOR
 DUAL INDEX OPTION DRIVE.



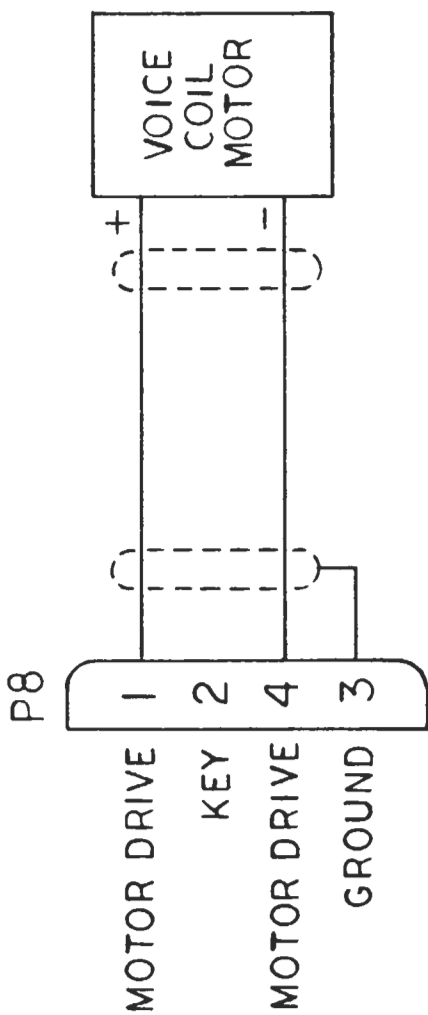
PERSCI, INC.

SCHEMATIC
 LED ASSEMBLY
 SIDE 0

270/272/277 SHT 10F1

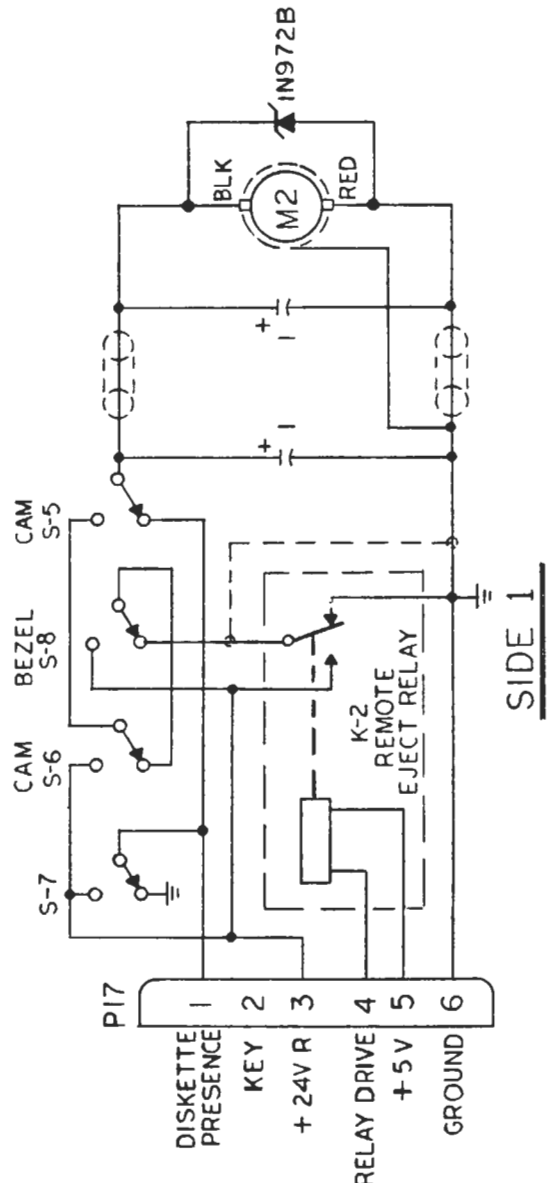
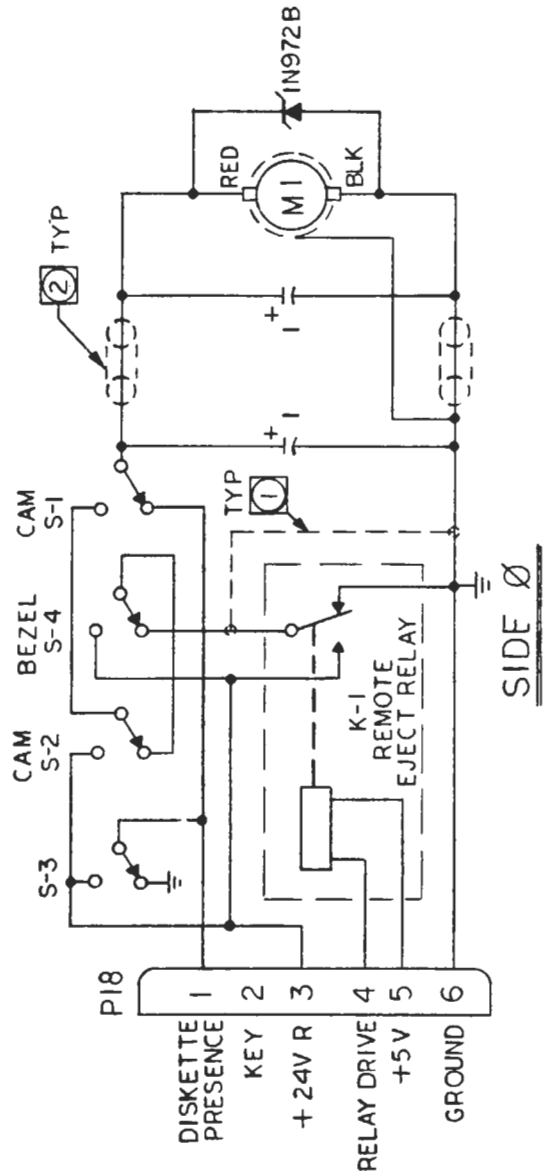
200241

B




		PERSCI, INC.	
SCHEMATIC POSITIONER MOTOR			
270/272/277	SHT 1 OF 1	200242	B

REV. DESCRIPTION		200243 B	
REV.	DESCRIPTION	CHK.	DATE APPROVED
A	MFG RELEASE		
B	ECO 109		



- NOTES:
- ③ ALL SWITCHES SHOWN NORMALLY CLOSED.
 - ② FERRITE BEAD PERSCI 100031.
 - ① OPTIONAL WIRING WITHOUT RELAY.



PERSCI, INC.

SCHEMATIC
EJECT MOTOR ASSEMBLY

270/272/277	SHT 10F1	200243	B
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MATERIAL LIST

REV
STITLE
ASSEMBLY, PCB DATA AND INTERFACEDWG NO.
200263-000REV
S

SHEET 1 OF 5

MODEL 270 BASIC BOARD

PERSCI, INC.

DWG NO.
200263-000

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
1	BOARD, PROCESSED	200262	1	REV H
2				
3				
4				
5				
6				
7				
8				
9				
10				
11	IC LM311N	150600	3	U18, 22, 61
12	IC LM1408	150664	1	U55
13	IC MC1458C-P1	150602	2	U40, 51
14	IC 7400	150603	5	U15, 28, 53, 57, 60
15	IC 7404	150604	4	U20, 30, 38, 41
16	IC 7408	150605	4	U26, 29, 45, 54
17	IC 7432	150608	4	U19, 50, 56, 58
18	IC 7474	150609	6	U14, 24, 39, 46, 47, 52
19	IC 7486	150611	1	U21
20	IC 74123	150612	4	U10, 12, 25, 44
21	IC 74193	150614	2	U42, 43
22	IC 75451	150616	1	U17
23	IC 75452	150617	2	U31, 36
24	IC 75453	150618	9	U2, 3, 4, 5, 6, 7, 8, 23, 59
25	IC 72733	150619	2	U33, 35
26	IC 7416	150621	2	U13, 48
27	IC 7406	150622	1	U37
28	IC SN72306P	150646	2	U34, 32
29				
30	RESISTOR NETWORK 4.7K	150050	1	U9
31	RESISTOR NETWORK 220/330	150051	1	U1
32				
33				

MATERIAL LIST

REV
S

TITLE
ASSEMBLY, PCB DATA AND INTERFACE

DWG NO.
200263-000

REV
S

SHEET 2 OF 5

MODEL 270 BASIC BOARD

PERSCI, INC.

DWG NO.
200263-000

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
34	TRANSISTOR 2N4400	150200	5	Q2,26,27,28,31
35	TRANSISTOR 2N4402	150201	25	Q3,4,5,6,7,8,9,10, 13,16,17,18,19,20, 21,22,23,24,25, 29,30,32,33,34,35
36	TRANSISTOR 2N5460	150202	4	Q11,12,14,15
37	TRANSISTOR 2N2913	150203	1	Q1
38	TRANSISTOR 2N706A	150207	4	Q36,37,38,39
39				
40				
41				
42	DIODE 1N3064	150300	16	CR3,4,5,6,7,8, 9,10,11,12,13,14, 15,16,17,18
43	DIODE, ZENER 1N752A	150302	1	VR1
44	DIODE, ZENER 1N759A	150313	2	VR2,4
45	DIODE, ZENER 1N751A	150311	1	VR3
46	INDUCTOR 200UH	150094	1	L1
47	CAPACITOR, MICA .001UF	150102-102	2	C58,59
48				
49	CAPACITOR, MICA 100pf	150102-101	3	C1,50,51
50	CAPACITOR, MICA 510pf	150102-511	6	C21,26,46,49,14,50
51	CAPACITOR, MYLAR .001UF	150101-102	2	C3,4
52	CAPACITOR, CERAMIC .01UF	150103-103	15	C7,11,18,20,24,25, 28,30,34,37,38,43, 45,52,56
53	CAPACITOR, TANTL 10% 0.1UF	150100-104	3	C35,42,44
54	CAPACITOR, TANTL 10% 1UF	150100-105	23	C2,5,6,8,9,10,12, 13,15,16,17,19, 22, 23,27,29,33,39,47, 53,54,55,57

MATERIAL LIST

REV S
DWG NO. 200263-000

TITLE ASSEMBLY, PCB DATA AND INTERFACE		DWG NO. 200263-000		REV S	SHEET <u>3</u> OF <u>5</u>
MODEL 270 BASIC BOARD		PERSCI, INC.			
ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS	
55	CAPACITOR, TANTL 22UF	150100-226	1	C48	
56					
57					
58					
59	RESISTOR, VARIABLE 2K	150003-202	1	R154	
60					
61	RESISTOR 1/2 W., 5% 10	150002-100	2	R121,126	
62	RESISTOR 1/2 W., 5% 47	150002-470	2	R69,70	
63	RESISTOR 1/2 W., 5% 68	150002-680	4	R104,105,106,107	
64	RESISTOR 1/2 W., 5% 1K	150002-102	1	R169	
65	RESISTOR, 1/2 W., 1% 1.50K	150001-1501	1	R81	
66	RESISTOR 1/2 W., 1% 332	150001-3320	2	R13,14	
67	RESISTOR 1/2 W., 1% 1.78K	150001-1781	1	R133	
68	RESISTOR 1/2 W., 1% 3.01K	150001-3011	1	R78	
69	RESISTOR 1/2 W., 1% 10K	150001-1002	5	R108,109,147,148,149	
70	RESISTOR 1/2 W., 1% 24.9K	150001-2492	1	R152	
71	RESISTOR 1/2 W., 1% 30.1K	150001-3012	1	R146	
72	RESISTOR 1/2 W., 1% 4.64K	150001-4641	2	R86,87	
73					
74	RESISTOR 1/2 W., 5% 10	150000-100	13	R3,10, 12,18,19, 33,34,37,38,41, 42,56,77	
75	RESISTOR 1/2 W., 5% 47	150000-470	2	R26,27	
76	RESISTOR 1/2 W., 5% 100	150000-101	9	R23,29,82,83,84,85, 101,103,128.	
77	RESISTOR, 1/4 W., 5% 300	150000-301	4	R35,36,39,40	
78	RESISTOR 1/2 W., 5% 220	150000-221	7	R5,7,49,53,58, 120,125	
79	RESISTOR 1/2 W., 5% 330	150000-331	13	R6,8,9,15,16,17, 59,65,66,67,68, 119,124	

MATERIAL LIST

REV
STITLE
ASSEMBLY, PCB DATA AND INTERFACEDWG NO.
200263-000REV
S

SHEET 4 OF 5

MODEL 270 BASIC BOARD

PERSCI, INC.

DWG NO.
200263-000

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
80	RESISTOR $\frac{1}{4}$ W., 5% 510	150000-511	1	R111
81	RESISTOR $\frac{1}{4}$ W., 5% 1K	150000-102	24	R1,2,48,52,64,71, 72,73,74,89,92,95,98, 112,114,117,118,122, 123,132,134,158,166, 170
82	RESISTOR $\frac{1}{4}$ W., 5% 2K	150000-202	10	R22,24,28,30, 110,115,116,133, 137,139
83	RESISTOR $\frac{1}{4}$ W., 5% 430	150000-431	1	R25
84	RESISTOR $\frac{1}{4}$ W., 5% 3.9K	150000-392	4	R4,45,57,135
85	RESISTOR $\frac{1}{4}$ W., 5% 4.7K	150000-472	11	R60,61,175, 130,136,155,159, 160,161,167,168
86	RESISTOR $\frac{1}{4}$ W., 5% 5.1K	150000-512	2	R153,174
87	RESISTOR $\frac{1}{4}$ W., 5% 6.8K	150000-682	5	R46,47,50,51,62
88	RESISTOR $\frac{1}{4}$ W., 5% 10K	150000-103	24	R20,21,31,32,43,44, 54,55,79,131,151,156, 157,162,163,164,165, 171,172,173, 90,96
89	RESISTOR $\frac{1}{4}$ W., 5% 15K	150000-153	2	R100, 102 178,179
90	RESISTOR $\frac{1}{4}$ W., 5% 18K	150000-183	1	R63
91	RESISTOR $\frac{1}{4}$ W., 5% 20K	150000-203	2	R141,144
92	RESISTOR $\frac{1}{4}$ W., 5% 22K	150000-223	3	R75,76,80
93	RESISTOR $\frac{1}{4}$ W., 5% 30K	150000-303	3	R93,99,140
94				
95	RESISTOR $\frac{1}{4}$ W., 5% 39K	150000-393	2	R143,145
96	RESISTOR $\frac{1}{4}$ W., 5% 47K	150000-473	3	R150,176,177
97	RESISTOR $\frac{1}{4}$ W., 5% 220K	150000-224	2	R91,97
98	RESISTOR $\frac{1}{4}$ W., 5% 100K	150000-104	2	R113,129
99	RESISTOR $\frac{1}{4}$ W., 5% 240K	150000-244	1	R142
100	RESISTOR $\frac{1}{4}$ W., 5% 1MEG	150000-105	1	R127

MATERIAL LIST

REV B
DWG NO. 200263-001

TITLE ASSEMBLY, PCB DATA AND INTERFACE	DWG NO. 200263-001	REV B	SHEET 1 OF 1
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MODEL 270/272 SINGLE DENSITY	PERSCI, INC.
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ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
	USE BASIC BD 200263-000			
	LATEST REVISION AND			
	ADD THE FOLLOWING:			
1				
2				
3	CAPACITOR, TANTL., 10% 0.1UF	150100-104	1	C36
4	CAPACITOR, TANTL., 10% 0.1UF	150100-104	2	C40,41
5				
6	RESISTOR ¼ W., 5% 36K	150000-363	2	R88,94
7				
8	WIRE, INSULATED AWG 24		A/R	JUMPER FROM A TO B
				JUMPER FROM D TO E
				JUMPER FROM F TO G
				JUMPER FROM H TO J
				JUMPER FROM M TO P
				JUMPER FROM R TO S
				JUMPER FROM W TO X
				JUMPER FROM AB TO AC
				JUMPER FROM AD TO AE
				JUMPER FROM AH TO AJ
				JUMPER FROM AL TO AM
				JUMPER FROM AY TO AT
				JUMPER FROM AV TO AW
				JUMPER FROM BA TO BB
				JUMPER FROM BD TO BE
				JUMPER FROM BK TO BM
				CHASSIS GND W1
	NOTE: JUMPER POINTS NOT LISTED			
	ARE OPEN (NOT USED)			

MATERIAL LIST

REV C
DWG NO. 200263-004

TITLE		DWG NO.		REV	SHEET
ASSEMBLY, PCB DATA AND INTERFACE		200263-002		C	1 OF 1
MODEL 270 DOUBLE DENSITY		PERSCI, INC.			
ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS	
	USE BASIC BD 200263-000				
	LATEST REVISION AND				
	ADD THE FOLLOWING:				
1	IC 74193	150614	2	U16,27	
2					
3	CAPACITOR, TANTL., 10% 0.1UF	150100-104	1	C36	
4	CAPACITOR, TANTL., 10% 1UF	150100-105	2	C40,41	
5					
6	RESISTOR, 1/4 W., 5% 11K	150000-113	2	R38,94	
7					
8	WIRE, INSULATED AWG 24		A/R	JUMPER FROM A TO B	
				JUMPER FROM D TO E	
				JUMPER FROM F TO G	
				JUMPER FROM H TO J	
				JUMPER FROM M TO P	
				JUMPER FROM R TO S	
				JUMPER FROM W TO Y	
				JUMPER FROM AA TO AB	
				JUMPER FROM AD TO AF	
				JUMPER FROM AH TO AK	
				JUMPER FROM AL TO AM	
				JUMPER FROM AT TO AY	
				JUMPER FROM AV TO AW	
				JUMPER FROM BA TO BB	
				JUMPER FROM BD TO BE	
				JUMPER FROM BH TO BJ	
				JUMPER FROM BK TO BM	
				SECTOR "0" JUMPER 16	
	NOTE: JUMPER POINTS NOT LISTED			SECTOR "1" JUMPER ?	
	ARE OPEN (NOT USED)			CHASSIS GND W1	

MATERIAL LIST

REV E
DWG NO. 200263-00

TITLE		DWG NO.		REV	SHEET
ASSEMBLY, PCB DATA AND INTERFACE		200263-003		E	1 OF 1
MODEL 277 ROTARY SELECT		PERSCI, INC.			
ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS	
	USE BASIC BD 200263-000				
	LATEST REVISION AND				
	ADD THE FOLLOWING:				
1					
2					
3					
4	CAPACITOR, TANTL., 10% 0.1UF	150100-104	3	C40,41,36	
5					
6	RESISTOR, 1/2 W., 5% 36K	150000-363	2	R38,94	
7	MODULE, SELECT	200288-005	1	U11	
8	WIRE, INSULATED, AWG 24		A/R	JUMPER FROM A TO B	
				JUMPER FROM J TO Z	
				JUMPER FROM K TO L	
				JUMPER FROM N TO P	
				JUMPER FROM S TO T	
				JUMPER FROM U TO V	
				JUMPER FROM W TO X	
				JUMPER FROM AB TO AC	
				JUMPER FROM AD TO AE	
				JUMPER FROM AH TO AJ	
				JUMPER FROM AM TO AN	
				JUMPER FROM AP TO AR	
				JUMPER FROM AS TO AT	
				JUMPER FROM AV TO AW	
				JUMPER FROM BA TO BB	
				JUMPER FROM BD TO BE	
				JUMPER FROM BK TO BM	
				CHASSIS GND W1	
	NOTE: JUMPER POINTS NOT LISTED ARE OPEN (NOT USED)				

9 EPT 4 - 290
MATERIAL LIST

REV C
DWG NO. 200263-00.

TITLE		DWG NO.		REV	SHEET 1 OF 1
ASSEMBLY, PCB DATA AND INTERFACE		200263-005		C	
MODEL 270, 16 SECTORS			PERSCI, INC.		
ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS	
	USE BASIC BD 200263-000				
	LATEST REVISION AND				
	ADD THE FOLLOWING:				
1	IC 74193	150614	2	U16,27	
2					
3	CAPACITOR, TANTL., 10% 0.1UF	150100-104	1	C36	
4	CAPACITOR, TANTL., 10% 1UF	150100-105	2	C40,41	
5					
6	RESISTOR, 1/4W., 5% 11K	150000-113	2	R38,94	
7					
8	WIRE, INSULATED, AWG 24		A/R	JUMPER FROM A TO B	
				JUMPER FROM D TO E	
				JUMPER FROM F TO G	
				JUMPER FROM H TO J	
				JUMPER FROM M TO P	
				JUMPER FROM R TO S	
				JUMPER FROM W TO Y	
				JUMPER FROM AA TO AB	
				JUMPER FROM AD TO AF	
				JUMPER FROM AH TO AK	
				JUMPER FROM AL TO AM	
				JUMPER FROM AT TO AY	
				JUMPER FROM AV TO AW	
				JUMPER FROM BA TO BB	
				JUMPER FROM BD TO BE	
				JUMPER FROM BH TO BF	
				JUMPER FROM BK TO BM	
				SECTOR "0" JUMPER 16	
				SECTOR "1" JUMPER 16	
	NOTE: JUMPER POINTS NOT LISTED			CHASSIS GND W1	
	ARE OPEN (NOT USED)				

MATERIAL LIST

REV
200263-00,
DWG NO.

TITLE		DWG NO.		REV	SHEET
ASSEMBLY, PCB DATA AND INTERFACE		200263-007			1 OF 1
MODEL 270 HARD SECTOR 32 SECTORS		PERSCI, INC.			
ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS	
	USE BASIC BD 200263-000				
	LATEST REVISION AND ADD				
	THE FOLLOWING:				
1	ASSY, SELECT MODULE	200288-003	1	U11	
2					
3	CAPACITOR, TANTL., 10% 0.1UF	150100-104	1	C36	
4	CAPACITOR, TANTL., 10% 1UF	150100-105	2	C40,41	
5					
6	RESISTOR, 1/2 W., 5% 11K	150000-113	2	R88,94	
7					
8	WIRE, INSULATED, AWG 24		A/R	JUMPER FROM A TO B	
				JUMPER FROM D TO E	
				JUMPER FROM F TO G	
				JUMPER FROM H TO J	
				JUMPER FROM N TO P	
				JUMPER FROM R TO S	
				JUMPER FROM W TO Y	
				JUMPER FROM AA TO AB	
				JUMPER FROM AD TO AF	
				JUMPER FROM AH TO AK	
				JUMPER FROM AL TO AM	
				JUMPER FROM AT TO AY	
				JUMPER FROM AU TO AW	
				JUMPER FROM BA TO BB	
				JUMPER FROM BD TO BE	
				JUMPER FROM BH TO BJ	
				JUMPER FROM BK TO BM	
				SECTOR "0" JUMPER 32	
				SECTOR "1" JUMPER 32	
	NOTE: JUMPER POINTS NOT LISTED			CHASSIS GND W1	
	ARE OPEN (NOT USED)				

- 9 EPT 4 - 292 -
MATERIAL LIST

REV B
DWG NO. 200263-008

TITLE		DWG NO.		REV	SHEET
ASSEMBLY, PCB DATA AND INTERFACE		200263-008		B	1 OF 1
MODEL 270 SINGLE DENSITY, SELECTABLE DRIVE		PERSCI, INC.			
ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS	
	USE BASIC BD 200263-000				
	LATEST REVISION AND				
	ADD THE FOLLOWING:				
1	ASSY., SELECT MODULE	200288-003	1	U11	
2					
3	CAPACITOR, TANTL., 10% 0.1UF	150100-104	1	C36	
4	CAPACITOR, TANTL., 10% 0.1UF	150100-104	2	C40,41	
5					
6	RESISTOR, 1/4 W., 5% 36K	150000-363	2	R88,94	
7					
8	WIRE, INSULATED AWG 24		A/R	JUMPER FROM A TO B	
				JUMPER FROM D TO E	
				JUMPER FROM F TO G	
				JUMPER FROM H TO J	
				JUMPER FROM M TO P	
				JUMPER FROM R TO S	
				JUMPER FROM W TO X	
				JUMPER FROM AB TO AC	
				JUMPER FROM AD TO AE	
				JUMPER FROM AH TO AJ	
				JUMPER FROM AL TO AM	
				JUMPER FROM AY TO AT	
				JUMPER FROM AV TO AW	
				JUMPER FROM BA TO BB	
				JUMPER FROM BD TO BE	
				JUMPER FROM BK TO BM	
				CHASSIS GND W1	
	NOTE: JUMPER POINTS NOT LISTED				
	ARE OPEN (NOT USED)				

MATERIAL LIST

REV C
DWG NO. 200263-009

TITLE		DWG NO.		REV	SHEET
ASSEMBLY, PCB DATA AND INTERFACE		200263-009		C	1 OF 1
MODEL 270 SELECTABLE DRIVE, 16 SEPARATED SECTORS		PERSCI, INC.			
ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS	
	USE BASIC BD 200263-000				
	LATEST REVISION AND				
	ADD THE FOLLOWING:				
1	IC 74193	150614	2	U16,27	
2	IC 75455	150618	1	U59 'DELETE'	
3	CAPACITOR, TANTL., 10% 0.1UF	150100-104	1	C36	
4	CAPACITOR, TANTL., 10% 1UF	150100-105	2	C40,41	
5					
6	RESISTOR, 1/4 W., 5% 11K	150000-113	2	R88,94	
7	ASSY., SELECT MODULE	200288-003	1	U11	
8	WIRE, INSULATED AWG 24		A/R	JUMPER FROM A TO B	
				JUMPER FROM D TO E	
				JUMPER FROM F TO G	
				JUMPER FROM H TO J	
				JUMPER FROM M TO P	
				JUMPER FROM R TO S	
				JUMPER FROM W TO Y	
				JUMPER FROM AA TO AB	
				JUMPER FROM AD TO AF	
				JUMPER FROM AH TO AK	
				JUMPER FROM AL TO AM	
				JUMPER FROM AT TO AY	
				JUMPER FROM AV TO AW	
				JUMPER FROM BA TO BB	
				JUMPER FROM BD TO BE	
				JUMPER FROM BH TO BJ	
				JUMPER FROM BK TO BM	
				SECTOR "0" JUMPER 16	
				SECTOR "1" JUMPER 16	
	NOTE: JUMPER POINTS NOT LISTED			CHASSIS GND W1	
	ARE OPEN (NOT USED)				

9 EPT 4 - 294
MATERIAL LIST

REV 5
 DWG NO. 200263-010

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
TITLE ASSEMBLY, PCB DATA AND INTERFACE		DWG NO. 200263-010		REV 5
MODEL 277 HARD SECTOR 32 SECTOR ROTARY SELECT		PERSCI, INC.		
SHEET 1 OF 1				
1	USE BASIC BD 200263-000			
2	LATEST REVISION AND			
3	ADD THE FOLLOWING:			
3	CAPACITOR, TANTL., 10% 0.1UF	150100-104	1	C36
4	CAPACITOR, TANTL., 10% 1.0UF	150100-105	2	C40,41
5				
6	RESISTOR, 1/4 W., 5% 11K	150000-113	2	R88,94
7	MODULE, SELECT	200288-005	1	U11
8	WIRE, INSULATED, AWG 24		A/R	JUMPER FROM A TO B
				JUMPER FROM J TO Z
				JUMPER FROM K TO L
				JUMPER FROM N TO P
				JUMPER FROM S TO T
				JUMPER FROM W TO Y
				JUMPER FROM AA TO AB
				JUMPER FROM AD TO AF
				JUMPER FROM AH TO AK
				JUMPER FROM AM TO AN
				JUMPER FROM AP TO AR
				JUMPER FROM AS TO AT
				JUMPER FROM AV TO AW
				JUMPER FROM BC TO BB
				JUMPER FROM BD TO BE
				JUMPER FROM BL TO BM
				SECTOR "0" JUMPER 32
				SECTOR "1" JUMPER 32
	NOTE: JUMPER POINTS NOT LISTED			CHASSIS GND W1
	ARE OPEN (NOT USED)			

MATERIAL LIST

REV B
DWG NO. 200263-011

TITLE ASSEMBLY, PCB DATA AND INTERFACE	DWG NO. 200263-011	REV A	SHEET 1 OF 1
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MODEL 277 ROTARY SELECT MFM 32 SECTOR **PERSCI, INC.**

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
	USE BASIC BD 200263-000			
	LATEST REVISION AND			
	ADD THE FOLLOWING:			
1				
2				
3	CAPACITOR, TANTL., 10% 0.1UF	150100-104	1	C36
4	CAPACITOR, TANTL., 10% 1.0UF	150100-105	2	C40,41
5				
6	RESISTOR, 1/4 W., 5% 11K	150000-113	2	R38,94
7	MODULE, SELECT	200238-005	1	U11
8	WIRE, INSULATED, AWG 24		A/R	JUMPER FROM A TO B
				JUMPER FROM J TO Z
				JUMPER FROM K TO L
				JUMPER FROM N TO P
				JUMPER FROM S TO T
				JUMPER FROM W TO Y
				JUMPER FROM AA TO AB
				JUMPER FROM AD TO AF
				JUMPER FROM AH TO AK
				JUMPER FROM AM TO AN
				JUMPER FROM AP TO AR
				JUMPER FROM AS TO AT
				JUMPER FROM AV TO AW
				JUMPER FROM BC TO BB
				JUMPER FROM BD TO BE
				JUMPER FROM BH TO BJ
				JUMPER FROM BL TO BM
				SECTOR "0" JUMPER 32
				SECTOR "1" JUMPER 32
	NOTE: JUMPER POINTS NOT LISTED			CHASSIS GND W1
	ARE OPEN (NOT USED)			

MATERIAL LIST

REV C
200263-012
DWG NO.

TITLE
ASSEMBLY, PCB DATA AND INTERFACE

DWG NO.
200263-012

RFV
C

SHEET 1 OF 2

MODEL 270 DOUBLE DENSITY
EXTERNAL PLO SYNC

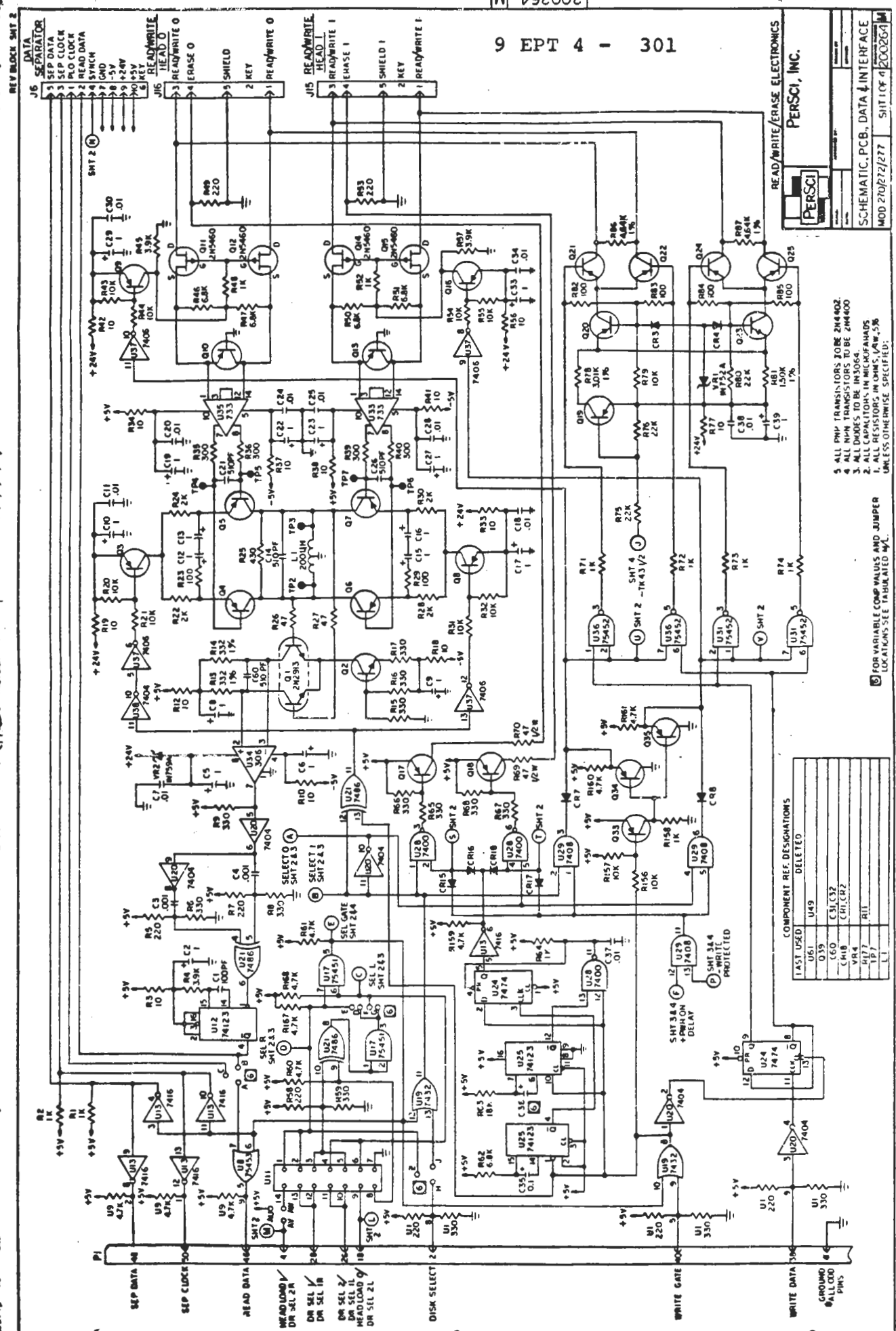
PERSCI, INC.

ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS
	USE BASIC BD 200263-000 REV "H"			
	OR LATER REVISION AND ADD THE			
	FOLLOWING:			
1				
2				
3	CAPACITOR, TANTL., 10% 0.1 UF	150100-104	1	C36
4	CAPACITOR, TANTL., 10% 0.1 UF	150100-104	2	C40, 41
5				
6	RESISTOR, 1/4 W., 5% 36K	150000-363	2	R88, 94
7	MODULE SELECT	200288-001	1	U11
8	WIRE, INSULATED AWG 24		A/R	JUMPER FROM A TO B
				JUMPER FROM D TO E
				JUMPER FROM F TO G
				JUMPER FROM H TO J
				JUMPER FROM M TO P
				JUMPER FROM R TO S
				JUMPER FROM W TO X
				JUMPER FROM AB TO AC
				JUMPER FROM AD TO AE
				JUMPER FROM AH TO AJ
				JUMPER FROM AL TO AM
				JUMPER FROM AY TO AT
				JUMPER FROM AV TO AW
				JUMPER FROM BA TO BB
				JUMPER FROM BD TO BE
				JUMPER FROM BK TO BM
				CHASSIS GND W1
			*	JUMP BH TO U11 PIN 10
	NOTE: JUMPER POINTS NOT LISTED			
	ARE OPEN (NOT USED)			
	*INSTALL ON BACK SIDE OF PCB			
	USING ITEM 129			

MATERIAL LIST

REV (f)
DWG NO. 200263-013

TITLE		DWG NO.		REV	SHEET
ASSEMBLY, PCB DATA AND INTERFACE		200263-013		/	1 OF 1
MODEL 270 SPECIAL INTERFACE		PERSCI, INC.			
ITEM NO.	DRAWING TITLE	DWG NO.	QTY	REMARKS	
	USE BASIC BD 200263-000				
	REVISION 'N' AND LATER				
	ADD THE FOLLOWING				
1					
2					
3	CAPACITOR, TANTL., 10% 0.1UF	150100-104	1	C36	
4	CAPACITOR, TANTL., 10% 0.1UF	150100-104	2	C40,41	
5					
6	RESISTOR 1/4W., 5% 36K	150000-363	2	R88,94	
7	MODULE, SELECT	200288-003	1	U11	
8	WIRE, INSULATED AWG24		A/R	JUMPER FROM A TO B	
				JUMPER FROM D TO E	
				JUMPER FROM F TO G	
				JUMPER FROM H TO J	
				JUMPER FROM M TO P	
				JUMPER FROM R TO S	
				JUMPER FROM W TO X	
				JUMPER FROM AA TO AB	
				JUMPER FROM AD TO AE	
				JUMPER FROM AK TO AH	
				JUMPER FROM AM TO AN	
				JUMPER FROM AY TO AT	
				JUMPER FROM AV TO AW	
				JUMPER FROM BA TO BB	
				JUMPER FROM BD TO BE	
				JUMPER FROM BK TO BM	
				JUMPER FROM U TO V	
				SECTOR O JUMPER I	
				SECTOR I JUMPER I	
				CHASSIS GND WI	
	NOTE: JUMPER POINTS NOT LISTED				
	ARE OPEN (NOT USED)				



REV BLOCK SMT 2

J6 SEPARATOR

1 SEP DATA
2 SEP CLOCK
3 PLO CLOCK
4 READ DATA
5 GND
6 -5V
7 +24V
8 KEY
9 READWRITE HEAD 0
10 SHIELD
11 KEY
12 READWRITE HEAD 0

J15 READWRITE HEAD 1
3 READWRITE HEAD 1
4 ERASE 1
5 SHIELD 1
2 KEY
1 READWRITE HEAD 1

READWRITE/ERASE ELECTRONICS

PERSICI, INC.

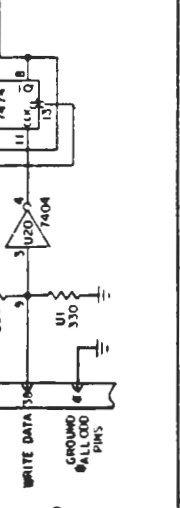
SCHEMATIC, PCB, DATA INTERFACE
MOD 27012/277 SHIT OF 4 200264 M

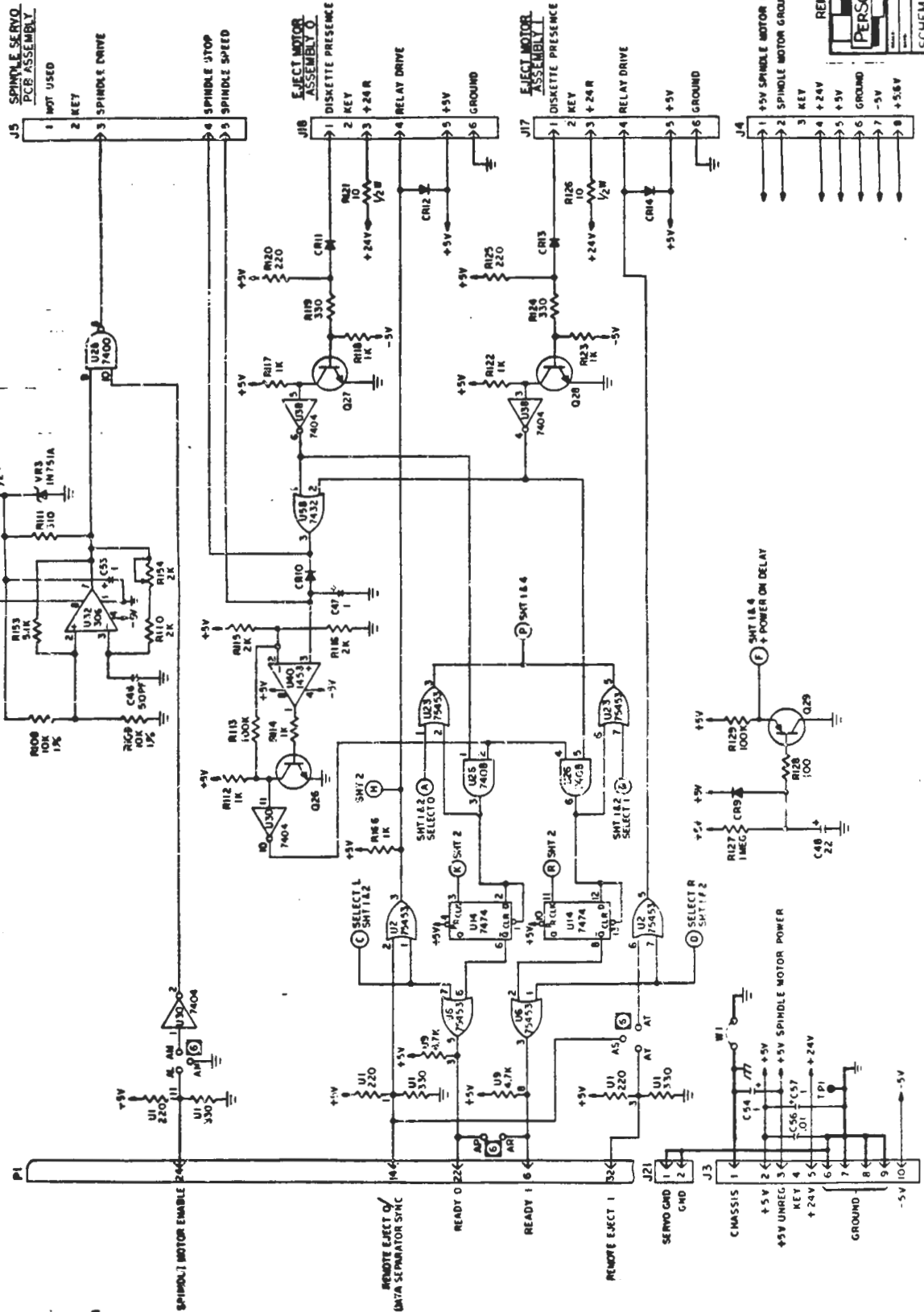
- 5 ALL PNP TRANSISTORS TO BE 2N4402
- 4 ALL NPN TRANSISTORS TO BE 2N4400
- 3 ALL DIODES TO BE IN3064
- 2 ALL CAPACITORS IN MICROFARADS
- 1 ALL RESISTORS IN OHMS UNLESS OTHERWISE SPECIFIED.

FOR VARIABLE COMP VALUES AND JUMPER LOCATIONS SEE TABULATED ML.

COMPONENT REF. DESIGNATIONS

LAST USED	DELETED
U61	U49
Q39	C31, C32
CGO	CR1, CR2
CR8	R4
W4	R5
W5	R6
W6	R7
W7	R8
W8	R9
W9	R10
W10	R11
W11	R12
W12	R13
W13	R14
W14	R15
W15	R16
W16	R17
W17	R18
W18	R19
W19	R20
W20	R21
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W89	R90
W90	R91
W91	R92
W92	R93
W93	R94
W94	R95
W95	R96
W96	R97
W97	R98
W98	R99
W99	R100





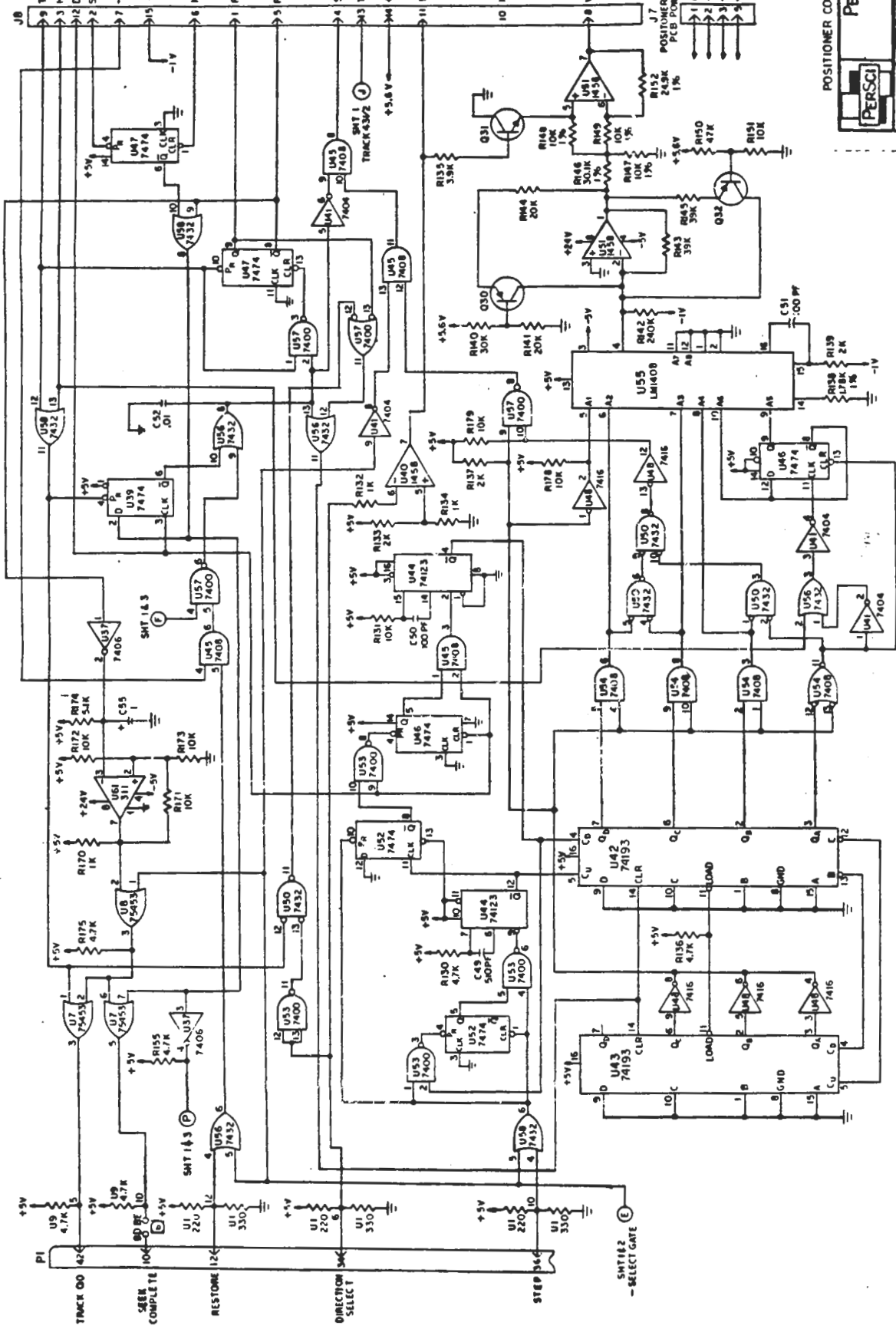
PERSCI, INC.

SCHEMATIC PCB, DATA & INTERFACE

MOD 270/272/277 SMT 3 OF 4 200268-1M

944 5272

POSITIONER SERVO PCB ASSEMBLY



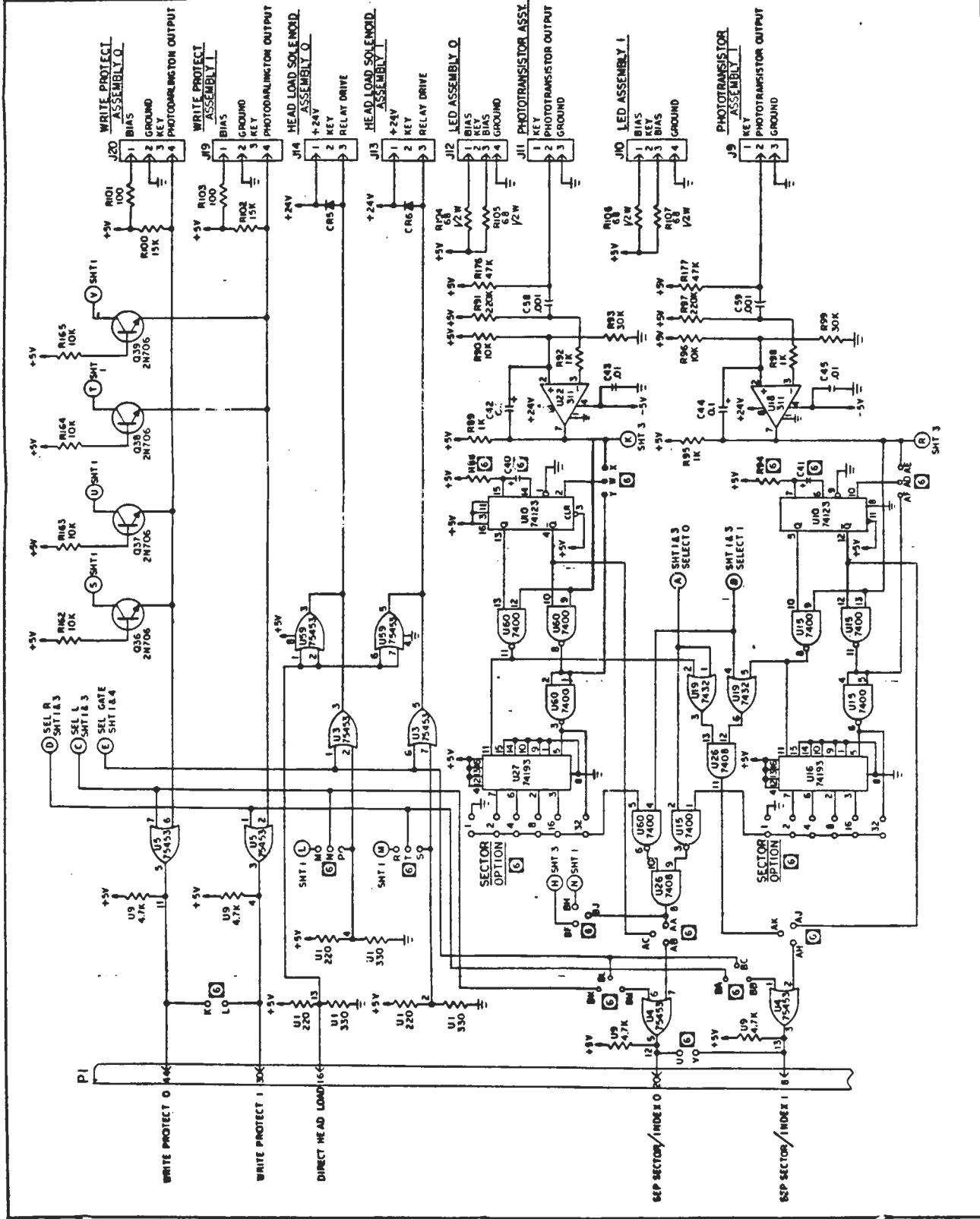
POSITIONER CONTROL CIRCUITS

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SCHEMATIC, PCB, DATA & INTERFACE

MOD 270/272/277 SMT 4 OF 4 200264 M

REV	DESCRIPTION	DATE	BY	CHKD
A	IMP REL	1/25/72	JL	JL
B	ECC #12	1/25/72	JL	JL
C	ECC #13	1/25/72	JL	JL
D	ECC #14	1/25/72	JL	JL
E	ECC #15	1/25/72	JL	JL
F	ECC #16	1/25/72	JL	JL
G	ECC #17	1/25/72	JL	JL
H	ECC #18	1/25/72	JL	JL
I	ECC #19	1/25/72	JL	JL
J	ECC #20	1/25/72	JL	JL
K	ECC #21	1/25/72	JL	JL
L	ECC #22	1/25/72	JL	JL
M	ECC #23	1/25/72	JL	JL



WRITE PROTECT, H.L.O.D. INDEX

PERSCI, INC.

PERSCI

SCHEMATIC, PCB, DATA & INTERFACE

MOD 270272/27

SMT 2 OF 4 200264M

PERSCI, INC.

**12210 Nebraska Ave
W Los Angeles
CA 90025**

October 1978

