Processor Technology

Dear Sol-PCB Customer:

The enclosed documentation on the Sol-PCB and PM-5204 printed circuit boards includes the following information:

1) five Sol schematic diagrams
2) complete revised parts list
3) assembly drawings for Sol & PM
4) S-100 Bus specification
5) memory allocation table
6) I/O port allocation
7) control and status bit definition
8) user switch option selection table

Many of the mechanical parts for the Sol Terminal Computer are hard to obtain, so we have made available the following items:

Item No.	Price	Includes
Sol-CONKIT	$59.00	J1 through J11 connectors, personality module card guides, card guide brackets and handle bracket.
Sol-PRELIM	14.00	Preliminary Sol manual describing assembly and checkout procedures, plus much additional information. Very helpful when bringing up Sol.
Sol-SS	40.00	IC socket kit

We have sent the source listing for the CONSOL^{tm} Personality module software to INTERFACE AGE magazine. This article is currently expected to be published in the December 1976 issue but publication schedules can vary. The CONSOL software allows the Sol to be used as a stand-alone computer system or as a terminal. The following commands are implemented:

BASIC (executes at zero)
ENTER (in hexidecimal)
EXEC (at hex address)
DUMP (in hexidecimal)
TERM (terminal mode)
TLOAD (load memory from cassette)

The Sol-PCB boards sold for $40 each are warranteed for thirty days against defects in materials and workmanship. The warranty is void if, in the opinion of PTC, the printed circuit board has been abused during assembly. Warranty is limited in any case to replacement of defective printed circuit boards.

Processor Technology can not provide direct support via telephone or letter to Sol-PCB purchasers. The documentation provided should be sufficient to easily build and debug a Sol unit. NOTE: please do not make parts substitutions!

If you are in any way dissatisfied with your unassembled Sol-PCB please feel free to return it to us postpaid for a full refund.

Have fun!

PROCESSOR TECHNOLOGY CORPORATION 6200 HOLLIS STREET EMERYVILLE CA 94608 (415) 652-8080
CABLE ADDRESS "PROCTEC"

Table 1. Sol-PC Parts List.

INTEGRATED CIRCUITS

- 1 AM0026 or DM0026 (U104)
- 1 4N26 (U39)
- 5 8T97 (U67,68,77,80,81)
- 2 1458CP or 1558CP (U56,108)
- 1 1489A (U38)
- 2 TMS6011NC (U51,69)
- 1 MCM6574 or MCM6575 (U25)
- 1 4001 (U102)
- 2 4013 (U100,113)
- 1 4019 (U111)
- 1 4023 (U98)
- 1 4024 (U86)
- 1 4027 (U101)
- 3 4029 (U1,11,84)
- 1 4030 (U99)
- 2 4046 (U85,110)
- 2 4049 (U88,109)
- 1 4520 (U112)
- 1 74H00 (U91)
- 3 74LS00 (U44,48,55)
- 2 74LS02 or 9LS02 (U53,60)
- 4 74LS04 (U24,45,49,54)
- 1 74S04 (U92)
- 3 7406 (U57,58,87)
- 2 74LS10 (U47,61)
- 3 74LS20 (U23,59,83)
- 1 74LS86 (U74)
- 8 74LS109 (U43,52,63,64,70,72,73,75)
- 1 74LS136 (U22)
- 3 74LS138 (U34,35,36)
- 3 74LS157 (U12,30,32)
- 4 74LS163 or 25LS163 (U28,31,33,40)
- 1 74166 (U41)
- 2 74173 (U95,96)
- 10 74LS175 or 25LS175 (U2,13,26,27,42,76,90,93,97,106)
- 4 74LS253 (U65,66,78,79)
- 7 74LS367 (U29,37,50,71,89,94,107)
- 1 8080, 8080A or 9080A (U105)
- 1 8836 or 8T380 (U46)
- 16 91L02APC or 2102L1PC (U3 - 10, U14 - 21)
- 1 93L16 (U62)

TRANSISTORS

- 2 2N2222 (Q4 & 5)
- 2 2N2907 (Q1 & 2)
- 1 2N4360 (Q3)

DIODES

- 9 1N4148 or 1N914 (D1,D3 - 10)
- 1 1N5231B Zener Diode (D11)
- 4 1N4001 (D2,12,13,14)

CRYSTAL

- 1 14.318 MHz in HC-18/U Case (XTAL)

RELAYS

- 2 DIP Reed, Sigma 191-TE1A15S (K1 & 2)

Table 1. Sol-PC Parts List (Continued).

RESISTORS

2	47	ohm, ¼ watt, 5%
1	75	ohm, ¼ watt, 5%
1	100	ohm, ¼ watt, 5%
3	100	ohm, ½ watt, 5%
1	200	ohm, ¼ watt, 5%
13	330	ohm, ¼ watt, 5%
1	330	ohm, ½ watt, 5%
3	470	ohm, ¼ watt, 5%
2	470	ohm, ½ watt, 5%
9	680	ohm, ¼ watt, 5%
64	1.5K	ohm, ¼ watt, 5%
1	3.3K	ohm, ¼ watt, 5%
6	5.6K	ohm, ¼ watt, 5%
32	10 K	ohm, ¼ watt, 5%
1	15 K	ohm, ¼ watt, 5%
2	39 K	ohm, ¼ watt, 5%
2	47 K	ohm, ¼ watt, 5%
3	50 K	ohm, Potentiometer
3	100 K	ohm, ¼ watt, 5%
2	150 K	ohm, ¼ watt, 5%
2	1 M	ohm, ½ watt, 5%
1	2.2M	ohm, ¼ watt, 5%
2	3.3M	ohm, ¼ watt, 5%

CAPACITORS

1	10	pfd, disc
1	330	pfd, disc
3	680	pfd, monolythic or disc ceramic
6	.001	ufd, disc
2	.001	ufd, Mylar tubular
2	.01	ufd, Mylar tubular
37	.047	ufd, disc
12	.1	ufd, disc
1	.1	ufd, Mylar tubular
1	.68	ufd, monolythic ceramic
1	1	ufd, tantalum, dipped
5	15	ufd, tantalum, dipped
1	100	ufd, aluminum electrolytic

CONNECTORS

1	25-pin Female, AMP206584-1 (J1)
1	25-pin Male, AMP206604-1 (J2)
2	20-pin Header, 3M3492-2002 (J3 & 4)
1	30-pin Right Angle Edge Connector, VIKING 3KH15/75KC15 (J5)
2	Miniature Phone Jack (J6 & 7)
2	Subminiature Phone Jack (J8 & 9)
1	7-pin Right Angle Molex (J10)
1	100-pin Edge Connector, TI H322150-02-6A (J11)
1	Molex-type DC Power Cable, J11 mating (prefabricated)

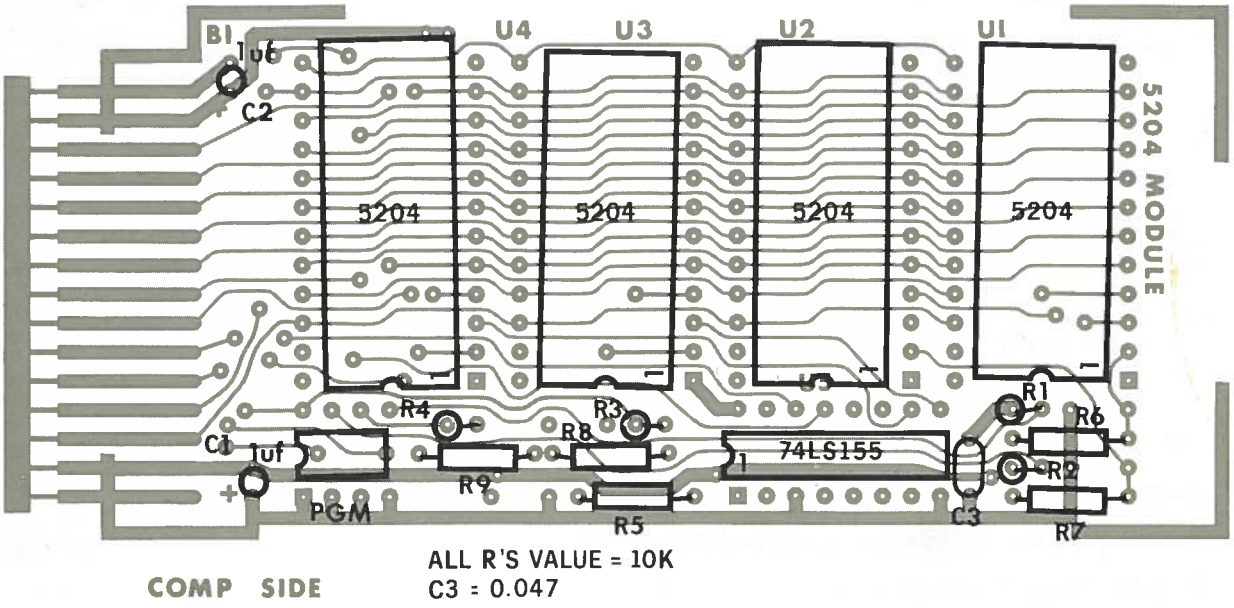
Table 1. Sol-PC Parts List (Continued).

MISCELLANEOUS

1 Sol-PCB Circuit Board	2 Card Guide, SAE1250F
2 8-pin DIP Socket	10 #4 Lockwasher, internal tooth
29 14-pin DIP Socket	2 #4 Insulating Washer, 0.05
74 16-pin DIP Socket	4 4-40 x 1/4 Binder Head Screw
1 24-pin DIP Socket	6 4-40 x 7/16 Binder Head Screw
3 40-pin DIP Socket	2 4-40 x 5/8 Binder Head Screw
2 DIP Switch, 6 position (S1&4)	10 4-40 Hex Nut
2 DIP Switch, 8 position (S2&3)	1 Length Solder
1 Length 72-ohm Coaxial Cable	1 Manual
1 Tie Wrap	1 Personality Module Kit (contents listed below)
2 Mounting Bracket, Sol-1040	

PERSONALITY MODULE KIT, PM5204

1 PM5204 PC Board	1 16-pin DIP Socket
2 5204 EPROM (U1,U2)	1 24-pin DIP Socket
1 74LS155 (U5)	1 Bracket, Sol-1045
9 10K ohm, 1/4 watt, 5% Film Resistor	2 2-56 Binder Head Screw
1 .047 ufd Capacitor, Disc Ceramic	
2 1 ufd Capacitor, Tantalum Dipped	



J3 Keyboard Connector (between U64 and U65)

Sol-PC, Rev. 2,E
10/18/76

pin no.	Signal name	pin no.	Signal name
1	ground	11	ground
2	+5v	12	+5v
3	$\overline{\text{Kbd Data Ready}}$	13	$\overline{\text{Restart}}$
4	$\overline{\text{Break}}$	14	$\overline{\text{Local}}$
5	Kbd Data Ø A	15	KBd Data 4 E
6	Kbd Data 1 B	16	KBd Data 5 F
7	Kbd Data 2 C	17	KBD Data 6 G
8	Kbd Data 3 D	18	KBD Data 7 H
9	+5v	19	+5v
10	ground	20	ground

J4 Display Expansion Connector (between U28, 29)

pin no.	Signal name	pin no.	Signal name
1	ground	11	ground
2	N.C.	12	N.C.
3	Char. addr. 4	13	Dot Clock, 14.318MHz
4	Character clock	14	Composite sync. out
5	Char. addr. Ø A	15	TTL Serial Data Out
6	Char. addr. 1	16	Composite blanking out
7	Char. addr. 2	17	Scan advance out
8	Char. addr. 3	18	Char. addr. 5
9	N.C.	19	N.C.
10	ground	20	ground

J5 Personality Module Edge Connector

pin no.	Signal name	pin no.	Signal name
A1	Ground	B1	Ground
A2	+5VDC	B2	+5VDC
A3	Addr. 9	B3	Addr. Ø
A4	Addr. 8	B4	Addr. 4
A5	Addr. 7	B5	Addr. 3
A6	INT Bus Ø	B6	Addr. 2
A7	INT Bus 1	B7	Addr. 1
A8	INT Bus 2	B8	Addr. 5
A9	INT Bus 3	B9	Addr. 6
A10	INT Bus 4	B10	C4
A11	INT Bus 5	B11	CØ
A12	Program Ø	B12	INT Bus 6
A13	Program 1	B13	INT Bus 7
A14	Program 2	B14	-12VDC
A15	Program 3	B15	+12VDC

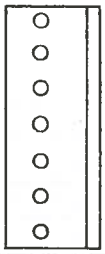
J6 Audio Out for CUTS Cassette Interface: Mini-phone jack at rear panel

J7 Audio In for CUTS Cassette Interface: Mini-phone jack at rear panel

J8 Tape Motor Control 1: (See output port FA, bit 7) Sub-mini jack at rear panel

J9 Tape Motor Control 2: (See output port FA, bit 6) Sub-mini jack at rear panel

J10 DC Power Connector, Sol-PC



S-100 Bus Definitions

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	+8V	+8 Volts	Unregulated voltage on bus, supplied to PC boards and regulated to 5V supplied by Sol-20 supply
2	-16V	-16 Volts	Positive unregulated voltage supplied by Sol-20 power supply
3	XRDY	EXTERNAL READY	External ready input to CPU ready circuitry
4	VI0	Vectored Interrupt Line #0	
5	VI1	Vectored Interrupt Line #1	
6	VI2	Vectored Interrupt Line #2	
7	VI3	Vectored Interrupt Line #3	
8	VI4	Vectored Interrupt Line #4	
9	VI5	Vectored Interrupt Line #5	
10	VI6	Vectored Interrupt Line #6	
11	VI7	Vectored Interrupt Line #7	
12	XRDY2	EXTERNAL READY #2	not used by Sol-PC
13 to 17	TO BE DEFINED		
18	$\overline{\text{STAT DSB}}$	STATUS DISABLE	-Allows the buffers for the 8 status lines to be tri-stated
19	$\overline{\text{C/C DSB}}$	COMMAND/CONTROL DISABLE	-Allows the buffers for the 6 output command/control lines to be tri-stated
20	UNPROT	UNPROTECT	-not used by Sol-PC electronics
21	$\overline{\text{SS}}$	SINGLE STEP	-not used by Sol-PC
22	$\overline{\text{ADD DSB}}$	ADDRESS DISABLE	-Allows the buffers for the 16 address lines to be tri-stated
23	$\overline{\text{DO DSB}}$	DATA OUT DISABLE	-Allows the buffers for the 8 data output lines to be tri-stated
24	Ø2	PHASE 2 CLOCK	
25	Ø1	PHASE 1 CLOCK	
26	PHLDA	HOLD ACKNOWLEDGE	Processor command/control output signal that appears in response to the HOLD signal; indicates that the data and address bus will go to the high impedance state and processor will enter HOLD state after completion of the current machine cycle.

PIN NUMBER	SYMBOL	NAME	FUNCTION
27	PWAIT	WAIT	-Processor command/control signal that appears in response to the HOLD signal; indicates that the data and address bus will go to the high impedance state and processor will enter HOLD state after completion of the current machine cycle
28	PINTE	INTERRUPT ENABLE	-Processor command/control output signal; indicates interrupts are enabled, as determined by the contents of the CPU internal interrupt flip-flop. When the flip-flop is set (Enable Interrupt instruction), interrupts are accepted by the CPU; when it is reset (Disable Interrupt instruction), interrupts are inhibited.
29	A5	Address Line #5	
30	A4	Address Line #4	
31	A3	Address Line #3	
32	A15	Address Line #15 (MSB)	
33	A12	Address Line #12	
34	A9	Address Line #9	
35	DI01	Data In/Out line #1	same as pin 94
36	DIOØ	Data In/Out line #0	same as pin 95
37	A10	Address Line #10	
38	DIO4	Data In/Out Line #4	same as pin 91
39	DIO5	Data In/Out Line #5	same as pin 92
40	DIO6	Data In/Out Line #6	same as pin 93
41	DIO2	Data In/Out Line #2	same as pin 88
42	DIO3	Data In/Out Line #3	same as pin 89
43	DIØ7	Data In/Out Line #7	same as pin 90
44	SM1	MACHINE CYCLE 1	-Status output signal that indicates that the processor is in the fetch cycle for the first byte of an instruction
45	SOUT	OUTPUT	-Status output signal that indicates the address bus contains the address of an output device and the data bus will contain the ouput data when PWR is active
46	SINP	INPUT	-Status output signal that indicates the address bus contains the address of an input device and the input data should be placed on the data bus when PDBIN is active
47	SMEMR	MEMORY READ	-Status output signal that indicates the data bus will be used to read memory data
48	SHLTA	HALT ACKNOWLEDGE	- Status output signal that acknowledges a HALT instruction
49	$\overline{\text{CLOCK}}$	$\overline{\text{CLOCK}}$	- Inverted output of the Ø2 CLOCK
50	GND	GROUND	
51	+8V	+8 Volts	Unregulated input to 5 volt regulators supplied by Sol-20 power supply
52	-16V	-16 Volts	Negative unregulated voltage supplied by Sol-20 power supply

Pinouts: Parallel Data Interface (PDI) as used on Processor Tech. Sol System

Sept. 30, 1976

MASTER UNIT-Male connector

J2 Pin #	Signal mnemonic	Signal name	J2 pin#	Signal mnemonic	Signal name
1	CG	Chassis Ground	14	US	Unit Select
2	SG	Signal Ground	15	OE	Output Enable
3	IE	Input Enable	16	$\overline{XDR}$	eXternal Device Ready
4	$\overline{DR}$	Data Ready	17	$\overline{OL}$	Output Load
5	$\overline{IAK}$	Input Acknowledge	18	OD7	Output Data,bit 7
6	ID7	Input Data, bit 7	19	OD6	Output Data, bit 6
7	ID6	Input Data, bit 6	20	OD5	Output Data, bit 5
8	ID5	Input Data, bit 5	21	OD4	Output Data, bit 4
9	ID4	Input Data, bit 4	22	OD3	Output Data, bit 3
10	ID3	Input Data, bit 3	23	OD2	Output Data, bit 2
11	ID2	Input Data, bit 2	24	OD1	Output Data, bit 1
12	ID1	Input Data, bit 1	25	OD0	Output Data, bit 0
13	ID0	Input Data, bit 0			

Pinouts: Serial Data Interface (SCI) as used on Processor Tech. Sol System

Female connector-DB25S

J1 pin#	Signal mnemonic	Signal name	J1 pin#	Signal mnemonic	Signal name
1	CG	Chassis Ground	8	CD	Carrier Detect
2	TD	Transmit Data	11	CLO	Current Loop Output
3	RD	Receive Data	12	LR1	Loop Receiver 1
4	RTS	Request To Send	13	LR2	Loop Receiver 2
5	CTS	Clear To Send	20	DTR	Data Terminal Ready
6	DSR	Data Set Ready	23	LCS	Loop Current Source
7	SG	Signal Ground			

Note 1: Many pins not specified here are used in EIA RS-232C specification. USE THEM WITH CAUTION.

Note 2: Terminals output on pins 2,4 & 20 and input on pins 3,5 & 6 for EIA type hookups. Modems and computer mainframes output on pins 3,5 & 6 and input on pins 2,4 & 20.

Note 3: Current loop hookups are the same for terminals, modems,mainframes.

STATUS PORT INPUT BIT ASSIGNMENTS

PORT F8 (STATUS, SERIAL COMM. CHANNEL)

BIT	SIGNAL NAME	FUNCTION	ACTIVE DIRECTION
Ø	SCD	Serial Carrier Detect (EIA)	1 carrier
1	SDSR	Serial Data Set Ready (EIA)	Ø link ok
2	SPE	Serial Parity Error	1 error
3	SFE	Serial Framing Error	1 error
4	SOE	Serial Overrun Error	1 error
5	SCTS	Serial Clear to Send (EIA)	Ø clear
6	SDR	UART Serial Data Ready	1 ready
7	STBE	UART Serial Transmit Buffer Empty	1 empty

PORT FA (AUX. STATUS, CASSETTE TAPE INTERFACE, PARALLEL I/O, KEYBOARD INPUT)

BIT	SIGNAL NAME	FUNCTION	ACTIVE DIRECTION
Ø	KDR	Keyboard Data Ready	Ø ready
1	PDR	Parallel Data Ready	Ø ready
2	PXDR	Parallel eXternal Device Ready	Ø ready
3	TFE	Tape Framing Error	1 error
4	TOE	Tape Overrun Error	1 error
5	not used		
6	TDR	Tape Data Ready	1 ready
7	TTBE	Tape Transmitter Buffer Empty	1 empty

PORT FE (DISPLAY STATUS)

BIT	SIGNAL NAME	FUNCTION	ACTIVE DIRECTION
Ø	SOK	Scroll OK; ¼ sec timeout after scroll	Ø time complete

CONTROL PORT OUTPUT BIT ASSIGNMENTS

PORT F8 (CONTROL, SERIAL COMM. CHANNEL)

BIT	SIGNAL NAME	FUNCTION	ACTIVE DIRECTION
4	SRTS	Serial Request to Send	1 request

PORT FA (CONTROL, PARALLEL I/O, CUTS CASSETTE I/O)

BIT	SIGNAL NAME	FUNCTION	ACTIVE DIRECTION
3	PIE	Parallel Input Enable	1 pin 3 J2 low
4	PUS	Parallel Unit Select	0 pin 14 J2 low
5	TBR	Tape Baud Rate (300/1200)	0 1200 Baud
6	TT2	Tape Transport 2	0 run tape
7	TT1	Tape Transport 1	0 run tape

PORT FE (SCROLL CONTROL, DISPLAY SECTION)

BIT	SIGNAL NAME	FUNCTION	ACTIVE DIRECTION
Ø - 3	BDLA	Beginning Display Line Absolute address	4-bit data nybble
4 - 7	FDSP	First Displayed Line Screen Position	4-bit data nybble

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CONNECTOR DESIGNATION

J1	Serial data	J6	Cassette Tape Audio Out
J2	Parallel Data	J7	Cassette Tape Audio In
J3	Keyboard	J8	Tape Motor 1
J4	Display Expansion	J9	Tape Motor 2
J5	ROM Personality Module	J10	PC Power
		J11	S-100 Bus Expansion

PIN NUMBER	SYMBOL	NAME	FUNCTION
53	SSWI	SENSE SWITCH INPUT	not used by Sol
54	EXT CLR	EXTERNAL CLEAR	not used by Sol-PC electronics
55	RTC	REAL TIME CLOCK	not used by Sol-PC electronics
56	STSTB	STATUS STROBE	not used by Sol
57	DIGI	DATA INPUT GATE #1	When low forces PDBINS low and forces CPU input multiplexers to the DIO bus. During CPU DBIN cycle, disables CPU DIO bus drivers
58	FRDY	FRONT PANEL READY	-When low disables MWRITE driver
59 to 64	TO BE DEFINED		
65	MREQ	MEMORY REQUEST	- Z 80 signal not used by Sol-PC electronics
66	REF	REFRESH	- Z 80 signal not used by Sol-PC electronics
67	PHANTOM	PHANTOM DISABLE	-Output from CPU section used to disable RAM or ROM during power on initialization program execution
68	MWRITE	MEMORY WRITE	-Indicates that the data present on the Data Out Bus is to be written into the memory location currently on the address bus
69	PS	PROJECT STATUS	-not used by Sol-PC electronics
70	PROT	PROTECT	-not used by Sol-PC electronics
71	RUN	RUN	- not used by Sol-PC electronics
72	PRDY	PROCESSOR READY	- Memory and I/O input to the CPU Board wait circuitry
73	PINT	INTERRUPT REQUEST	- The processor recognizes an interrupt request on this line at the end of the current instruction or while halted. If the processor is in the HOLD state or the Interrupt Enable flip-flop is reset, it will not honor the request.
74	PHOLD	HOLD	-Processor command/control input signal that requests the processor enter the HOLD state; allows an external device to gain control of address and data buses as soon as the processor has completed its use of these buses for the current machine cycle
75	PRESET	RESET	-Processor command/control input; while activated, the content of the program counter is cleared and the instruction register is set to 0
76	PSYNC	SYNC	-Processor command/control output; provides a signal to indicate the beginning of each machine cycle
77	PWR	WRITE	-Processor command/control output; used for memory write or I/O output control. Data on the data bus is stable while the PWR is active
78	PDBIN	DATA BUS IN	-Processor command/control output; indicates to external circuits that the data bus is in the input mode

PIN NUMBER	SYMBOL	NAME	FUNCTION
79	A0	Address Line #0	(LSB)
80	A1	Address Line #1	
81	A2	Address Line #2	
82	A6	Address Line #6	
83	A7	Address Line #7	
84	A8	Address Line #8	
85	A13	Address Line #13	
86	A14	Address Line #14	
87	A11	Address Line #11	
88	DI02	Data In/Out Line #2	same as pin 41
89	DI03	Data In/Out Line #3	same as pin 42
90	DI07	Data In/Out Line #7	same as pin 43
91	DI04	Data In/Out Line #4	same as pin 38
92	DI05	Data In/Out Line #5	same as pin 39
93	DI06	Data In/Out Line #6	same as pin 40
94	DI01	Data In/Out Line #1	same as pin 35
95	DIOØ	Data In/Out Line #0	same as pin 36
96	SINTA	INTERRUPT ACKNOWLEDGE	-Status output signal; acknowledges signal for INTERRUPT request
97	$\overline{SWO}$	WRITE OUT	-Status output signal; indicates that the operation in the current machine cycle will be a WRITE memory or output function
98	SSTACK	STACK	-Status output signal indicates that the address bus holds the pushdown stack address from the Stack Pointer
99	$\overline{POC}$	POWER-ON CLEAR	
100	GND	GROUND	

SWITCH FUNCTION DEFINITION -- Display Ctrl---Schematic Drawing #4

Switch No.	Mnemonic	Function ON	OFF
S1-1	RST	Restart to Zero	RUN (Dwg. #1)
S1-2	not used		
S1-3	BLANK	Blank Ctrl Characters	Display Ctrl Char.
S1-4	Polarity		
S1-5	BLINK	Blinking cursor	*Solid or NO cursor
S1-6	SOLID	Solid cursor	*Blinking or NO cursor

*NO cursor if S1-5 and S1-6 are off at same time.
Both switches should not be on at the same time.

Drawing #3 -- Sense Switch

Switch No.	Mnemonic	Function ON	OFF	
S2-1	SSWØ	LSB, data bit	Ø=LO	HI
S2-2thruS2-7		etc.	LO	HI
S2-8	SSW7	MSB data bit 7	LO	HI

SERIAL I/O BAUD RATE SWITCH -- Schematic Drawing #3

Switch No.	Mnemonic	Function ON	OFF
S3-1	75	75 BAUD	* Do not turn more than one switch on at a time
S3-2	11	110 BAUD	
S3-3	15	150 BAUD	
S3-4	30	300 BAUD	
S3-5	60	600 BAUD	
S3-6	12	1200 BAUD	
S3-7	24/48	2400 or 4800(normally 2400 if not jumpered K to M)	
S3-8	96	9600 BAUD	

SERIAL I/O CONTROL -- Schematic Drawing #3

Switch No.	Mnemonic	ON	OFF
S4-1	PS	Parity even	Parity odd (if S4-5 on)
S4-2	WLS 1	Data word length	8bits 7bits 6bits 5bits
S4-3	WLS 2		ON ON OFF OFF
			ON OFF ON OFF
S4-4	SBS	1 stop bit	2 stop bits (1.5 if 5bits/word)
S4-5	PI	Parity	No parity
S4-6	F/$\overline{H}$	Half duplex	Full duplex

MEMORY ALLOCATION: ON CARD

Hexidecimal Address	Function
CØØØ - C7FF	Personality Module ROM or PROM (2048 words)
C8ØØ - CBFF	System RAM (1024 words)
CCØØ - CFFF	Display RAM Memory (1024 characters)

ON CARD INPUT PORT ALLOCATION

Hexidecimal Port Address	Function
F8	Status, Serial Comm. channel
F9	Serial Communication Channel Data
FA	Aux. Status, Cassette tape interface, parallel I/O, keyboard input
FB	Audio Cassette (CUTS) Data
FC	Keyboard Data (from J3)
FD	Parallel Port Data (from J2)
FE	Display Status
FF	Sense Switch (S2-1 thru S2-8)

OUTPUT PORTS

Hex Port Address	Function
F8	Control, Serial Comm. Channel
F9	Data, Serial Comm. Channel
FA	Control, Parallel I/O, CUTS Cassette I/O
FB	Data, CUTS audio cassette Interface
FC	Alarm (optional)
FD	Data, Parallel output Data channel
FE	Scroll control, Display Section
FF	not used in Sol-PC

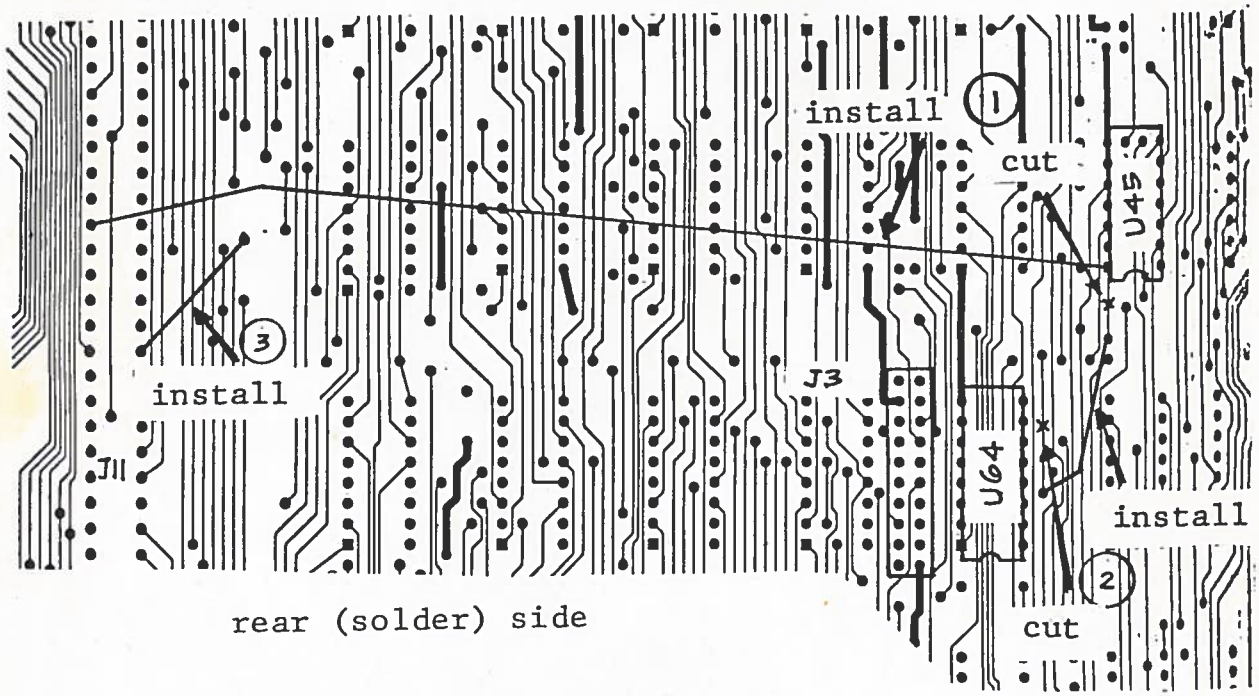
SOL - PC MODIFICATION REVISION LEVEL D

Due to layout errors connections to pins 28, 73 and 74 have been interchanged. These signals are used by DMA and interrupt devices. Correction requires three cuts and installation of three jumpers. Use 24 gauge wire supplied with the kit for these changes.

1. Cut trace on rear side of board connecting pin 1 of U45 with feedthrough directly below. Install jumper wire on rear side of board connecting pin 1 of U45 with pin 73 of J11.

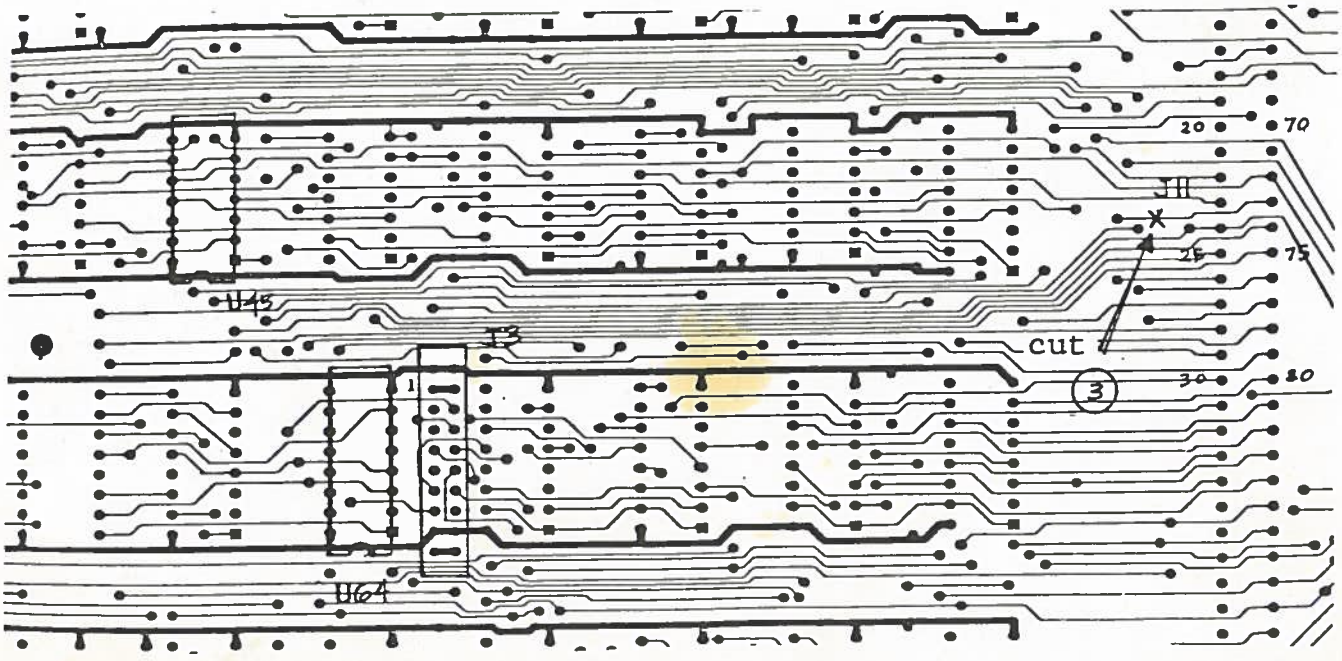
2. Cut trace connecting the feedthrough adjacent to pins 13 and 14 of U64 with the feedthrough directly above (on rear side of board). Install jumper wire as shown on the rear side of the board.

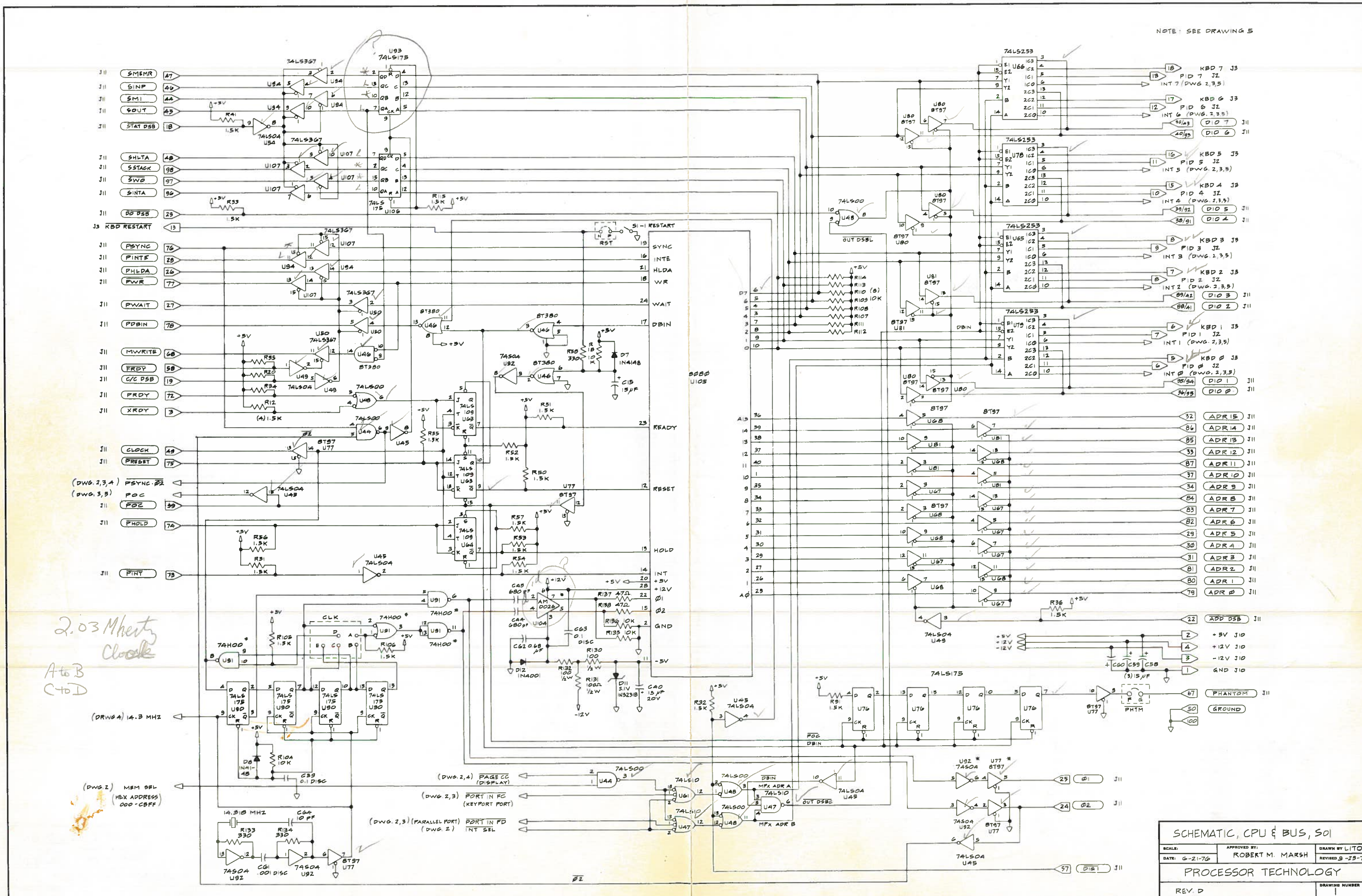
3. Cut trace on front side of the board connecting the feedthrough immediately below and to the left of the "J11" designation with pin 73 of J11. Install a jumper wire from this feedthrough to pin 28 of J11 on the rear side of the board.



rear (solder) side

front (component) side





NOTE: SEE DRAWING 5
SCHEMATIC, CPU & BUS, SOI
SCALE:
DATE: 6-21-76
APPROVED BY: ROBERT M. MARSH
DRAWN BY LITO
REVISED 9-23-76
PROCESSOR TECHNOLOGY
REV. D
DRAWING NUMBER 1
8080 U105
SYNC
INTE
HLDA
WR
WAIT
DBIN
READY
RESET
HOLD
INT
+5V
+12V
GND
-5V
S1-1 RESTART
RST
CLK
14.318 MHZ
(DWG 4) 14.3 MHZ
(DWG. 2) MEM SEL (HEX ADDRESS) 000-CBFF
(DWG. 2,4) PAGE CC (DISPLAY)
(DWG. 2,3) PORT IN FC (KEYPORT PORT)
(DWG. 2,3) (PARALLEL PORT) PORT IN FD
(DWG. 2) INT SEL
(DWG. 2,3,4) PSYNC·Ø2
(DWG. 3,5) POC
SMEMR
SINP
SMI
SOUT
STAT DSB
SHLTA
SSTACK
SWO
SINTA
DO DSB
J3 KBD RESTART
PSYNC
PINTE
PHLDA
PWR
PWAIT
PDBIN
MWRITE
FRDY
C/C DSB
PRDY
XRDY
CLOCK
PRESET
POC
PHOLD
PINT
ADD DSB
+5V J10
+12V J10
-12V J10
GND J10
PHANTOM
GROUND
PHTM
Ø1
Ø2
DIGI
OUT DSBL
MFX ADR A
MFX ADR B
2.03 Mhertz Clock
A to B
C to D

NOTE: SEE DRAWING 5

(DWG. 1,3,4) $\overline{PSYNC} \cdot \overline{\emptyset 2}$

J11 Ø2 24
J11 PHANTOM 67
J11 ADR 15 32
J11 ADR 14 86
J11 ADR 13 85
J11 ADR 12 33
J11 SINP 40
J11 ADR 11 87
J11 PWR 77
J11 SOUT 45
J11 FDBIN 78
J11 ADR 10 37
J11 ADR 9 34
J11 ADR 8 84
J11 MWRITE 68
J11 ADR 7 83
J11 ADR 6 82
J11 ADR 5 29
J11 ADR 4 30
J11 ADR 3 31
J11 ADR 2 81
J11 ADR 1 80
J11 ADR Ø 79

74LS04 U24
74LS136 U22
R13 1.5K +5V
R14 1.5K +5V
R15 1.5K +5V
74LS136 U22
74LS20 U23
74LS04 U2A
74LS04 U24

74LS138 U34 MEM. DECODER
74LS138 U35 OUT PORT DECODER
74LS138 U36 IN PORT DECODER

74LS109 U70
U71 74LS367
RGO 1.5K +5V
74LS02 U53
74LS04 U54
74LS02 U53
74LS20 U23

72 PRDY J11

PAGE CC DISPLAY SECT. MEMORY (DWG. 4)
MEM SEL (DWG. 1) (000 - C8FF)

PORT OUT FE DISPLAY SECTION (DWG. 4)
PORT OUT FD PARALLEL (DWG. 3)
PORT OUT FB TAPE (DWG. 5)
PORT OUT FA AUX CTRL (DWG. 3,5)
PORT OUT F9 UART (DWG. 3)
PORT OUT F8 CTRL (DWG. 3)

U83 74LS20
INT SEL (DWG. 1)

PORT IN FF SENSE SWITCH
PORT IN FE DISPLAY SECTION (DWG. 4)
PORT IN FD PARALLEL (DWG. 1)
PORT IN FC KEYBOARD (DWG. 1)
PORT IN FB TAPE (DWG. 5)
PORT IN FA AUX STATUS (DWG. 5)
PORT IN F9 UART (DWG. 3)
PORT IN F8 STATUS (DWG. 3)

J5 PERSONALITY MODULE CONNECTOR
A1 +12V
A2 -12V
A,B14 +5V
A,B15 J5

INT 0 (DWG. 1,3,5)
INT 1
INT 2
INT 3
INT 4
INT 5
INT 6
INT 7 (DWG. 1,3,5)

J11 DIO Ø 36/95
J11 DIO 1 35/94
J11 DIO 2 41/88
J11 DIO 3 42/89
J11 DIO 4 38/91
J11 DIO 5 39/92
J11 DIO 6 40/93
J11 DIO 7 43/90

91L02A U3 RAM
91L02A U4 RAM
91L02A U5 RAM
91L02A U6 RAM
91L02A U7 RAM
91L02A U8 RAM
91L02A U9 RAM
91L02A U10 RAM

SCHEMATIC, MEMORY & DECODER, SOL

SCALE:	APPROVED BY: ROBERT M. MARSH	DRAWN BY LITO	
DATE: 6/15/76		REVISED 9-23-76	

PROCESSOR TECHNOLOGY

REV. D

DRAWING NUMBER 2

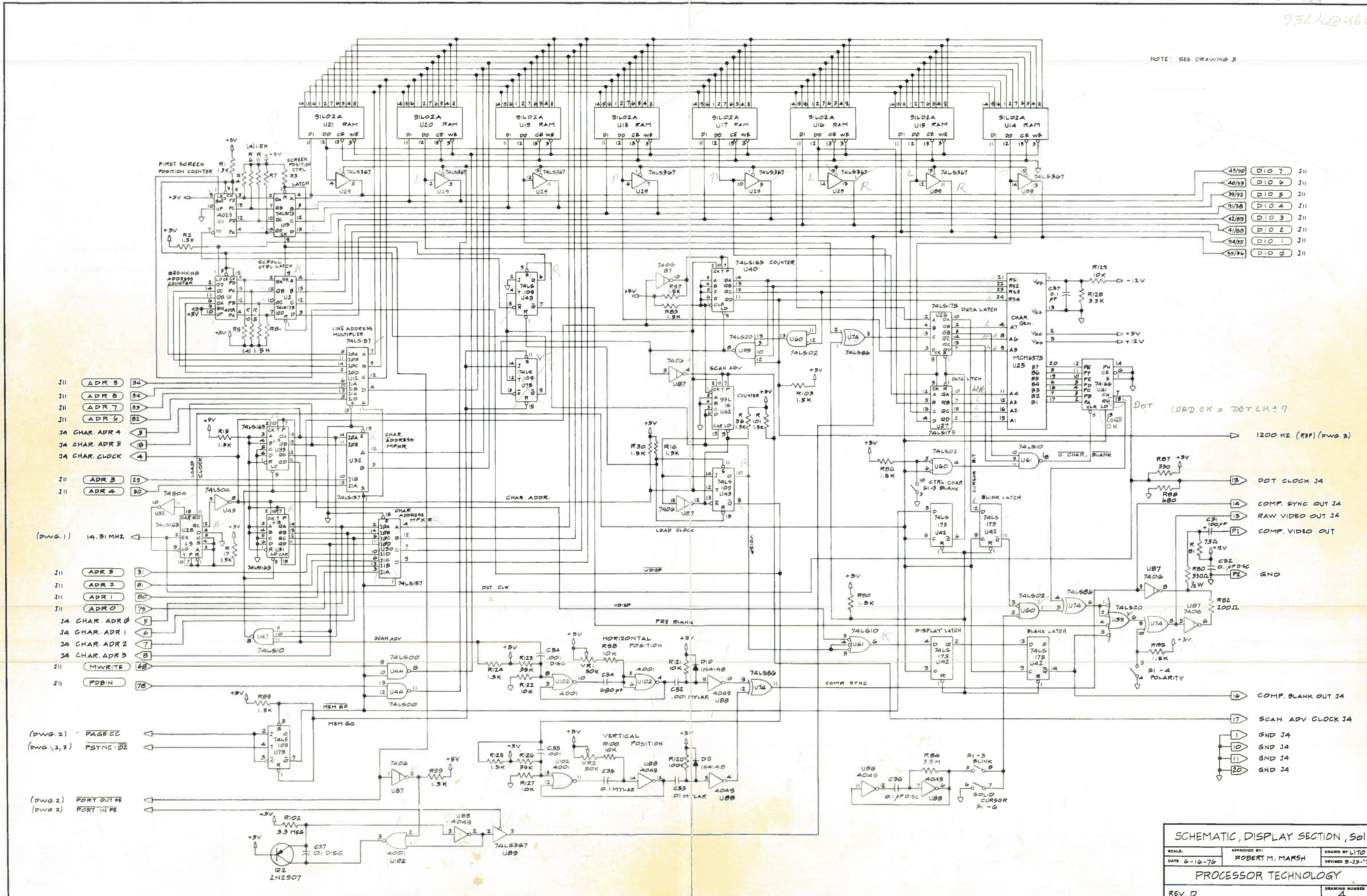
J1 (CLEAR TO SEND-EIA) SCTS
J1 (CARRIER DETECT-EIA) SCD
J1 (DATA SET READY-EIA) SDSR
(DWG.2) PORT OUT FB
(DWG 2) PORT OUT FA
(DWG 2) PORT IN FB
(DWG.2) PORT IN FB
(DWG.1,5) POC
J1 (SERIAL LOOP CURRENT SOURCE) SLCS
J1 (RECEIVED DATA - EIA) SRD
J1 (SERIAL LOOP RECEIVE 1) SLR1
J1 (SERIAL LOOP RECEIVE 2) SLR2
J3 (KEYBOARD BREAK) BRK
POC
(DWG.2) PORT OUT FB
J11 DIO 7
J11 DIO 6
J11 DIO 5
J11 DIO 4
(DWG.2) PORT OUT FD
J11 DIO 3
J11 DIO 2
J11 DIO 1
J11 DIO 0
(DWG.2) PORT IN FF
J2 (PARALLEL DATA RDY) PDR
J2 (PARALLEL EXT. DEV. RDY) PXDR
(DWG. 5) 2400 HZ
(DWG 5) 4800 HZ
(DWG 5) 1200 HZ (A)
(DWG 5) 38400 HZ
(DWG 5) 19200 HZ
(DWG 4) PLL 1200 HZ (REF)
(DWG.2) PORT IN FD
J11 Ø2
(DWG.2) PORT IN FC
J3 KEYBOARD DATA READY
(DWG.2) PORT IN FA
(DWG.1,2,4) PSYNC · Ø2

TAPE CTR. LATCH (PORT FA)
PARITY INHIBIT
STOP BIT SELECT
WORD LENGHT 2
WORD LENGHT 1
PARITY SELECT
HALF DUPLEX/LOCAL DATA
FULL/HALF DUPLEX S4-6
BAUD RATE SW
KEYBOARD STATUS
PARALLEL INPUT PORT STATUS
PARALLEL OUTPUT PORT STROBE

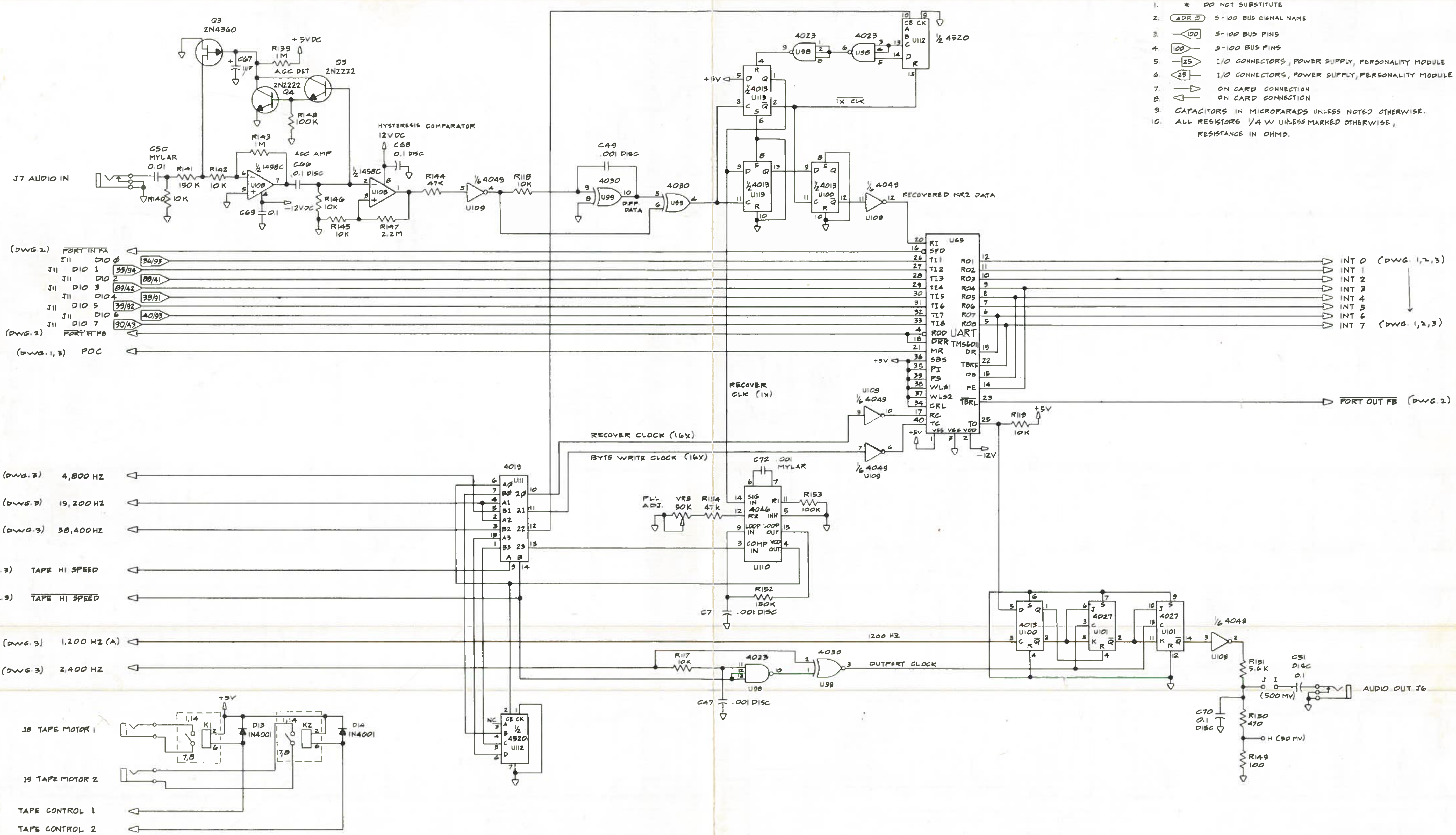
3 PIE (PARALLEL INPUT ENABLE) J2
TAPE HI SPEED (DWG 3)
TAPE CONTROL 1 (DWG 5)
TAPE CONTROL 2 (DWG 3)
TAPE HI SPEED (DWG 3)
14 PUS (PARALLEL UNIT SELECT) J2
11 SCLO (SERIAL CURRENT LOOP OUT) J1
INT 7 (DWG. 1,2,5)
INT 6 (DWG. 1,2,5)
INT 5 (DWG. 1,2,5)
INT 4 (DWG. 1,2,5)
INT 3 (DWG. 1,2,5)
INT 2 (DWG. 1,2,5)
INT 1 (DWG. 1,2,5)
INT Ø (DWG. 1,2,5)
14 KBD LOC J8
2 STD (TRANSMITTED DATA-EIA) J1
20 SDTR (DATA TERMINAL READY-EIA) J1
4 SRTS (REQUEST TO SEND-EIA) J1
1 GND J1
7 GND J1
18 POD 7 J2
19 POD 6 J2
20 POD 5 J2
21 POD 4 J2
1 GND J2
2 GND J2
15 POB (PARALLEL OUTPUT END) J2
22 POD 3 J2
23 POD 2 J2
24 POD 1 J2
25 POD Ø J2
5 PIAK (PARALLEL INPUT ACK) J2
17 POL (PARALLEL OUTPUT LOAD) J2

NOTE: SEE DRAWING 5

SCHEMATIC, INPUT/OUTPUT, SOI		
SCALE:	APPROVED BY: ROBERT M. MARSH	DRAWN BY LITO
DATE: 6-18-76		REVISED 9-23-'76
PROCESSOR TECHNOLOGY		
REV D		DRAWING NUMBER 3



NOTE: SEE DRAWING 5
91L02A U21 RAM
91L02A U20 RAM
91L02A U19 RAM
91L02A U18 RAM
91L02A U17 RAM
91L02A U16 RAM
91L02A U15 RAM
91L02A U14 RAM
74LS367
FIRST SCREEN POSITION COUNTER
SCREEN POSITION CTRL LATCH
BEGINNING ADDRESS COUNTER
SCROLL CTRL LATCH
LINE ADDRESS MULTIPLIER 74LS157
CHAR. ADDRESS MPXR
74LS163 COUNTER U40
SCAN ADV
74LS175 DATA LATCH
CHAR. GEN. MCM6575 U25
DOT CLOCK J4
COMP. SYNC OUT J4
RAW VIDEO OUT J4
COMP. VIDEO OUT
GND
1200 HZ (RBF) (DWG. 3)
LOAD CK = DOT CK ÷ 9
C CHAR. BLANK
CTRL CHAR S1-3 BLANK
BLINK LATCH
DISPLAY LATCH
BLANK LATCH
S1-4 POLARITY
COMP. BLANK OUT J4
SCAN ADV CLOCK J4
GND J4
HORIZONTAL POSITION
VERTICAL POSITION
COMP. SYNC
S1-5 BLINK
SOLID CURSOR S1-6
CHAR. ADDR.
LOAD CLOCK
DOT CLK
HDISP
VDISP
PRE BLANK
MEM GO
(DWG. 1) 14.31 MHZ
(DWG. 2) PAGE CC
(DWG. 1,2,3) PSYNC · Ø2
(DWG. 2) PORT OUT FE
(DWG. 2) PORT IN FE
ADR 9
ADR 8
ADR 7
ADR 6
J4 CHAR. ADR 4
J4 CHAR. ADR 5
J4 CHAR. CLOCK
ADR 5
ADR 4
ADR 3
ADR 2
ADR 1
ADR 0
J4 CHAR. ADR Ø
J4 CHAR. ADR 1
J4 CHAR. ADR 2
J4 CHAR. ADR 3
MWRITE
PDBIN
DIO 7
DIO 6
DIO 5
DIO 4
DIO 3
DIO 2
DIO 1
DIO Ø
Q2 2N2907
SCHEMATIC, DISPLAY SECTION, SOL
DATE: 6-16-76
APPROVED BY: ROBERT M. MARSH
DRAWN BY LITO
REVISED 9-23-76
PROCESSOR TECHNOLOGY
REV. D
DRAWING NUMBER 4


J7 AUDIO IN
C50 MYLAR 0.01
Q3 2N4360
+5VDC
R139 1M
C67 1µF
AGC DET
Q5 2N2222
2N2222 Q4
R148 100K
R143 1M
1/2 1458C
ASC AMP
C66 0.1 DISC
HYSTERESIS COMPARATOR
12VDC
C68 0.1 DISC
R144 47K
1/6 4049
R118 10K
C49 .001 DISC
4030
DIFF DATA
4023
1/2 4520
1/2 4013
U113
U100
RECOVERED NRZ DATA
U69
UART
TMS6011
(DWG. 2) PORT IN FA
J11 DIO 0
J11 DIO 1
J11 DIO 2
J11 DIO 3
J11 DIO 4
J11 DIO 5
J11 DIO 6
J11 DIO 7
(DWG. 2) PORT IN FB
(DWG. 1, 3) POC
INT 0 (DWG. 1,2,3)
INT 1
INT 2
INT 3
INT 4
INT 5
INT 6
INT 7 (DWG. 1,2,3)
PORT OUT FB (DWG. 2)
RECOVER CLK (1X)
RECOVER CLOCK (16X)
BYTE WRITE CLOCK (16X)
4019
U111
C72 .001 MYLAR
PLL ADJ.
VR3 50K
R114 47K
R153 100K
4046
U110
R152 150K
C7 .001 DISC
(DWG. 3) 4,800 HZ
(DWG. 3) 19,200 HZ
(DWG. 3) 38,400 HZ
(DWG. 3) TAPE HI SPEED
(DWG. 3) TAPE HI SPEED
(DWG. 3) 1,200 HZ (A)
(DWG. 3) 2,400 HZ
1200 HZ
R117 10K
OUTPORT CLOCK
C47 .001 DISC
4013 U100
4027 U101
1/6 4049 U109
R151 5.6K
C51 DISC 0.1
(500 MV)
AUDIO OUT J6
C70 0.1 DISC
R150 470
H (50 MV)
R149 100
J8 TAPE MOTOR 1
J9 TAPE MOTOR 2
K1
K2
D13 1N4001
D14 1N4001
(DWG. 3) TAPE CONTROL 1
(DWG. 3) TAPE CONTROL 2

NOTES:

1. ✱ DO NOT SUBSTITUTE
2. (ADR 0) S-100 BUS SIGNAL NAME
3. —(100) S-100 BUS PINS
4. [100]— S-100 BUS PINS
5. —[25]> I/O CONNECTORS, POWER SUPPLY, PERSONALITY MODULE
6. <[25]— I/O CONNECTORS, POWER SUPPLY, PERSONALITY MODULE
7. —▷ ON CARD CONNECTION
8. ◁— ON CARD CONNECTION
9. CAPACITORS IN MICROFARADS UNLESS NOTED OTHERWISE.
10. ALL RESISTORS 1/4 W UNLESS MARKED OTHERWISE, RESISTANCE IN OHMS.

SCHEMATIC, AUDIO TAPE I/O, S01		
SCALE:	APPROVED BY: ROBERT M. MARSH	DRAWN BY LITO
DATE: 6-28-76		REVISED 9-29-76
PROCESSOR TECHNOLOGY		
REV. D		DRAWING NUMBER 5

54336 PRINTED ON NO. 1000H-10 CLEARPRINT

Personality Module

J5

J1

Serial Comm. Port

J4

Display Exp.

J3

Keyboard

J11

S-100 BUS

J10

J2

Parallel Data Port

J6

J7

J8

J9

MCM6574

6011 UART

6011 UART

8080

SPARE

SPARE

Serial No.

Rev E

SOLID
BLINK
WHT CHAR
CTRL CHAR
RESTART

NONE
NONE
BLK CHAR
NONE
RUN

DIP SW
S1

VIDEO OUTPUT
GND

P1
P2

VR2 VERT. POS.
VR1 HORIZ. POS.

TAPE AUDIO OUT
TAPE AUDIO IN

SERIAL CTRL
SENSE SW
BAUD RATE

relay
relay

TM1
TM2

XTAL