Radio Shack®

Service Manual

26-3801/3802

TRS-80®
MODEL 100
PORTABLE COMPUTER

Catalog Numbers 26-3801/3802

CUSTOM MANUFACTURED FOR RADIO SHACK TC A DIVISION OF TANDY CORPORATION

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Fig. 1-1 Front View

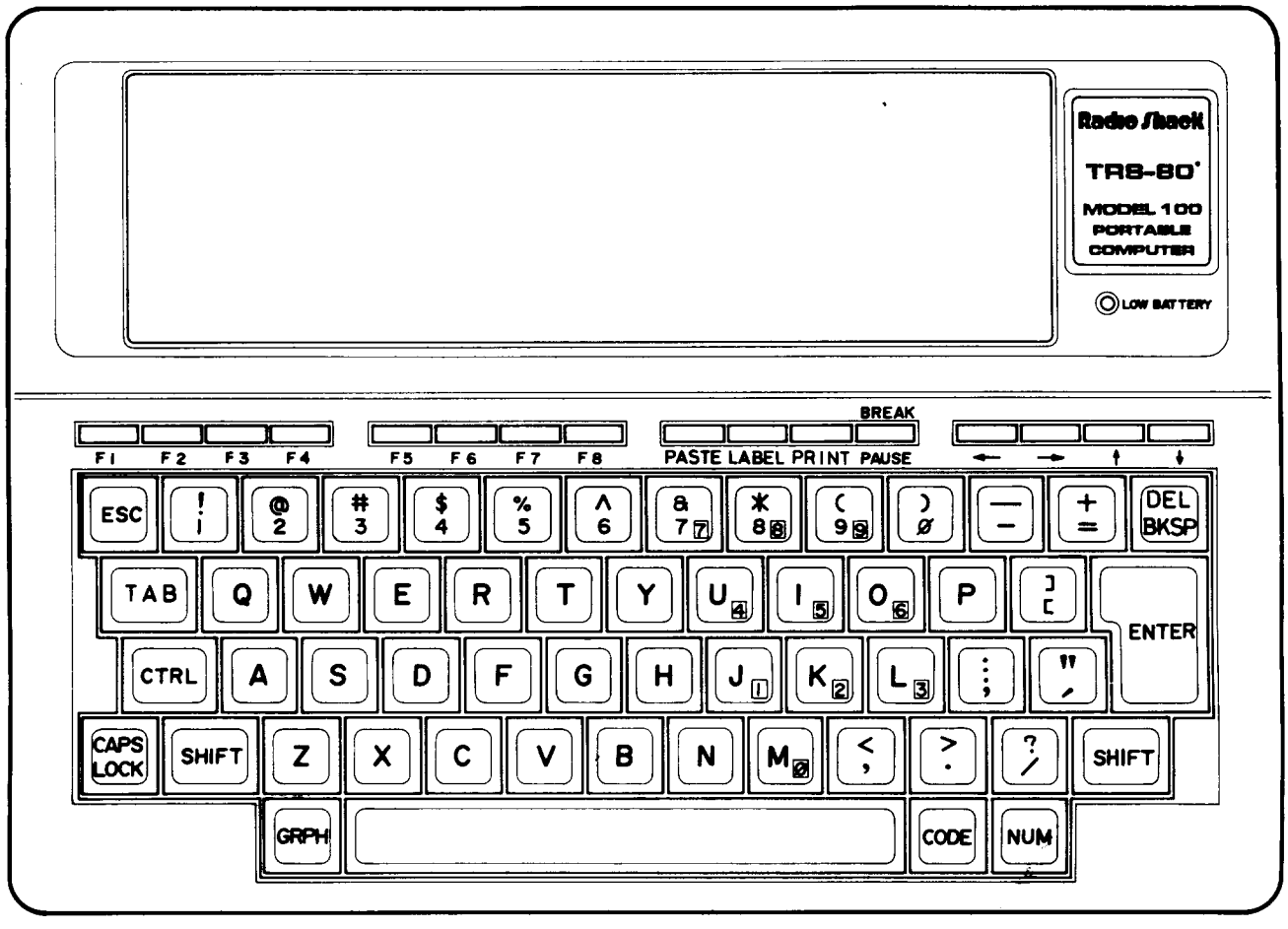


Fig. 1-2 Keyboard Layout

INTRODUCTION

GENERAL

This manual is prepared for the TRS-80 Model 100 technicians working in field or in repair centers.
The user of this manual should be acquainted with Z-80 and 80C85 (8085) microprocessors and also with 81C55 PIO and IM6402 UART LSIs.
Detailed technical information for those microprocessors and LSIs is provided in APPENDIX C of this manual.

This manual consists of seven sections and three appendices:

- Section I
  This section gives general information on the TRS-80 Model 100 such as specifications, switch functions connectors and special features.
- Section II
  This section describes the disassembly and reassembly procedures.
- Section III
  This section describes preventive maintenance and adjustment of the TRS-80 Model 100.
- Section IV
  This section describes general theory of the TRS-80 Model 100 operation, including operational theory of main P.C. Board assembly, LCD Board assembly and keyboard assembly.
- Section V
  This section describes how to troubleshoot the TRS-80 Model 100.
- Section VI
  This section provides a part list and an exploded view of the TRS-80 Model 100.
- Section VII
  This section provides schematics, P.C. Board diagrams and silk screen views of P.C. Boards of the TRS-80 Model 100.
- Appendix A provides instructions for installing the optional ROM and additional RAMs.
- Appendix B provides character code chart of the Model 100.
- Appendix C provides technical information of microprocessors and UART LSIs.

The Model 100, a portable computer that fits easily into a regular sized briefcase, has many special features and functions for home and business use.
Its five built-in Application Programs offer various uses:

- BASIC
  BASIC lets you write and run your own programs.
  Also, BASIC provides various mathematic functions (as described in PART-III of owner's manual).
- TEXT
  TEXT Lets you create new files containing memos, documents or text of any kind.
- ADDRSS
  ADDRSS lets you get information such as addresses and telephone numbers from the ADRS file.
- SCHEDL
  SCHEDL lets you get information concerning appointments, meetings, etc., from the NOTE file.
- TELCOM
  TELCOM lets you use the TRS-80 Model 100 as an auto-dialer or for computer-to-computer communications.

In addition to Application Programs, you can connect the following peripherals to the Model 100:

- **Cassette recorder** to store programs or data on cassette tape.
- **Printer** to print copies of documents, programs or data.
- **Bar code reader** to identify the product marking codes of various marchandises. (Optional/extra software required.)
- **Communication interface** to transfer/receive data to/from the Model 100 and another computer (Acoustic Coupler or Modem Cable required).

SPECIFICATIONS

(1) Main Components

(a) Keyboard

71 keys (9 x 8 matrix)

- Alphabet keys 27
- Number keys 10
- Picture-control keys 7
- Function keys 8
- Special symbol keys 8
- Mode keys 5
- Other special-use keys 6

(b) LCD display

- Display panel ..... 240 x 64 Full-dot matrix
  1/32 Duty
  1/6.66 Bias
- Dot pitch ..... 0.8 x 0.8 mm
- Dot size ..... 0.73 x 0.73 mm
- Effective display area ..... 191.2 x 50.4 mm

(c) Operation batteries

- Batteries ..... Four type AA Alkaline-manganese batteries
- Operation time ..... Five days (At four hours/day)
  Twenty days (At one hour/day)
  (Note: With I/O disconnected)

(d) Memory protection battery (On main P.C.B.)

- Battery ..... Rechargeable battery
- Protection time ..... About 40 days (8 KB)
  About 10 days (32 KB)
- Recharge method ..... Trickle charge by AC adapter or operation batteries

(e) LSIs

- CPU 80C85
  Code and pin compatible with 8085
- ROM ..... Maximum 64 KB (2 Banks of 32 KB)
  Standard 32 KB
  Option 32 KB

- RAM ..... Maximum 32 KB
  Standard 8 KB RAM PACK
  Incremental 8 KB RAM pack on P.C.B.
- Clock/Calender μPD1990AC
  No leap year/No February 29

(f) Dimensions ..... 11-4/5" (L) x 8-4/9" (D) x 2" (H)
(g) Weight ..... 3·lbs. 13.5 oz.

(2) I/O Interface

(a) RS-232C
Conforms to EIA Standard
Signal ..... TXR (Transmit Data)
RXR (Receive Data)
RTS (Request to Send)
CTS (Clear to Send)
DSR (Data Set Ready)
DTR (Data Terminal Ready)

Communications Protocol
- Word length ..... 6, 7 or 8 bits
- Parity ..... NON, EVEN or ODD
- Stop Bit Length ..... 1 or 2 bits
- Baud Rate ..... 75, 110, 300, 600, 1200, 2400, 4800, 9600, 19200 BPS
- Maximum Transmission Distance .... 5 meters
- Driver maximum voltage output ..... ±5 volts
- Driver minimum voltage output ..... ±3.5 volts
- Receiver maximum voltage input .... ±18 volts
- Receiver minimum voltage input .... ±3 volts

(b) Modem/Coupler
Conforms to BEL103 Standards
- Baud Rate ..... 300 BPS
- Programmable Items
  * Data length ..... 6, 7 or 8 bits
  * Parity ..... NON, EVEN or ODD
  * Stop bit ..... 1 or 2 bits
- Full Duplex ..... Answer mode/Originate mode, Switchable
- Other functions ..... Hang-up function
  Auto dialer function

(c) Audio cassette interface
- Data Rate ..... 1500 BPS
  (MARK: 2400 Hz, SPACE: 1200 Hz)

(d) Printer interface
Conforms to Centronics Interface Standards
- Handshake Signal ..... $\overline{\text{STROBE}}$, BUSY, $\overline{\text{BUSY}}$

(3) Special functions

Automatic power OFF

When there is no program operation (awaiting command) for ten minutes, the power is automatically cut off.

To start again, the power switch must be switched OFF and then ON, thus releasing the automatic power OFF condition. (The display will be the same as before the power was cut off)

CONNECTORS, SWITCHES AND CONTRAST VR

(1) Connectors

RS-232C	25 pins (DB-25S)
Printer	26 pins (FRC2-C26-L13-ON)
Modem	8 pins (TCS-4490)
Cassette	8 pins (TCS-4480)
Bar Code Reader	9 pins (A-7224)
System Bus	40 pins (IC socket)
AC Adapter	5.5 mm diameter (center-minus)

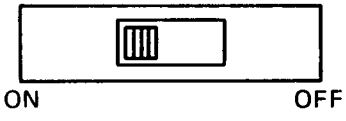
(2) Switches

(a) POWER Switch

Move this switch towards the front to turn the power ON. To conserve the batteries, the Model 100 automatically turns the power off if you do not use it for 10 minutes.

When an automatic power-off occurs, the switch will still be in the ON position even though the power is OFF.

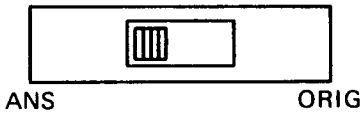
To turn the power ON, move the switch to the OFF position, then back ON.



(b) ANS/ORIG Selector

If you are originating a phone call to another computer, set this switch to ORIG.

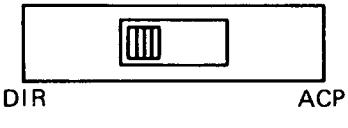
If another computer is calling your Model 100, set to ANS.



(c) DIR/ACP Selector

This selector allows you to select either direct or acoustic coupler connection.

If you are communicating with another computer over the phone lines via the built-in Direct Connect Modem, set this switch to DIR position. If you are using the optional/extra Model 100 Acoustic Coupler (26-3805), set this selector to ACP position.



(d) MEMORY POWER Switch

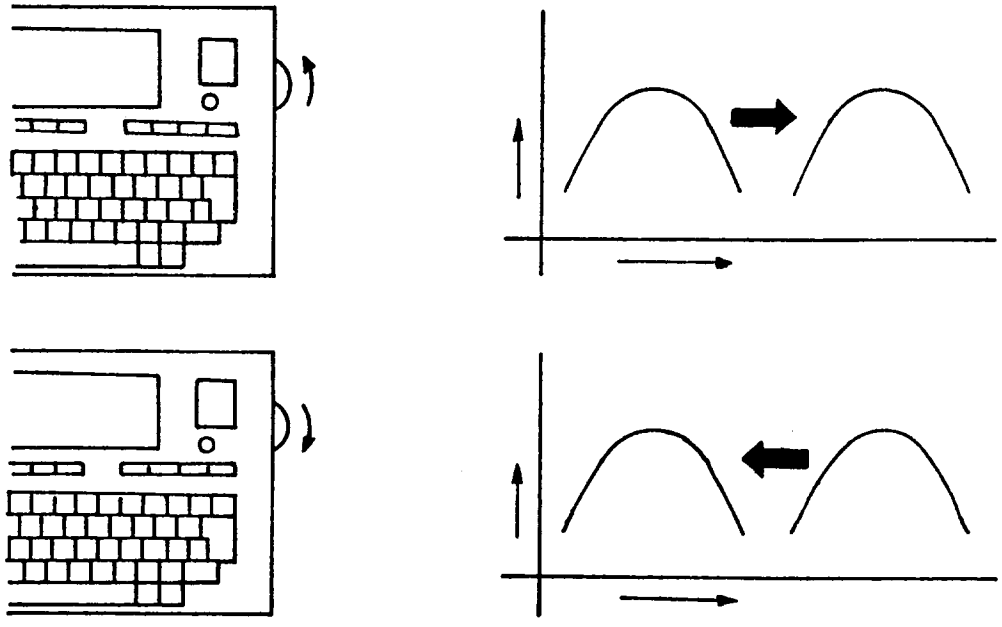
This switch is for preventing discharge of the Ni-Cad battery for RAM back-up.
The Model 100 will not operate regardless of the setting of the power switch unless this switch is ON.
Set this switch to OFF position if the Model 100 is not to be used for a long time.
Note that the RAM will not be backed up when this switch is set to the OFF position.

(e) RESET Switch

If the Model 100 "lock-up" (ie., the display will "freeze" and all keys seem to be inoperative), press this button to return to the Main Menu (start-up) screen. It's highly unlikely that the Model 100 will lock-up when you are using the built-in Application Programs.
However, this situation may occur with customized programs.

(f) DISPLAY ADJUSTMENT DIAL

This control is for adjusting the contrast of the LCD display relative to the viewing angle.



SECTION II

DISASSEMBLY/REASSEMBLY

DISASSEMBLY

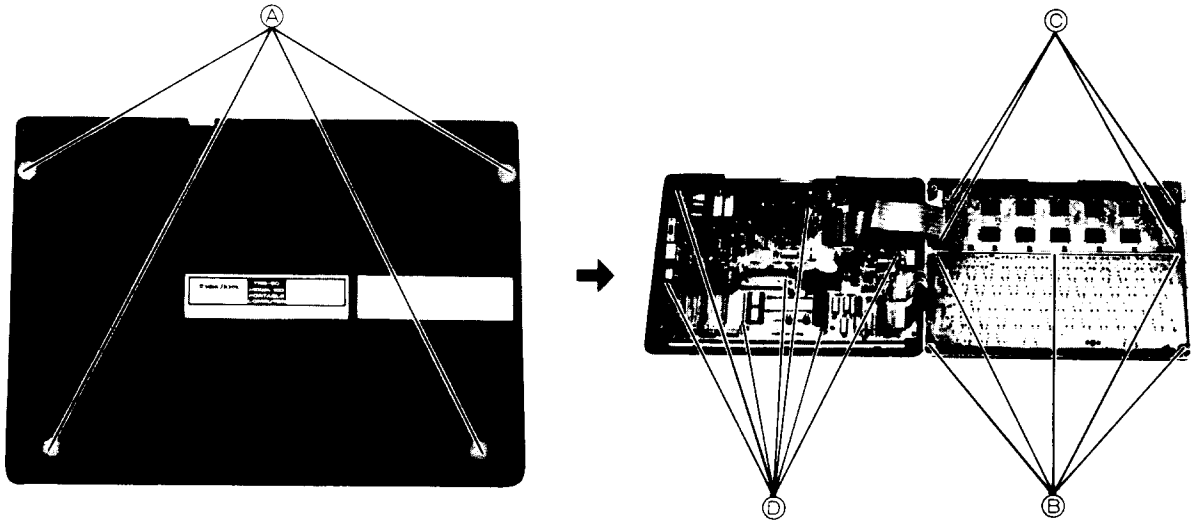
CASE:

(1) Disconnect the cables from the unit.
Taking care not to scratch any key top, turn the unit over and remove the four screws Ⓐ from the upper and lower cases.

(2) Remove the upper case; it opens to the right side.
Note that the upper and lower cases are secured by snaps.
Also, do not apply too much force when pulling open; the LCD and keyboard connectors are attached.

(3) Remove the LCD and key board connectors from the main P.C.B.

(4) Remove the buzzer connector from LCD P.C.B.



K/B P.C.B.:

(1) Remove the five screws Ⓑ and then remove the K/B P.C.B. and K/B supports.

LCD P.C.B.:

(1) Remove the four screws Ⓒ and then remove the LCD P.C.B.

MAIN P.C.B.:

(1) Remove the seven screws Ⓓ.

(2) Remove the MAIN P.C.B. upward, taking care when removing the RESET switch and battery contact spring.

MAIN P.C.B.:

(1) Align the screw positions of the lower case with the MAIN P.C.B.. Gently insert the MAIN P.C.B. from the rear and place the reset switch knob in the proper notch.

(2) Secure the battery contact spring.

(3) Attach the MAIN P.C.B. to the lower case by using the seven M3 x 8 screws.

LCD P.C.B.:

(1) Attach the LCD P.C.B. to the upper case by using the four M3 x 3 screws.

(2) Insert the buzzer connector in the LCD P.C.B.

K/B P.C.B.:

(1) Align the two K/B supports with the holes in the P.C.B. and attach them so that they fit to the P.C.B. edge.

(2) Align the K/B supports and K/B P.C.B. holes with the upper case screws.

(3) Attach the K/B supports and K/B P.C.B. to the upper case by using the five M3 x 8 screws.

CASE:

(1) Position the upper case to the risght side of the lower case, taking care not to scratch the key top.

(2) Attach the LCD and K/B connectors to the MAIN P.C.B.

(3) Place the upper case over the lower case, taking care that the cable is not pulled out of place.

(4) Align the upper and lower cases so that the tabs fit well.

(5) Turn the cases over, and secure them together by using the four M3 x 8 screws.

SECTION III

PREVENTIVE MAINTENANCE

ADJUSTMENT OF THE TRS-80 Model 100

The TRS-80 Model 100 is completely aligned and adjusted at the factory during production. Therefore no electrical adjustments will be required.

CLEANING OF THE BODY AND LCD DISPLAY

(1) To avoid operational trouble, keep the TRS-80 Model 100 clean always.
(2) To clean the body and LCD, use soft, dry, lint-free cloth.
(3) For tough stains, clean the body or LCD using benzol.
Do not use any other solvents except for benzol.

MODEM TRANSMITTING LEVEL ADJUSTMENT

(1) Set the DIR/ACP switch to DIR position.
(2) Connect a 600 Ohm dummy Load between Pin-1 (RXMD) and Pin-7 (TXMD) of the MODEM CONNECTOR (CN4).
(3) Connect a AC Voltmeter between RXMD and TXMD.
(4) Set the TRS-80 MODEL 100 in BASIC mode and enter following commands to generate carrier.
OUT 178, 47 (ENTER)
OUT 168, 02 (ENTER)
(5) Adjust VR2 so as to read −14 to −17 dBm on the AC Voltmeter both for ANS/ORIG modes.

SECTION IV

THEORY OF OPERATION

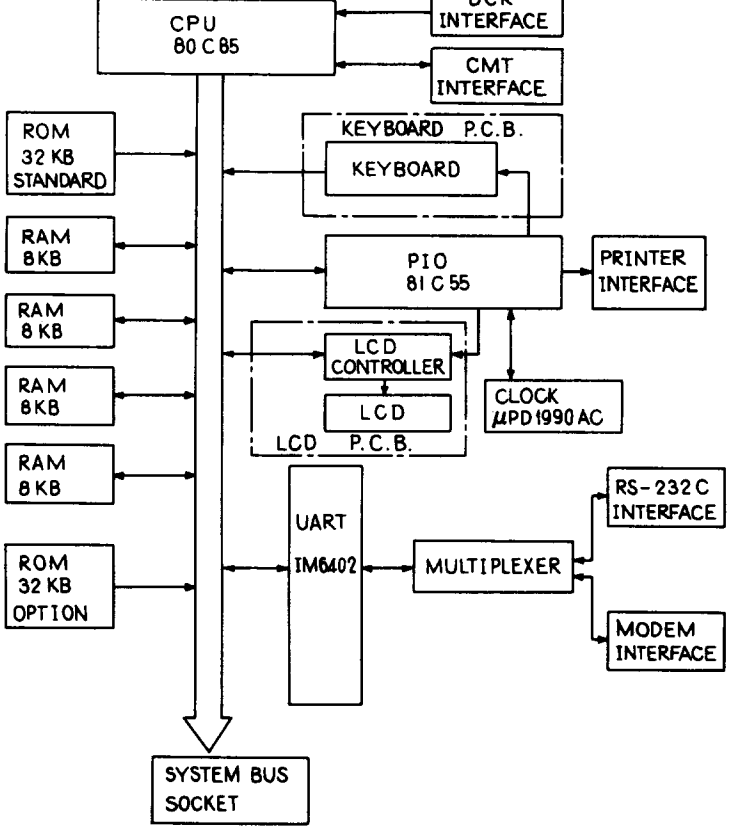


Fig. 4-1 System Block Diagram

GENERAL

The TRS-80 Model 100 has three principal LSIs:

- **80C85 CPU**
  This is the Central Processing Unit which control all functions.
- **81C55 PIO**
  This is the Parallel Input/Output interface controller which controls the parallel printer, key board, buzzer, clock and LCD.
- **IM6402 UART**
  This is the Universal Asyncronous Receiver Transmitter which controls the serial interface (RS-232C or MODEM).

The Input/Output for a cassette recorder and the Input of the BCR are controlled by CPU directly through its SOD, SID and RST 5.5 terminals.
ROM and RAMs are connected to the system bus. ROM is available only for alternative selection of Standard or Optional.

NOTE: On the figure in this section, the solid line shows high-level active line and the broken line shows low-level active line.

- CPU
- MEMORY
- ADDRESS DECODING AND BANK SELECTION
- MEMORY MAP
- I/O MAP and I/O PORT DESCRIPTION
- KEYBOARD
- CASSETTE INTERFACE CIRCUIT
- PRINTER INTERFACE CIRCUIT
- BAR CODE READER INTERFACE CIRCUIT
- BUZZER CONTROL CIRCUIT
- SYSTEM BUS
- LCD INTERFACE CIRCUIT
- CLOCK CONTROL CIRCUIT
- SERIAL INTERFACE CIRCUIT
- LIQUID CRYSTAL DISPLAY
- POWER SUPPLY AND AUTO POWER OFF CIRCUIT
- RESET CIRCUIT

CPU (MSM80C85ARS)

1-chip, 8-bit C-MOS microprocessor.
The MSM80C85ARS (80C85) is a complete 8-bit parallel Central Processing Unit (CPU). Its instruction set is a fully compatible with the 8080A microprocessor, and designed to improve the present 8080A's performance with higher system speed.
The 80C85 uses a multiplexed data bus. The CPU bus is divided into two sections — the 8-bit address bus and the other, 8-bit address and data bus. For the Model 100, the data bus and the address bus are separated by M1 (TC40H373P: Octal D type latch). The performance of the bus line is increased by M2 (TC40H245P: Octal bi-directional bus buffer) and M21 (TC40H244P: Octal buffer/driver).

MEMORY

The memory of the Model 100 consists of a 32KB ROM and a 32KB RAM (standard 8KB with 8KB increment each), and a 32KB BANK ROM (optional).

(1) RAM (Random Access Memory)

The model 100 has a RAM pack consisting of four 2KB RAMs (each 2048 x 8 bits) mounted on a ceramic mother board for a total of 8KB (8192 x 8 bits).
The standard RAM pack equipped in the Model 100 is M9.
Memory can be increased to 32KB by installing M6, M7, and M8.
The internal wiring diagram of the RAM pack is shown in Fig. 4-2.

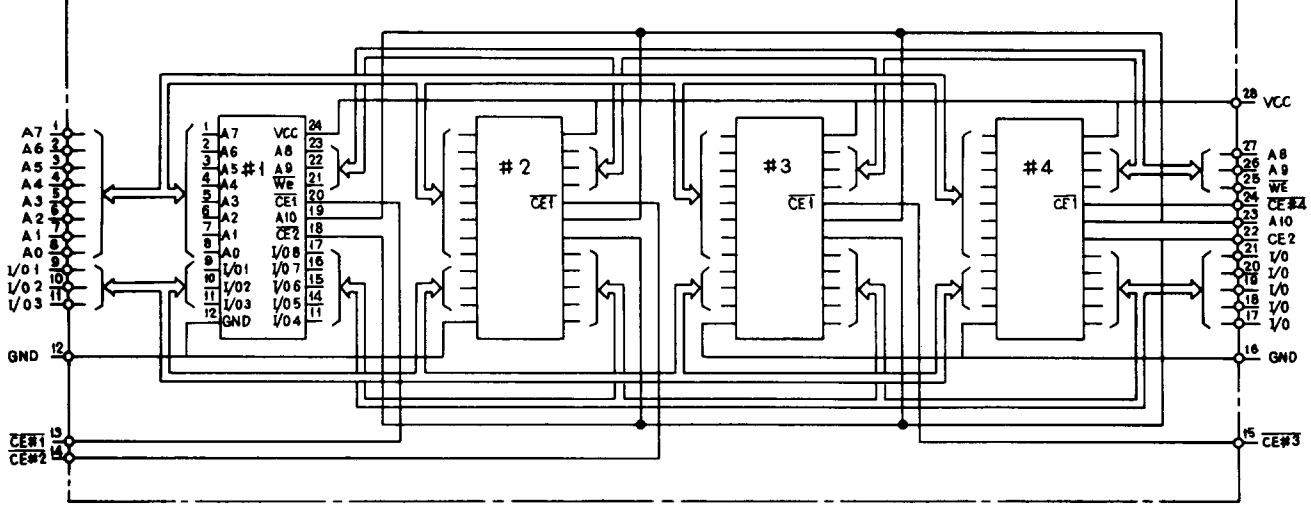


Fig. 4-2 Internal Wiring Diagram of RAM Pack

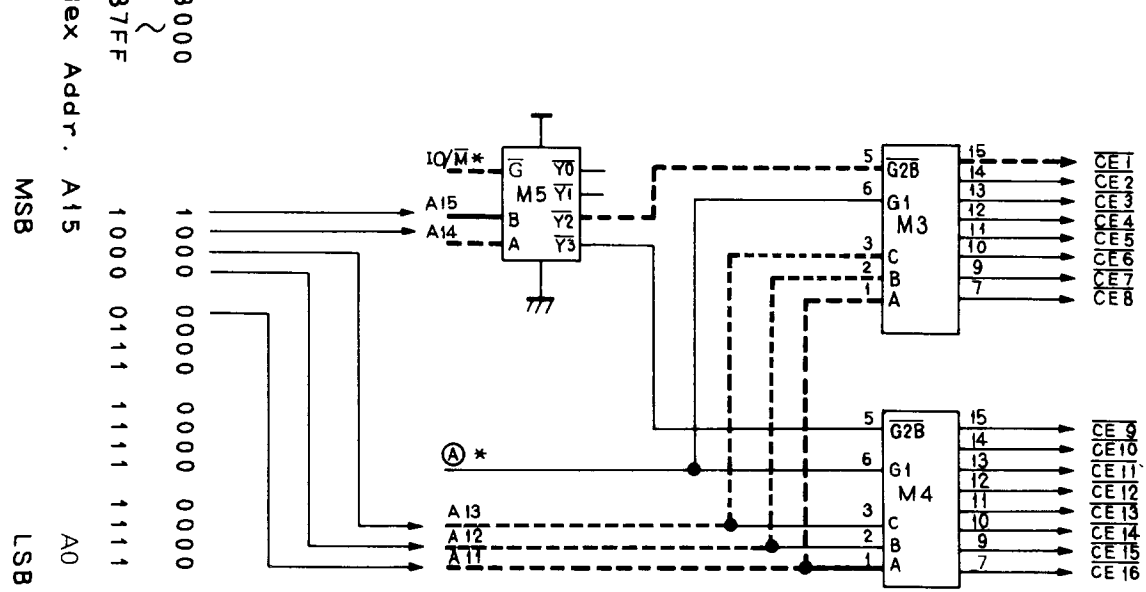
(2) ROM (Read Only Memory)

The ROM used in the Model 100 is a synchronous 32KB (256K bits) memory.
It is operated only by +5V power source with access time of 600 nsec (Max.)
The ALE (Address Latch Enable) is used as the synchronous signal with CPU.
The BASIC and BIOS Programs (BIOS operates the LCD, printer, etc.) are stored in ROM.
An optional ROM can be installed in the special IC socket by removing the ROM cover on the bottom case of the Model 100.
Various types of application programs may be stored in the optional ROM.

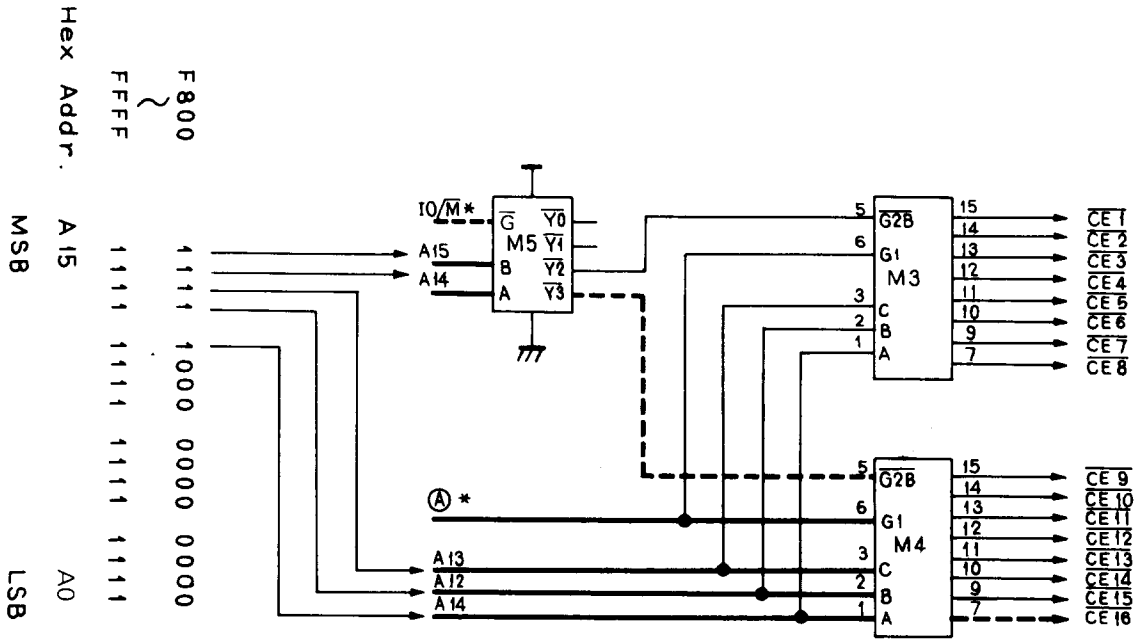
ADDRESS DECODING AND BANK SELECTION

(1) Address decoding for RAM chip selection

Although four 8KB RAM packs are installed, 16 chip-select signals are necessary, because 16 x 2KB RAMs are actually used.
Moreover, because the RAM area is addressed from 8000H to FFFFH (see Fig. 4-3), the control signal consists of IO/$\overline{M}$, A15 and A14, and the 16 chip select signals consist of A13, A12 and A11.
M5 (TC40H139, dual 2 to 4 line decoder/demultiplexer) generates control signal, and M3 and M4 (TC40H138, 3 to 8 line decoder/demultiplexer) generate the 16 chip select signals.



Address decoding for RAM chip 1
(8000H to 87FFH)



Address decoding for RAM chip 16
(F800H to FFFFH)

Fig. 4-3 Address Decoding for RAM Chip

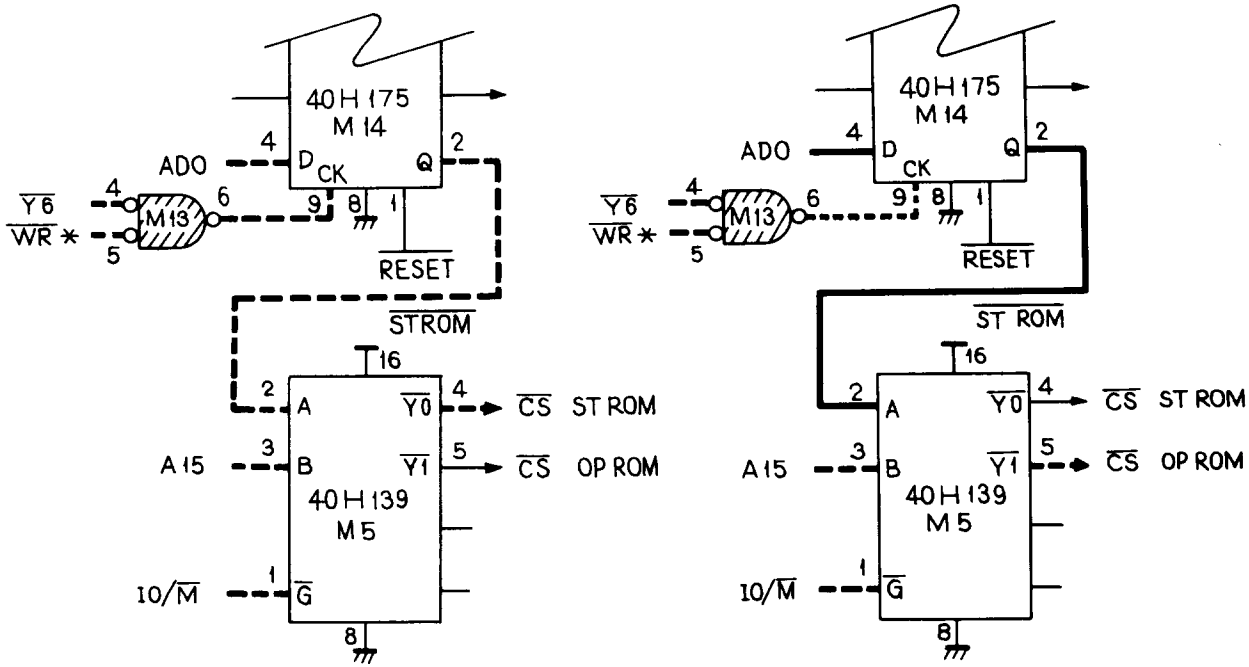
The ROMs (both standard and optional) installed in the Model 100 are the 32KB 1-chip type. As shown in the memory map, the address space is positional from 0000H to 7FFFH.

The chip-select signals are generated by A15 and $\overline{\text{STROM}}$.

As shown in Fig. 4-4, AD0 is latched at M14 (TC40H175 quad "D" type F/F) by $\overline{\text{WR}}$ signal and $\overline{\text{Y6}}$. Then $\overline{\text{STROM}}$ signal is generated (refer I/O port description).

The chip-select signal of each ROM is generated by the IO/$\overline{\text{M}}$ signal at M5 (TC40H139).

The standard ROM is selected by the L $\overline{\text{STROM}}$ signal and the optional ROM by H $\overline{\text{STROM}}$ signal.



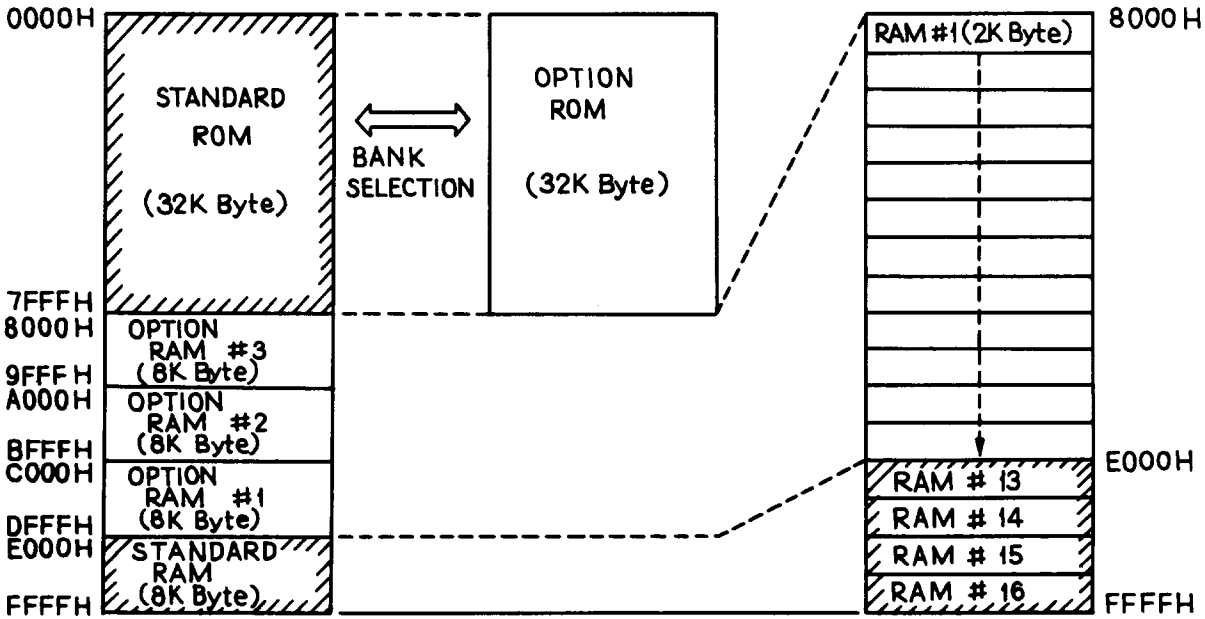
Standard ROM chip selection

Optional ROM chip selection

Active line with high-level

Active line with low-level

Fig. 4-4 Standard and Optional ROM Selection



Addressing of additional RAMs start from higher address.

Fig. 4-5 Memory Map

As shown in Fig. 4-6, I/O address decode circuit, consisting of M-16 (40H138), decodes address signals A12 to A15 and generates the I/O control signal $\overline{Y0}$ to $\overline{Y6}$ and Y7.

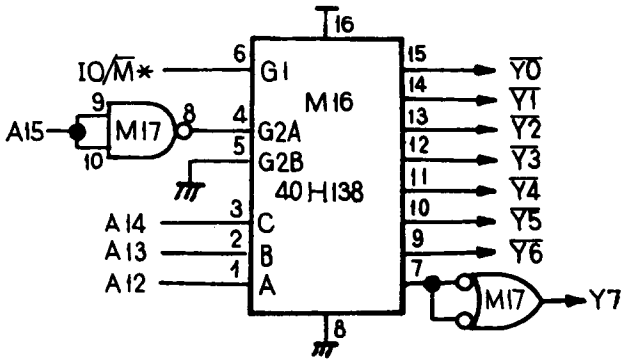


Fig. 4-6 I/O Address Decoder Circuit

Because the LCD driver-select signal Y7 is active "H", the output of M16 (40H138) is inverted by M17 (40H000).
Table 4-1 shows how the select signals ($\overline{Y0}$ to $\overline{Y6}$ and Y7) for the I/O device and I/O address are used.

Address	Signal	Active Level	Application
70H–7FH	–	–	Free area for optional unit and other select signal of various circuits made by user.
80H–8FH	$\overline{Y0}$	L	Device-select signal for optional I/O controller unit.
90H–9FH	$\overline{Y1}$	L	Device-select signal for optional answering telephone unit.
A0H–AFH	$\overline{Y2}$	L	Bit 0: For ON/OFF of relay for signal selection of telephone unit. Bit 1: Used for generation of ENABLE signal of LSI (MC14412) for MODEM.
B0H–BFH	$\overline{Y3}$	L	PIO (81C55) chip-select signal.
C0H–CFH	$\overline{Y4}$	L	ENABLE signal for data input/output port of UART.
D0H–DFH	$\overline{Y5}$	L	ENABLE signal to set various modes and read port of UART.
E0H–EFH	$\overline{Y6}$	L	ENABLE signal for STROM and REMOTE, and input data from keyboard. Also, strobe signal for printer and clock.
F0H–FFH	Y7	H	ENABLE signal for LCD driver LSI.

Table 4-1 I/O Map

Table 4-2 shows the I/O address of each port of PIO (81C55) in the Table 4-1.

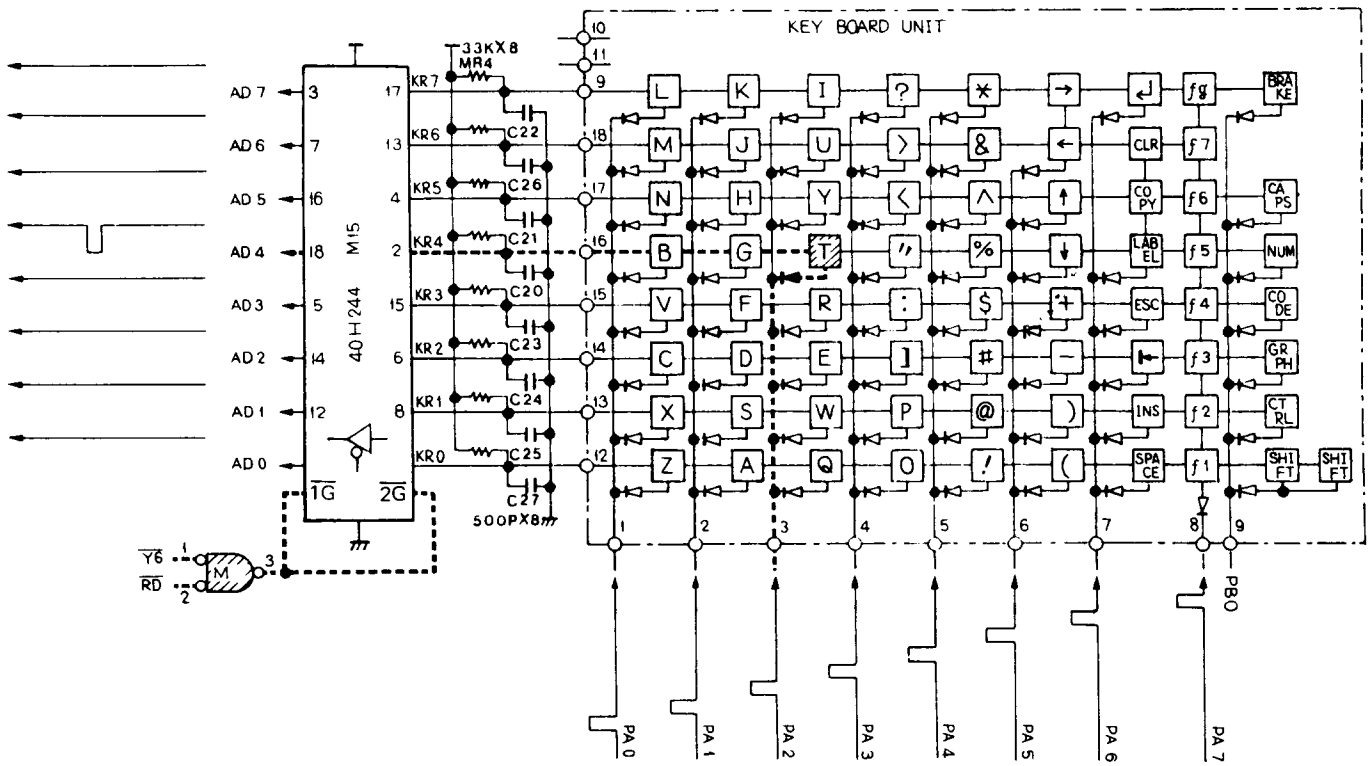
Address	Port or Register
B0H or B8H	Command/status register (internal)
B1H or B9H	Port A
B2H or BAH	Port B
B3H or BBH	Port C
B4H or BCH	Timer register lower byte
B5H or BDH	Timer register upper byte
B6H, B7H, B8H and B9H	Not used

Table 4-2 I/O Address of Each Port

KEYBOARD

Key strobe signals are emitted from PB0 and PA0 – PA7 of 81C55, and the return signals from the keyboard pass through the octal bus buffer IC (40H244) and go to the CPU. The data input port I/O address at this time is E0H – EFH.

Condition of pressing "T" key is shown in Fig. 4-7.



The cassette interface circuitry is divided into three sections:

- Modulation
- Demodulation
- Remote

In Modulation, serial data is modulated and converted into a recording signal.
In Demodulation, the playback signal is demodulated and converted into a digital signal.
Remote is the part of the circuit that enables or disables the recorder's motor.

(1) Modulation Section

Modulation is accomplished in several steps. First, serial data from the SOD terminal of the CPU is inverted (by M34). Then the DC component is removed (by C63). Finally, the data passes through an integrator (consisting of R51 and C64) and, after voltage division, out to a recorder AUX inputs Figure 4-8 shows the modulation circuit of the Cassette Interface.

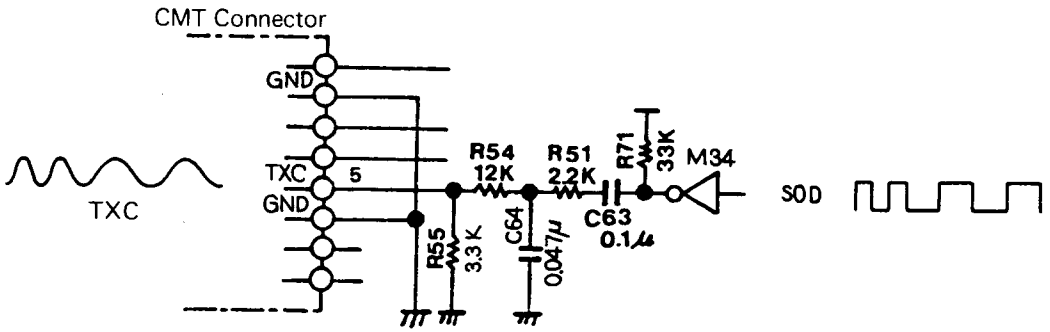
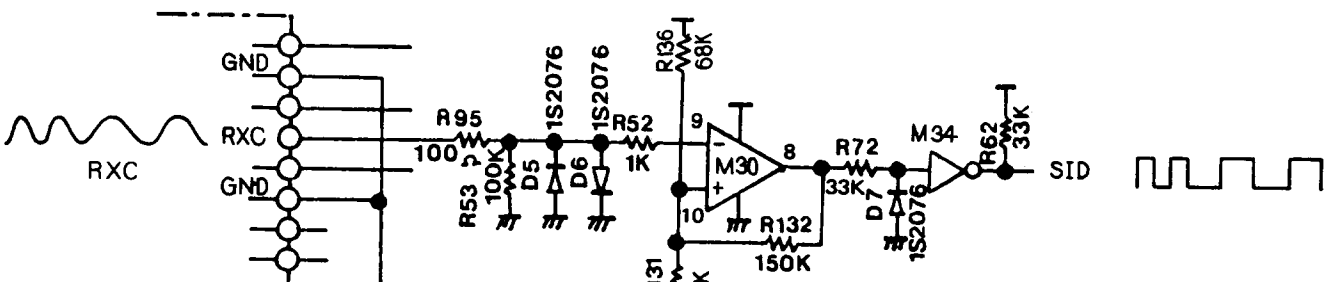


Fig. 4-8 Modulation Circuit of Cassette Interface

(2) Demodulation Section

The signal input from the earphone jack of the cassette recorder passes through D5 and D6, clamp circuit, and it is then emitted from a comparator circuit composed of an operation amplifier IC (TL064, M30). Then, the input signal is converted into a digital signal and applied to the SID terminal of the CPU. Fig. 4-9 shows the demodulation circuit.

In this circuit, D7 clamps the negative voltage output of the comparator.



(3) Remote Section

By writing-in data "1" into bit 3 of the output port (40H175, M14) specified by I/O addresses E0H – EFH, the $\overline{\text{REMOTE}}$ signal output is changed to "L" level.

Then, T6 switches ON and Relay RY1 is energized. This causes the recorder controls to operate. (Refer Figure 4-10)

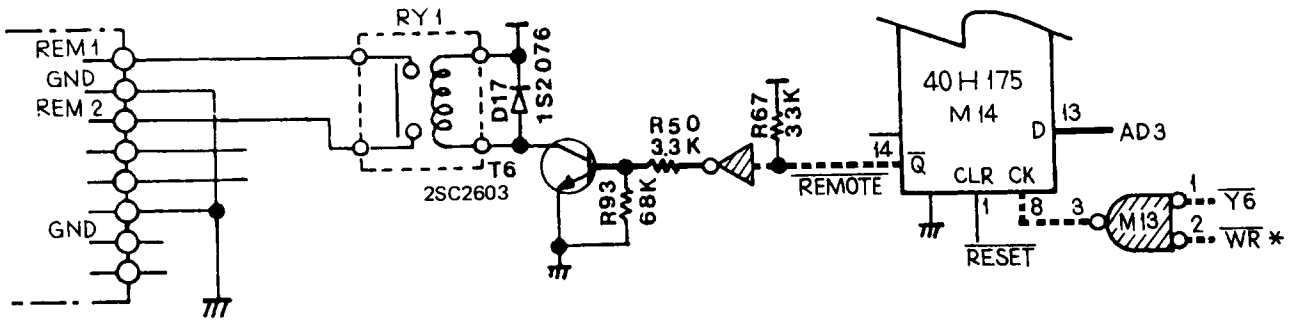


Fig. 4-10 Remote Circuit of Cassette Interface

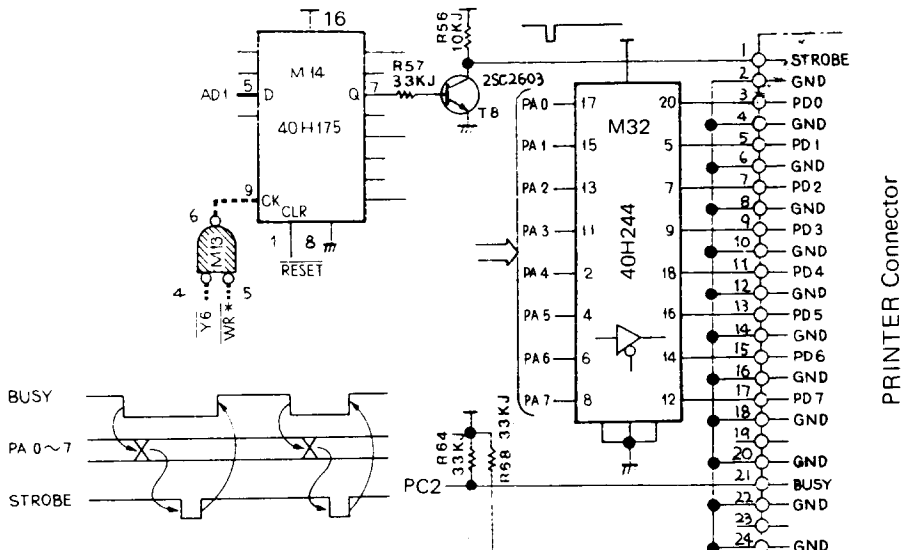
PRINTER INTERFACE CIRCUIT

The printer interface circuit conforms to Centronics standards.

As shown in Figure 4-11, the BUSY signal from the printer is read from PC2 of 81C55. If the condition is NOT BUSY (PC2: "L" level), the 8-bit data (PA0 – PA7 from 81C55) is sent to the printer. By writing-in data "1" into bit 1 of the output port (40H175: M14) indicated by I/O address E0H – EFH, T8 is switched ON and the "L" level $\overline{\text{STROBE}}$ signal is sent to the printer.

As soon as the printer receives this $\overline{\text{STROBE}}$ signal, the BUSY signal is changed to the "H" level indicating that the printer is in busy condition. The CPU then waits for a while until this BUSY signal reaches the "L" level. When BUSY signal becomes "L", the CPU ceases output of data (PA0 – PA7) 1 byte of print data is completed.

If the printer is ON-LINE, the $\overline{\text{BUSY}}$ signal is the "H" level. But when OFF-LINE, the signal becomes "L" and transmission of print data to the printer is not possible.



BAR CODE READER INTERFACE CIRCUIT

The input signal from the bar code reader is subjected to waveform shaping, inverted by Schmitt type inverter (M34), and then delivered the 81C55 PC3 and 80C85 RST 5.5 terminals.
When the bar code reader reads the first white part of the bar code, an "L" signal is generated which is then inverted by M34. As soon as RST 5.5 interaction occurs, data input starts.
Then as the bar code reader is moved across the bars, "H" and "L" signals (which correspond to white and black area respectively) are generated continuously and inversion signals are delivered to PC3 of 81C55 as serial data. (Refer to Fig. 4-12)

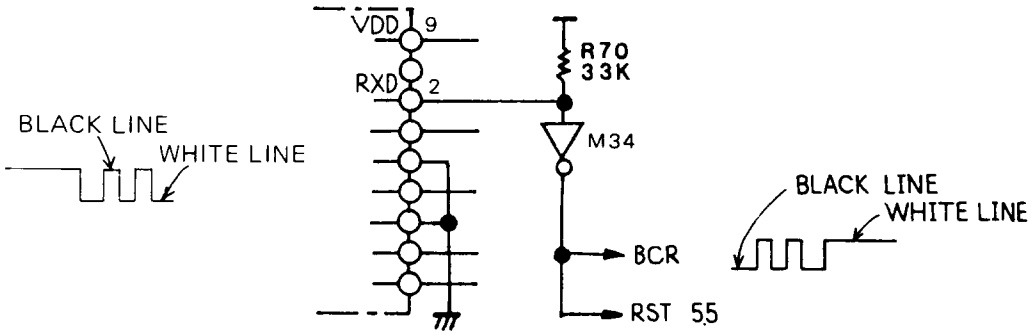


Fig. 4-12 Bar Code Reader Interface Circuit

BUZZER CONTROL CIRCUIT

There are two ways to activate the buzzer. One is to sound buzzer with the specified frequency by emitting a signal from PB5 of 81C55 and the other, by using the timer output of 81C55.

(1) Signal from PB5 of 81C55

When PB2 of 81C55 is at "H" level, the buzzer is sounded by repeatedly switching of buzzer drive transistor ON and OFF. This is caused by "H", "L", "H", "L" . . . output signals from PB5 synchronizing with the frequency for sounding the buzzer.

(2) Using 81C55 timer output

In this method, the buzzer is made to sound by setting the 81C55 timer in the square wave output mode and the value corresponding to the frequency which will sound the buzze. With PB5 at "H" level, the buzzer will sound whenever PB2 is switched to "L".
PB uses this as the buzzer ON/OFF control signal. (Refer to Fig. 4-13)

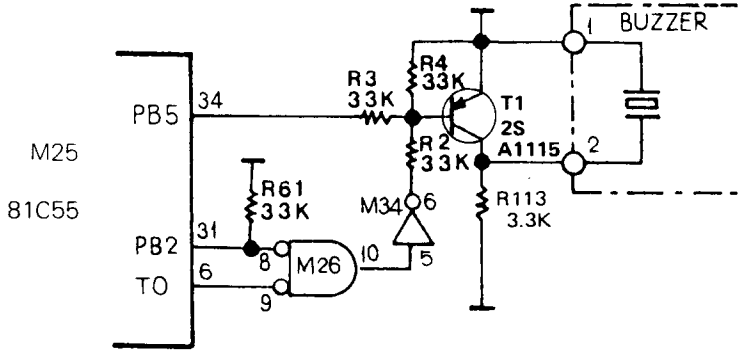


Fig. 4-13 Buzzer Control Circuit

SYSTEM BUS

To expand the use of external devices, a 40-pin system bus is made up of the 40-pin IC SOCKET. As shown in Table 4-3, the 80C85 address bus, data bus, and control bus can all be connected to the external system from the system bus, thus making system expansion easy. In addition, the optional I/O control unit and RAM file unit can be connected to this system bus.

Pin No.	Signal	Input or output	Pin No.	Signal	Input or output
1	VDD	–	40	VDD	–
2	GND	–	39	GND	–
3	AD0	In/output	38	AD1	In/output
4	AD2	In/output	37	AD3	In/output
5	AD4	In/output	36	AD5	In/output
6	AD6	In/output	35	AD7	In/output
7	A8	Output	34	A9	Output
8	A10	Output	33	A11	Output
9	A12	Output	32	A13	Output
10	A14	Output	31	A15	Output
11	GND	–	30	GND	–
12	$\overline{RD}$*	Output	29	$\overline{WR}$*	Output
13	IO/$\overline{M}$*	Output	28	S0	Output
14	ALE*	Output	27	S1	Output
15	CLK	Output	26	$\overline{Y0}$	Output
17	Ⓐ*	Output	25	RESET*	Output
27	INTR	Input	24	INTA	Output
18	GND	–	23	GND	–
19	RAM RST	Output	22	NC	–
20	NC	–	21	NC	–

(Note: NC = no connection)

Table 4-3 System BUS Pin Assignments

The following is an explanation of each signal in Table 4-3 except the CPU signal.

- Ⓐ* signal (pin 16) . . . . . NAND output signal of the $\overline{RD}$* signal and $\overline{WR}$* signal; used by optional RAM file
- RAM RST signal (pin 19) . . . . . Enable signal (external C-MOS RAM)
- $\overline{Y0}$ signal (pin 26) . . . . . Device select signal of optional I/O controller unit

Table 4-4, below, shows the DC characteristic of each system bus signal.

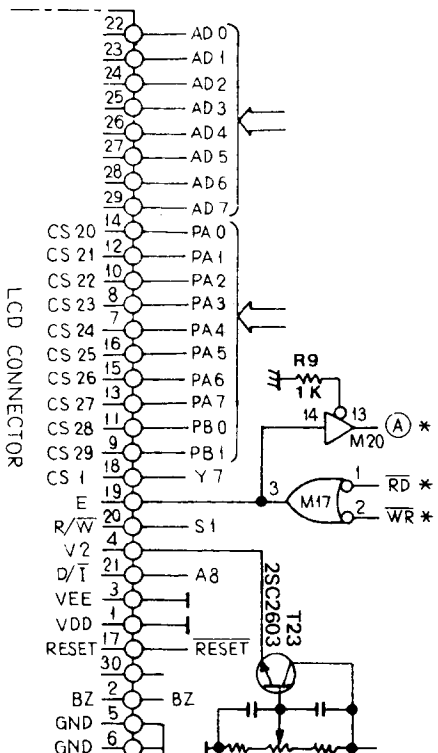
Item	S0, S1, Y0, CLK	Signals other than at left
High-level output voltage (VOH)	2.4V min (IOH = −400 μA)	4.95V min (IOH = −1 μA)
Low-level output voltage (VOL)	0.45V max (IOL = 2 mA)	0.05V max (IOL = 1 μA)
High-level output current (IOH)	−400 μA min (VOH = 2.4V)	−0.8 mA min (VOH = 4.5V)
Low-level output current (IOL)	2 mA min (VOL = 0.45V)	4.0 mA min (VOL = 0.5V)
High-level input voltage (VIH)	–	4.0V min
Low-level input voltage (VIL)	–	1.0V max

Table 4-4 System BUS DC Characteristics

Note: Values shown in Table 4-4 are at normal temperature (Ta = 25°C) and power (VDD = 5.0V)

LCD INTERFACE CIRCUIT

The LCD interface circuit links the LCD driver and the CPU. (See Fig. 4-14)



The following signals are necessary for the interface with the LCD driver.

- AD0 – AD7 ..... For write-in of control data or display data to the LCD driver; signal line for read-out from driver
- Y7 ..... LCD driver enable signal
- PA0 – PA7, PB0, PB1 ..... Chip enable signal for each LCD driver
- S1 ..... Indicates whether data is being written into the LCD driver (S1 = "L") or read out (S1 = "H")
- A8 ..... Register-select signal in the LCD driver; AD0 – AD7 data are display data when A8 = "H", and are command or status data when A8 = "L"
- E ..... NAND output signal of $\overline{RD}$ signal and $\overline{WR}$ signal; indicates the timing of the LCD driver data read/write
- V2 ..... Voltage to keep the LCD driver voltage standard; LCD display can be changed by changing the V2 voltage by VR2

Fig. 4-15 shows the operating timing of each signal.

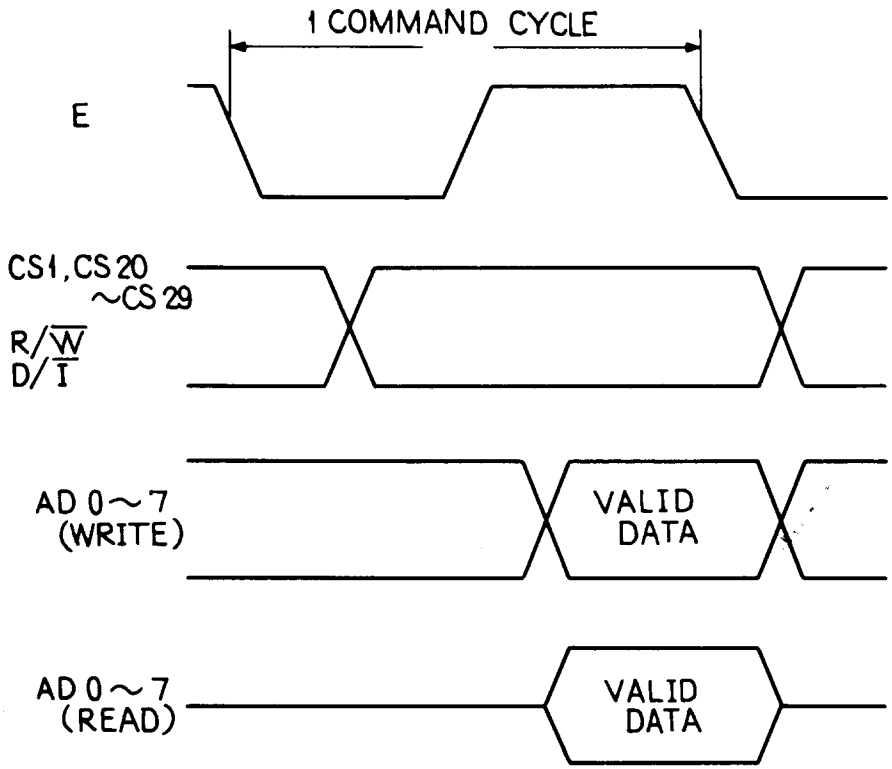
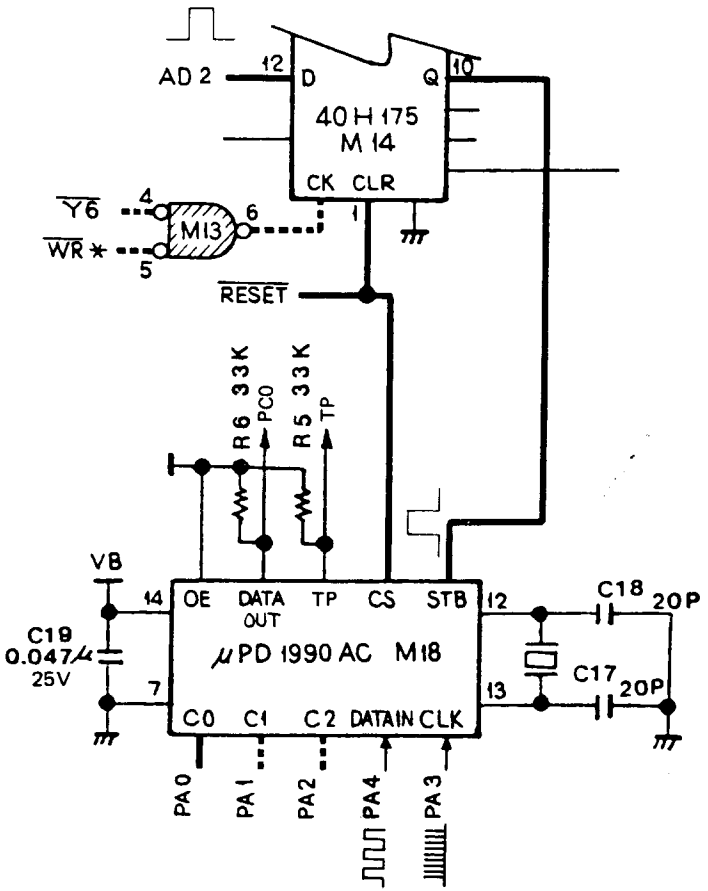


Fig. 4-15 LCD Interface Timing Chart

A clock LSI (μPD1990AC) is used in the clock control circuit so that the time can be set and read by BASIC commands.
As shown in Fig. 4-16 to 4-19, when the Model 100 is in the operable condition (RESET is "H" level), commands and data can be input and output to μPD1990AC (M18) from, the CPU at will.
In addition, because battery voltage VB is applied to the μPD1990AC, the clock functions even when the Model 100 power switch is OFF.
The clock LSI C0 – C2, DATA IN and CLK terminals are connected to the 81C55 PA0 – PA4 terminals, and DATA OUT terminal is connected to the 81C55 PC0 terminal. The STB signal is provided from bit 2 of the output port made by M14 (40H175).
The TP output signal is connected to the RST7.5 interruption input terminal of the CPU. Square waves are output from the TP (4 ms cycle), and one key scan occurs every 4 ms because of the RST7.5 interruption to the CPU.

(a) Time Set Sequence

The CPU sets μPD1990AC to the register shift mode with the "100" pattern of C0 – C2 and the strobe signal which is generated by AD2, $\overline{Y6}$ and $\overline{WR}$* signals passing through M14.
Then, the CPU sends the data of time and data information to the DATA IN terminal of μPD1990AC with timing clock (PA3).



Finally, the CPU sets the time set mode with the "010" pattern of C0 – C2, and the strobe signal.

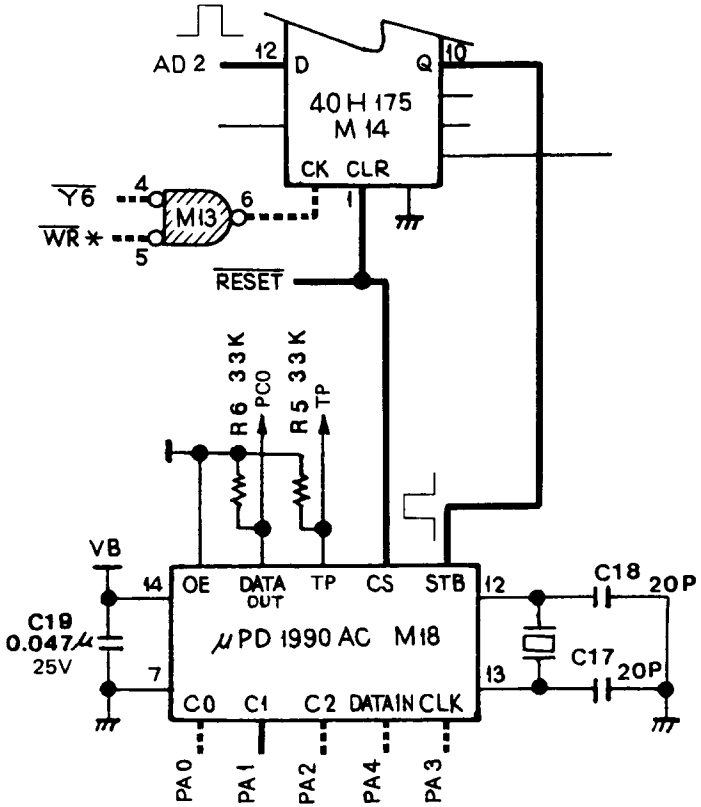
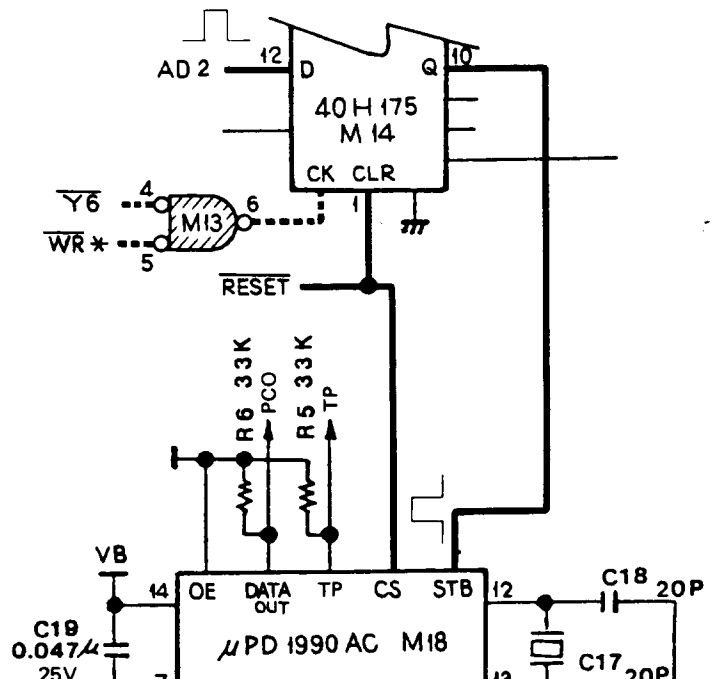


Fig. 4-17 Time Set Condition of μPD1990AC

(b) Time Read Sequence

The CPU sets μPD1990AC to the time read mode with the "110" pattern of C0 – C2, and the strobe signal.



data of time and data information from the DATA OUT terminal. At the same time, the CPU sends the PA3 signal which passes through 81C55 for the timing clock.

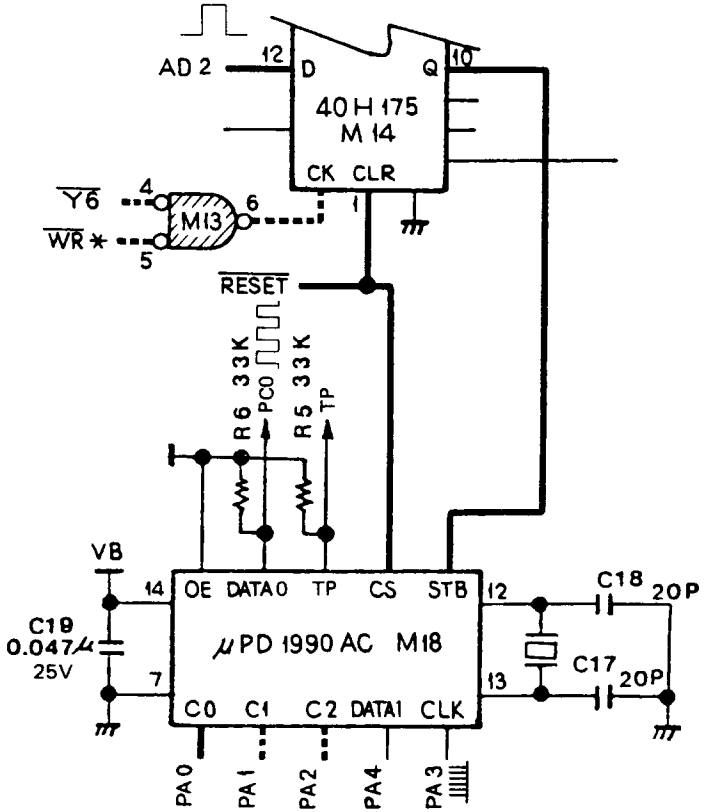


Fig. 4-19 Data Output Condition of μPD1990AC

SERIAL INTERFACE CIRCUIT

The serial interface circuit is divided into three parts; serial control, RS-232C, and Modem. The serial control circuit controls the changes and transmission/reception of data (parallel data and serial) between the CPU and the Modem and RS-232C circuits.

(1) Serial Control Circuit

As shown in Fig. 4-20, serial control of the Model 100 is performed by the UART LSI (IM6402). The CPU begins data transmission/reception after the control word — which determines the mode (transmission/reception) — is written into the control register selected by the $\overline{Y5}$ signal.

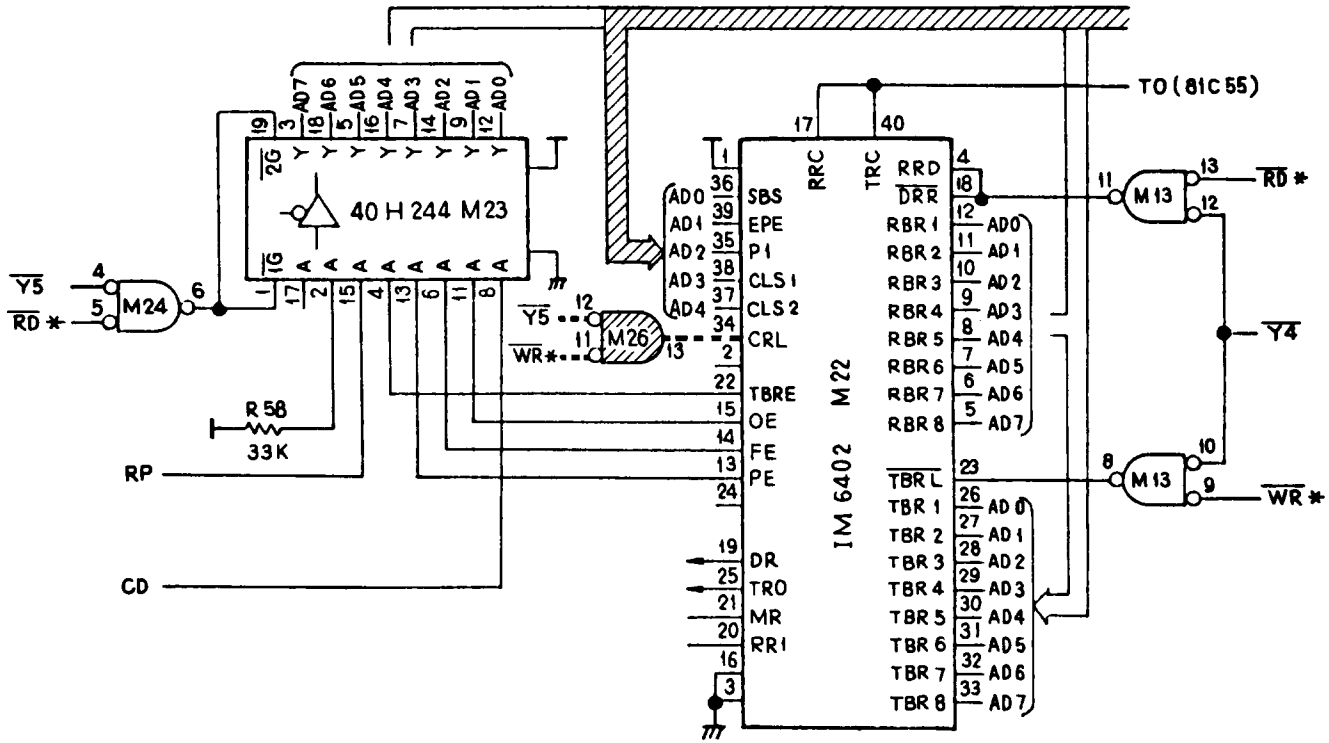


Fig. 4-20 Control Register Load Condition of IM6402

For transmission, the condition of the IM6402 TBRE signal from bit 4 of the status input port (M23) selected by the $\overline{Y5}$ signal is read. If it is "L", it waits until it becomes "H" (See Fig. 4-21).

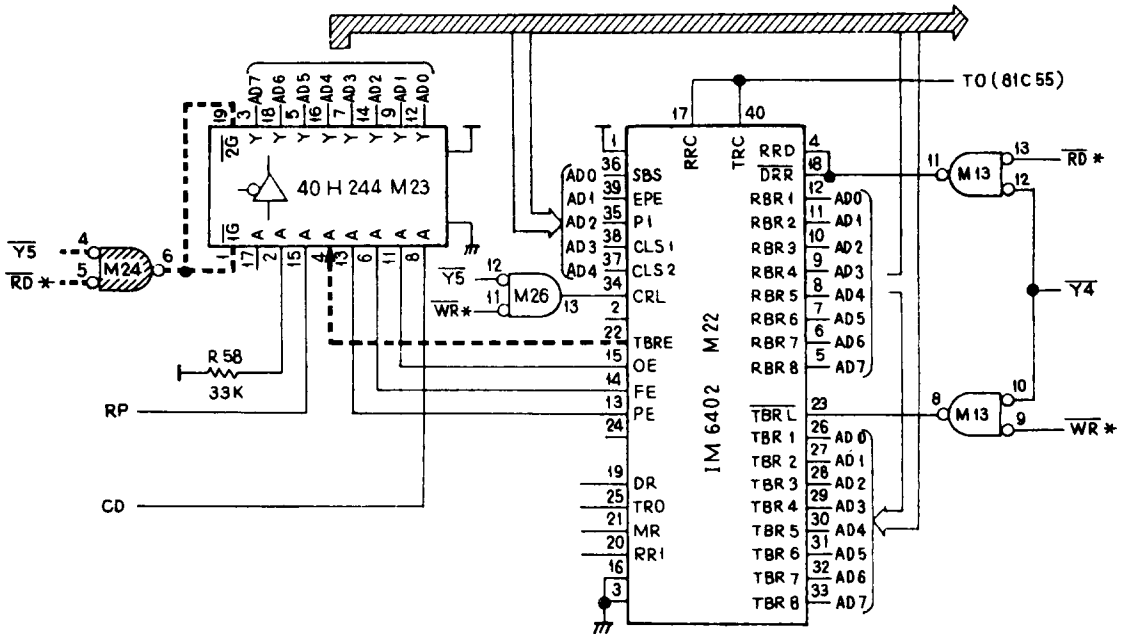
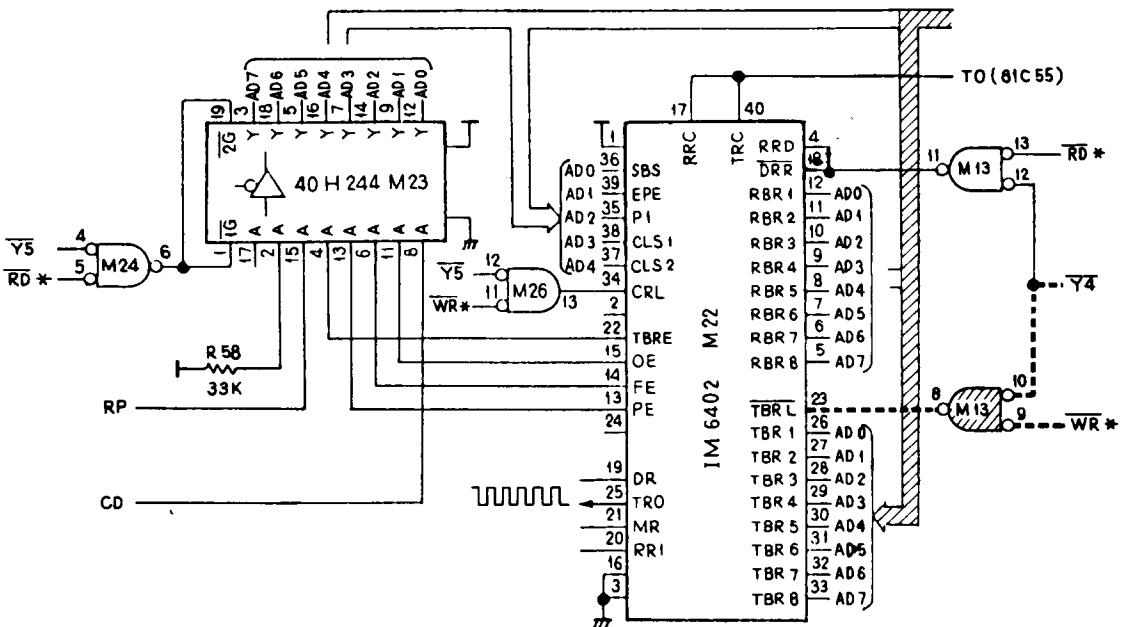


Fig. 4-21 Status Read Condition of IM6402

When the TBRE signal becomes "H", data transmission is possible. If the transmission data is written into the transmitter buffer register (TBR1 – TBR8), the data is output as serial data, including the start, parity and stop bits from the TRO terminal (See Fig. 4-22).



For reception, when data enters the RRI terminal, the DR terminal changes from "L" to "H", and the RST 6.5 interruption notifies the CPU that reception data has entered IM6402, as shown in Fig. 4-23.

The CPU reads the OE, FF and PE signals from the status input port (M23). If there is no error when the serial data is received, the reception data from the receive buffer register selected by $\overline{Y4}$ can be read as 8-bit parallel data.

The IM6402 serial transmission/reception reference clock signal is taken from the TO terminal by setting the 81C55 timer.

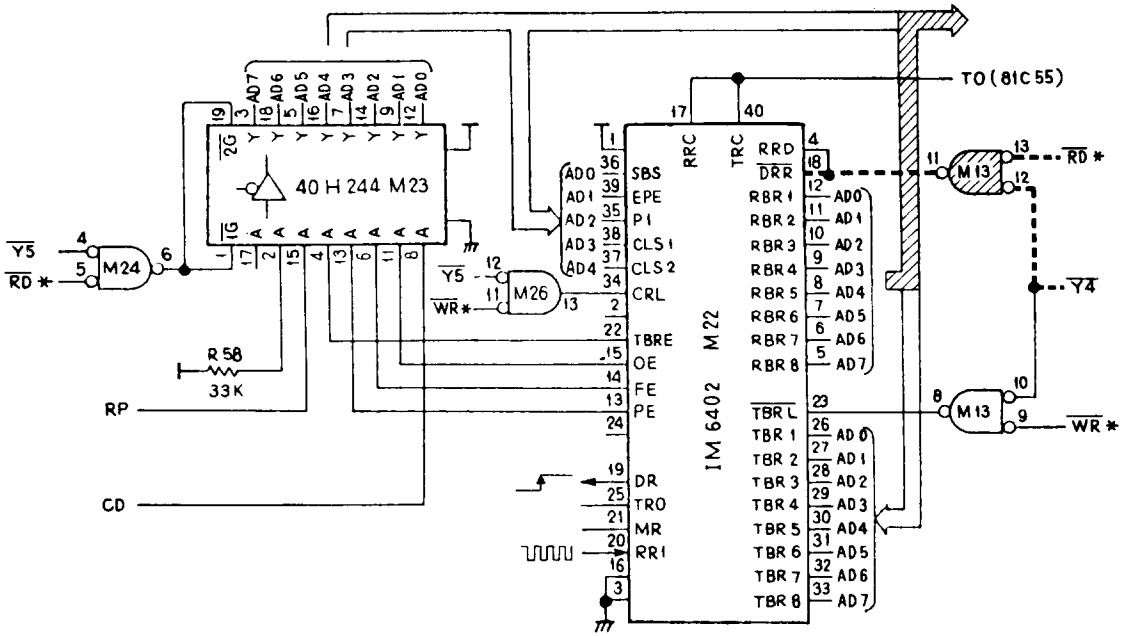


Fig. 4-23 Data Reception Condition of IM6402

In addition, the status input port bit 5 RP signal is held as an option for MODEM operation

Table 4-5 below shows the signal correspondence between the data bus, status bit, and control register of IM6402.

Data bus	Control register	Status bit
AD0	SBS (Stop Bit Select)	–
AD1	EPE (Even Parity Enable)	OE (Overrun Error)
AD2	PI (Parity Inhibit)	FE (Framing Error)
AD3	CLS1 (Character Length Selected 1)	PE (Parity Error)
AD4	CLS2 (Character Length Selected 2)	TBRE (Transmitter Buffer Register Empty)
AD5	–	–
AD6	–	–
AD7	–	–

Table 4-5 Status Bit and Control Register of IM6402

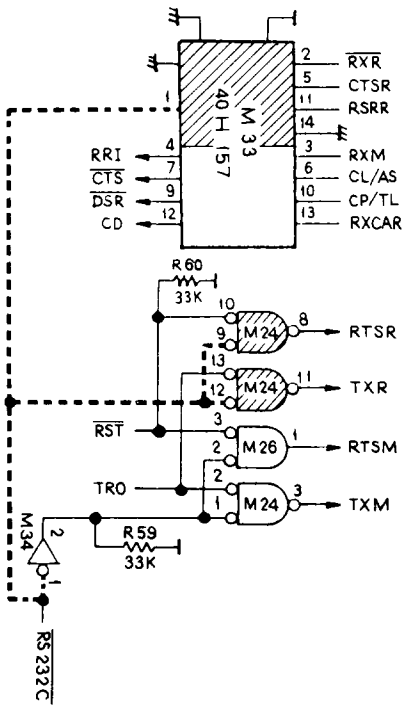
(2) MODEM/RS-232C Exchange Circuit

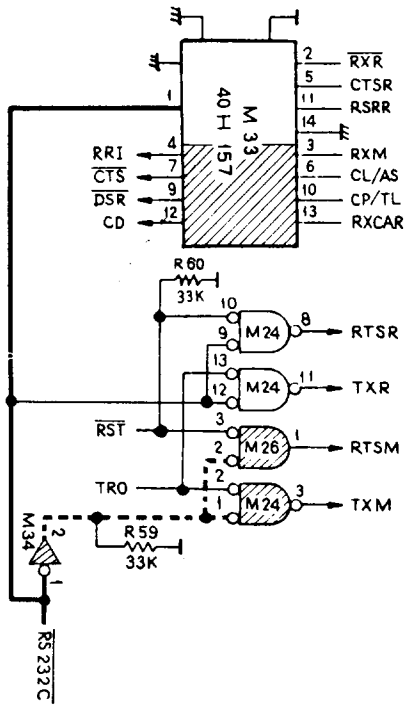
Because the serial input/output port which forms IM6402 is one channel only, the circuit shown in Fig. 4-24 is multiplexed to $\overline{\text{RS-232C}}$ and the MODEM.

The $\overline{\text{RS-232C}}$ signal (PB3 terminal of 81C55) determines whether the serial port is to be used as RS-232C or as MODEM. When the $\overline{\text{RS-232C}}$ signal is "L", the serial port is used as RS-232C, when it is "H", the port is used as MODEM.

The reception signal, including the control signal, is demultiplexed at 40H157 (M33). The transmission signal is multiplexed at M24 and M26.

The $\overline{\text{CTS}}$ and $\overline{\text{DSR}}$ signals (as the serial port) are input to PC4 and PC5 of 81C55, and the CD signal is input from bit 0 of the status input port (M23). Output signals $\overline{\text{DTR}}$ and $\overline{\text{RTS}}$ are output from PB6 and PB7 of 81C55.





(3) RS-232C Interface Circuit

In the RS-232C transmission circuit, after the DC component is removed from the IM6402 TRO, $\overline{RTS}$, and $\overline{DTR}$ signals by the coupling capacitor (0.039 μF 50V), the signals are leveled to ±5V signals by the Schmitt trigger type inverter IC (M35), and then are output as RS-232C transmission signals.

In the RS-232C reception circuit, the DSRR, CTSR, and RXR signals from the external RS-232C line are subjected to waveform shaping and inverted by M35 and diode 1S1535, and then converted to +5V or GND level signals. The signals are then demultiplexed by 40H157 (M33) and converted to $\overline{CTS}$, $\overline{DRS}$ and RRI signals which can be controlled by the CPU. (See Fig. 4-25)

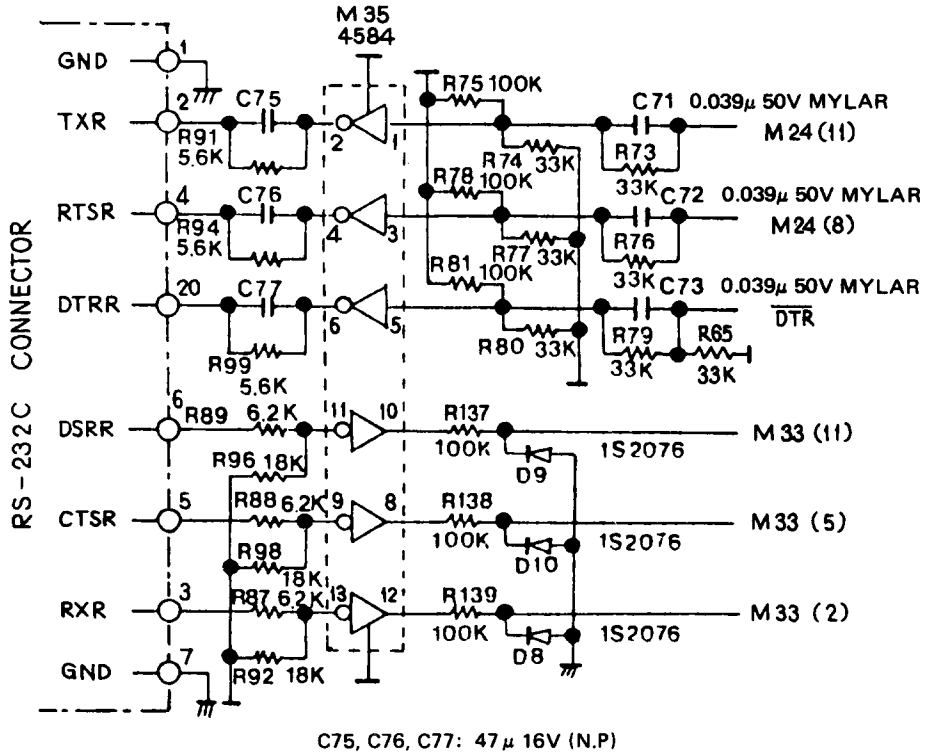


Fig. 4-25 RS-232C Interface Circuit

Table 4-6 shows the application of each signal of the RS-232C circuit.

Symbol	Name	Application
TXR	Transmit Data	Data Output from RS-232C
RXR	Receive Data	Data Input to RS-232C
RTSR	Request to Send	
CTSR	Clear to Send	
DSRR	Data Set Ready	
DTRR	Data Terminal Ready	

(4) Modulation/Demodulation LSI and Peripheral Circuit

The Modem circuitry consists of the Modulation/Demodulation LSI, the transmission filter, the reception filter, and other circuits.

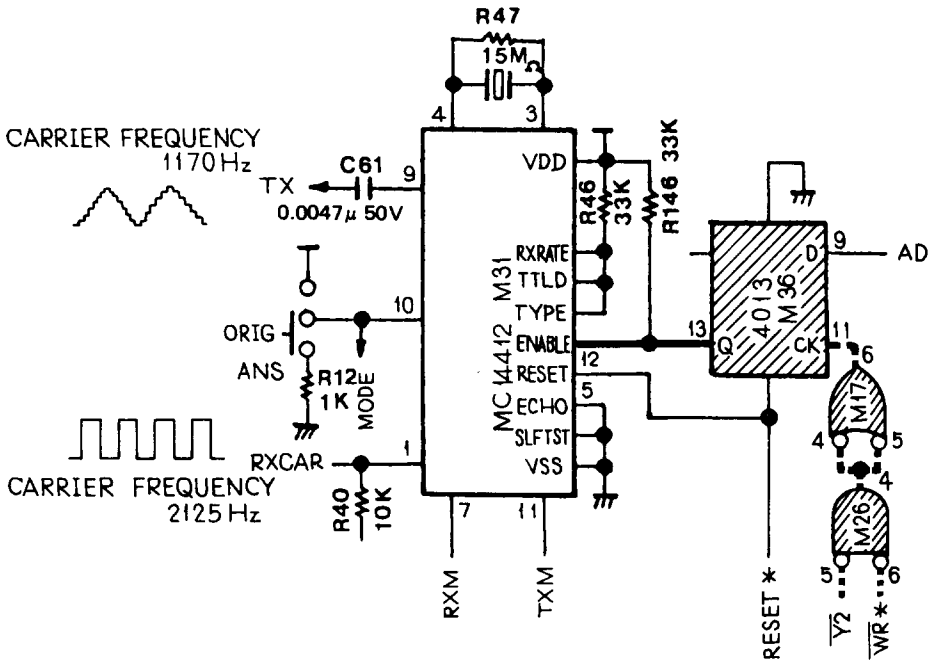
The Rx Rate and Type terminals of MC14412 (M31) are pulled up to VDD.

The baud rate is set to 300 bps, and the U.S. Standard is selected.

Since the ECHO and SELF TEST terminals are not needed, they are grounded (level = 0).

The Q output (En signal) of port M36 selected by bit 1 of the Y2 port is input to the ENABLE terminal until the unit is in the MODE mode.

In addition, the signal designated by the ORIG-ANS switch is input to MODE input, and it switches between the Originate mode or the Answer mode. (See Fig. 4-26)



(ORIGIN MODE)

Fig. 4-26 MODEM LSI and Peripheral Circuit

(5) Transmission Filter Circuit (USA version only)

The transmit carrier signal output from the Tx CAR terminal is DC by C61. The signal level is adjusted to −26.5 dB by the control VR2. The signal then passes through the transmission band-pass filter and is sent to the telephone line or the acoustic coupler.

The transmission circuit is composed of an active filter (consisting of an operation amplifier) and the intermediate frequency which changes according to the mode (Answer or Originate).

Depending on the ORIG-ANS switch setting, transistor T4 is ON or OFF so that R42 is 2.3 kΩ for the answer mode, and the combined resistance of the R42 and R45 values determines the originate mode.

The intermediate frequency of the active filter is 1,170 Hz for the originate mode, and 2,125 Hz for the answer mode. (See Fig. 4-27)

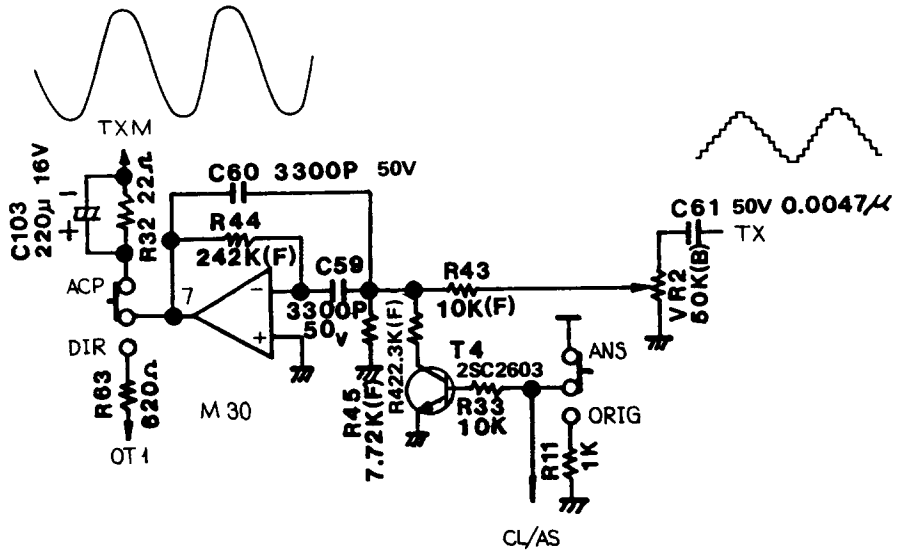


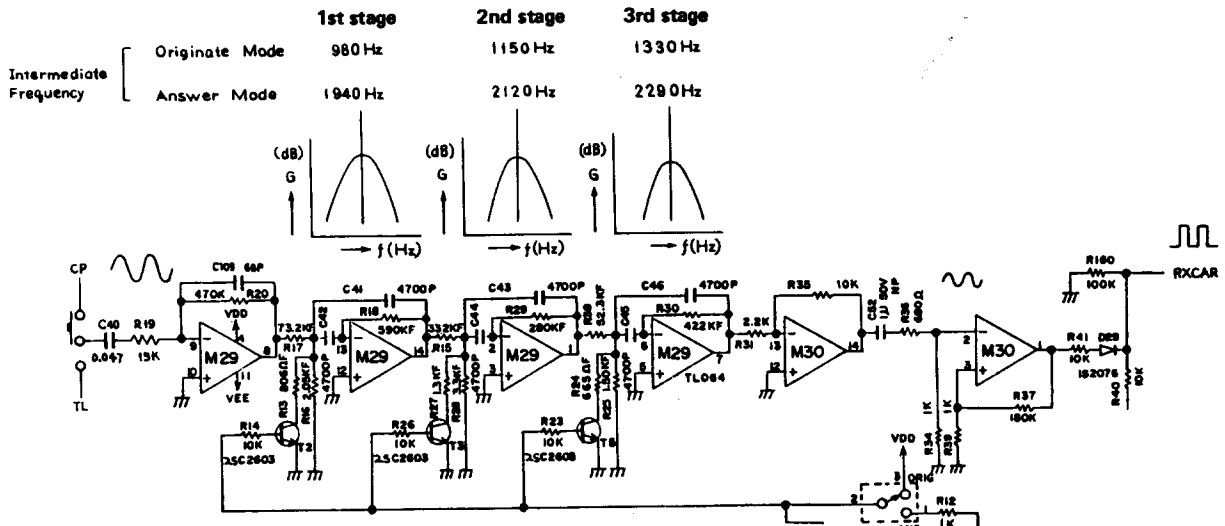
Fig. 4-27 Transmission Filter Circuit

(6) Reception Filter and Comparator Circuit

As shown in Fig. 4-28, the reception circuit input signal is amplified when passing through coupling capacitor (C40), and amplified again as it, passes through 3-stage band-pass filter (composed of an active filter), the signal then passes through the comparator, and after being changed to a square-wave, is input at the RX CAR terminal of MC14412.

Intermediate frequencies of the 3-stage active filter are shown below.

The switching of intermediate frequency for the Originate and Answer modes is accomplished by switching T2, T3 and T5 ON or OFF according to ORIG-ANS switch setting, thus changing the value of resistors, R16, R28 and R25.



When the acoustic coupler is used, the transmission and reception signals are directly connected to the connector (TXM, RXM). When the modem cable is used, they are connected to the secondary side of the driver transformer. The primary side of this transformer is connected to the telephone line via the connector (TXMD, RXMD).

The ACP-DIR switch is used for selection of the acoustic coupler or the direct method of connection to the telephone line.

When the Model 100 is used in the terminal mode, relay RY3 separates the telephone receiver audio input signal (TL) to prevent interference. RY2, another relay, separates the Modem circuit and the telephone at the conclusion of use in the terminal mode and is also used as an automatic dialer.

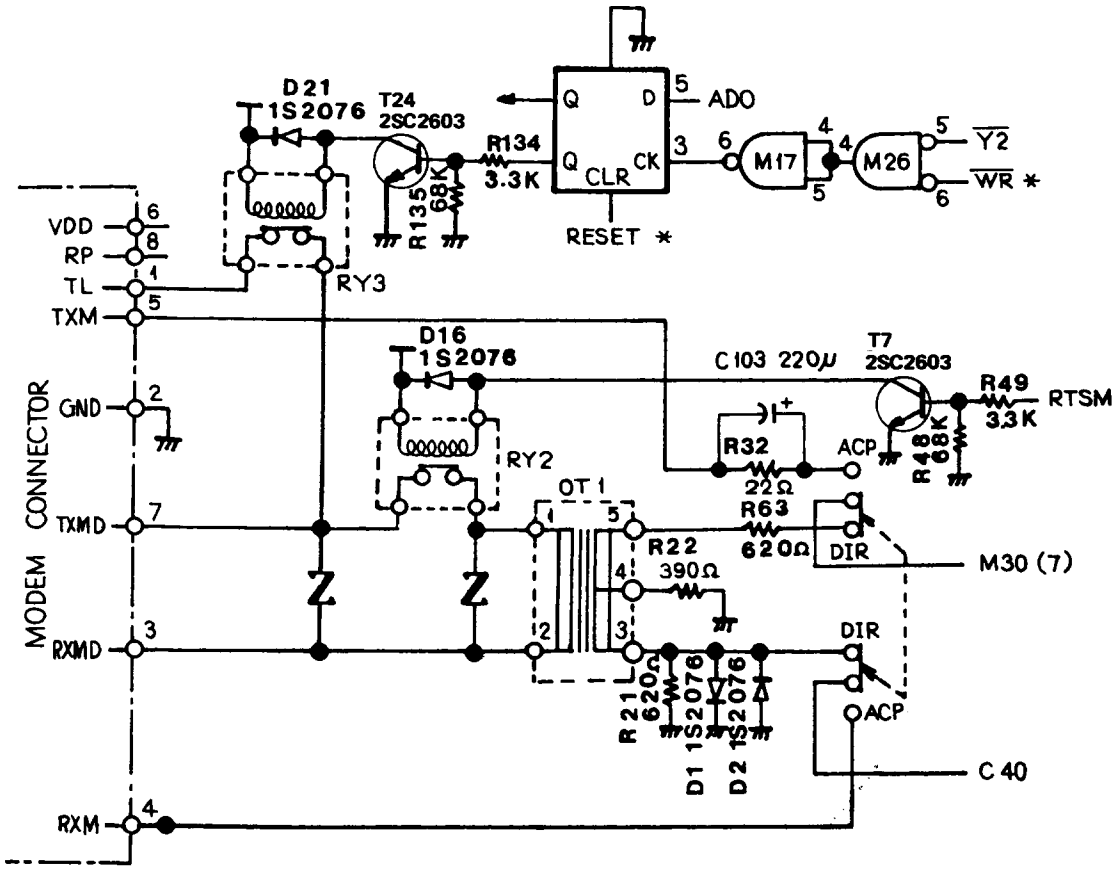


Fig. 4-29 MODEM Connector Interface Circuit

The technical description of the Model 100 LCD is divided into 3 sections:

1. LCD Panel
2. LCD Control Circuit
3. LCD Waveform

(1) LCD Panel

Liquid crystal is a substance midway between a liquid and a solid, although its appearance is much like a liquid. From an electrical and optical stand point, it possesses the properties of a crystal. Items which use this substance are called liquid crystal display elements. The LCD used in the Model 100 is a TN (Twisted Nematic) type of liquid crystal. Its basic construction is shown in Fig. 4-30.

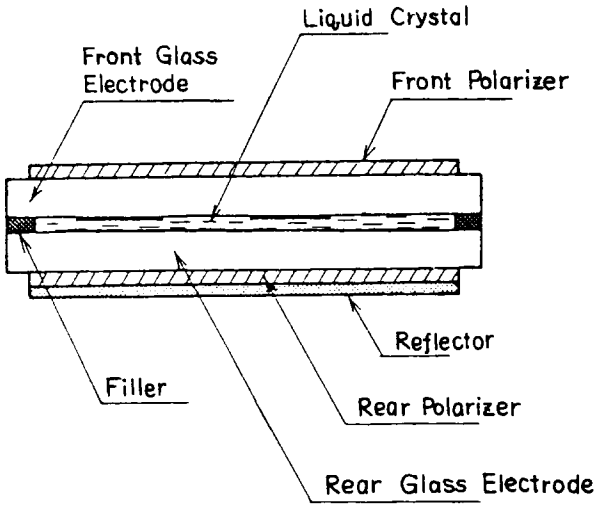


Fig. 4-30 Construction of LCD Panel

The LCD operates as an "electric shutter" that controls the passage of light.
If voltage is applied, the transmission of light is blocked, otherwise, light is allowed to pass so that letters and numbers can be displayed.

Fig. 4-31 demonstrates how the LCD operates:

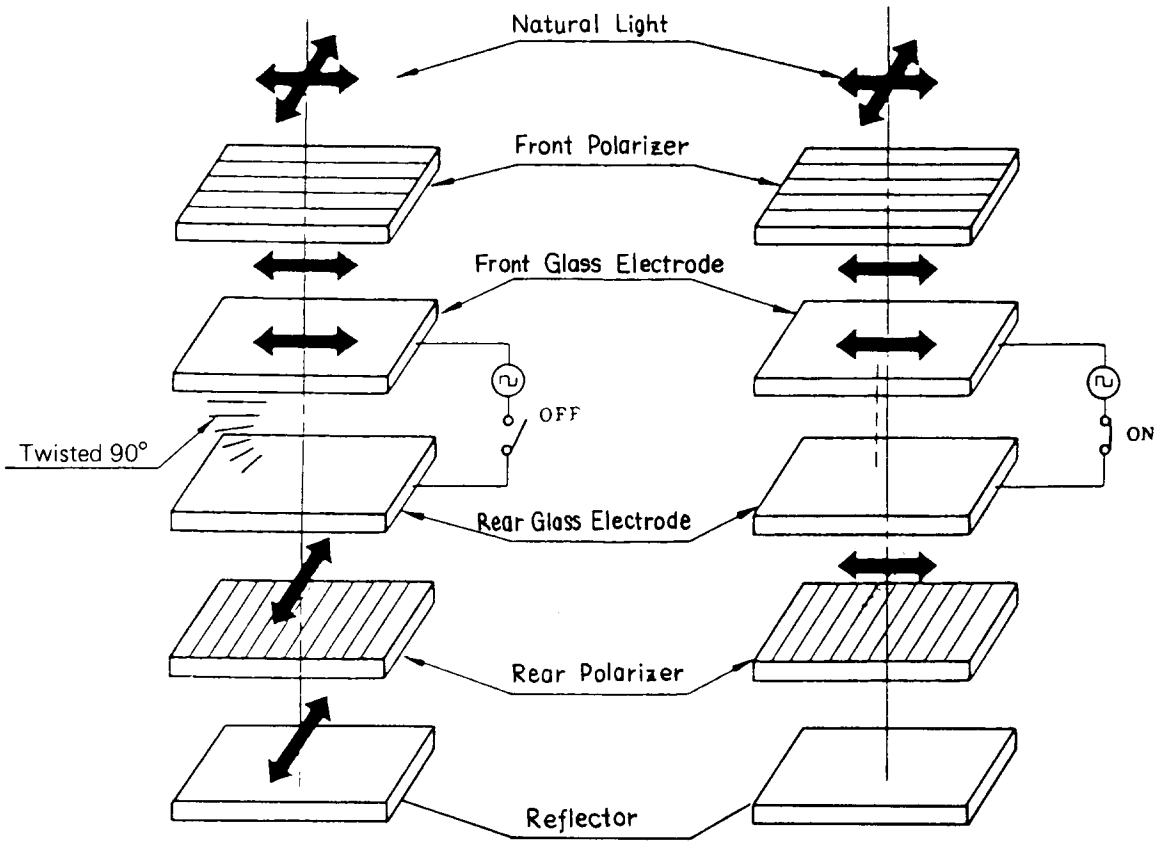
(1) The liquid-crystal display element is sandwiched between the two polarization plates. The polarized axes of the upper and lower plates are placed at right angles to each other to use the optical "twisting" of light.

(2) As shown in Fig. 4-31(a), if voltage is not applied, the liquid-crystal molecules between the upper and lower plates twist 90° to distribute light. This results in a 90° optical movement and the transmission of light.

(3) In Fig. 4-31(b), however, voltage is applied and the liquid appears frosted in current-carrying areas, thus blocking light transmission.

(a) Voltage is not applied

(b) Voltage is applied



Light is passed
Bright

Light is interrupted
Dark

The LCD used in the Model 100 is composed of electrodes in a matrix arrangement (back scan 64, segments 480). Refer to Fig. 4-32.

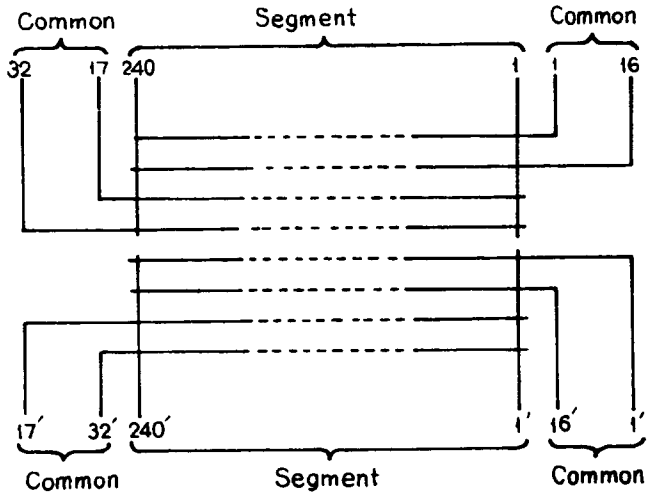


Fig. 4-32 LCD Electrodes

Because this LCD operates on a 1/32 duty time-division drive, the upper 32 and lower 32 back scanning is performed by the same signal.
The angle of the field of vision is 30° in the range that contrasts. K = 1.4 or more (brightness of non-illuminated segment)/(brightness of illuminated segment).

This range can be set at will from 0° to 90° by adjusting the LCD drive voltage with the DISP control VR.

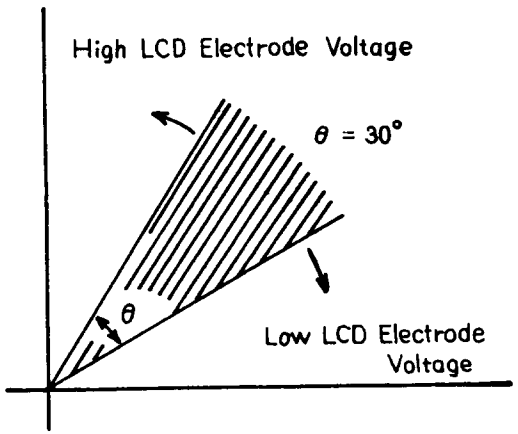


Fig. 4-33 LCD View Angle

Caution: The polarization plate attached to the surface of the LCD panel is easily scratched, and must be handled with great care.
To clean contacts or the display surface, slightly dampen a soft cloth, with benzine and wipe gently. Do not use organic solvents such as alcohol.

(2) LCD Control Circuit

Refer to the LCD PCB circuit diagram (Fig. 4-34) while reading this section.

ICs M11 and M12 (HD44103) are back-scan driver ICs. The timing signal necessary for the display is generated by the built-in oscillator, and by C5, and R10. This timing signal is also supplied to the segment driver side for control of the display.

There are 16 HD44103 back-scan signal outputs. M11 and M12 are cascade connected, and a 1/32 duty back-scan signal is made. By using a C and R only at the M11 side, a timing signal is generated, and M12 is controlled by that signal. M11 can then be considered to be the master IC and M12 the slave. The basic oscillation frequency is about 430 kHz.

Fig. 4-43 shows the internal logic composition.

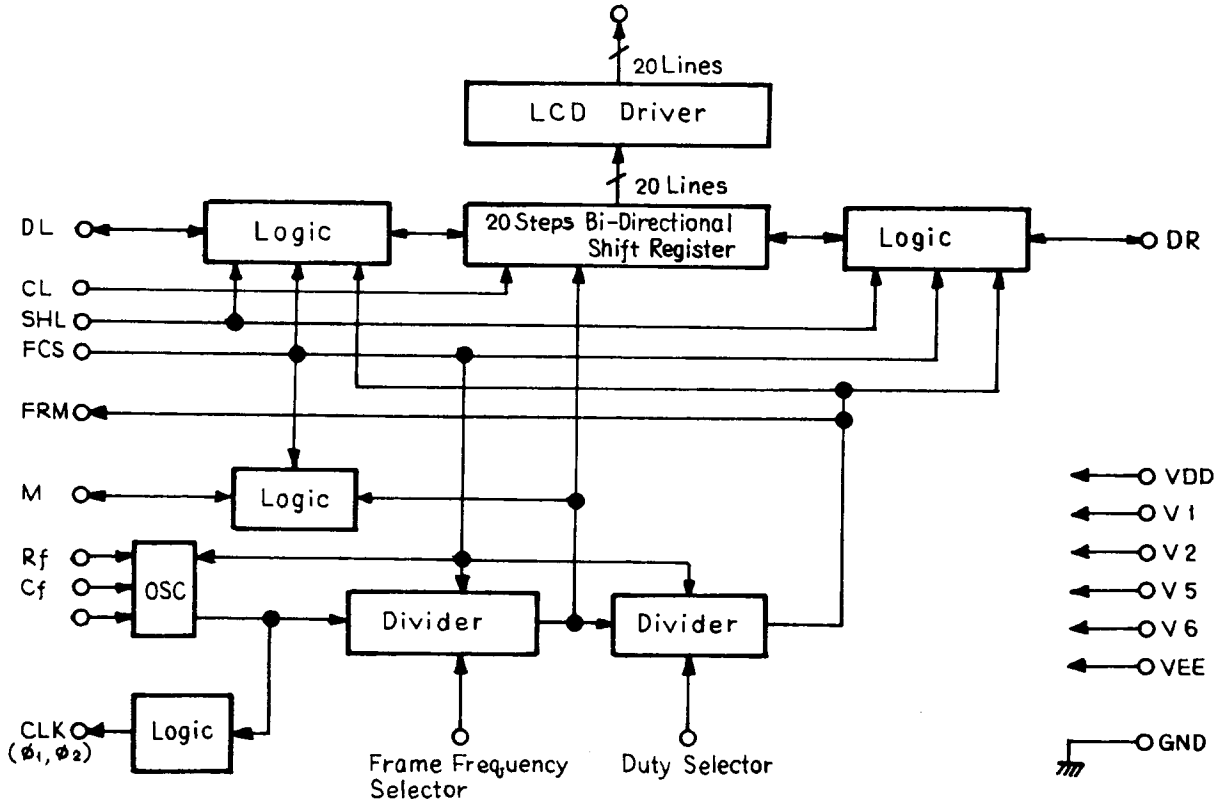


Fig. 4-34 HD44103 Internal Logic Diagram

The timing signals are M, FRM, CLK (ϕ_1, ϕ_2) and CL. The M signal inverts the LCD drive waveform one image at a time to change it to AC. Because the continuous application of DC to the LCD would shorten the element life, an alternating electric field is applied to the liquid crystal surface during drive to make the waveforms symmetrical and reduce the DC component.

The FRM signal is the display repeat frequency, the signal which sets the number of scans per second. For the Model 100, FRM $\simeq$ 70 Hz.

The ϕ_1 and ϕ_2 signals are the locks for HD44102 RAM operation.

One bit of data from the built-in RAM corresponds to one dot of illumination or non-illumination on the display. The driver output is 50 lines.
The transfer of the display data is accomplished by 8-bit parallel data. This IC has several types of commands, and the D/I (H: data, L: command) signal distinguishes between commands and data.
Fig. 4-35 shows the internal logic composition.

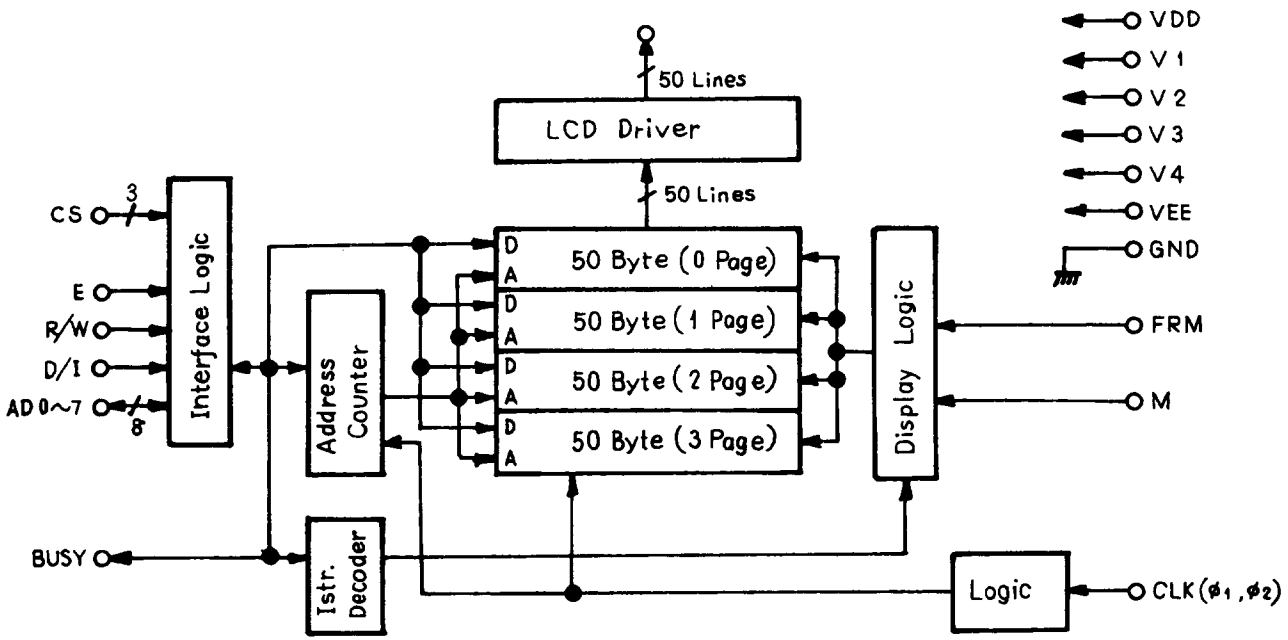


Fig. 4-35 HD44102 Internal Logic Diagram

Because the Model 100 has 240 segments each (upper and lower), the M5 and M10 segment output Y41 – Y50 becomes NO-CONNECTION. The power supplied to these IC's, in addition to VDD (+5V) and VEE (–5V), also includes V1 – V6.
VDD and VEE are the power supplies which operate the IC logic, and V1 – V6 make the LCD signal.
V1 – V6 are made up by the resistance splitting of R1, R2, R3, R4 and R5. By passing through operation amplifier M13 (HA17902), the output impedance of the power supply is lessened.
Capacitors C3, C4, C6, C7 and C8 augment the peak current during LCD illumination.
R11, R12 and R13 are resistors for IC latch-up prevention.
This board also includes a low-power detection LED and buzzer connectors.

(3) LCD Waveform

To drive the liquid-crystal elements by the 1/32 duty line-sequential drive method, the LCD of the Model 100 makes sequential selection of the 32 scanning electrodes.

For each dot, the display signal passes through the signal electrodes and is applied 32 times for one display. At this point, the signal is necessary at each dot only one time, and the signals for the other 31 times correspond to other dots on the same signal electrode.

The maximum voltage applied to the Common electrode and Segment electrode is the potential difference between V1 and V2.

In addition, a is the bias coefficient which determines, from the standpoint of contrast, the maximum ratio between the illumination voltage and the non-illumination voltage.

When that ratio is greatest in relation to the effective ON and OFF voltages, a = 6.66.

Thus, for V1, V2, V3, V4, V5 and V6:

V1 = VEE (−5V)

V2 = V (About 0 ~ 4V)

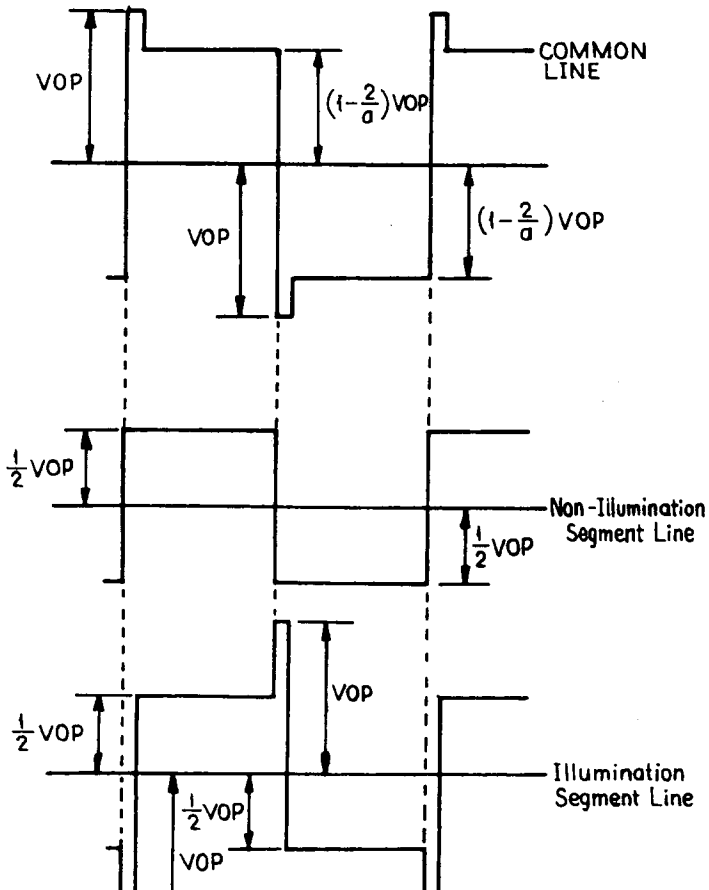
V3 = 2/aV

V4 = (1 − 2/a)V

V5 = (1 − 1/a)V

V6 = a/aV

Fig. 4-31 shows the drive waveform for illumination and non-illumination.



POWER SUPPLY AND AUTO POWER OFF CIRCUIT

The Model 100 logic circuits use ±5V. This power is supplied by the DC/DC converter.
Also, the power supply has an Automatic Power OFF function (this circuit is shown in Fig. 4-37).
The circuits will be described by dividing them into the circuit which supplies the power, and the low-power detection and automatic power OFF circuits.

(1) DC/DC Converter Circuit

OT2 is a converter transformer which oscillates T21 and T22 and generates voltage at the secondary side of the transformer.

At the same time the power is switched ON, a very slight collector current flows to T21 and T22. Also, voltage between pins 7 and 9 of the converter transformer is generated, and the T22 base potential becomes positive. In other words, the base polarity becomes biased in the forward direction. This voltage causes the T21 and T22 base current to flow, and the collector current is increased. When the current can longer increase, because of transistor saturation and converter coil resistance, the voltage between pins 7 and 9 begins to attenuate, causing T21 and T22 to be cut off all at once because of the reverse playback action.

Until immediately before the transistor is cut off, excitation current flows to the transformer.

Because the current is suddenly dropped as a result of the transistor cut-off, a counter voltage is generated, the distributed capacity of the coil is charged, and, as a result, an oscillation voltage is generated at the base coil.

Then, when the base potential progresses to a half cycle of the oscillation voltage, it is biased in the forward direction, T21 and T22 are switched ON once again, and oscillation such as that shown in Fig. 4-38 occurs.

In this way, AC voltage corresponding to the number of windings is generated at the secondary side of the converter, and this voltage is rectified and smoothed by D13, D15, C84 and C85.

Moreover, the voltage fluctuations of VDD (+5V) are fed back to the primary side of the oscillation transistor by T13, D4, R121 and C92 to improve stability. C81 and R126 are a differentiation circuit designed to make the playback operation of the oscillation transistor easier. AC short circuits the circuit, so that the oscillation frequency is affected by the time-constant of this C and R. Because feedback is applied by VDD, which makes stability difficult, VEE (−5V) is stabilized by R97 and D14. (The voltage at both each of C85 is about −7V.)

(2) Low-Power Detection and Automatic Power OFF Circuitry

The low-power detection circuit illuminates an LED warning lamp when the battery voltage decreases. If it continues decreasing, the system power will be switched OFF just before the voltage becomes so low that the converter cannot operate.

There are about 20 minutes between the time when the LED lamp illuminates and the system is switched OFF (if no I/O devices are connected).

Battery voltage is detected by splitting the resistance of R144, R108, R105 and R116. When battery voltage (VL) becomes 4.1V ± 0.1V, T16 is switched OFF, T17 is switched ON, T19 is driven, and the LED illuminates. (The LED is located on the LCD PCB.)

When VL becomes 3.7V ± 0.1V, T14 is switched OFF, T15 is switched ON, and LPS changes from "H" to "L". This signal is inverted by M27, and fed to the TRAP terminal of 80C85. If the CPU acknowledges this signal, it sends the P.C.S. signal which passes through the PB4 of 81C55 after the internal operations.

The P.C.S. signal is active "H".

When P.C.S. becomes "H", the Q output of M28 (4013: "D" type F/F) becomes "H", T20 operates, and the oscillation of the converter is stopped.

If there is no operation for 10 minutes or more (awaiting a command for 10 minutes or more), P.C.S. is output from PB4 of 81C55.

When the power switch is switched OFF, T18 is switched OFF, the M28 RESET terminal becomes "H" and oscillation is resumed by switching the power switch ON. If, however, the power is reduced by the L.P.S. signal, battery replacement is necessary. R123 and R112 are resistors to provide hysteresis.

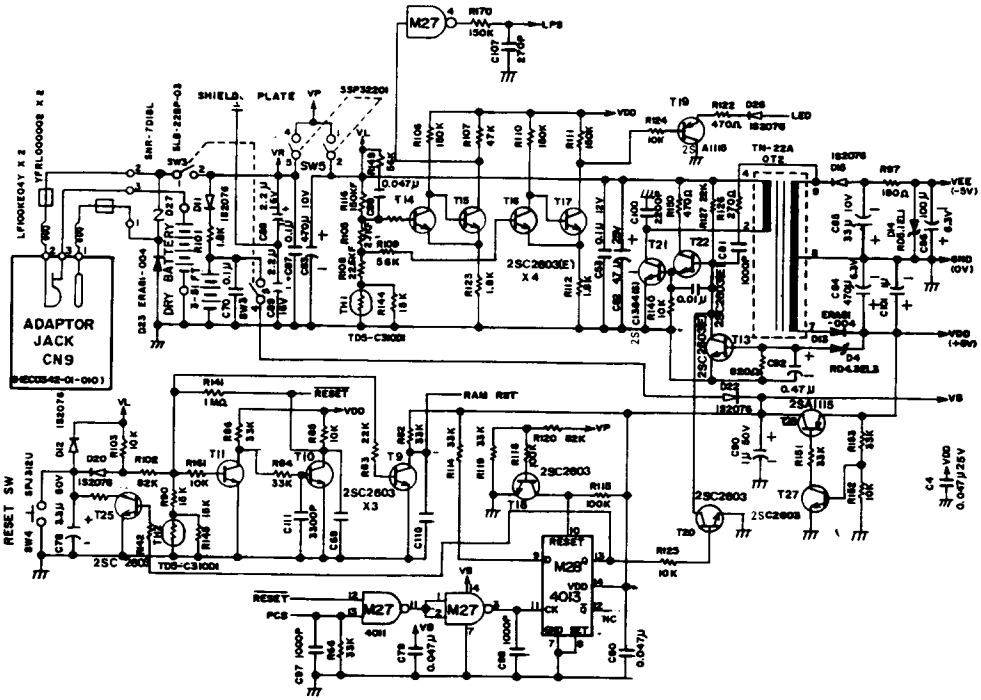


Fig. 4-37 Power Supply and Reset Circuit

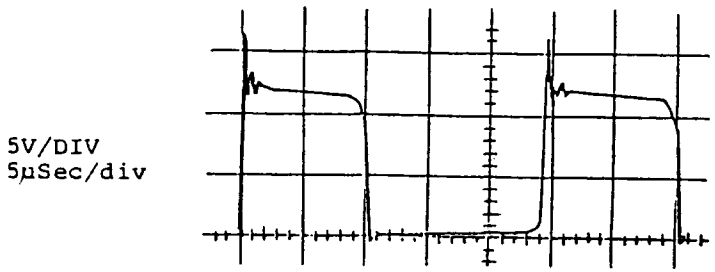


Fig. 4-38 Oscillation Waveform

RESET CIRCUIT

This circuit supplies the CPU $\overline{\text{RESET}}$ signal and also the RAM RST signal as the RAM protecting signal when the power decreases.

The circuit diagram is shown in Fig. 4-37.

R103 and C78 delay the introduction of input power so that T11 is switched ON and T10 is switched OFF about 20 sec. after VDD is activated, with the result that the $\overline{\text{RESET}}$ signal changes from "L" to "H".

In the same way, RAM RST signal is generated by T9 and changes from "H" to "L".

R141 provides hysteresis to the $\overline{\text{RESET}}$ signal.

Thermistor TH2 suppresses $\overline{\text{RESET}}$ signal fluctuations due to temperature.

T25 receives the signal during automatic power OFF, short-circuiting both ends of C78, and resets the system.

The $\overline{\text{RESET}}$ signal is active "L", and RAM RST signal is active "H".

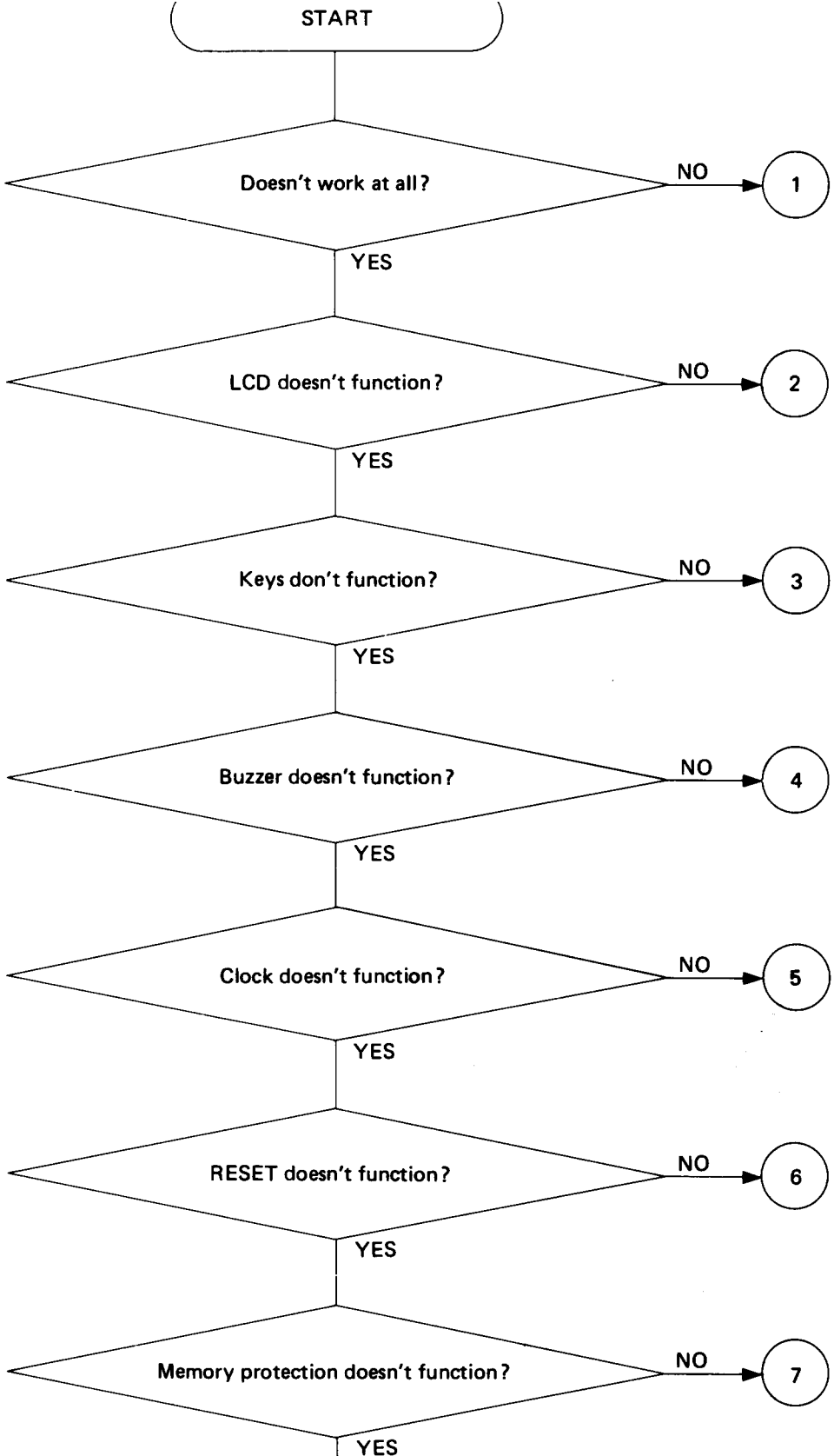
SECTION V

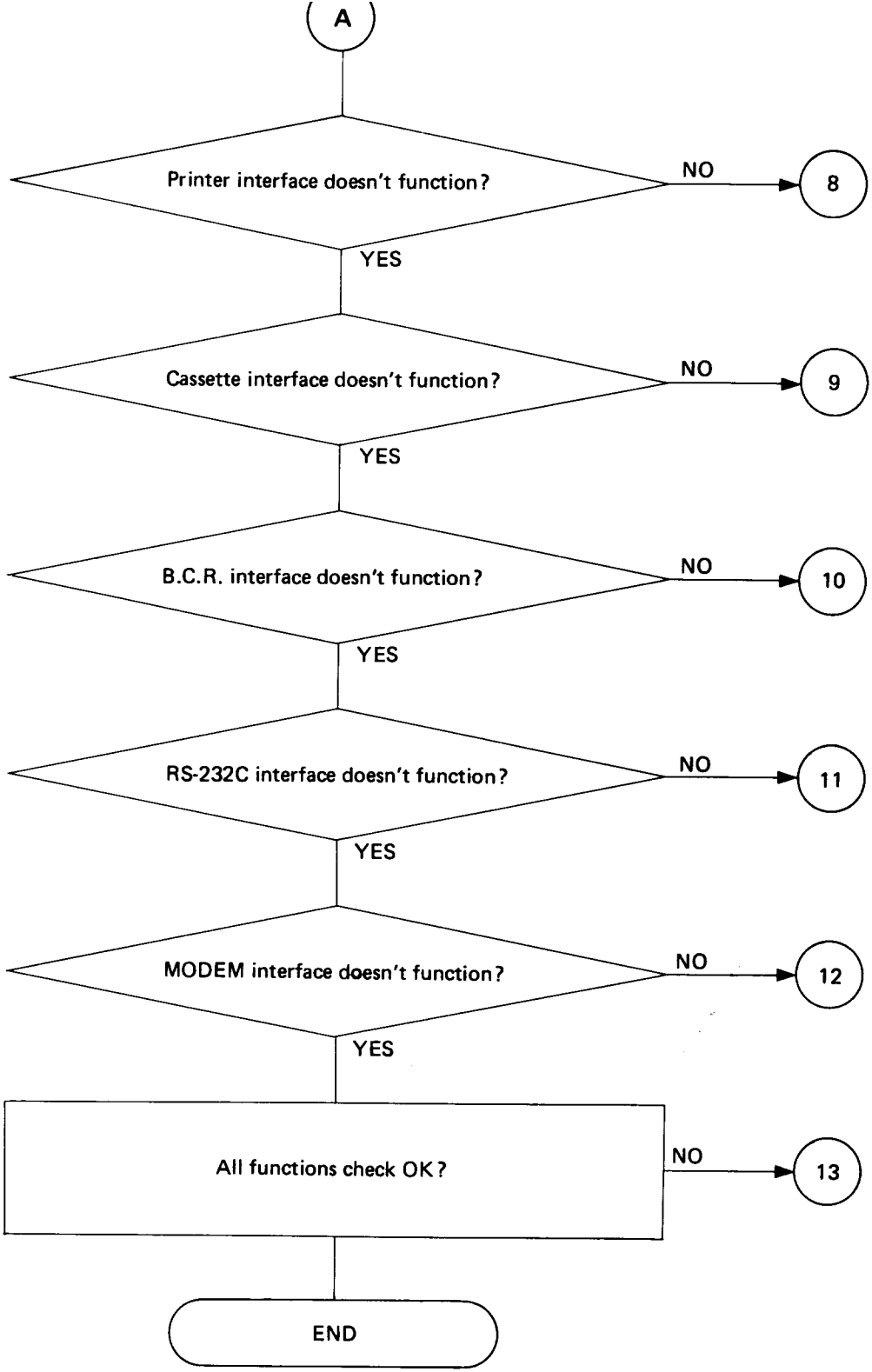
TROUBLESHOOTING

HOW TO MAKE USE OF THIS SECTION

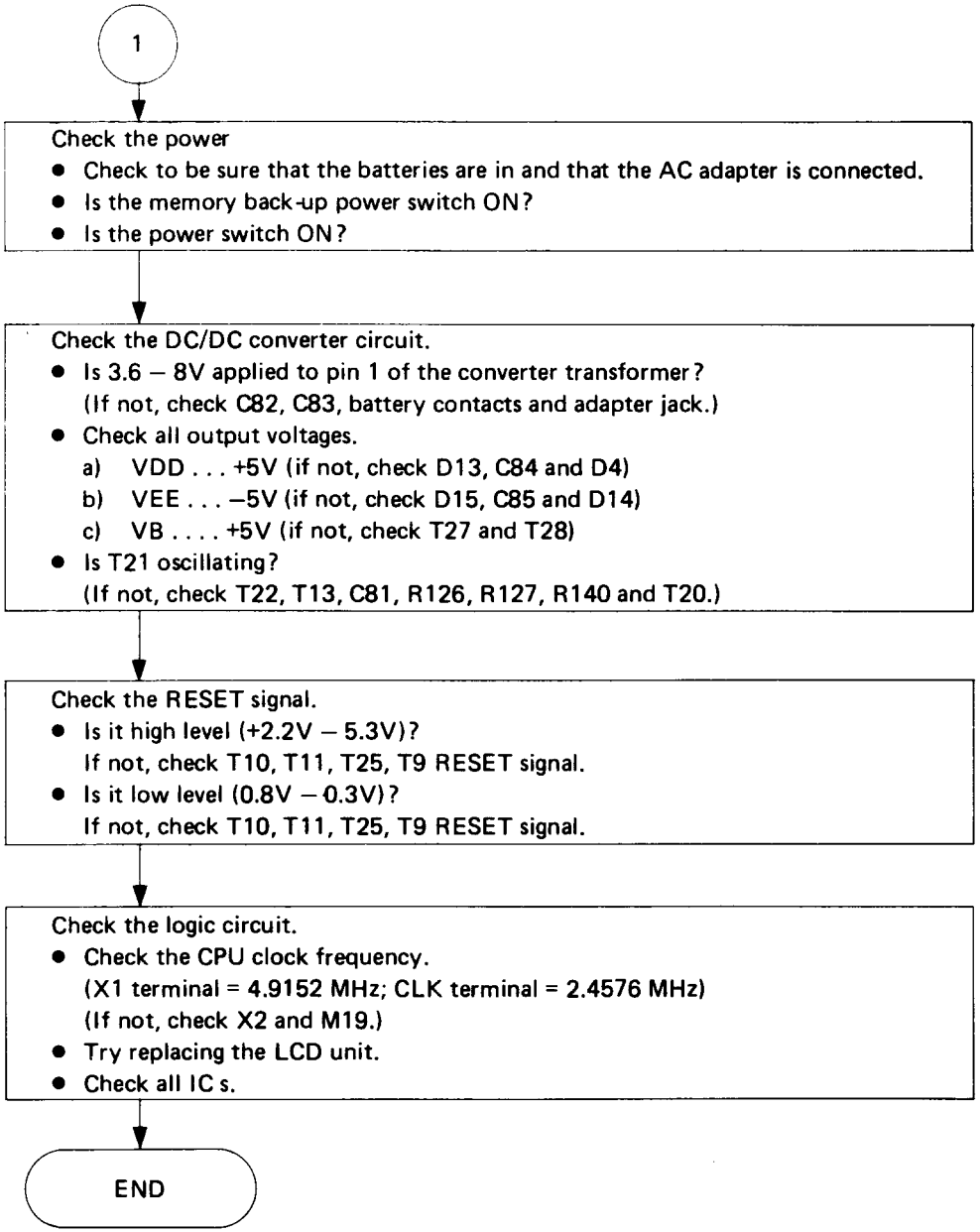
This section shows you how to go about solving a problem or malfunction that has been identified. All you have to do, is find the problem in the Troubleshooting Flowchart and refer to the section indicated by the number. Each section then identifies the components associated with the circuit in question and provides remedial instructions.

After completing any repairs, you should re-check each functional item according to the CHECK LIST. You can make use of the CHECK LIST even if the location and condition of the malfunction are not readily clear.

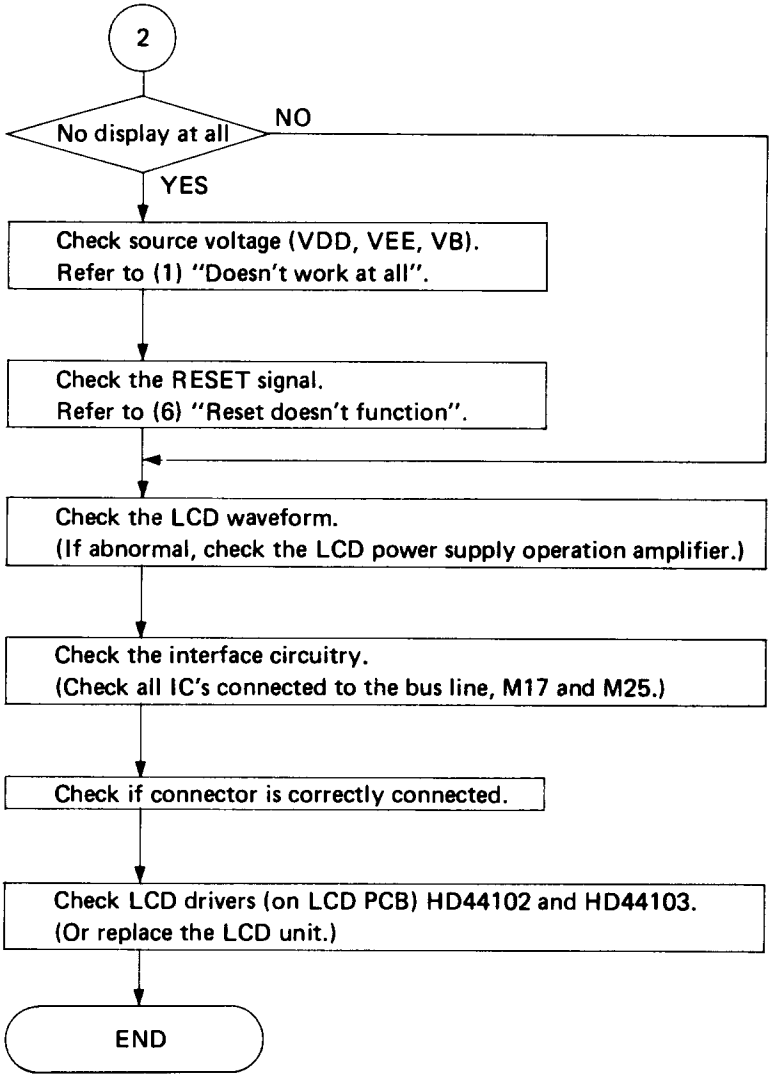

START
Doesn't work at all?
NO
1
YES
LCD doesn't function?
NO
2
YES
Keys don't function?
NO
3
YES
Buzzer doesn't function?
NO
4
YES
Clock doesn't function?
NO
5
YES
RESET doesn't function?
NO
6
YES
Memory protection doesn't function?
NO
7
YES


A
Printer interface doesn't function?
NO
8
YES
Cassette interface doesn't function?
NO
9
YES
B.C.R. interface doesn't function?
NO
10
YES
RS-232C interface doesn't function?
NO
11
YES
MODEM interface doesn't function?
NO
12
YES
All functions check OK?
NO
13
END

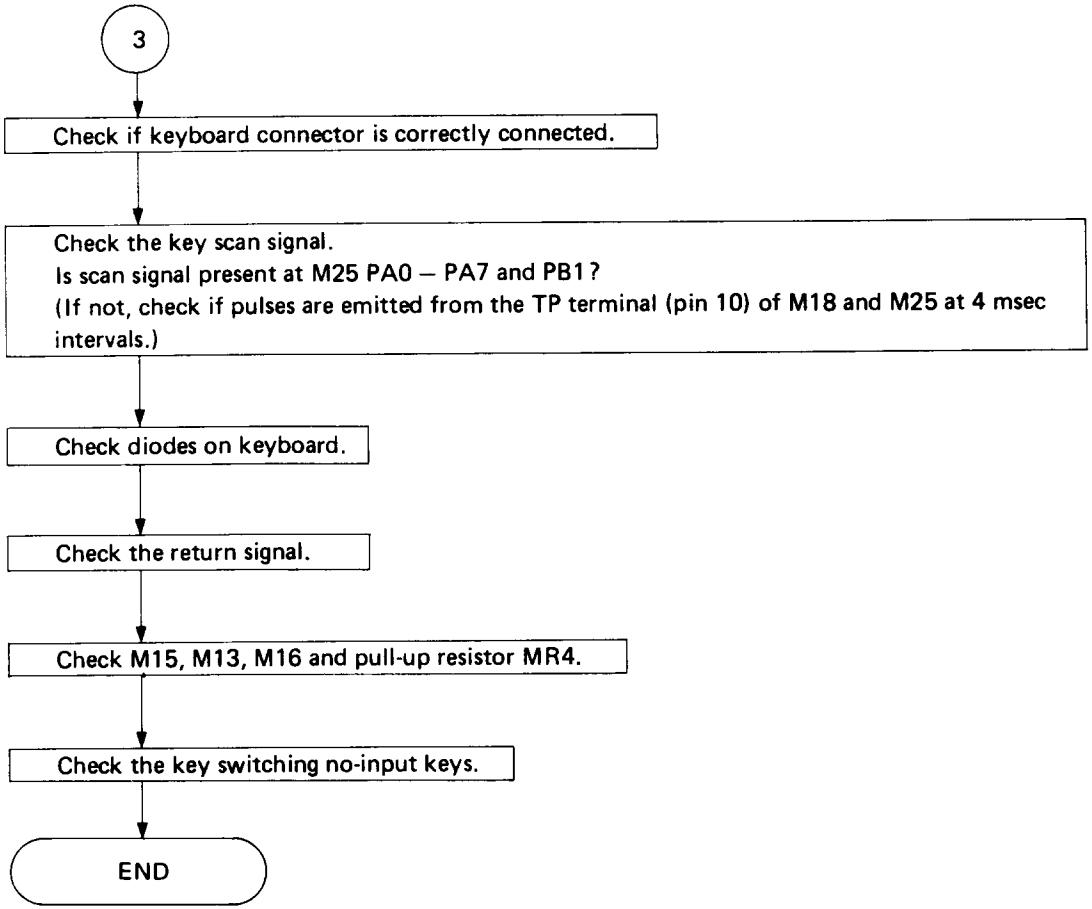
1. Doesn't work at all



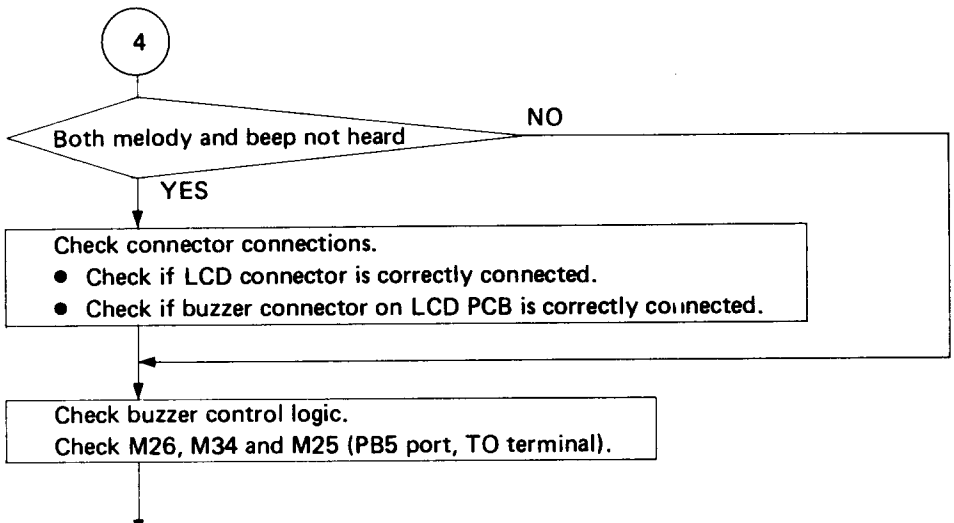
2. LCD doesn't function



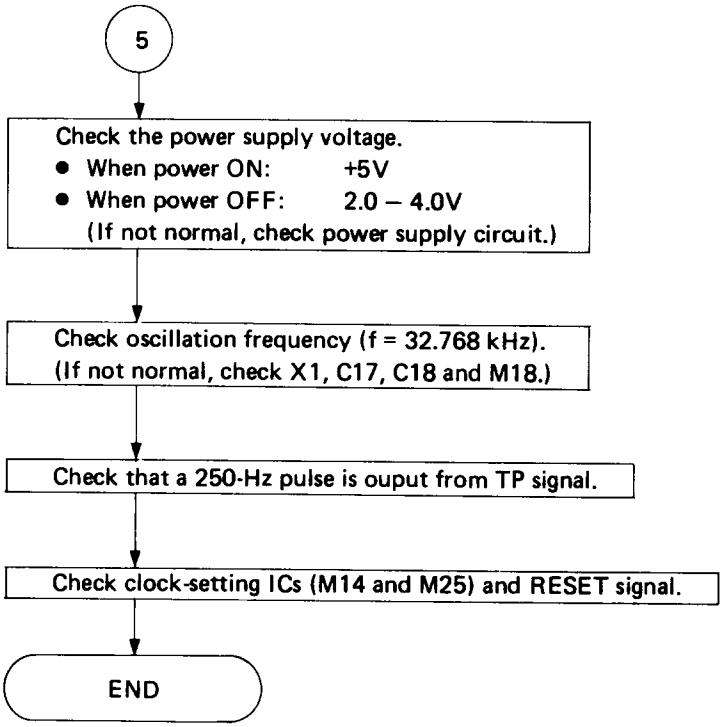
3. Key don't function



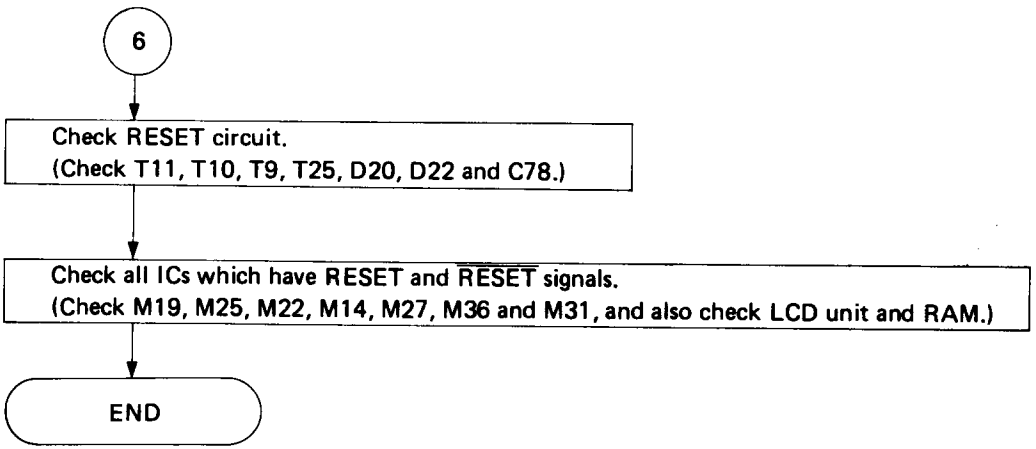
4. Buzzer doesn't function



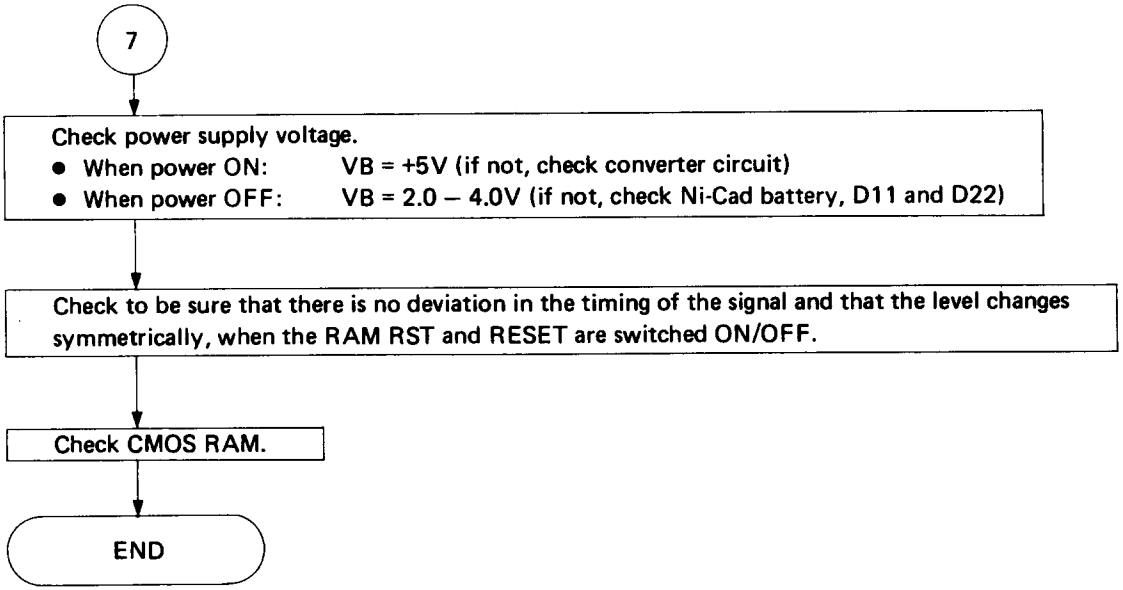
5. Clock doesn't function



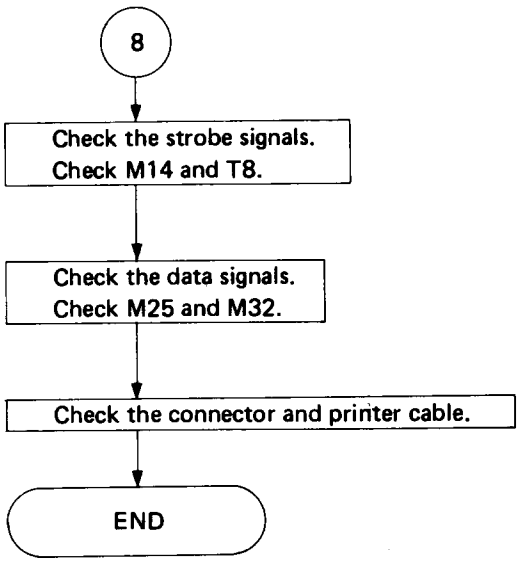
6. Reset doesn't function



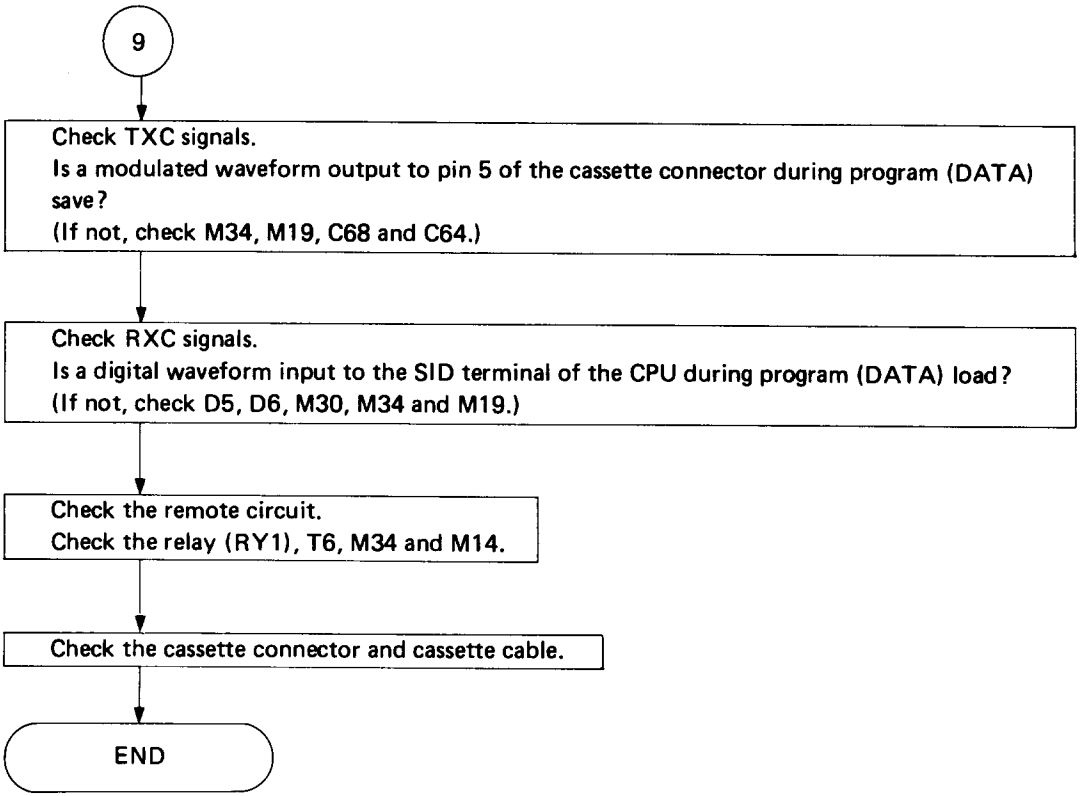
7. Memory protection doesn't function



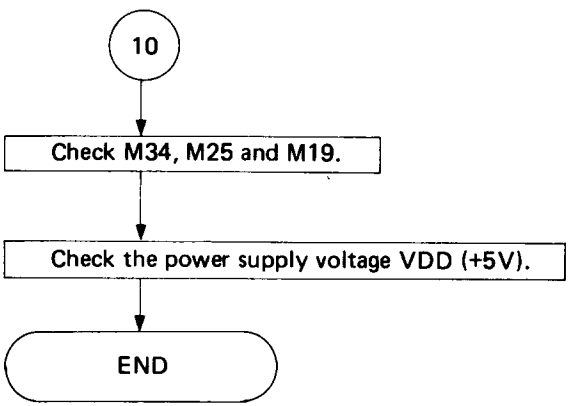
8. Printer interface doesn't function



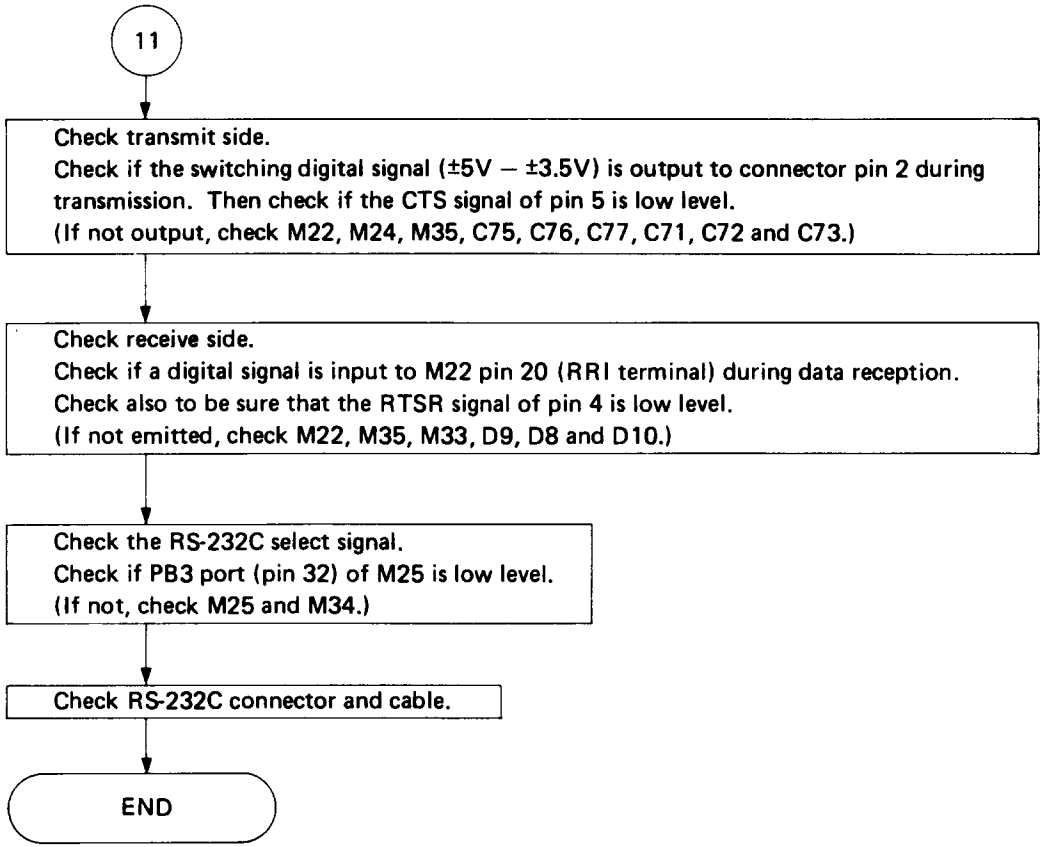
9. Cassette interface doesn't function



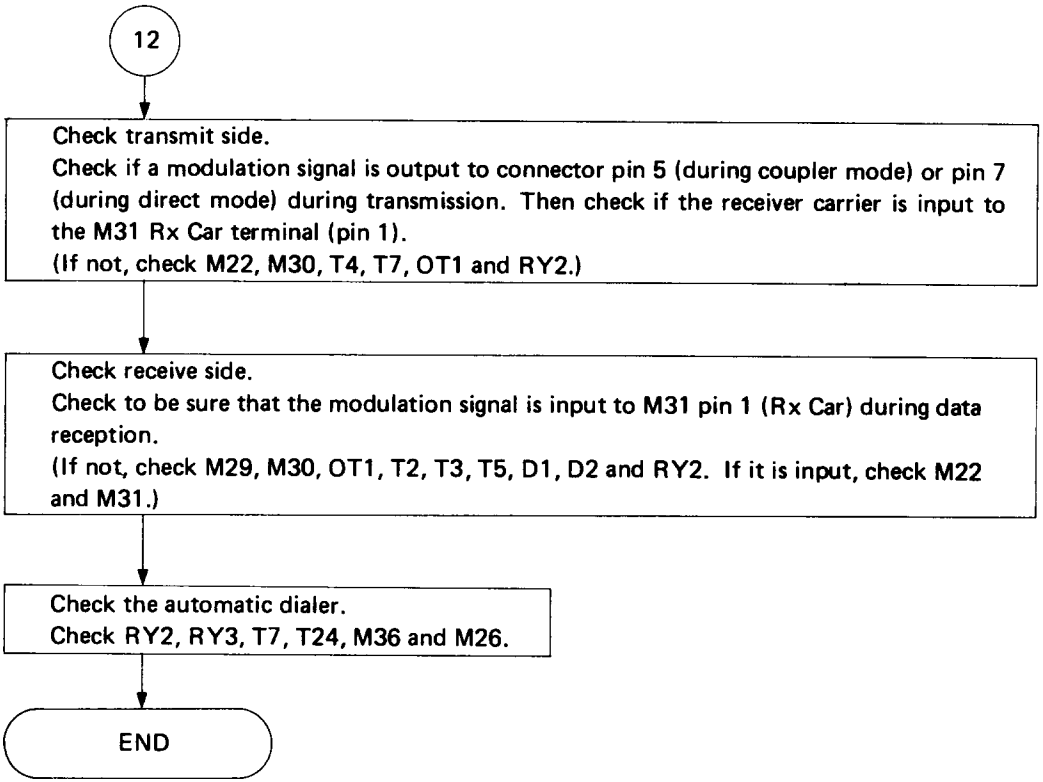
10. B.C.R. interface doesn't function



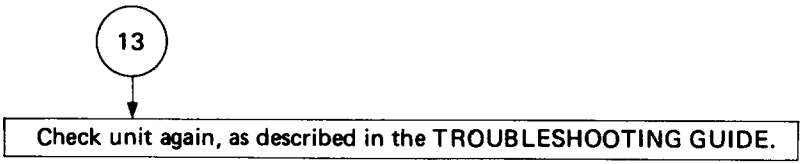
11. RS-232C interface doesn't function



12. Modem interface doesn't function



13. All functions check ok?



After completing any repairs or adjustments, check all functions with the following procedures TEST PROGRAM. Before beginning, however, perform a cold start (See procedure 4).

(1) Buzzer and LCD check (in BASIC mode)

```
20 FOR I = 0 TO 255
20 PRINT CHR$ (I)
30 NEXT I
40 END
```

Operation

After 1 beep the LCD display clears and then, all printable characters are displayed.

(2) Clock test (in BASIC mode)

(a) Setting the year, month, date, day, hour, minute and second

Year, month, date setting: DATE = "MM/DD/YY"

Day setting: DAY = "day" (example: Sundary = Sun)

Hour, minute, second setting: TIME = "HH:MM:SS"

(b) Confirmation of set data

Return to the Main Menu with the MENU command and verify that the calendar has changed to the desired settings.

(3) Keyboard test

Refer to key functions in the Owner's Manual, and check that all functions work.

(4) Reset function test (memory protection test)

(a) Warm start

Turn the Computer OFF and then ON, or, with the POWER switch ON, press RESET (on the rear). Check that all User files are displayed.

(b) Cold start

While pressing the CTRL and PAUSE keys, press the RESET switch and check that all previously created user files are erased and that the date and time are initialized.

(5) Printer interface test (in BASIC mode)

Input the characters to be printed out on the LCD display, and then, when the hard copy key PRINT is pressed, the displayed characters will all be printed out.

(6) Cassette interface test (in BASIC mode)

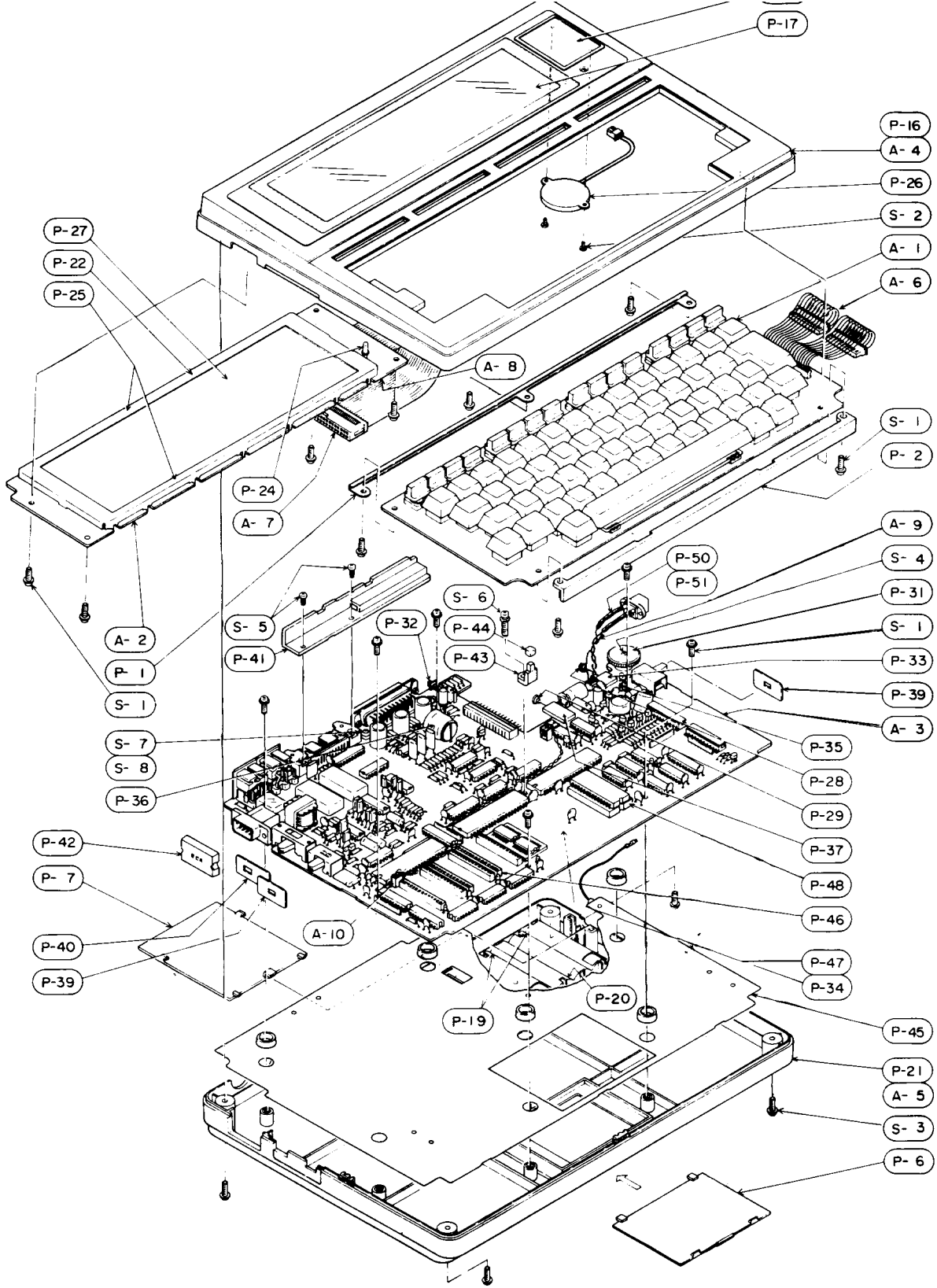
Type a three or four line program and then save it on tape using the CSAVE file name command. Then load the program with the CLOAD file name command and verify that the program was sowed accurately.

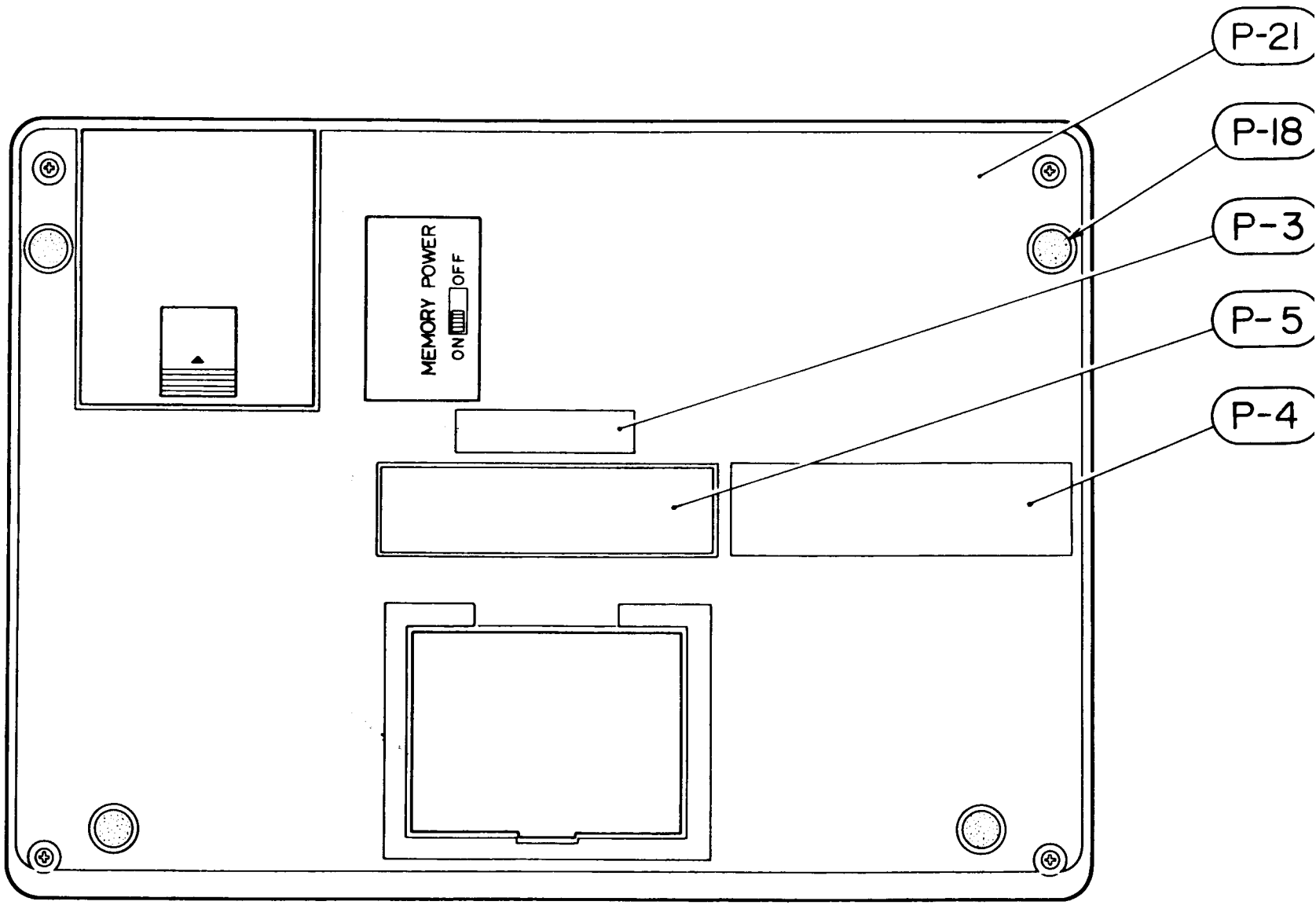
(7) RS-232C and Modem Tests

Prepare two units to transmit and receive data first through the RS-232C Interface, and then through the Modem. See the Owner's Manual for details.

SECTION VI

EXPLODED VIEW AND PARTS LIST


P-17
P-16
A- 4
P-26
S- 2
A- 1
A- 6
P-27
P-22
P-25
A- 8
S- 1
P- 2
P-24
A- 7
A- 9
P-50
P-51
S- 4
P-31
S- 6
P-44
S- 5
P-32
P-41
P-43
S- 1
P-33
A- 2
P- 1
S- 1
P-39
A- 3
S- 7
S- 8
P-36
P-35
P-28
P-29
P-37
P-42
P- 7
P-48
P-46
A-10
P-40
P-39
P-47
P-34
P-20
P-19
P-45
P-21
A- 5
S- 3
P- 6


P-21
P-18
P-3
P-5
P-4
MEMORY POWER
ON
OFF

CAPACITORS

C1	CAPACITOR, CERAMIC 0.047μF/25V/+-10%	ACC-473KFCP	CBF1E473KM
C2			
C3			
C4	CAPACITOR, CERAMIC 0.047μF/25V/+-10%	ACC-473KFCP	CBF1E473KM
C5	CAPACITOR, TANTALUM 1μF/10V/+-20%	ACC-105MCTP	CSSC010MDC
C6			
C7			
C8	CAPACITOR, TANTALUM 1μF/10V/+-20%	ACC-105MCTP	CSSC010MDC
C9	CAPACITOR, CERAMIC 0.1μF/16V/+-20%		CBF1B104MY
C10			
C11	CAPACITOR, CERAMIC 0.1μF/16V/+-20%		CBF1B104MY
C12	CAPACITOR, CERAMIC 0.047μF/25V/+-10%	ACC-473KFCP	CBF1E473KM
C13			
C14			
C15			
C16	CAPACITOR, CERAMIC 0.047μF/25V/+-10%	ACC-473KFCP	CBF1E473KM
C17	CAPACITOR, CERAMIC 20PF/50V/+-10%	ACC-200KJCP	CCFB200KCT
C18	CAPACITOR, CERAMIC 20PF/50V/+-10%	ACC-200KJCP	CCFB200KCT
C19	CAPACITOR, CERAMIC 0.047μF/25V/+-10%	ACC-473KFCP	CBF1E473KM
C20	CAPACITOR, CERAMIC 82PF/50V/+-10%	ACC-820KJCP	CCFB820K0T
C21			
C22			
C23			
C24			
C25			
C26			
C27	CAPACITOR, CERAMIC 82PF/50V/+-10%	ACC-820KJCP	CCFB820K0T
C28	CAPACITOR, CERAMIC 0.047μF/25V/+-10%	ACC-473KFCP	CBF1E473KM
C29	CAPACITOR, CERAMIC 10PF/50V/+-0.5%		CCFB100DCT
C30	CAPACITOR, CERAMIC 10PF/50V/+-0.5%		CCFB100DCT
C31	CAPACITOR, TANTALUM 1μF/10V/+-20%	ACC-105MCTP	CSSC010MDC
C32	CAPACITOR, CERAMIC 0.047μF/25V/+-10%	ACC-473KFCP	CBF1E473KM
C33			
C34			
C35	CAPACITOR, CERAMIC 0.047μF/25V/+-10%	ACC-473KFCP	CBF1E473KM
C36	CAPACITOR, CERAMIC 0.1μF/16V/+-20%		CBF1B104MY
C37	CAPACITOR, CERAMIC 0.1μF/16V/+-20%		CBF1B104MY
C38	CAPACITOR, CERAMIC 100PF/50V/+-5%		CCFB101JLT
C39	CAPACITOR, CERAMIC 0.047μF/25V/+-10%	ACC-473KFCP	CBF1E473KM
C40	CAPACITOR, MYLAR 0.047μF/50V/+-5%	ACC-473JJMP	CQMB473JTH
C41	CAPACITOR, POLY FILM 4700PF/100V/+-1%		CQPC472FEN
C42			
C43			
C44			
C45			
C46	CAPACITOR, POLY FILM 4700PF/100V/+-1%		CQPC472FEN
C47	CAPACITOR, CERAMIC 0.1μF/16V/+-20%		CBF1B104MY
C48	CAPACITOR, CERAMIC 0.1μF/16V/+-20%		CBF1B104MY
C49	CAPACITOR, ELEC. 10μF/16V/+-20%		CEAD100ADN
C50	CAPACITOR, ELEC. 10μF/16V/+-20%		CEAD100ADN
C52	CAPACITOR, ELEC. 1μF/50V/+75-10%		CEAG010NLN
C53	CAPACITOR, CERAMIC 0.1μF/16V/+-20%		CBF1B104MY

C60	CAPACITOR, MYLAR 3300PF/50V/+-5%	ACC-332JJMP	CQMB332JTH
C61	CAPACITOR, MYLAR 4700PF/50V/+-5%	ACC-472JJMP	CQMB472JTH
C62	CAPACITOR, CERAMIC 10000PF/50V/+100-0%		CKFB103PEM
C63	CAPACITOR, MYLAR 0.1μF/50V/+-10%		CQMB104KTH
C64	CAPACITOR, MYLAR 0.047μF/50V/+-10%		CQMB473KTH
C65	CAPACITOR, CERAMIC 0.047μF/25V/+-10%	ACC-473KFCP	CBF1E473KM
C66	↓	↓	↓
C67	CAPACITOR, CERAMIC 0.047μF/25V/+-10%	ACC-473KFCP	CBF1E473KM
C69	CAPACITOR, CERAMIC 1000PF/50V/+-10%		CKFB102KBT
C70	CAPACITOR, CERAMIC 0.1μF/16V/+-20%		CBF1B104MY
C71	CAPACITOR, MYLAR 0.039μF/50V/+-10%		CQMB393KTH
C72	↓		↓
C73	CAPACITOR, MYLAR 0.039μF/50V/+-10%		CQMB393KTH
C74	CAPACITOR, CERAMIC 0.047μF/25V/+-10%	ACC-473KFCP	CBFIE473KM
C75	CAPACITOR, ELEC. 47μF/16V/+-20%		CEAD470NLX
C76	↓		↓
C77	CAPACITOR, ELEC. 47μF/16V/+-20%		CEAD470NLX
C78	CAPACITOR, ELEC. 3.3μF/50V/+-75-10%	ACC-335XJAP	CEVG3R3ALN
C79	CAPACITOR, CERAMIC 0.047μF/25V/+-10%	ACC-473KFCP	CBF1E473KM
C80	CAPACITOR, CERAMIC 0.047μF/25V/+-10%	ACC-473KFCP	CBF1E473KM
C81	CAPACITOR, CERAMIC 1000PF/50V/+80-20%	ACC-102ZJCP	CKFB102ZFN
C82	CAPACITOR, ELEC. 4.7μF/25V/+-20%		CEAE4R7ADN
C83	CAPACITOR, ELEC. 470μF/10V/+30-10%	ACC-477RCAP	CEAC471ACX
C84	CAPACITOR, ELEC. 470μF/6.3V/+30-10%	ACC-477RBAP	CEAB471ACX
C85	CAPACITOR, ELEC. 33μF/10V/+-20%	ACC-336MCAP	CEAC330ADN
C86	CAPACITOR, ELEC. 100μF/6.3V/+75-10%	ACC-107XBAP	CEAB101ALN
C87	CAPACITOR, CERAMIC 0.1μF/16V/+-20%		CBF1B104MY
C88	CAPACITOR, TANTALUM 2.2μF/16V/+-20%	ACC-225MDTP	CSSD2R2MDC
C89	CAPACITOR, TANTALUM 2.2μF/16V/+-20%	ACC-225MDTP	CSSD2R2MDC
C90	CAPACITOR, ELEC. 1μF/50V/+-20%		CEAG010ADN
C91	CAPACITOR, CERAMIC 0.047μF/25V/+-10%	ACC-473KFCP	CBF1E473KM
C92	CAPACITOR, ELEC. 0.47μF/50V/+75-10%	ACC-474XJAP	CEAGR47ALN
C94	CAPACITOR, CERAMIC 8200PF/50V/+-10%	ACC-822KJCP	CKFB822KBT
C97	CAPACITOR, CERAMIC 1000PF/50V/+-10%		CKFB102KBT
C98	CAPACITOR, CERAMIC 1000PF/50V/+-10%		CKFB102KBT
C99	CAPACITOR, CERAMIC 0.047μF/25V/+-10%	ACC-473KFCP	CBF1E473KM
C100	CAPACITOR, CERAMIC 2200PF/50V/+-10%		CKFB222KBT
C101	CAPACITOR, TANTLUM 1μF/10V/+-20%	ACC-105MCTP	CSSC010MDC
C102	CAPACITOR, CERAMIC 100PF/50V/+-10%		CCFB101K0T
C103	CAPACITOR, ELEC. 220μF/10V/+30-10%	ACC-227RCAP	CEAC221ACX
C104	CAPACITOR, CERAMIC 10000PF/50V/+100-0%		CKFB103PEM
C105	CAPACITOR, TANTALUM 0.15μF/16V/+-20%	ACC-154MDTP	CSSDR15MDC
C106	CAPACITOR, TANTALUM 0.15μF/16V/+-20%	ACC-154MDTP	CSSDR15MDC
C107	CAPACITOR, CERAMIC 270PF/50V/+-10%	ACC-271KJCP	CCFB271K0T
C108	CAPACITOR, MYLAR 5600PF/50V/+-10%	ACC-562KJMP	CQMB562KTH
C109	CAPACITOR, CERAMIC 68PF/50V/+-10%		CCFB680K0T
C110	CAPACITOR, CERAMIC 1000PF/50V/+-10%		CKFB102KBT
C111	CAPACITOR, CERAMIC 3300PF/50V/+-10%		CBF1H332KT

CONNECTORS			
CN1	JACK, JUNCTION - KEYBOARD 5268-10A	AJ-7343	YJF10S050Z
CN2	JACK, JUNCTION - BCR CP-P26-09-30-134	AJ-7342	YJF09S045Z
CN3	JACK, JUNCTION - CMT TCS4480-01-1011	AJ-7340	YJF08S033Z
CN4	JACK, JUNCTION MODEM TCS4490-01-1111	AJ-7341	YJF08S034Z
CN5	JACK, JUNCTION PRINTER FRC2-C26-L13 ON	AJ-7345	YJF26S010Z
CN6	JACK, JUNCTION RS-232C	AJ-7344	YJF25S012Z
CN7	JACK, JUNCTION - LCD HU-30P-2G-L13	AJ-7346	YJF30S006Z
CN8	JACK, JUNCTION - LED LINE	AJ-7322	YJF02S041Z
CN9	JACK, HECO342-01-010	AJ-7338	YJB03S001Z
DIODES			
D1	DIODE, SILICON 1S2076		QDSS2076#B
D2	DIODE, SILICON 1S2076		QDSS2076#B
D4	DIODE, SILICON, ZENER, NEC RD4.3 EL3	ADX-1860	QDZ4R3EL3A
D5	DIODE, SILICON 1S2076		QDSS2076#B
D6	↓		↓
D7	↓		↓
D8	↓		↓
D9	↓		↓
D10	↓		↓
D11	↓		↓
D12	DIODE, SILICON 1S2076		QDSS2076#B
D13	DIODE, SILICON ERA81-004	ADX-1859	QDS81004XZ
D14	DIODE, SILICON, ZENER NEC RD5.1 EL1	ADX-1861	QDZ5R1EL1A
D15	DIODE, SILICON 1S2076		QDSS2076#B
D16	↓		↓
D17	DIODE, SILICON 1S2076		QDSS2076#B
D18	SURGE ABSORBER ERZ-C10DK361	ADX-1864	QNHDK361AN
D20	DIODE, SILICON 1S2076		QDSS2076#B
D21	↓		↓
D22	DIODE, SILICON 1S2076		QDSS2076#B
D23	DIODE, SILICON ERA81-004	ADX-1859	QDS81004XZ
D24	SURGE ABSORBER ERZ-C10K220 250A	ADX-1863	QNDDK220AN
D27	SURGE ABSORBER SNR-7D18L	ADX-1862	QNB7D18LAD
D28	DIODE, SILICON 1S2076		QDSS2076#B
D29	DIODE, SILICON 1S2076		QDSS2076#B

M1	I.C.,HI-SPEED C-MOS,OR GATE,TC40H373P	AMX-5820	QQ040373AT
M2	I.C.,HI-SPEED C-MOS,BUFFER,TC40H245P	AMX-5818	QQ040245AT
M3	I.C.,HI-SPEED C-MOS,DECODER,TC40H138P	AMX-5813	QQ040138AT
M4	I.C.,HI-SPEED C-MOS,DECODER,TC40H138P	AMX-5813	QQ040138AT
M5	I.C.,HI-SPEED C-MOS,DECODER,TC40H139P	AMX-5814	QQ040139AT
*M6	ASSEMBLY, RAM PACKAGE I.C. TC5518BF X 4	AMX-5799	QQHX1001A6
*M7	OR HM6117LFP-4 X 4		QQHX1002A6
*M8			
*M9			
M12	I.C.,C-MOS,MASKED ROM,LH535618	AMX-5821	QQ05356183
M13	I.C.,HI-SPEED C-MOS,OR GATE,TC40H032P	AMX-5812	QQ040032AT
M14	I.C.,HI-SPEED C-MOS,FLIP FLOP,TC40H175P	AMX-5816	QQ040175AT
M15	I.C.,HI-SPEED C-MOS,BUFFER,TC40H244P	AMX-5817	QQ040244AT
M16	I.C.,HI-SPEED C-MOS,DECODER,TC40H138P	AMX-5813	QQ040138AT
M17	I.C.,HI-SPEED C-MOS,NAND GATE,TC40H000P	AMX-5810	QQ040000AT
M18	I.C.,C-MOS,TIMER,D1990AC	AMX-5801	QQ001990BA
M19	I.C.,C-MOS,CPU,MSM80C85ARS	AMX-5806	QQ008085A5
M20	I.C.,HI-SPEED C-MOS,BUFFER,TC40H367P	AMX-5819	QQ040367AT
M21	I.C.,HI-SPEED C-MOS,BUFFER,TC40H244P	AMX-5817	QQ040244AT
M22	I.C.,C-MOS,UART,D3-6402-9	AMX-5805	QQ006402AZ
M23	I.C.,HI-SPEED C-MOS,BUFFER,TC40H244P	AMX-5817	QQ040244AT
M24	I.C.,HI-SPEED C-MOS,OR GATE,TC40H032P	AMX-5812	QQ040032AT
M25	I.C.,C-MOS,PI/O,MSM81C55RS	AMX-5807	QQ008155A5
M26	I.C.,HI-SPEED C-MOS,NOR GATE,TC40H002P	AMX-5811	QQ040002AT
M27	I.C.,C-MOS,NAND GATE,MN4011B OR	AMX-5802	QQ004011AN
M27	I.C.,C-MOS,NAND GATE,D4011C		QQ004011AA
M28	I.C.,C-MOS,D-FLIP FLOP,MN4013B OR	AMX-5804	QQ004013AN
M28	I.C.,C-MOS,D-FLIP FLOP,D4013C		QQ004013AA
M29	I.C.,BIPOLAR,OP AMP,TL064CN	AMX-5800	QQM00064AU
M30	I.C.,BIPOLAR,OP AMP,TL064CN	AMX-5800	QQM00064AU
M31	I.C.,C-MOS,MODEM,MC14412VP	AMX-5808	QQ014412AM
M32	I.C.,HI-SPEED C-MOS,BUFFER,TC40H244P	AMX-5817	QQ040244AT
M33	I.C.,HI-SPEED C-MOS,SELECTOR,TC40H157P	AMX-5815	QQ040157AT
M34	I.C.,C-MOS,SCHMITT TRIGGER,HD14584BP	AMX-5809	QQ014584AB
M35	I.C.,C-MOS,SCHMITT TRIGGER,HD14584BP	AMX-5809	QQ014584AB
M36	I.C.,C-MOS,D-FLIP FLOP,MN4013B OR	AMX-5804	QQ004013AN
M36.	I.C.,C-MOS,D-FLIP FLOP,D4013C		QQ004013AA
**P-38	I.C.,C-MOS,RAM,TC5518BF-25 OR	AMX-5839	QQ005518AT
**P-38	I.C.,C-MOS,RAM,HM6117LFP-4		QQ006117BB

* 26-3801 is installed on M9.
* 26-3802 is installed on M9, M8 and M7.

** P-38 is mounted on the RAM package I.C.

Ref. No.	Description	RS Part No.	Mfr's Part No.
RESISTOR ARRAYS			
MR1	RESISTOR ARRAY 100K X 8 1/8W/+-20%		RAB104M08X
MR2	RESISTOR ARRAY 100K X 8 1/8W/+-20%		RAB104M08X
MR3	RESISTOR ARRAY 33K X 8 1/8W/+-20%		RAB333M08X
MR4	RESISTOR ARRAY 33K X 8 1/8W/+-20%		RAB333M08X
MR5	RESISTOR ARRAY 100K X 8 1/8W/+-20%		RAB104M08X
MR6			

OT1	TRANSFORMER, DRIVER E6732B AC1000V	ATB-0472	TDZ19A002K
OT2	TRANSFORMER, CONVERTOR TN22A	ATB-0471	TC12RZ001B
RESISTORS			
R1	RES. CARBON 1K OHM/1/4W/+-5%		RD25PJ102X
R2	RES. CARBON 33K OHM/1/4W/+-5%		RD25PJ333X
R3	↓		↓
R4			
R5			
R6			
R7	RES. CARBON 33K OHM/1/4W/+-5%		RD25PJ333X
R8	RES. CARBON 1K OHM/1/4W/+-5%		RD25PJ102X
R9	↓		↓
R10			
R11			
R12	RES. CARBON 1K OHM/1/4W/+-5%		RD25PJ102X
R13	RES. METAL FILM 806 OHM/1/4W/+-1%	AN-0577BEC	RQBPF8060X
R14	RES. CARBON 10K OHM/1/4W/+-5%		RD25PJ103X
R15	RES. METAL FILM 33.2K OHM/1/4W/+-1%	AN-0622BEC	RQBPF3322X
R16	RES. METAL FILM 2.05K OHM/1/4W/+-1%	AN-0716BEC	RQBPF2051X
R17	RES. METAL FILM 73.2K OHM/1/4W/+-1%	AN-0612BEC	RQBPF7322X
R18	RES. METAL FILM 590K OHM/1/4W/+-1%	AN-0615BEC	RQBPF5903X
R19	RES. CARBON 15K OHM/1/4W/+-5%		RD25PJ153X
R20	RES. CARBON 470K/1/4W/+-5%		RD25PJ474X
R21	RES. CARBON 620 OHM/1/4W/+-5%		RD25PJ621X
R22	RES. CARBON 390 OHM/1/4W/+-5%		RD25PJ391X
R23	RES. CARBON 10K OHM/1/4W/+-5%		RD25PJ103X
R24	RES. METAL FILM 665 OHM/1/4W/+-1%		RQBPF6650X
R25	RES. METAL FILM 1.5K OHM/1/4W/+-1%	AN-0206BEC	RQBPF1501X
R26	RES. CARBON 10K OHM/1/4W/+-5%		RD25PJ103X
R27	RES. METAL FILM 1.30K OHM/1/4W/+-1%		RQBPF1301X
R28	RES. METAL FILM 3.3K OHM/1/4W/+-1%	AN-0230BEC	RQBPF3301X
R29	RES. METAL FILM 280K OHM/1/4W/+-1%	AN-0672BEC	RQBPF2803X
R30	RES. METAL FILM 422K OHM/1/4W/+-1%	AN-0419BEC	RQBPF4223X
R31	RES. CARBON 2.2K OHM/1/4W/+-5%		RD25PJ222X
R32	RES. CARBON 22 OHM/1/4W/+-5%		RD25PJ220X
R33	RES. CARBON 10K OHM/1/4W/+-5%		RD25PJ103X
R34	RES. CARBON 1K OHM/1/4W/+-5%		RD25PJ102X
R35	RES. CARBON 10K OHM/1/4W/+-5%		RD25PJ103X
R36	RES. CARBON 680 OHM/1/4W/+-5%		RD25PJ681X
R37	RES. CARBON 180K OHM/1/4W/+-5%		RD25PJ184X
R38	RES. METAL FILM 52.3K OHM/1/4W/+-1%	AN-0613BEC	RQBPF5232X
R39	RES. CARBON 1K OHM/1/4W/+-5%		RD25PJ102X
R40	RES. CARBON 10K OHM/1/4W/+-5%		RD25PJ103X
R41	RES. CARBON 10K OHM/1/4W/+-5%		RD25PJ103X
R42	RES. METAL FILM 2.3K OHM/1/4W/+-1%		RQBPF2301X
R43	RES. METAL FILM 10K OHM/1/4W/+-1%		RQBPF1002X
R44	RES. METAL FILM 242K OHM/1/4W/+-1%		RQBPF2423X
R45	RES. METAL FILM 7.97K OHM/1/4W/+-1%		RQBPF7971X
R46	RES. CARBON 33K OHM/1/4W/+-5%		RD25PJ333X
R47	RES. CARBON 15M OHM/1/4W/+-5%		RD25TJ156X
R48	RES. CARBON 68K OHM/1/4W/+-5%		RD25PJ683X

R54	RES. CARBON 12K OHM/1/4W/+-5%		RD25PJ123X
R55	RES. CARBON 3.3K OHM/1/4W/+-5%		RD25PJ332X
R56	RES. CARBON 10K OHM/1/4W/+-5%		RD25PJ103X
R57	RES. CARBON 33K OHM/1/4W/+-5%		RD25PJ333X
R58			
R59			
R60			
R61			
R62	RES. CARBON 33K OHM/1/4W/+-5%		RD25PJ333X
R63	RES. CARBON 620 OHM/1/4W/+-5%		RD25PJ621X
R64	RES. CARBON 33K OHM/1/4W/+-5%		RD25PJ333X
R65			
R66			
R67			
R68			
R70			
R71			
R72			
R73			
R74	RES. CARBON 33K OHM/1/4W/+-5%		RD25PJ333X
R75	RES. CARBON 100K OHM/1/4W/+-5%		RD25PJ104X
R76	RES. CARBON 33K OHM/1/4W/+-5%		RD25PJ333X
R77	RES. CARBON 33K OHM/1/4W/+-5%		RD25PJ333X
R78	RES. CARBON 100K OHM/1/4W/+-5%		RD25PJ104X
R79	RES. CARBON 33K OHM/1/4W/+-5%		RD25PJ333X
R80	RES. CARBON 33K OHM/1/4W/+-5%		RD25PJ333X
R81	RES. CARBON 100K OHM/1/4W/+-5%		RD25PJ104X
R82	RES. CARBON 33K OHM/1/4W/+-5%		RD25PJ333X
R83	RES. CARBON 22K OHM/1/4W/+-5%		RD25PJ223X
R84	RES. CARBON 33K OHM/1/4W/+-5%		RD25PJ333X
R85	RES. CARBON 10K OHM/1/4W/+-5%		RD25PJ103X
R86	RES. CARBON 33K OHM/1/4W/+-5%		RD25PJ333X
R87	RES. CARBON 6.2K OHM/1/4W/+-5%		RD25PJ622X
R88			
R89	RES. CARBON 6.2K OHM/1/4W/+-5%		RD25PJ622X
R90	RES. CARBON 15K OHM/1/4W/+-5%		RD25PJ153X
R91	RES. CARBON 5.6K OHM/1/4W/+-5%		RD25PJ562X
R92	RES. CARBON 18K OHM/1/4W/+-5%		RD25PJ183X
R93	RES. CARBON 68K OHM/1/4W/+-5%		RD25PJ683X
R94	RES. CARBON 5.6K OHM/1/4W/+-5%		RD25PJ562X
R95	RES. CARBON 100 OHM/1/4W/+-5%		RD25PJ101X
R96	RES. CARBON 18K OHM/1/4W/+-5%		RD25PJ183X
R97	RES. CARBON 180 OHM/1/4W/+-5%		RD25PJ181X
R98	RES. CARBON 18K OHM/1/4W/+-5%		RD25PJ183X
R99	RES. CARBON 5.6K OHM/1/4W/+-5%		RD25PJ562X
R101	RES. CARBON 1.8K OHM/1/4W/+-5%		RD25PJ182X
R102	RES. CARBON 82K OHM/1/4W/+-5%		RD25PJ823X
R103	RES. CARBON 10K OHM/1/4W/+-5%		RD25PJ103X
R104	RES. CARBON 56K OHM/1/4W/+-5%		RD25PJ563X
R105	RES. METAL FILM 2.7K OHM/1/4W/+-1%	AN-0224BEE	RQBPF2701X
R106	RES. CARBON 150K OHM/1/4W/+-5%		RD25PJ154X
R107	RES. CARBON 47K OHM/1/4W/+-5%		RD25PJ473X

R111	RES. CARBON 150K OHM/1/4W//+-5%		RD25PJ154X
R112	RES. CARBON 1.8K OHM/1/4W/+-5%		RD25PJ182X
R113	RES. CARBON 3.3K OHM/1/4W/+-5%		RD25PJ332X
R114	RES. CARBON 33K OHM/1/4W/+-5%		RD25PJ333X
R115	RES. CARBON 100K OHM/1/4W/+-5%		RD25PJ104X
R116	RES. METAL FILM 150K OHM/1/4W/+-1%		RQBPF1503X
R118	RES. CARBON 100K OHM/1/4W/+-5%		RD25PJ104X
R119	RES. CARBON 33K OHM/1/4W/+-5%		RD25PJ333X
R120	RES. CARBON 82K OHM/1/4W/+-5%		RD25PJ823X
R121	RES. CARBON 820 OHM/1/4W/+-5%		RD25PJ821X
R122	RES. CARBON 470 OHM/1/4W/+-5%		RD25PJ471X
R123	RES. CARBON 1.8K OHM/1/4W/+-5%		RD25PJ182X
R124	RES. CARBON 10K OHM/1/4W/+-5%		RD25PJ103X
R125	RES. CARBON 10K OHM/1/4W/+-5%		RD25PJ103X
R126	RES. CARBON 270 OHM/1/4W/+-5%		RD25PJ271X
R127	RES. CARBON 22K OHM/1/4W/+-5%		RD25PJ223X
R128	RES. CARBON 100K OHM/1/4W/+-5%		RD25PJ104X
R131	RES. CARBON 1K OHM/1/4W/+-5%		RD25PJ102X
R132	RES. CARBON 150K OHM/1/4W/+-5%		RD25PJ154X
R134	RES. CARBON 3.3K OHM/1/4W/+-5%		RD25PJ332X
R135	RES. CARBON 68K OHM/1/4W/+-5%		RD25PJ683X
R136	RES. CARBON 68K OHM/1/4W/+-5%		RD25PJ683X
R137	RES. CARBON 100K OHM/1/4W/+-5%		RD25PJ104X
R138	↓		↓
R139	RES. CARBON 100K OHM/1/4W/+-5%		RD25PJ104X
R140	RES. CARBON 10K OHM/1/4W/+-5%		RD25PJ103X
R141	RES. CARBON 1MEG OHM/1/4W/+-5%		RD25PJ105X
R142	RES. CARBON 33K OHM/1/4W/+-5%		RD25PJ333X
R144	RES. CARBON 15K OHM/1/4W/+-5%		RD25PJ153X
R145	RES. CARBON 15K OHM/1/4W/+-5%		RD25PJ153X
R146	RES. CARBON 33K OHM/1/4W/+-5%		RD25PJ333X
R149	RES. CARBON 56K OHM/1/4W/+-5%		RD25PJ563X
R150	RES. CARBON 470 OHM/1/4W/+-5%		RD25PJ471X
R151	RES. CARBON 33K OHM/1/4W/+-5%		RD25PJ333X
R152	RES. CARBON 10K OHM/1/4W/+-5%		RD25PJ103X
R153	RES. CARBON 33K OHM/1/4W/+-5%		RD25PJ333X
R154	RES. CARBON 10K OHM/1/4W/+-5%		RD25PJ103X
R156	RES. CARBON 100K OHM/1/4W/+-5%		RD25PJ104X
R157	RES. CARBON 33K OHM/1/4W/+-5%		RD25PJ333X
R158	RES. CARBON 100K OHM/1/4W/+-5%		RD25PJ104X
R159	RES. CARBON 100K OHM/1/4W/+-5%		RD25PJ104X
R160	RES. CARBON 100K OHM/1/4W/+-5%		RD25PJ104X
R161	RES. CARBON 10K OHM/1/4W/+-5%		RD25PJ103X
R162	RES. CARBON 100 OHM/1/8W/+-5%	AN-0132EBC	RD18TJ101X
R170	RES. CARBON 150K OHM/1/4W/+-5%		RD25PJ154X
RELAYS			
RY1	RELAY FBR211CD005-M	AR-8160	ZRA265101Z
RY2	RELAY FRL-764D05/1AS-T	AR-8159	ZRA164102Z
RY3	RELAY FRL-764D05/1BS-T MODEM	AR-8158	ZRA164101Z

SWITCHES			
SW1	SWITCH, SLIDE SHORTING KNOB 9MM,PWR,ANS	AS-2843	SS020259ZA
SW2	SWITCH, SLIDE SSB34204, MODEM	AS-2845	SS040213ZA
SW3	SWITCH, SLIDE SLB-22B9-03 KNOB 3MM,BKUP	AS-2844	SS020260ZL
SW4	SWITCH, PUSH SPJ312U W/O KNOB, RESET	AS-7573	SP01ABA06A
SW5	SWITCH, SLIDE SHORTING KNOB 9MM,PWR,ANS	AS-2843	SS020259ZA
TRANSISTORS			
T1	XSISTOR 2SA1115 NO RANK PC300MW/FT200MH		QTA1115XAE
T2	XSISTOR 2SC2603 NO RANK PC300MW/FT200MH	AA-2SC2603	QTC2603XAE
T3			
T4			
T5			
T6			
T7			
T8			
T9			
T10			
T11	XSISTOR 2SC2603 NO RANK PC300MW/FT200MH	AA-2SC2603	QTC2603XAE
T13	XSISTOR 2SC2603 E-RANK PC300MW/FT200MHZ		QTC2603XCE
T14			
T15			
T16			
T17	XSISTOR 2SC2603 E-RANK PC300MW/FT200MHZ		QTC2603XCE
T18	XSISTOR 2SC2603 NO RANK PC300MW/FT200MH	AA-2SC2603	QTC2603XAE
T19	XSISTOR 2SA1115 NO RANK PC300MW/FT200MH		QTA1115XAE
T20	XSISTOR 2SC2603 NO RANK PC300MW/FT200MH	AA-2SC2603	QTC2603XAE
T21	XSISTOR 2SC1384 S-RANK PC750MW/FT200MHZ		QTC1384XHN
T22	XSISTOR 2SC2603 E-RANK PC300MW/FT200MHZ		QTC2603XCE
T23	XSISTOR 2SC2603 NO RANK PC300MW/FT200MH	AA-2SC2603	QTC2603XAE
T24			
T25			
T27	XSISTOR 2SC2603 NO RANK PC300MW/FT200MH	AA-2SC2603	QTC2603XAE
T28	XSISTOR 2SA1115 NO RANK PC300MW/FT200MH		QTA1115XAE
THERMISTERS			
TH1	THERMISTER 10K OHM/+-5% TD5-C310D1	AT-1235	QHQ5C31HZP
TH2	THERMISTER 10K OHM/+-5% TD5-C310D1	AT-1235	QHQ5C31HZP
VAR. RESISTORS			
VR1	VAR. RESISTOR 50K/B LCD CONTRAST		RV9A503B01
VR2	VAR. RESISTOR SEMI-FIXED 50K/B MODEM LE		RPSNB50303
CLYSTALS			
X1	XTAL OSCILLATOR 32.768KHZ +-20PPM	AMX-1011	XTR1A1001%
X2	XTAL OSCILLATOR 4.9152MHZ	AMX-1010	XBR1A1003X
X3	XTAL OSCILLATOR HC43/U 1MHZ	AMX-1009	XAZ1C2001X

MISCELLANEOUS			
A- 9	CONNECTOR - MAIN PCB ASSY	AJ-7323	ACCNA02GEA
A-10	CONNECTOR - MAIN PCB ASSY	AJ-7325	ACCNA05GEA
P-28	BATTERY TERMINAL - NEGATIVE	AHC-2156	MW361SN001
P-29	BATTERY TERMINAL - POSITIVE	AHC-2157	MW361SN003
P-31	KNOB, VOLUME	AK-5264	VF122SB001
P-32	KNOB, RESET	AK-5265	VK121SB004
P-33	SUPPORT, BATTERY - MINUS	AHC-2177	VS118SB001
P-34	SOCKET, I.C. ICA40-STG	AJ-7350	YSC40S002Z
P-35	TERMINAL, SHIELD PLATE	AJ-7351	YZC1150001
P-36	BATTERY NI-CAD 3-51FT	ACS-0100	ZBN036102Y
P-37	SUPPORT, BATTERY - POSITIVE		VS218SB002
P-46	SOCKET, I.C. SBA-STG	AJ-7347	YSC14S002Z
P-47	SOCKET, I.C. A-8878A-28S-1H	AJ-7348	YSC28S002Z
P-48	SOCKET, I.C. DICF-28CS	AJ-7349	YSC28S005Z
P-50	COIL,CHOKE 10μH/500mMA/AXIAL	ACA-8286	LF100KE04Y
P-51	FERRITE BEAD		YFRL000002
S-4	SCREW, PAN HEAD, MACHINE,M1.7X3,S-BLACK	AHD-2593	BSP21703NB
S-7	SCREW,PAN HEAD,SEMS,MACHINE,M3X8,S-ZNCR	AHD-2594	BSPC3008NZ
S-8	NUT, M3 Z-ZNCR THIN TYPE	AHD-7284	BNHCL30NSZ

LCD P.C.B. ASSEMBLY

Ref. No.	Description	RS Part No.	Mfr's Part No.
CAPACITORS			
LC1	CAPACITOR, CERA CHIP 0.1μF/25V/+80-20%	ACD-104ZFCX	CFKC104ZF%
LC2	↓	↓	↓
LC3	↓	↓	↓
LC4	CAPACITOR, CERA CHIP 0.1μF/25V/+80-20%	ACD-104ZFCX	CFKC104ZF%
LC5	CAPACITOR, CERA CHIP 18PF/25V/+-10%	ACD-180KFCX	CFKC180KC%
LC6	CAPACITOR, CERA CHIP 0.1μF/25V/+80-20%	ACD-104ZFCX	CFKC104ZF%
LC7	↓	↓	↓
LC8	↓	↓	↓
LC9	↓	↓	↓
LC10	CAPACITOR, CERA CHIP 0.1μF/25V/+80-20%	ACD-104ZFCX	CFKC104ZF%
LC11	CAPACITOR, CERA CHIP 1000PF/25V/+80-20%	ACD-102ZFCX	CFKC102ZF%
LC12	↓	↓	↓
LC13	↓	↓	↓
LC14	↓	↓	↓
LC15	↓	↓	↓
LC16	↓	↓	↓
LC17	↓	↓	↓
LC18	↓	↓	↓
LC19	↓	↓	↓
LC20	CAPACITOR, CERA CHIP 1000PF/25V/+80-20%	ACD-102ZFCX	CFKC102ZF%
LC21	CAPACITOR, CERA CHIP 220PF/25V/+80-20%	ACD-221ZFCX	CFKC221ZF%
LC22	↓	↓	↓
LC23	↓	↓	↓
LC24	↓	↓	↓
LC25	CAPACITOR, CERA CHIP 220PF/25V/+80-20%	ACD-221ZFCX	CFKC221ZF%

INTEGRATED CIRCUITS			
LM1	I.C.,C-MOS,DRIVER,HD44102CH	AMX-5797	QQ044102BB
LM2			
LM3			
LM4			
LM5			
LM6			
LM7			
LM8			
LM9			
LM10	I.C.,C-MOS,DRIVER,HD44102CH	AMX-5797	QQ044102BB
LM11	I.C.,C-MOS,DRIVER,HD44103BLD	AMX-5798	QQ044103BB
LM12	I.C.,C-MOS,DRIVER,HD44103BLD	AMX-5798	QQ044103BB
LM13	I.C.,BIPOLAR,OP AMP,HA17902P	AMX-5796	QQM17902PB
RESISTORS			
LR1	RESISTOR, CHIP 10K OHM/1/8W/+-2%		RJ8AMG103%
LR2	RESISTOR, CHIP 10K OHM/1/8W/+-2%		RJ8AMG103%
LR3	RESISTOR, CHIP 26.5K OHM/1/8W/+-2%		RJ8AMGA52%
LR4	RESISTOR, CHIP 10K OHM/1/8W/+-2%		RJ8AMG103%
LR5	RESISTOR, CHIP 10K OHM/1/8W/+-2%		RJ8AMG103%
LR6	RESISTOR, CHIP 100K OHM/1/8W/+-5%		RJ8AMJ104%
LR7			
LR8			
LR9			
LR10	RESISTOR, CHIP 100K OHM/1/8W/+-5%		RJ8AMJ104%
LR11	RESISTOR, CHIP 18 OHM/1/8W/+-5%		RJ8AMJ180%
LR12	RESISTOR, CHIP 150 OHM/1/8W/+-5%		RJ8AMJ151%
LR13			
LR14			
LR15			
LR16	RESISTOR, CHIP 150 OHM/1/8W/+-5%		RJ8AMJ151%
MISCELLANEOUS			
A-7	CORD ASSY - LCD CONNECTOR	AW-3058	ACCN812GEA
A-8	CONNECTOR ASSY, LCD PCB	AJ-7324	ACCNA03GEA
P-22	HOLDER - LCD	AHC-2154	MB861SF001
P-24	L.E.D. SLP-135B	AL-1458	QL1SP135BC
P-25	CONNECTOR, LCD SG TYPE	AJ-7321	VQ811RX001
P-27	L.C.D. LR202-C	AL-1459	ZXLR202CXB

KEY BOARD ASSEMBLY

Ref. No.	Description	RS Part No.	Mfr's Part No.
SWITCHES			
P-12	SWITCH,KEY - TACT	AS-7570	SK0101X10A
P-13	SWITCH,KEY - PUSH	AS-7571	SK0111X04A
P-14	SWITCH,KEY - LOCK TYPE	AS-7572	SK0111X05A
MISCELLANEOUS			
A-6	CORD ASSY -KEY BOARD CONNECTOR	AW-3057	ACCN870GEA

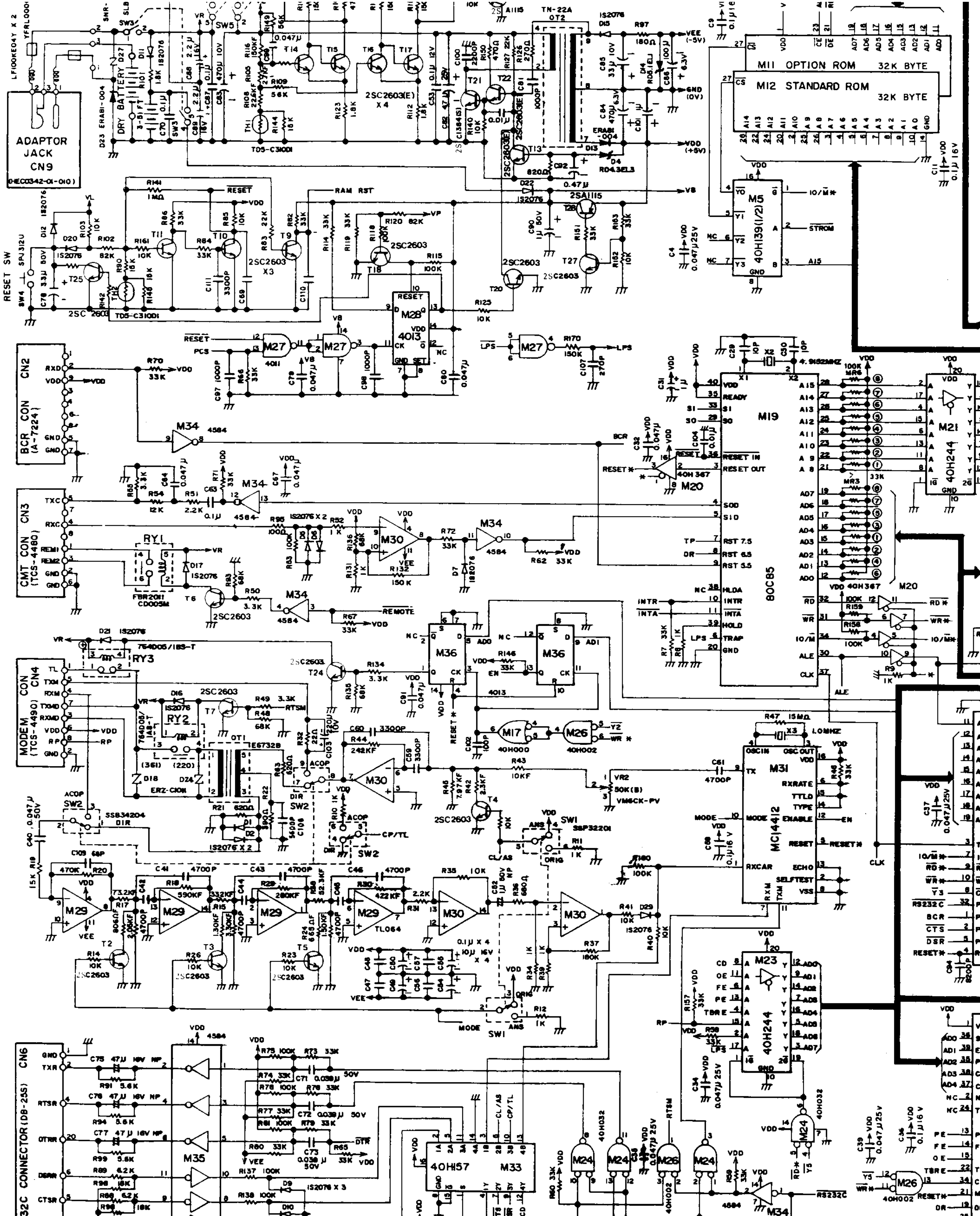
KEYTOPS

P-100	KEYTOP - TACT	AK-5205	VK121SB003
P-101	KEYTOP - 1	AK-5206	VK122SB004
P-102	KEYTOP - 2	AK-5207	VK122SB005
P-103	KEYTOP - 3	AK-5208	VK122SB006
P-104	KEYTOP - 4	AK-5209	VK122SB007
P-105	KEYTOP - 5	AK-5210	VK122SB008
P-106	KEYTOP - 6	AK-5211	VK122SB009
P-107	KEYTOP - 7	AK-5212	VK122SB010
P-108	KEYTOP - 8	AK-5213	VK122SB011
P-109	KEYTOP - 9	AK-5214	VK122SB012
P-110	KEYTOP - 0	AK-5215	VK122SB013
P-111	KEYTOP - A	AK-5216	VK122SB014
P-112	KEYTOP - B	AK-5217	VK122SB015
P-113	KEYTOP - C	AK-5218	VK122SB016
P-114	KEYTOP - D	AK-5219	VK122SB017
P-115	KEYTOP - E	AK-5220	VK122SB018
P-116	KEYTOP - F	AK-5221	VK122SB019
P-117	KEYTOP - G	AK-5222	VK122SB020
P-118	KEYTOP - H	AK-5223	VK122SB021
P-119	KEYTOP - I	AK-5224	VK122SB022
P-120	KEYTOP - J	AK-5225	VK122SB023
P-121	KEYTOP - K	AK-5226	VK122SB024
P-122	KEYTOP - L	AK-5227	VK122SB025
P-123	KEYTOP - M	AK-5228	VK122SB026
P-124	KEYTOP - N	AK-5229	VK122SB027
P-125	KEYTOP - O		VK122SB028
P-126	KEYTOP - P	AK-5231	VK122SB029
P-127	KEYTOP - Q	AK-5232	VK122SB030
P-128	KEYTOP - R	AK-5233	VK122SB031
P-129	KEYTOP - S	AK-5234	VK122SB032
P-130	KEYTOP - T	AK-5235	VK122SB033
P-131	KEYTOP - U	AK-5236	VK122SB034
P-132	KEYTOP - V	AK-5237	VK122SB035
P-133	KEYTOP - W	AK-5238	VK122SB036
P-134	KEYTOP - X	AK-5239	VK122SB037
P-135	KEYTOP - Y	AK-5240	VK122SB038
P-136	KEYTOP - Z	AK-5241	VK122SB039
P-200	KEYTOP - ESC	AK-5242	VK122SB040
P-201	KEYTOP - MINUS	AK-5243	VK122SB041
P-202	KEYTOP - EQUAL	AK-5244	VK122SB042
P-203	KEYTOP - DEL	AK-5245	VK122SB043
P-204	KEYTOP - BRACKET	AK-5246	VK122SB044
P-205	KEYTOP - ;	AK-5247	VK122SB045
P-206	KEYTOP - '	AK-5248	VK122SB046
P-207	KEYTOP - CAPS LOCK	AK-5249	VK122SB047
P-208	KEYTOP - COMMA	AK-5250	VK122SB048
P-209	KEYTOP - PERIOD	AK-5251	VK122SB049
P-210	KEYTOP - /	AK-5252	VK122SB050
P-211	KEYTOP - GRPH	AK-5253	VK122SB051
P-212	KEYTOP - CODE	AK-5254	VK122SB052
P-213	KEYTOP - NUM	AK-5255	VK122SB053

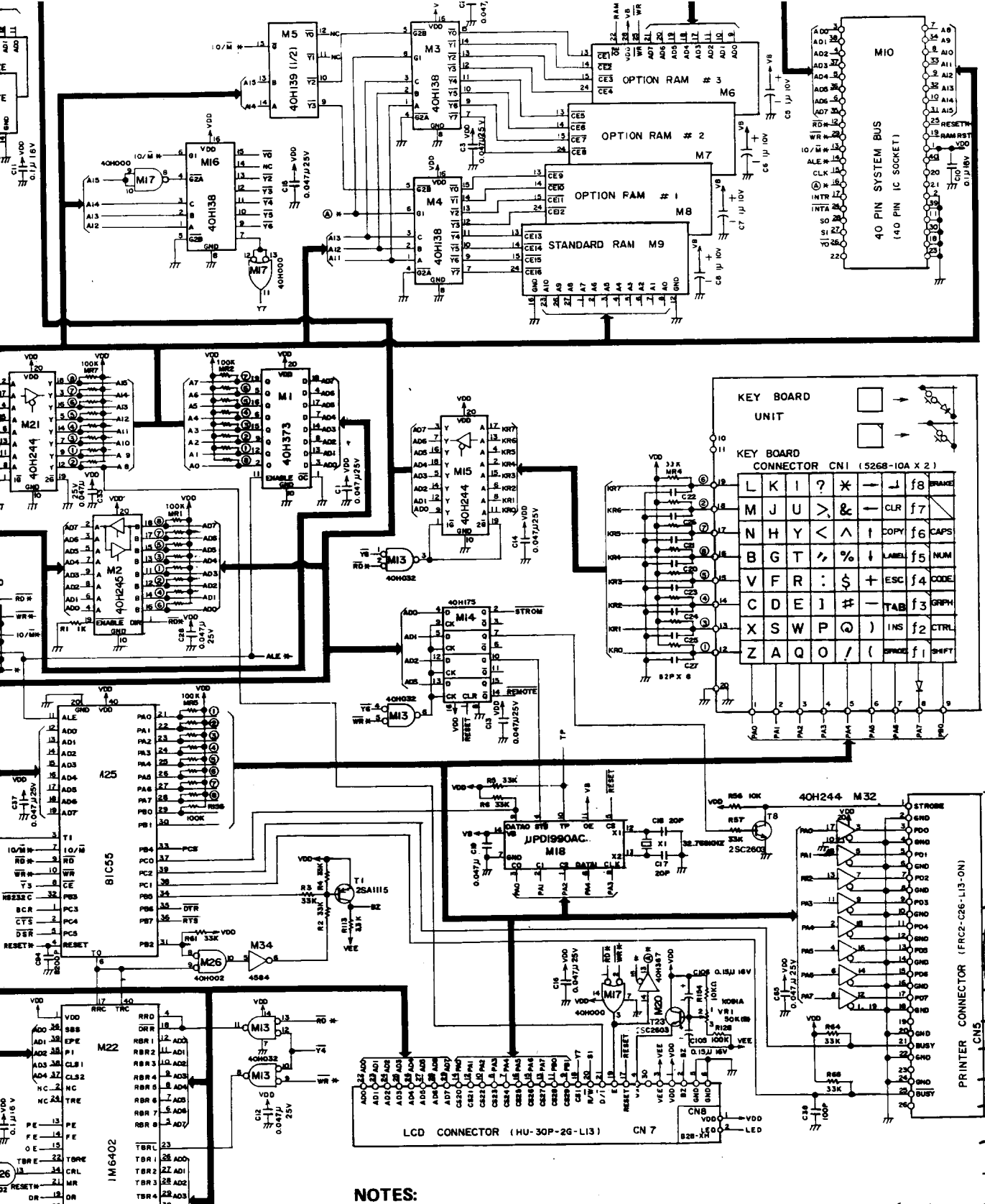
A-1	KEYBOARD ASSEMBLY		AFYX1****1
A-2	P.C.B. ASSY - LCD	AX-9349	APLX1002AA
A-3	P.C.B. ASSY - MAIN (26-3801)	AX-9350	APLX1003AA
	(26-3802)		APLX1003BA
A-4	CASE ASSEMBLY, TOP	AZ-6913	AMX1****01
P-15	PLATE, MODEL	AHC-2178	MVMX1****1
P-16	CASE,TOP - SILVER		VB883SM001
P-17	FILTER	AZ-6914	VS868AC002
A-5	CASE ASSEMBLY, BOTTOM	AZ-6915	AMX1****02
P-18	FOOT, RUBBER	AF-0364	##P4157***
P-19	BATTERY TERMINAL - FRONT	AHC-2179	MW261LJ009
P-20	BATTERY TERMINAL - REAR	AHC-2180	MW261LJ010
P-21	CASE, BOTTOM		VB883SB008
P-26	BUZZER ASSEMBLY	AB-7119	AYX1N***01
P-6	COVER, ROM	ADA-0386	VS667SB002
P-7	COVER, BATTERY	ADB-0455	VS668SB002
P-8A	POUCH	AZ-6916	AMX1****03
P-3	PLATE, NAME	AHC-2181	KLX1****01
P-4	LABEL - FCC (26-3801 USA VERSION ONLY)		KL000304XX
	(26-3802 USA VERSION ONLY)		KL000305XX
P-5	PLATE - SERIAL NUMBER (26-3801)		MVSX1****1
	(26-3802)		MVSX1****2
P-1	SUPPORT, KEYBOARD - FRONT	AHC-2182	MU821LJ001
P-2	SUPPORT, KEYBOARD - REAR	AHC-2183	VL821SB001
P-43	SUPPORT, KEYBOARD - MIDDLE	AHC-2233	VL122SB001
P-44	SUPPORT, CAP, KEYBOARD	AHC-2232	VB111RB001
P-39	PLATE, BLIND - LEFT	AHC-2184	VS326SB003
P-40	PLATE, BLIND - RIGHT	AHC-2185	VS326SB004
P-41	CAP, RS-232C - CONNECTOR COVER	AHC-2234	VL722SB002
P-42	CAP, B.C.R. - CONNECTOR COVER	AHC-2235	VE32JPB001
P-45	PLATE, SHIELD	ART-4964	AMX1****04
S-1	SCREW, CUP HEAD, MACHINE, M3X8, S-ZNCR	AHD-1865	BSP43008NZ
S-2	SCREW, PAN HEAD, MACHINE, M2X4, PLASTIC	AHD-2612	BSPP2004NP
S-5	SCREW, PAN HEAD, TAPPING, M3X10, S-ZNCR	AHD-2619	BTPP3010BZ
S-6	SCREW,PAN HEAD,SEMS,MACHINE,M3X10,S-ZNCR	AHD-1867	BSPN3010NZ
S-3	SCREW,HARDWARE KIT,SEMS,MACHINE,M3X8,X4	AHW-2603801	NSAX110001

SECTION VII

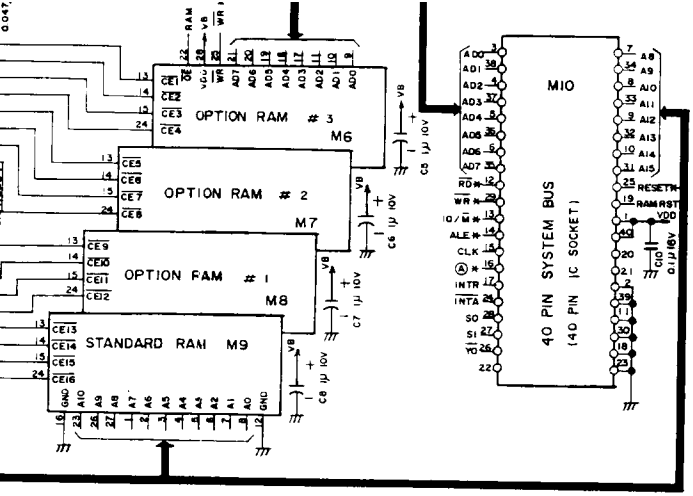
DIAGRAMS

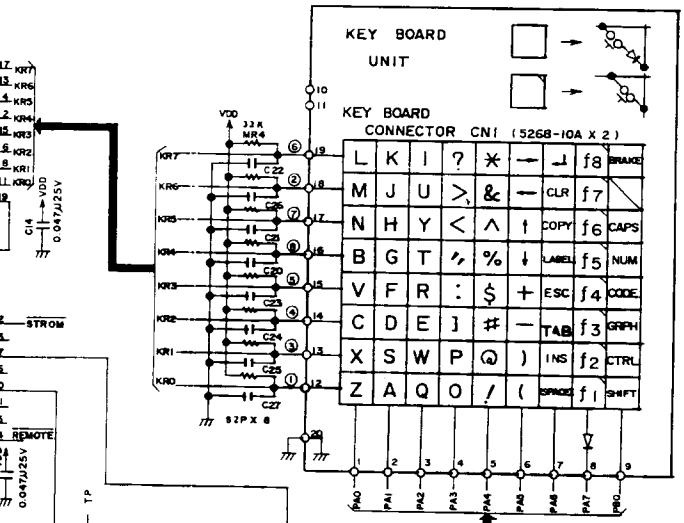


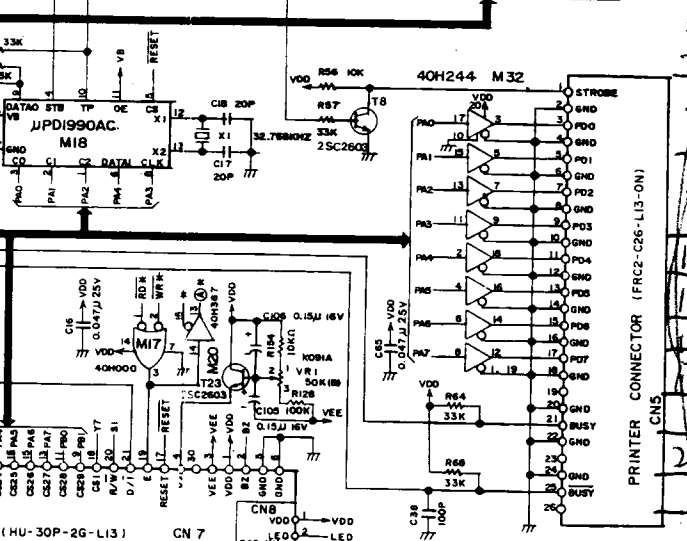
ADAPTOR JACK CN9
DRY BATTERY
M11 OPTION ROM 32K BYTE
M12 STANDARD ROM 32K BYTE
M5 40H139(1/2)
TN-22A OT2
RESET SW
RAM RST
M28 4013
M27 4011
CN2 BCR CON (A-7224)
CN3 CMT CON (TCS-4480)
CN4 MODEM CON (TCS-4490)
M19 80C85
M21 40H244
M20 40H367
M34 4584
RY1
RY2
RY3
M36 4013
M17 40H000
M26 40H002
M31 MC14412
M30
M29 TL064
SW1
SW2
M23 40H244
CN6
RS232C CONNECTOR (DB-25S)
M35
M33 40H157
M24 40H032



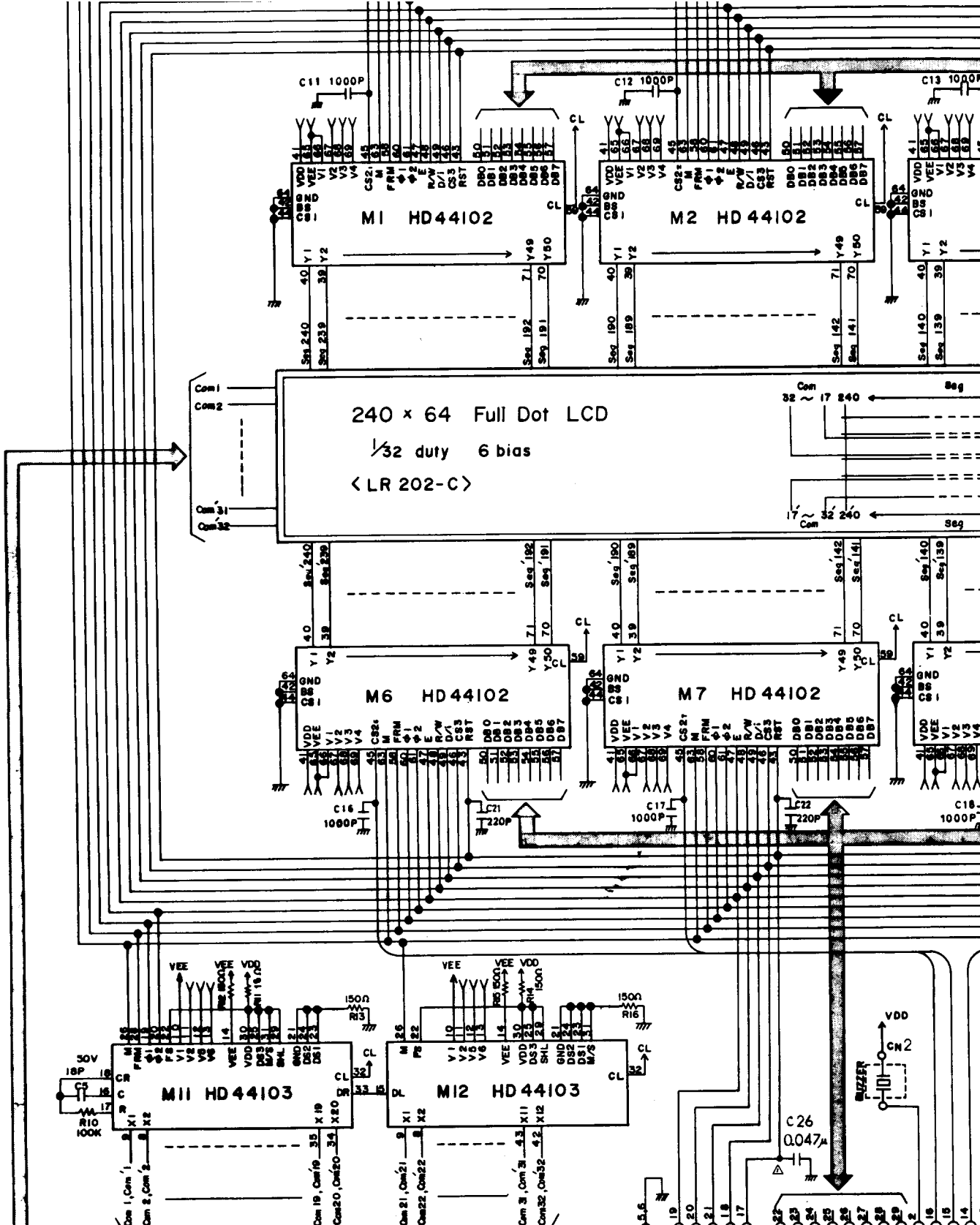
RS	R/W	STROBE
1	1	
3	2	D0
5	3	D1
7	4	D2
9	5	D3
11	6	D4
13	7	D5
15	8	D6
17	9	D7
	10	ACK
21	11	BUSY
	12	PAPER
	13	SELECT
	14	AUTO F
	15	ERROR

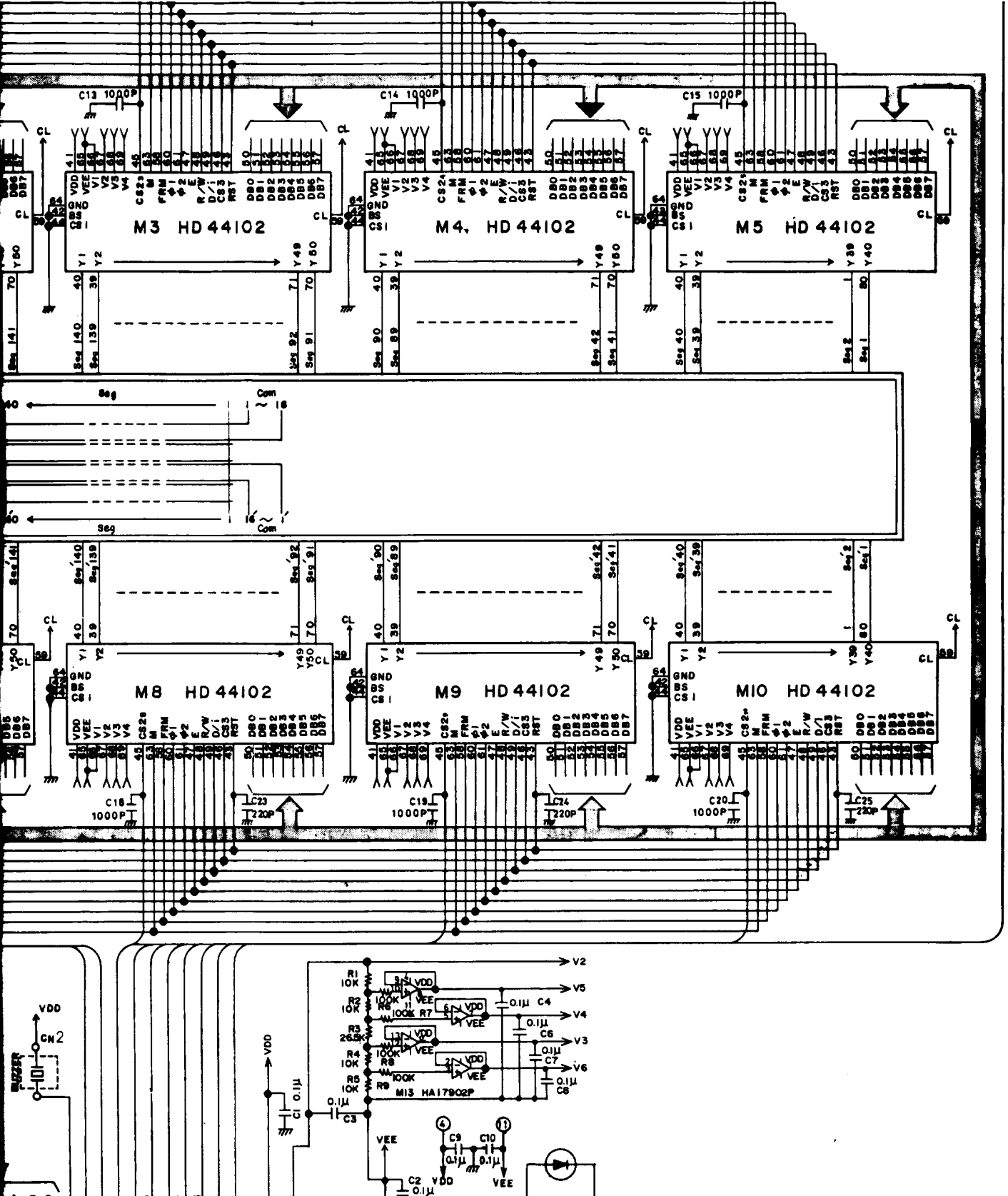


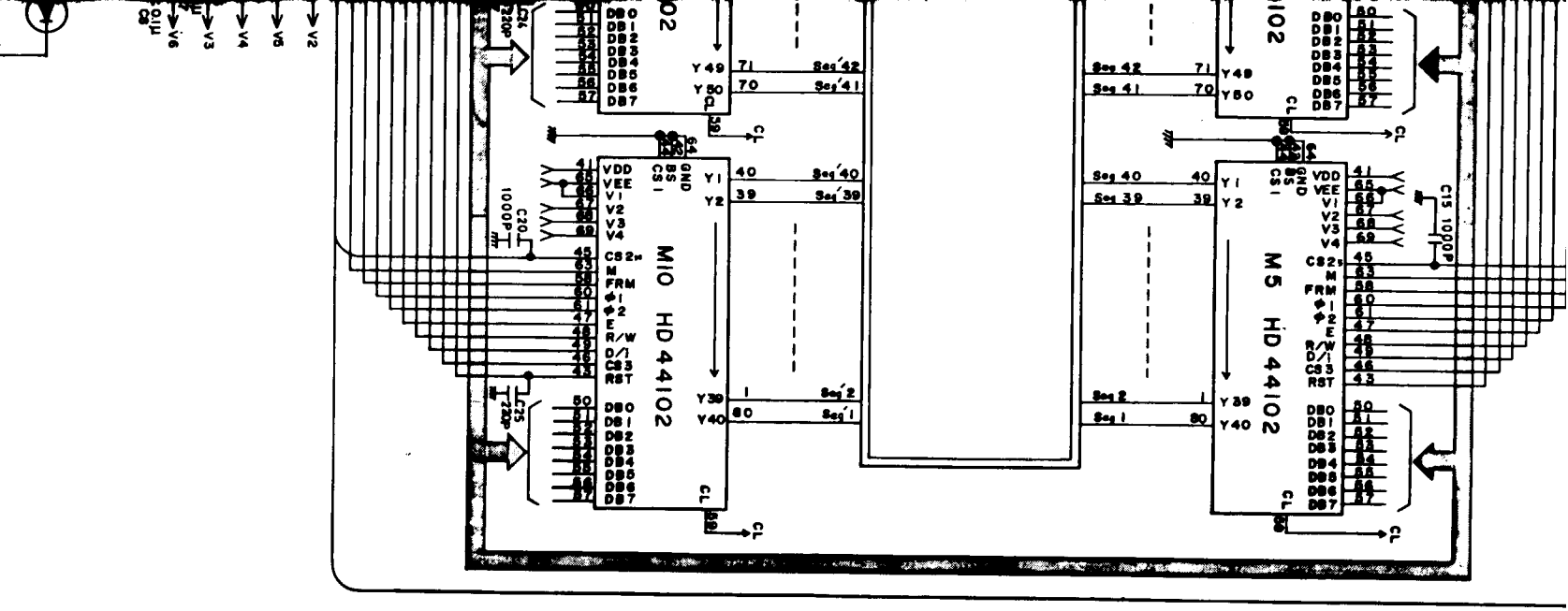


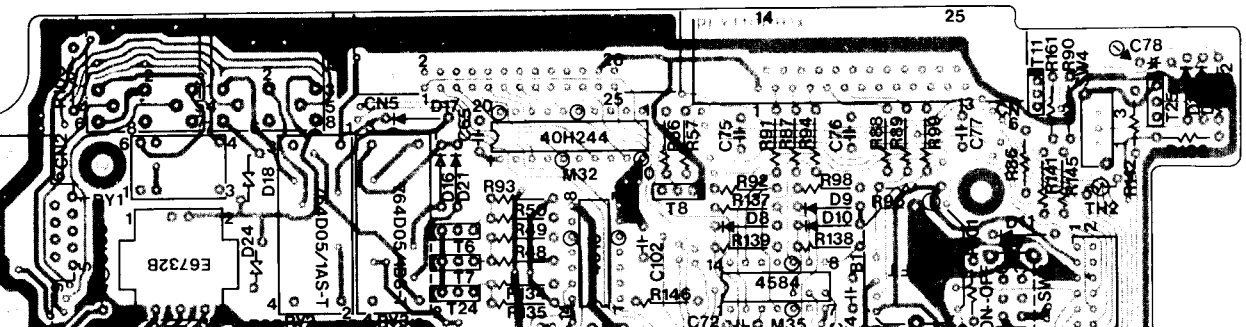


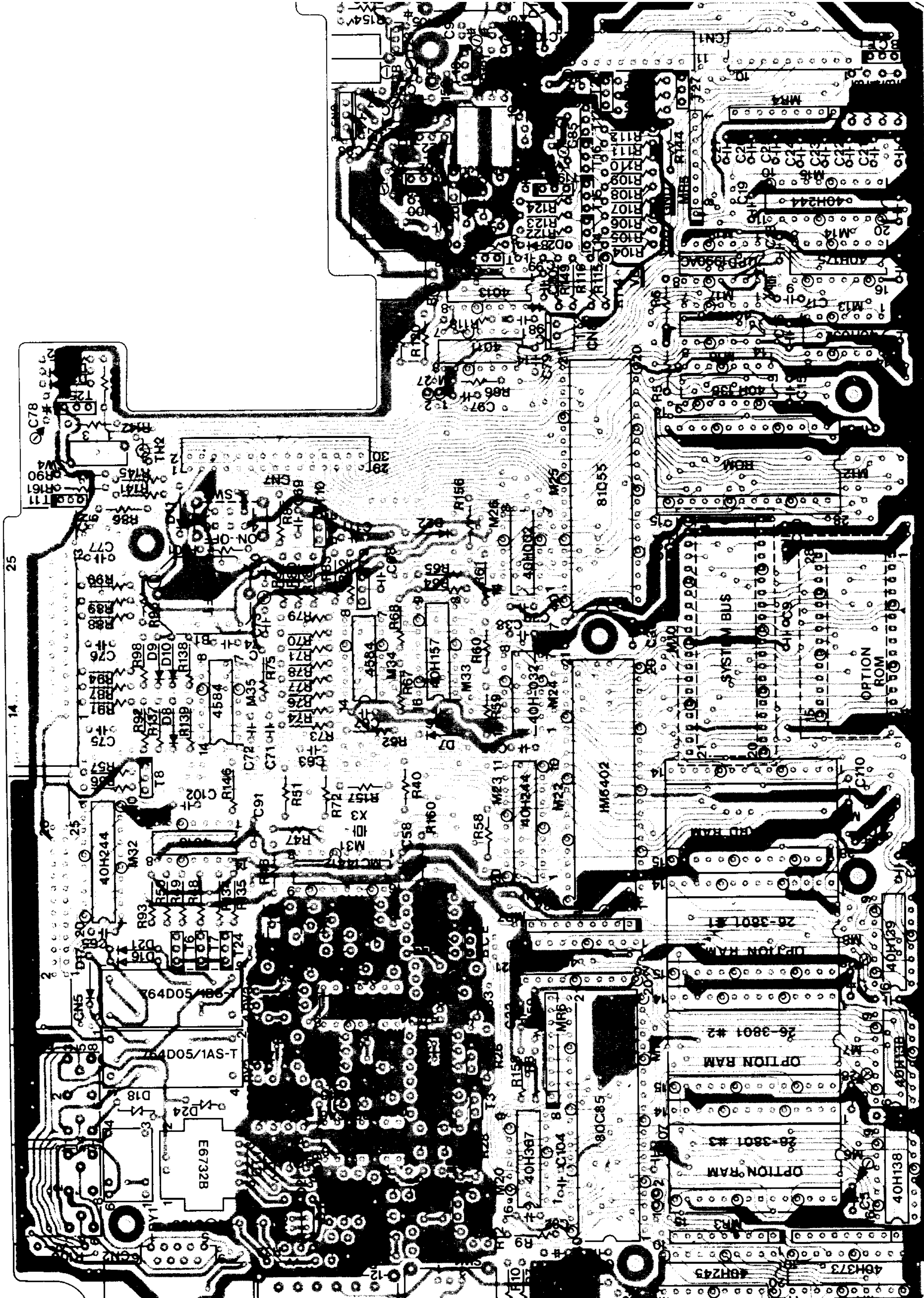
	1	STROBE
3	2	D0
5	3	D1
7	4	D2
9	5	D3
11	6	D4
13	7	D5
15	8	D6
17	9	D7
	10	ACK
21	11	BUSY
	12	PAPER EMPTY
	13	SELECT
	14	AUTO FEAT
	15	ERROR


240 × 64 Full Dot LCD
1/32 duty 6 bias
<LR 202-C>
M1 HD44102
M2 HD44102
M6 HD44102
M7 HD44102
M11 HD44103
M12 HD44103
C11 1000P
C12 1000P
C16 1000P
C17 1000P
C21 220P
C22 220P
C26 0.047μ
R10 100K
R13 150Ω
R14 150Ω
R16 150Ω
50V 18P
VDD
VEE
CN2
BUZZER
Com1
Com2
Com31
Com32
Seg

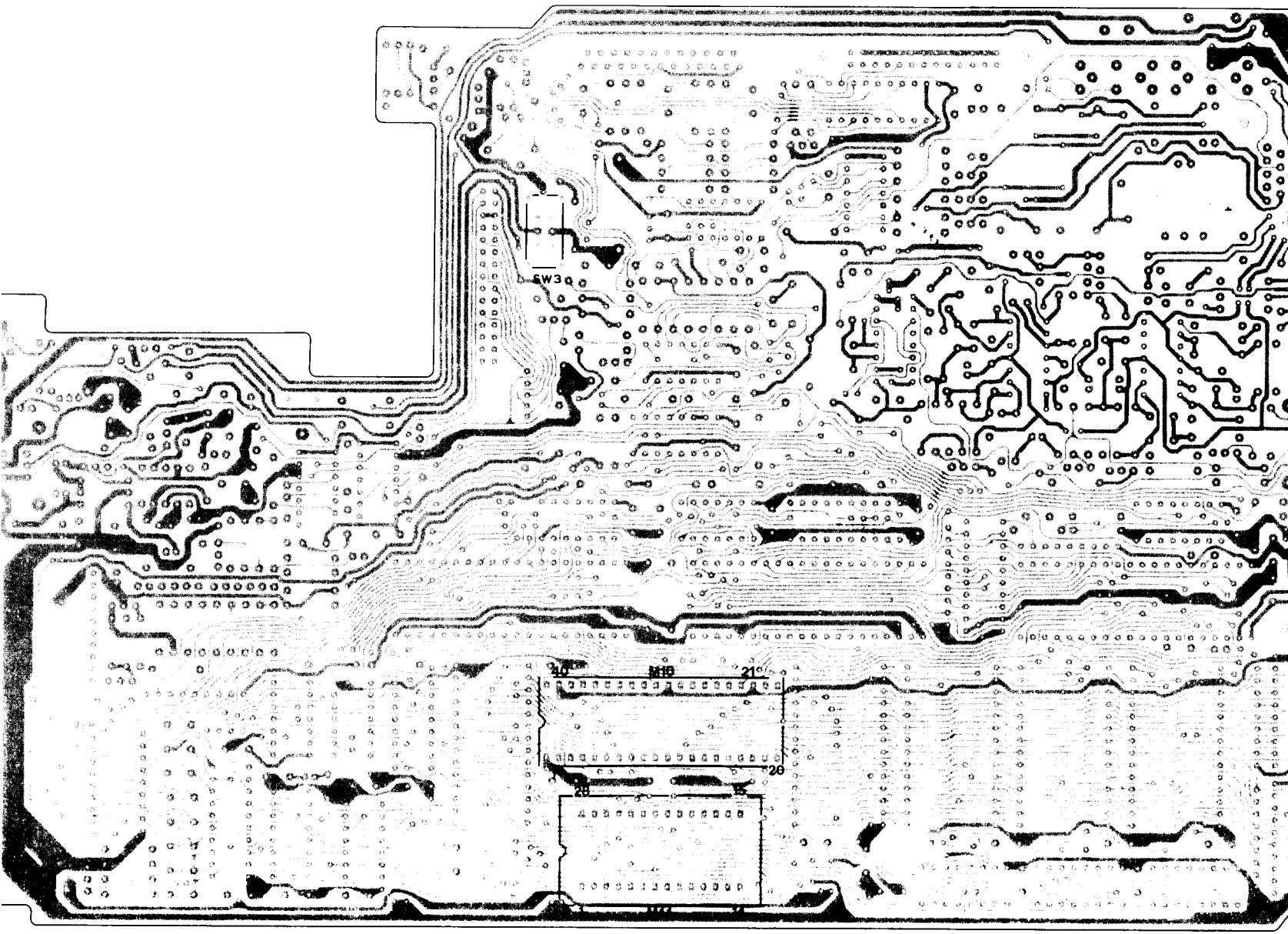

M3 HD44102
M4 HD44102
M5 HD44102
M8 HD44102
M9 HD44102
M10 HD44102
C13 1000P
C14 1000P
C15 1000P
C16 1000P
C19 1000P
C20 1000P
C23 220P
C24 220P
C25 220P
Seg
Com
M13 HA17902P
R1 10K
R2 10K
R3 26.5K
R4 10K
R5 10K
R6 100K
R7 100K
R8 100K
R9 100K
C1 0.1μ
C2 0.1μ
C3 0.1μ
C4 0.1μ
C6 0.1μ
C7 0.1μ
C8 0.1μ
C9 0.1μ
C10 0.1μ
V2
V5
V4
V3
V6
VDD
VEE
CN2
BUZZER


M10 HD 44102
M5 HD 44102
VDD
VEE
V1
V2
V3
V4
CS2
M
FRM
Φ2
E
R/W
D/I
CS3
RST
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
Y1
Y2
Y39
Y40
Y49
Y50
Seg 1
Seg 2
Seg 39
Seg 40
Seg 41
Seg 42
C15 1000P
C25 220P


CN5
40H244
M32
E6732B
4584
C78



SYSTEM BUS
OPTION ROM
OPTION RAM
26-3801 #1
26-3801 #2
26-3801 #3
IM6402
81C55
80C85
40H244
40H138
40H367
4584
E6732B
764D05/1AS-T


SW3
40
M16
21
20
1
20
15

(TOP VIEW)

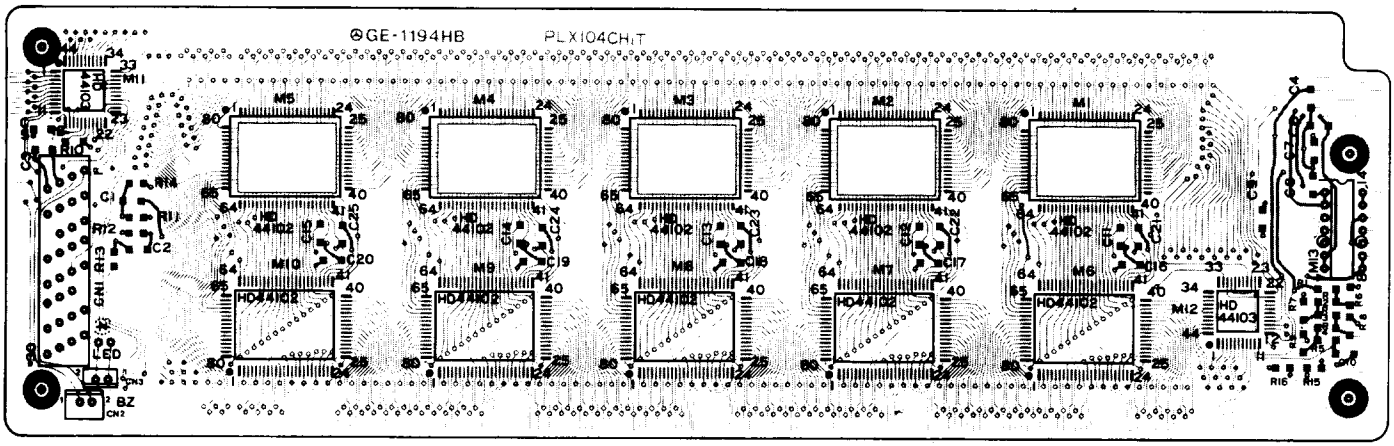


Fig. 7-5 LCD P.C.B. – Component Side

(BOTTOM VIEW)

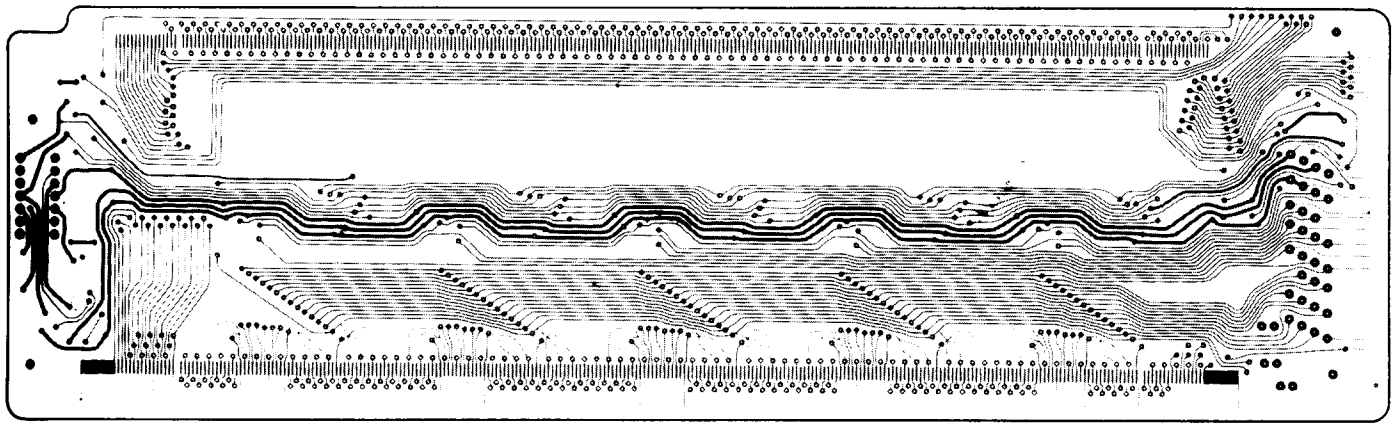


Fig. 7-6 LCD P.C.B. – Circuit Side

APPENDIX A

INSTALLATION OF OPTIONAL RAMs AND ROM

Open the Top and Bottom Case of the Model 100 (refer to Section II, DISASSEMBLY/REASSEMBLY).
On the Main P.C. Board, you can find 3 IC sockets marked "Optional RAM 26-3801 #1, 2 and 3".
Insert optional RAMs into these sockets.
Prior to inserting the RAMs, make sure that all the pins of the RAM are correctly aligned against the socket pins.

(2) Installation of optional ROM

Using the coin, remove the ROM Cover on the Bottom Case.
You will find an IC socket with a plastic housing.
Insert optional ROM into this socket.
On the P.C. Board, at the four corners of the IC socket, you will find the number of pins, such as 1, 14, 15 and 28.
Pay attention that pin-1 of the ROM is correctly aligned against pin-1 of the IC socket.

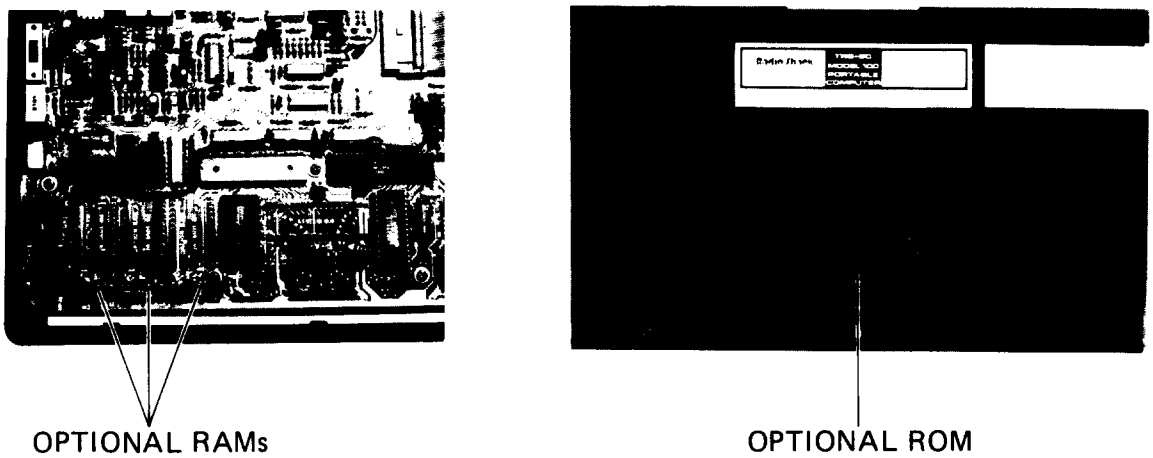


Fig. A-1 Installation of Optional RAMs and ROM

APPENDIX B

CHARACTER CODE TABLE

Decimal	Hex	Binary	Printed Character	Keyboard Character
0	00	00000000		CTRL @
1	01	00000001		CTRL A
2	02	00000010		CTRL B
3	03	00000011		CTRL C
4	04	00000100		CTRL D
5	05	00000101		CTRL E
6	06	00000110		CTRL F
7	07	00000111		CTRL G
8	08	00001000		CTRL H
9	09	00001001		CTRL I
10	0A	00001010		CTRL J
11	0B	00001011		CTRL K
12	0C	00001100		CTRL L
13	0D	00001101		CTRL M
14	0E	00001110		CTRL N
15	0F	00001111		CTRL O
16	10	00010000		CTRL P
17	11	00010001		CTRL Q
18	12	00010010		CTRL R
19	13	00010011		CTRL S
20	14	00010100		CTRL T
21	15	00010101		CTRL U
22	16	00010110		CTRL V
23	17	00010111		CTRL W
24	18	00011000		CTRL X
25	19	00011001		CTRL Y
26	1A	00011010		CTRL Z
27	1B	00011011		ESC
28	1C	00011100		→
29	1D	00011101		←
30	1E	00011110		↓
31	1F	00011111		↑
32	20	00100000		SPACEBAR
33	21	00100001	!	!
34	22	00100010	"	"
35	23	00100011	#	#
36	24	00100100	$	$
37	25	00100101	%	%
38	26	00100110	&	&
39	27	00100111	'	'
40	28	00101000	(	(
41	29	00101001	)	)
42	2A	00101010	*	*
43	2B	00101011	+	+
44	2C	00101100	,	,
45	2D	00101101	-	-
46	2E	00101110	.	.
47	2F	00101111	/	/
48	30	00110000	0	0
49	31	00110001	1	1
50	32	00110010	2	2
51	33	00110011	3	3
52	34	00110100	4	4
53	35	00110101	5	5
54	36	00110110	6	6
55	37	00110111	7	7
56	38	00111000	8	8
57	39	00111001	9	9
58	3A	00111010	:	:
59	3B	00111011	;	;
60	3C	00111100	<	<
61	3D	00111101	=	=
62	3E	00111110	>	>
63	3F	00111111	?	?
64	40	01000000	@	@
65	41	01000001	A	A
66	42	01000010	B	B
67	43	01000011	C	C
68	44	01000100	D	D
69	45	01000101	E	E
70	46	01000110	F	F
71	47	01000111	G	G
72	48	01001000	H	H
73	49	01001001	I	I
74	4A	01001010	J	J
75	4B	01001011	K	K
76	4C	01001100	L	L
77	4D	01001101	M	M
78	4E	01001110	N	N
79	4F	01001111	O	O
80	50	01010000	P	P
81	51	01010001	Q	Q
82	52	01010010	R	R
83	53	01010011	S	S
84	54	01010100	T	T
85	55	01010101	U	U
86	56	01010110	V	V
87	57	01010111	W	W
88	58	01011000	X	X
89	59	01011001	Y	Y
90	5A	01011010	Z	Z
91	5B	01011011	[	[
92	5C	01011100	\	GRPH -
93	5D	01011101	]	]
94	5E	01011110	^	^

* For uppercase letters A-Z, press SHIFT or CAPS LOCK before pressing the Keyboard Character.

Decimal	Hex	Binary	Printed Character	Keyboard Character
95	5F	01011111	_	_
96	60	01100000	\	GRAPH |
97	61	01100001	a	A
98	62	01100010	b	B
99	63	01100011	c	C
100	64	01100100	d	D
101	65	01100101	e	E
102	66	01100110	f	F
103	67	01100111	g	G
104	68	01101000	h	H
105	69	01101001	i	I
106	6A	01101010	j	J
107	6B	01101011	k	K
108	6C	01101100	l	L
109	6D	01101101	m	M
110	6E	01101110	n	N
111	6F	01101111	o	O
112	70	01110000	p	P
113	71	01110001	q	Q
114	72	01110010	r	R
115	73	01110011	s	S
116	74	01110100	t	T
117	75	01110101	u	U
118	76	01110110	v	V
119	77	01110111	w	W
120	78	01111000	x	X
121	79	01111001	y	Y
122	7A	01111010	z	Z
123	7B	01111011	{	GRAPH 9
124	7C	01111100	|	GRAPH _
125	7D	01111101	}	GRAPH 0
126	7E	01111110	~	GRAPH |
127	7F	01111111		DEL
128	80	10000000	☎	GRAPH p
129	81	10000001		GRAPH m
130	82	10000010	(×	GRAPH f
131	83	10000011		GRAPH x
132	84	10000100		GRAPH c
133	85	10000101		GRAPH a
134	86	10000110		GRAPH h
135	87	10000111		GRAPH t
136	88	10001000	ı	GRAPH I
137	89	10001001	\ ¯	GRAPH r
138	8A	10001010	≠	GRAPH /
139	8B	10001011	Σ	GRAPH s
140	8C	10001100	≈	GRAPH '
141	8D	10001101	±	GRAPH =
142	BE	10001110	∫	GRAPH i
143	BF	10001111	◀	GRAPH e

* For lowercase letters a-z, be sure CAPS LOCK is not pressed "down."

Decimal	Hex	Binary	Printed Character	Keyboard Character
144	90	10010000		GRAPH y
145	91	10010001		GRAPH u
146	92	10010010		GRAPH ;
147	93	10010011		GRAPH q
148	94	10010100		GRAPH w
149	95	10010101		GRAPH b
150	96	10010110		GRAPH n
151	97	10010111		GRAPH
152	98	10011000		GRAPH o
153	99	10011001		GRAPH .
154	9A	10011010		GRAPH I
155	9B	10011011		GRAPH k
156	9C	10011100		GRAPH 2
157	9D	10011101		GRAPH 3
158	9E	10011110		GRAPH 4
159	9F	10011111		GRAPH 5
160	A0	10100000		CODE
161	A1	10100001	a	CODE x
162	A2	10100010	ç	CODE c
163	A3	10100011	£	GRAPH 8
164	A4	10100100	`	CODE '
165	A5	10100101	μ	CODE M
166	A6	10100110		CODE)
167	A7	10100111		CODE _
168	A8	10101000	†	CODE +
169	A9	10101001	§	CODE s
170	AA	10101010	R	CODE R
171	AB	10101011	C	CODE C
172	AC	10101100	¼	CODE p
173	AD	10101101	¾	CODE :
174	AE	10101110	½	CODE
175	AF	10101111	¶	CODE 0
176	B0	10110000	¥	GRAPH 7
177	B1	10110001	A	CODE A
178	B2	10110010	O	CODE O
179	B3	10110011	U	CODE U
180	B4	10110100	¢	GRAPH 6
181	B5	10110101	~	CODE |
182	B6	10110110	a	CODE a
183	B7	10110111	o	CODE o
184	B8	10111000	u	CODE u
185	B9	10111001	B	CODE S
186	BA	10111010	TM	CODE T
187	BB	10111011	é	CODE d
188	BC	10111100	ü	CODE .
189	BD	10111101	è	CODE v
190	BE	10111110	¨	CODE =
191	BF	10111111	£	CODE F
192	C0	11000000	à	CODE I
193	CI	11000001	ê	CODE 3

Decimal	Hex	Binary	Printed Character	Keyboard Character
194	C2	11000010	ì	CODE 8
195	C3	11000011	ò	CODE 9
196	C4	11000100	ù	CODE 7
197	C5	11000101	·	CODE -
198	C6	11000110	e	CODE e
199	C7	11000111	ı	CODE i
200	C8	11001000	a	CODE q
201	C9	11001001	ı	CODE k
202	CA	11001010	o	CODE l
203	CB	11001011	u	CODE j
204	CC	11001100	y	CODE y
205	CD	11001101	n̈	CODE n
206	CE	11001110	ä	CODE z
207	CF	11001111	ö	CODE
208	D0	11010000	Ä	CODE !
209	D1	11010001	Ë	CODE #
210	D2	11010010	ï	CODE "
211	D3	11010011	Ö	CODE (
212	D4	11010100	Ü	CODE &
213	D5	11010101	ï	CODE I
214	D6	11010110	E	CODE E
215	D7	11010111	E	CODE D
216	D8	11011000	A	CODE Q
217	D9	11011001	I	CODE K
218	DA	11011010	O	CODE L
219	DB	11011011	U	CODE J
220	DC	11011100	Y	CODE Y
221	DD	11011101	U	CODE <
222	DE	11011110	E	CODE V
223	DF	11011111	A	CODE X
224	ED	11100000		GRPH Z
225	E1	11100001	(upper left)	GRPH !
226	E2	11100010	(upper right)	GRPH @
227	E3	11100011	(lower left)	GRPH #
228	E4	11100100	(lower right)	GRPH $
229	E5	11100101		GRPH %
230	E6	11100110		GRPH
231	E7	11100111	(upper)	GRPH Q
232	E8	11101000	(lower)	GRPH W
233	E9	11101001	(left)	GRPH E
234	EA	11101010	(right)	GRPH R
235	EB	11101011		GRPH A
236	EC	11101100		GRPH S
237	ED	11101101		GRPH D
238	EE	11101110		GRPH F
239	EF	11101111		GRPH X
240	F0	11110000	⌐	GRPH U
241	F1	11110001	—	GRPH P
242	F2	11110010	¬	GRPH O
243	F3	11110011	⊤	GRPH I
244	F4	11110100	⊢	GRPH J
245	F5	11110101	|	GRPH .
246	F6	11110110	└	GRPH M
247	F7	11110111	┘	GRPH >
248	F8	11111000	⊥	GRPH <
249	F9	11111001	┤	GRPH L
250	FA	11111010	┼	GRPH K
251	FB	11111011		GRPH H
252	FC	11111100		GRPH T
253	FD	11111101		GRPH G
254	FE	11111110		GRPH Y
255	FF	11111111		GRPH C

APPENDIX C

LSI DESCRIPTION

This appendix contains an explanation of the following LSI description.

- MSM80C85ARS (CPU)
- MSM81C55RS (PIO)
- IM6402 (UART)
- μPD1990AC (TIMER)
- MC14412 (MODEM)
- TC5518BF-25 (RAM)
- LH-535618 (ROM)

(1) MSM80C85ARS (CPU)

1 chip, 8 bit C-MOS Microprocessor.

The MSM80C85ARS (80C85) is an 8-bit parallel Central Processing Unit (CPU). It's instruction set is a full compatible with the 8080A microprocessor.

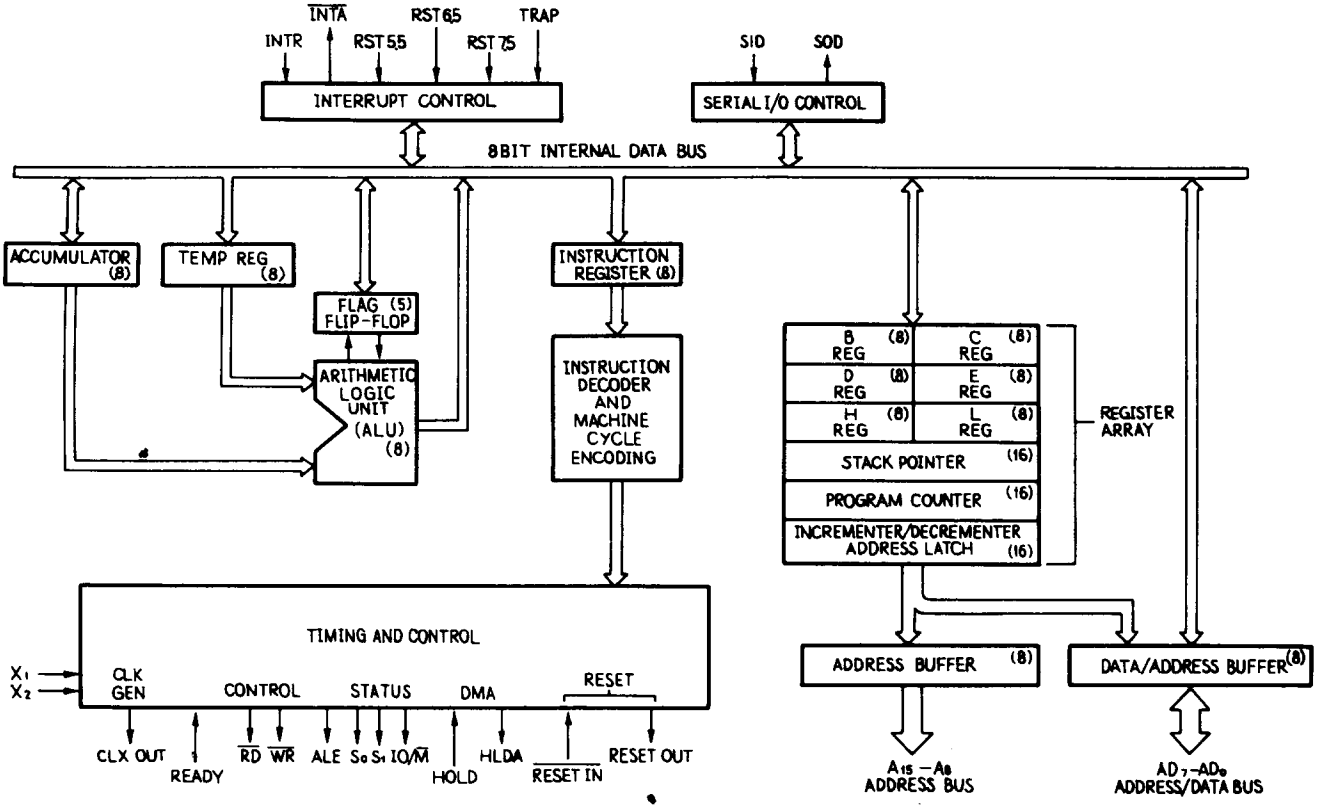
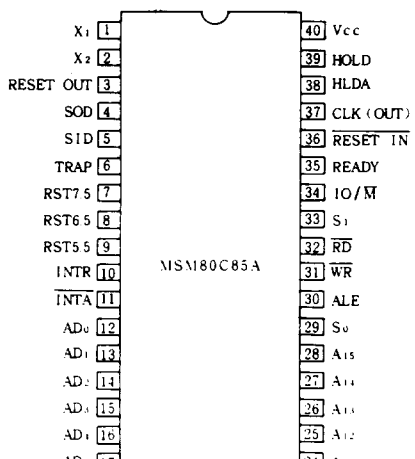


Fig. C-1 80C85 Functional Block Diagram



(a) 80C85 FUNCTIONAL PIN DESCRIPTION

Symbol	Function
$A_8 - A_{15}$ (Output, 3-state)	Address BUS: The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.
AD_{0-7} (Input/Output, 3-state)	Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
ALE (Output)	Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.
S_0, S_1, and IO/$\overline{M}$ (Output)	Machine cycle status:

IO/$\overline{M}$	S_1	S_0	Status
0	0	1	Memory write
0	1	0	Memory read
1	0	1	I/O write
1	1	0	I/O read
0	1	1	Opcode fetch
1	1	1	Interrupt Acknowledge
*	0	0	Halt
*	X	X	Hold
*	X	X	Reset

* = 3-state (high impedance)

X = unspecified

S_1 can be used as an advanced R/$\overline{W}$ status. IO/$\overline{M}$, S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.

$\overline{RD}$ (Output, 3-state)	READ control: A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.
$\overline{WR}$ (Output, 3-state)	WRITE control: A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. 3-stated during Hold and Halt modes and during RESET.

Symbol	Function
READY (Input)	If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the CPU will wait and integral number of clock cycles for READY to go high before completing the read or write cycle.
HOLD (Input)	HOLD indicates that another master is requesting the use of the address and data buses. The CPU, upon receiving the hold request, will relinguish the use of the bus at the completion of the current bus transfer (internal processing can continue). The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.
HLDA (Output)	HOLD ACKNOWLEDGE: Indicates that the CPU has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the bus one half clock cycle after HLDA goes low.
INTR (Input)	INTERRUPT REQUEST: is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.
$\overline{INTA}$ (Output)	INTERRUPT ACKNOWLEDGE: is used instead of (and has the same timing as) $\overline{RD}$ during the Instruction cycle after an INTR is accepted.
RST 5.5 RST 6.5 RST 7.5 (Inputs)	RESTART INTERRUPTS: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 1. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.
TRAP (Input)	TRAP interrupt is a nonmaskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5 – 7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table C-1.)
$\overline{RESET\ IN}$ (Input)	Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{RESET\ IN}$ is a Schmitt-triggered input, allowing connection to an RC network for power-on RESET delay.

RESET OUT (Output)	Indicates CPU is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X_1, X_2 (Input)	X_1 and X_2 are connected to a crystal, LC, or RC network to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK (Output)	Clock Output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.
SID (Input)	Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
SOD (Output)	Serial output data line. The output SOD is set or reset as specified by the SIM instruction.
Vcc	+5 volt supply.
GND	Ground Reference.

Name	Priority	Address Branched to (1) when Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge AND high level until sampled.
RST7.5	2	3CH	Rising edge (latched).
RST6.5	3	34H	High level until sampled.
RST5.5	4	2CH	High level until sampled.
INTR	5	See Note (2)	High level until sampled.

Table C-1 80C85 Interrupt Priority, Restart Address and Sensitivity

Notes: (1) The processor pushes the PC on the stack before branching to the indicated address.
(2) The address branched to depends on the instruction provided to the CPU when the interrupt is acknowledged.

(b) 80C85 FUNCTIONAL DESCRIPTION

The 80C85 has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The 80C85 register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8 bits
PC	Program Counter	16-bit address
BC, DE, HL	General-Purpose Registers: data pointer (HL)	8 bits x 6 or 16 bits x 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

The 80C85 uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The 80C85 provides $\overline{RD}$, $\overline{WR}$, S_0, S_1, and IO/$\overline{M}$ signals for bus control. An interrupt Acknowledge signal ($\overline{INTA}$) is also provided. HOLD, READY, and all interrupts are synchronized with the processor's internal clock. The 80C85 also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the 80C85 has three maskable, vector interrupt pins and one nonmaskable TRAP interrupt.

(c) 80C85 INTERRUPT AND SERIAL I/O

The 80C85 has 5 interrupt inputs: INTR, RST5.5, RST6.5, RST7.5, and TRAP. INTR is identical in function to the 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector inde-

There are two different types of inputs in the restart interrupts. RST5.5 and RST6.5 are *high level-sensitive* like INTR (and INT on the 8080) and are recognized with the same timing as INTR. RST7.5 is *rising edge-sensitive*.

For RST7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. The RST7.5 request flip-flop remains set until the request is serviced.

Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{\text{RESET IN}}$ to the 80C85. The RST-7.5 internal flip-flop will be set by a pulse on the RST7.5 pin even when the RST7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and $\overline{\text{RESET IN}}$.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP — highest priority, RST7.5, RST6.5, RST5.5, INTR — lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher prority interrupt. RST5.5 can interrupt an RST7.5 routine if the interrupts are re-enabled before the end of the RST7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive. The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Fig. C-3 illustrates the TRAP interrupt request circuitry within the 80C85. Note that the servicing of any interrupt (TRAP, RST7.5, RST6.5, RST5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

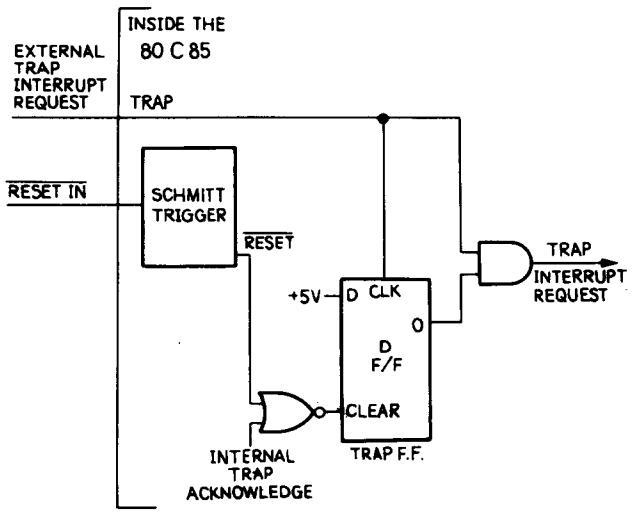


Fig. C-3 80C85 TRAP and RESET in Circuit

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disable prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR, or RST5.5–7.5 will provide current interrupt Enable status, revealing that Interrupts are disabled.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is ready by RIM, and SIM sets the SOD data.

(e) BASIC SYSTEM TIMING

The 80C85 has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Fig. C-4 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines ($IO/\overline{M}$, S_1, S_0) and the three control signals ($\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$). (See Table C-2.) The status lines can be used as advanced controls (for device selection, for example), since they become active at the T_1 state, at the outset of each machine cycle. Control lines $\overline{RD}$ and $\overline{WR}$ become active later, at the time when the transfer of data is to taken place, so are used as command lines.

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of READY or HOLD inputs). Any T state must be one of ten possible states, shown in Table C-3.

MACHINE CYCLE			STATUS			CONTROL		
			$IO/\overline{M}$	S_1	S_0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
OPCODE FETCH	(OF)		0	1	1	0	1	1
MEMORY READ	(MR)		0	1	0	0	1	1
MEMORY WRITE	(MW)		0	0	1	1	0	1
I/O READ	(IOR)		1	1	0	0	1	1
I/O WRITE	(IOW)		1	0	1	1	0	1
ACKNOWLEDGE of INTR	(INA)		1	1	1	1	1	0
BUS IDLE	(BI):	DAD	0	1	0	1	1	1
		ACK, of RST, TRAP	1	1	1	1	1	1
		HALT	TS	0	0	TS	TS	1

Table C-2 80C85 Machine Cycle Chart

Machine Strate	Status & Buses				Control		
	S_1, S_0	$IO/\overline{M}$	A_8-A_{15}	AD_0-AD_7	$\overline{RD}, \overline{WR}$	$\overline{INTA}$	ALE
T_1	X	X	X	X	1	1	1*
T_2	X	X	X	X	X	X	0
T_{WAIT}	X	X	X	X	X	X	0
T_3	X	X	X	X	X	X	0
T_4	1	0†	X	TS	1	1	0
T_5	1	0†	X	TS	1	1	0
T_6	1	0†	X	TS	1	1	0
T_{RESET}	X	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	1	0
T_{HOLD}	X	TS	TS	TS	TS	1	0

* ALE not generated during 2nd and 3rd machine cycles of DAD instruction.

† $IO/M = 1$ during $T_4 - T_6$ of INA machine cycle.

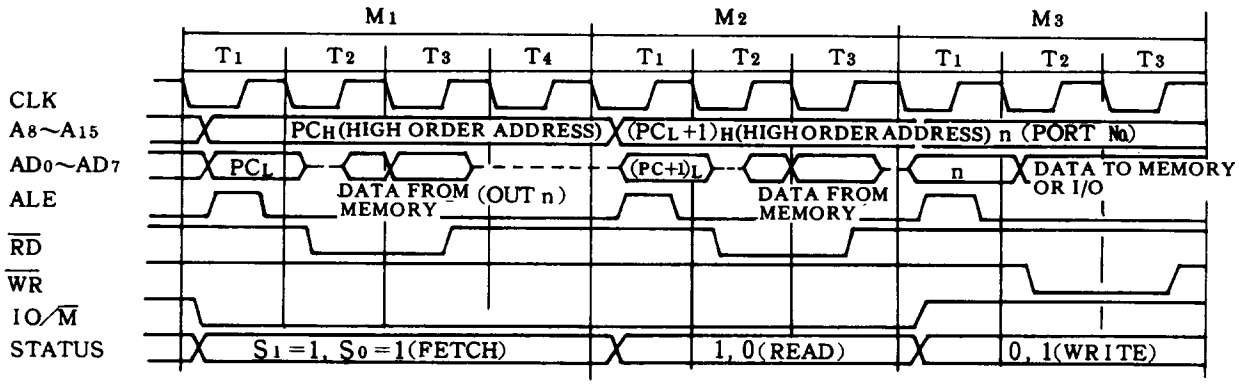


Fig. C-4 80C85 Basic System Timing

Ambient Temperature Under Bias	−40°C to +85°C
Storage Temperature	−55°C to +150°C
Voltage on Any Pin with Respect to Ground	−0.5°C to +7V
Power Dissipation	1.0 Watt

Table C-4 80C85 Absolute Maximum Ratings

(e) 80C85 WAVEFORM

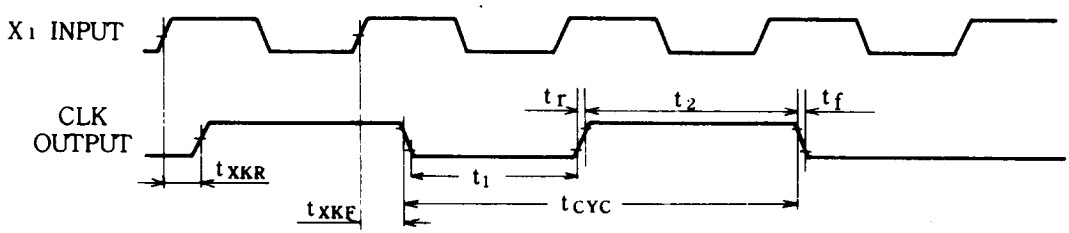
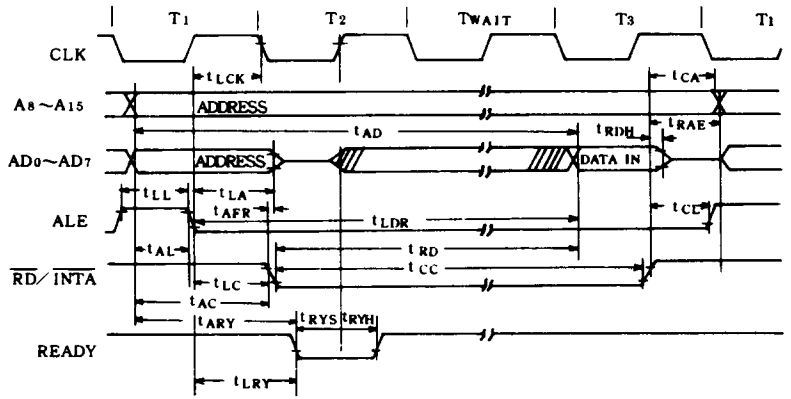
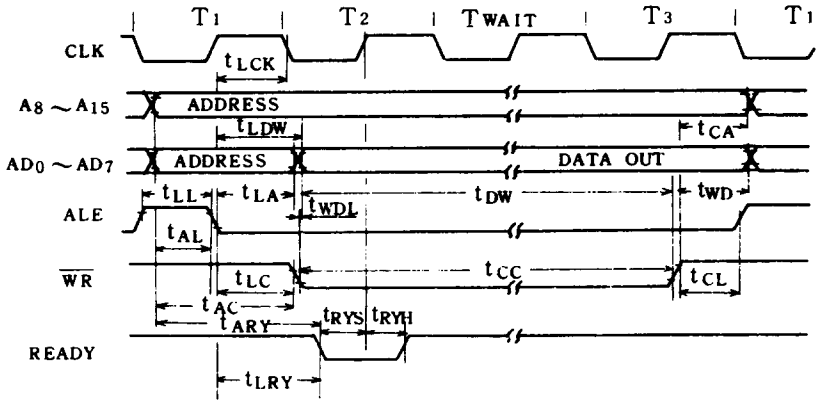


Fig. C-5 80C85 Clock Timing Waveform

Read Operation



Write Operation



Read operation with Walt Cycle (Typical) — same READY timing applies to WRITE operation

Fig. C-6 80C85 BUS Timing

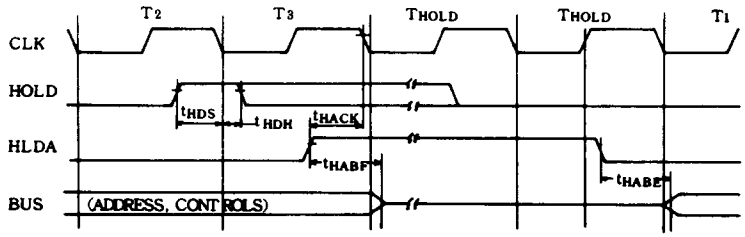
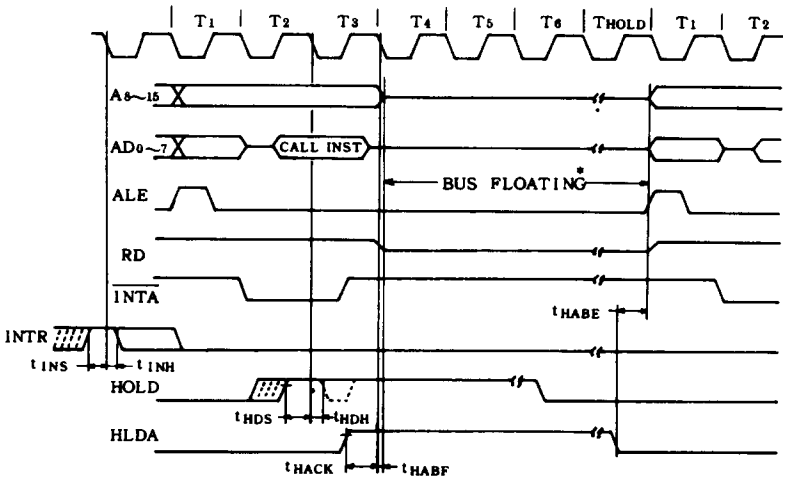


Fig. C-7 80C85 Hold Timing



* IO/M is also floating during this time.

Fig. C-8 80C85 Interrupt and Hold Timing

(2) MSM81C55RS (PIO)

C-MOS, 2048-bit STATIC RAM with I/O PORTS and TIMER

The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on the chip to provide either a square wave or terminal count pulse for the CPU system, depending on the timer mode.

The 81C55 RAM is not used in the MODEL 100. A timer/counter is used as the clock generator necessary for communication and to generate the melody.

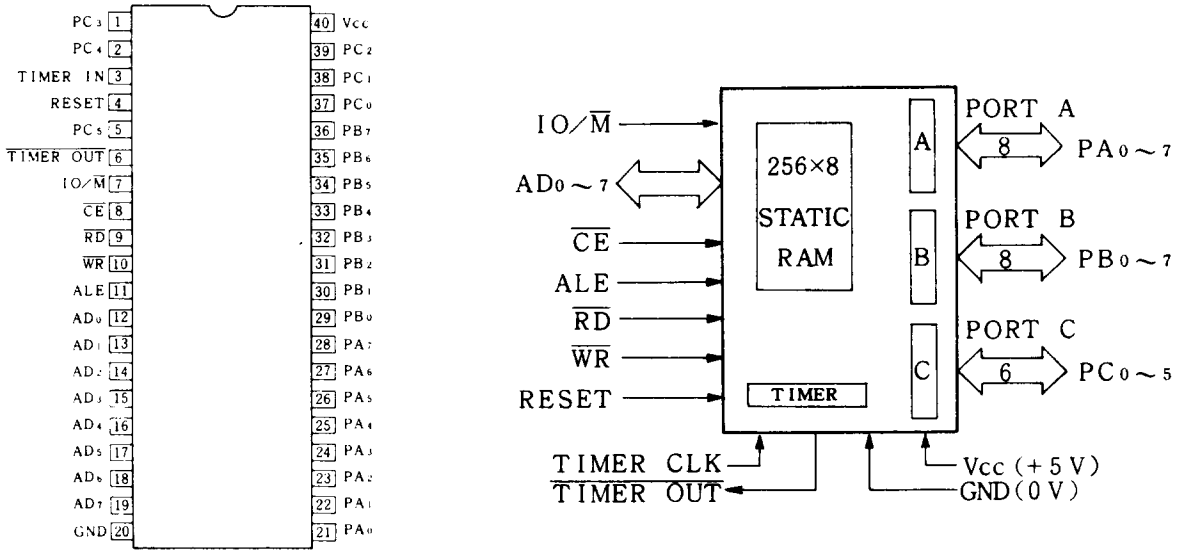


Fig. C-9 81C55 Pin Configuration and Block Diagram

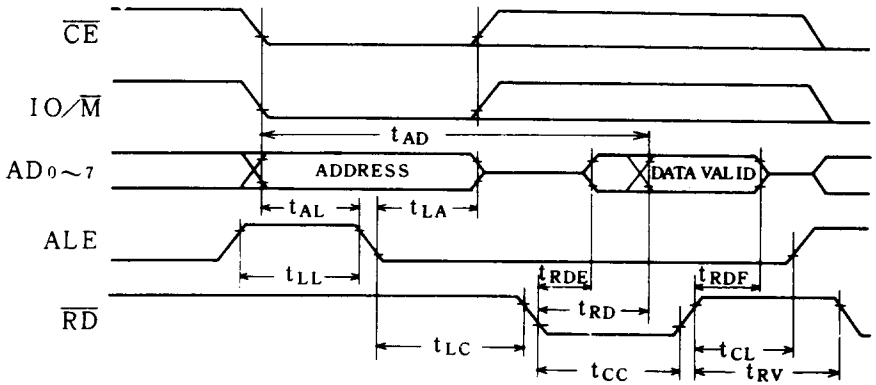
(a) 81C55 PIN FUNCTIONS

Symbol	Function
RESET (Input)	Pulse provided by the 80C85 to initialize the system (connect to 80C85 RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two 80C85 clock cycle times.
AD_{0-7} (Input)	3-state Address/Data lines that interface with the CPU lower 8-bit Address/ Data Bus. The 8-bit address is latched into the address latch inside the 81C55 on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{M}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{WR}$ or $\overline{RD}$ input signal.
$\overline{CE}$	Chip Enable:

Symbol	Function
$\overline{RD}$ (Input)	Read control: Input low on this line with the Chip Enable active enables and AD_{0-7} buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
$\overline{WR}$ (Input)	Write control: Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register depending on IO/$\overline{M}$.
ALE	Address Latch Enable: This control signal latches both the address on the AD_{0-7} lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.
IO/$\overline{M}$ (Input)	Selects memory if low and I/O and command/status registers if high.
PA_{0-7} (8) (Input/Output)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PB_{0-7} (8)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PC_{0-5} (6) (Input/Output)	These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC_{0-5} are used as control signals, they will provide the following: PC_0 – A INTR (Port A Interrupt) PC_1 – ABF (Port A Buffer Full) PC_2 – $\overline{A\ STB}$ (Port A Strobe) PC_3 – B INTR (Port B Interrupt) PC_4 – $\overline{B\ BF}$ (Port B Buffer Full) PC_5 – B STB (Port B Strobe)
TIME IN (Input)	Input to the counter-timer.
$\overline{TIMER\ OUT}$ (Output)	Timer output. This output can be either a square wave or a pulse depending on the timer mode.
Vcc	+5 volt supply.
GND	Ground Reference.

(b) 81C55 WAVEFORM

a. **Read Cycle**



b. **Write Cycle**

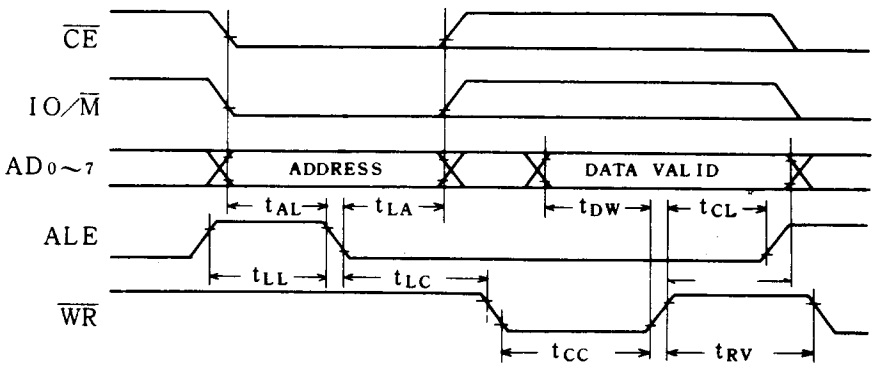
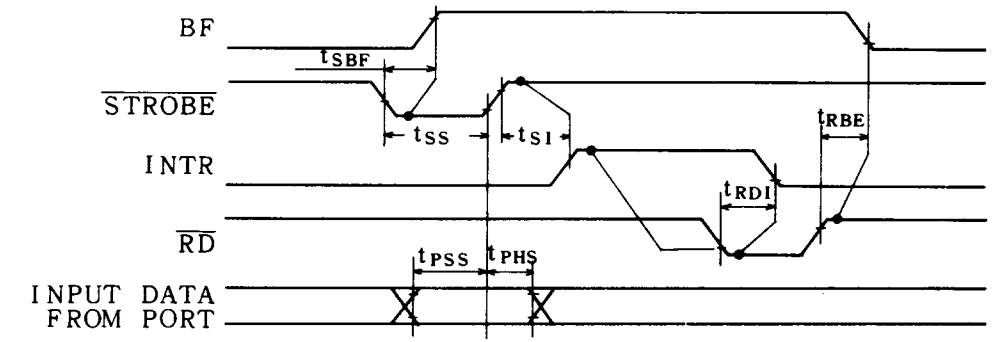


Fig. C-10 81C55 Read/Write Timing Diagrams



b. Strobed Output Mode

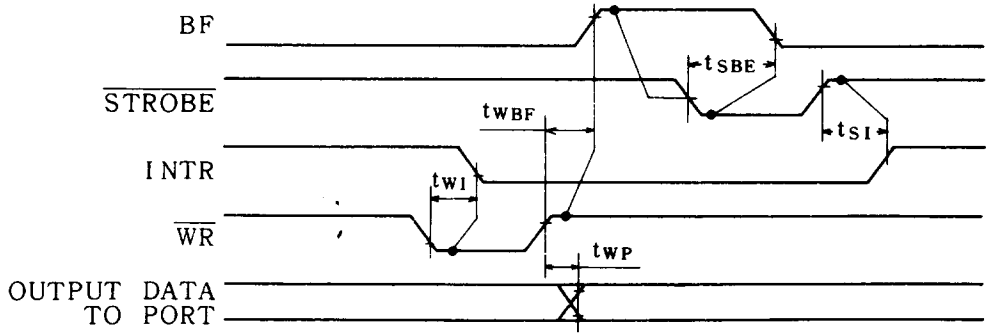
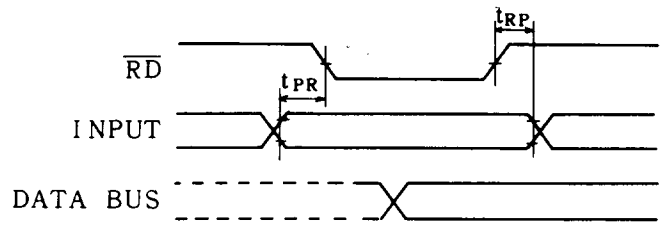
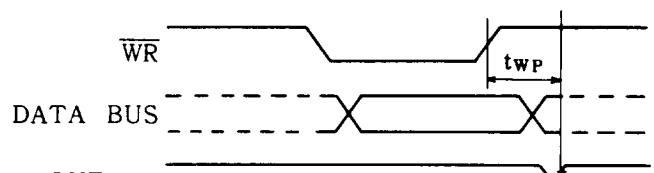


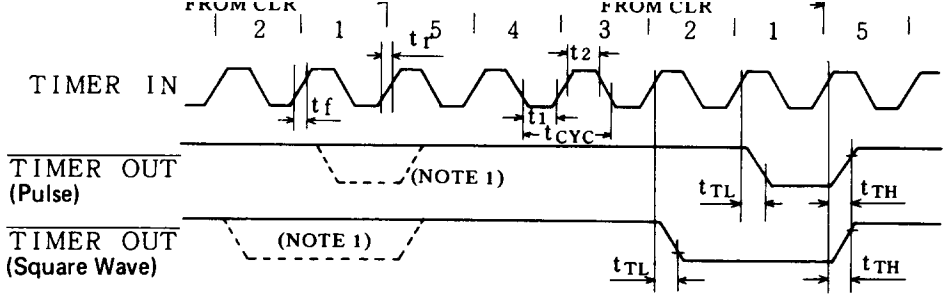
Fig. C-11 81C55 Strobed I/O Timing

a. Basic Input Mode



b. Basic Output Mode





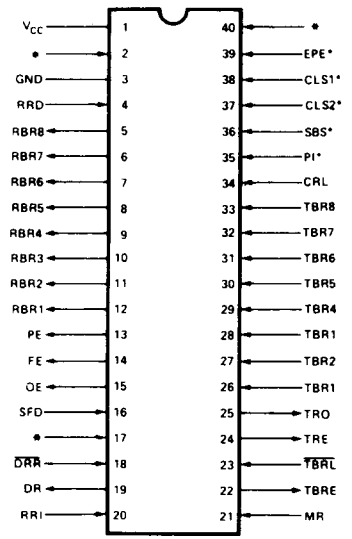
NOTE 1. The timer output is periodic if in an automatic reload mode (M1 MODE BIT = 1)

Fig. C-13 81C55 Timer Output Waveform Countdown from 5 to 1

(3) IM6402 (UART)

The IM6402 is a CMOS/LSI subsystem for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits. The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits many be one or two or one and one-half when transmitting 5 bit code.

The IM6402 can be used in a wide range of applications including modems, printers, peripherals and remote data aquisition systems. CMOS/LSI technology permits operation clock frequencies up to 2.0 MHz (125K Baud) an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 300 mW to 10 mW. Status logic increases flexibility and simplifies the user interface.



* Shown in Table C-5

Fig. C-14 IM6402 Pin Layout

CONTROL WORD					DATA BITS	PARITY BIT	STOP BIT(S)
CLS2	CLS1	PI	EPE	SBS			
L	L	L	L	L	5	ODD	1
L	L	L	L	H	5	ODD	1.5
L	L	L	H	L	5	EVEN	1
L	L	L	H	H	5	EVEN	1.5
L	L	H	X	L	5	DISABLED	1
L	L	H	X	H	5	DISABLED	1.5
L	H	L	L	L	6	ODD	1
L	H	L	L	H	6	ODD	2
L	H	L	H	L	6	EVEN	1
L	H	L	H	H	6	EVEN	2
L	H	H	X	L	6	DISABLED	1
L	H	H	X	H	6	DISABLED	2
H	L	L	L	L	7	ODD	1
H	L	L	L	H	7	ODD	2
H	L	L	H	L	7	EVEN	1
H	L	L	H	H	7	EVEN	2
H	L	H	X	L	7	DISABLED	1
H	L	H	X	H	7	DISABLED	2
H	H	L	L	L	8	ODD	1
H	H	L	L	H	8	ODD	2
H	H	L	H	L	8	EVEN	1
H	H	L	H	H	8	EVEN	2
H	H	H	X	L	8	DISABLED	1
H	H	H	X	H	8	DISABLED	2

X = Don't Care

Table C-5 IM6402 Control Word Format

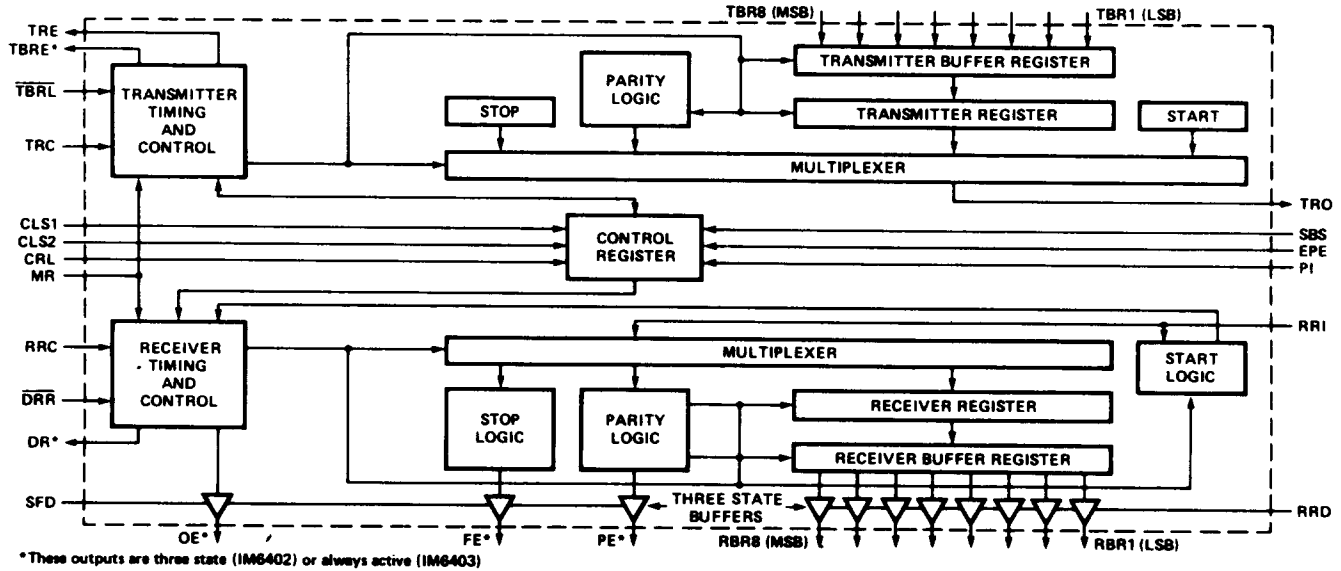


Fig. C-15 IM6402 Functional Block Diagram

IM6402 Pin Functions

Symbol	Description
Vcc	Positive Voltage Supply
NC	No Connection
GND	Ground
RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding outputs RBR1—RBR8 to a high impedance state.
RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
RBR7	See Pin 5-RBR8
RBR6	See Pin 5-RBR8
RBR5	See Pin 5-RBR8
RBR4	See Pin 5-RBR8
RBR3	See Pin 5-RBR8

Symbol	Function
RBR2	See Pin 5-RBR8
RBR1	See Pin 5-RBR8
PE	A high level on PARITY ERROR indicates received parity does not match parity programmed by control bits. When parity is inhibited this output is low.
FE	A high level on FRAMING ERROR indicates the first stop bit was invalid.
OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the received buffer register.
SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.
RRC	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
DRR	A low level on DATA RECEIVED RESET clears the data received output DR to a low level.
DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
MR	A high level on MASTER RESET clears PE, FE, OE, and DR to a low level and sets the transmitter output to a high level after 18 clock cycles. MR does not clear the receiver buffer register. This input must be pulsed at least once after power up.
TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
TBRL	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1—TBR8 into the transmitter buffer register. A low to high transition on TBRL indicates data transfer to the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end.

Symbol	Function
TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1—TBR8. For character formats less than 8 bits the TBR8, 7 and 6 inputs are ignored corresponding to the programmed word length.
TBR2	See Pin 26-TBR1
TBR3	See Pin 26-TBR1
TBR4	See Pin 26-TBR1
TBR5	See Pin 26-TBR1
TBR6	See Pin 26-TBR1
TBR7	See Pin 26-TBR1
TBR8	See Pin 26-TBR1
CRL	A high level on CONTROL REGISTER LOAD loads the control register.
PI	A high level on PARITY INHIBIT inhibits parity generation. Parity checking and forces PE output low.
SBS	A high level on STOP BIT SELECT selects 1.5 stop bits for 5 character format and 2 stop bits for other lengths.
CLS2	These inputs program the CHARACTER LENGTH SELECTED (CLS1 low CLS2 low 5 bits) (CLS1 high CLS2 low 6 bits) (CLS1 low CLS2 high 7 bits) (CLS1 high CLS2 high 8 bits).
CLS1	See Pin 37-CLS2.
EPE	When P1 is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
TRC	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

(4) μPD1990AC (TIMER)

The μPD1990AC is a C-MOS integrated circuit with a clock function which has been designed for connection to a microcomputer.

This IC independently measures the month, date, day of the week, hour, minute and second, and will output and input these time data freely upon command from the microprocessor. By employing this IC, the microprocessor is free from performing clock functions and can be devoted exclusively to other complex operations.

The μPD1990AC employes the oscillation of a 32.768 kHz crystal as a reference. All functions are enclosed in a 14-pin dual in-line package.

(a) Features

- Marks time (hours, minutes & seconds) and calendar (months, date and day of the week).
- Serial inputting and outputting of data. (Input & output code: All digits are binary coded decimals, except the month, which is a hexadecimal code.)
- The reference frequency is 32.768 kHz, which is generated by a crystal oscillator circuit.
- Provided with timing pulse outputs. (Selection of 64 Hz, 256 Hz or 2048 Hz is possible.)
- By using the CS (chip selection) terminal, multi-chip applications are possible.

(b) Function specifications

- Reference frequency (Xtal osc.)
  32.768 kHz
- Data
  Hours, minutes, seconds, months, data and days of the week ("hours" by 24 hour system) (automatic adjustment of long and short months)
- Data input-output and clock
  Serial input, serial output
  Data input and output in synchronization with the clock input from CLK.
- Time pulse output
  Either 64 Hz, 256 Hz or 2048 Hz can be selected by command.
- Mode selection
  Selected according to input to $C_0 - C_2$.
  C_2 = 0 Register control (control of data input-output)
  C_2 = 1 TP control (control of time pulses) & test control (control of test mode).
  Commands are latched by the STB (strobe) input
- Chip select
  CLK and STB inputs prohibited by CS input
- Prohibition of data output
  DATA OUT terminal will become high impedance when the OUT ENABL is input. Has no relation with other actions.

(c) Terminals

- Input terminals

DATA IN	Data input of 40-bit shift register
CLK	Shift clock input of 40-bit shift register
$C_0 - C_2$	Command input (3 bit)

CS — Chip select input (Prohibits CLS & STB)

OUT ENBL — Output control input
(Makes the DATA OUT high impedance by inputting low level)

- Output terminals
  - DATA OUT — Data output of 40-bit shift register
  - TP — Time pulse output
- Oscillation terminals
  - XTAL 1 — Oscillation inverter input (OSC IN)
  - XTAL 2 — Oscillation inverter output (OSC OUT)
- Power supply terminals
  - VDD — Plus power supply
  - GND (Vss) — Common line

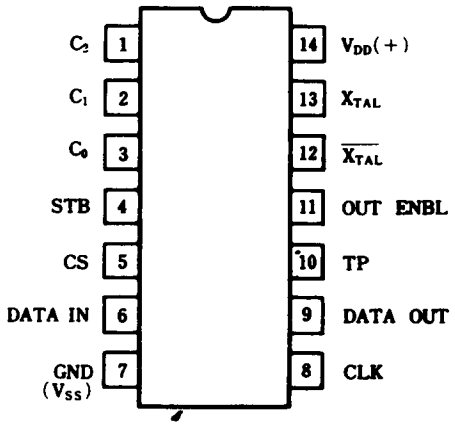


Fig. C-16 μPD1990AC Pin Layout

(d) Block Diagram

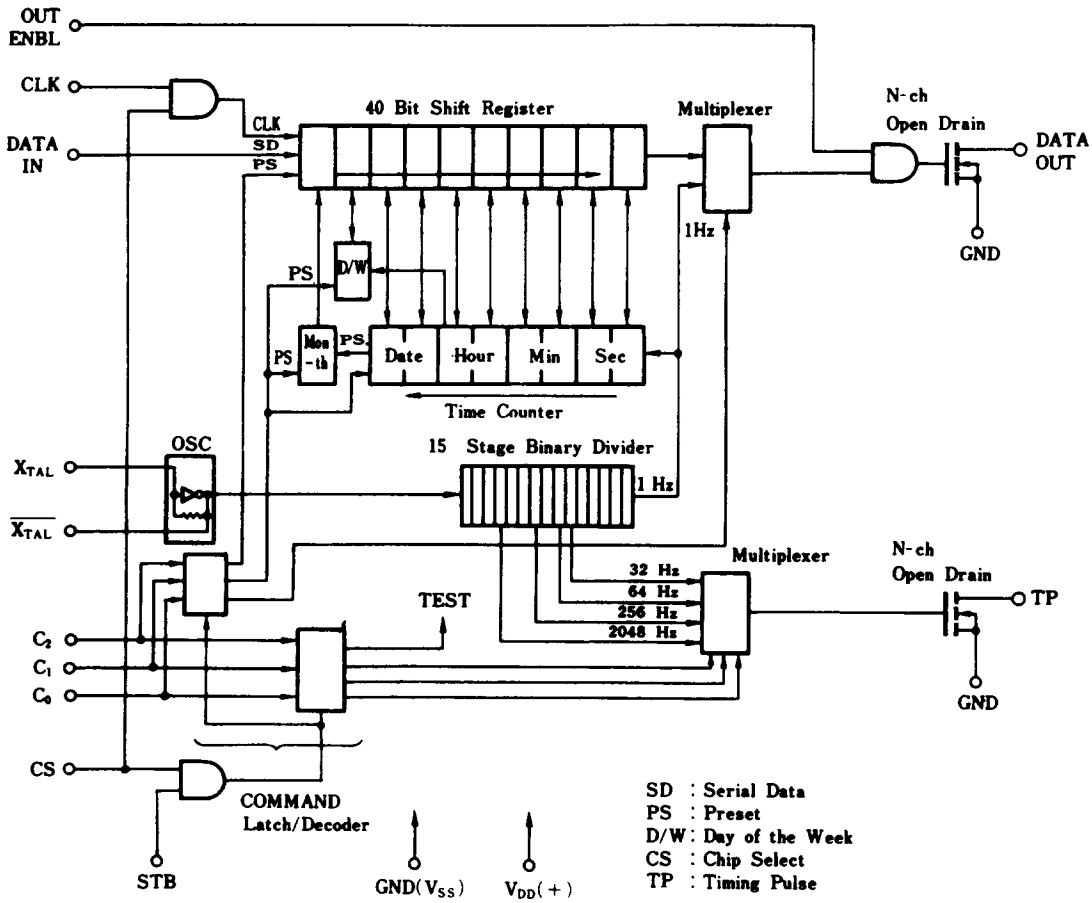


Fig. C-17 μPD1990AC Block Diagram

(e) Command Input Timing Diagram

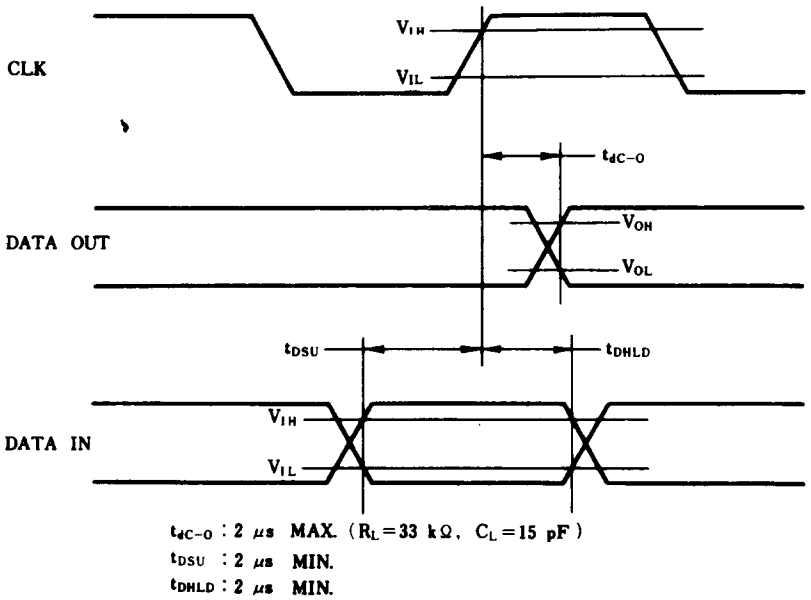


Fig. C-18 μPD1990AC Command Input Timing Diagram

Commands designated by C_0, C_1 and C_2 will be written into the latch when the STB terminal becomes high level, and will be held until a different command of the same group is written-in.

(f) Data Input/Output Timing Diagram

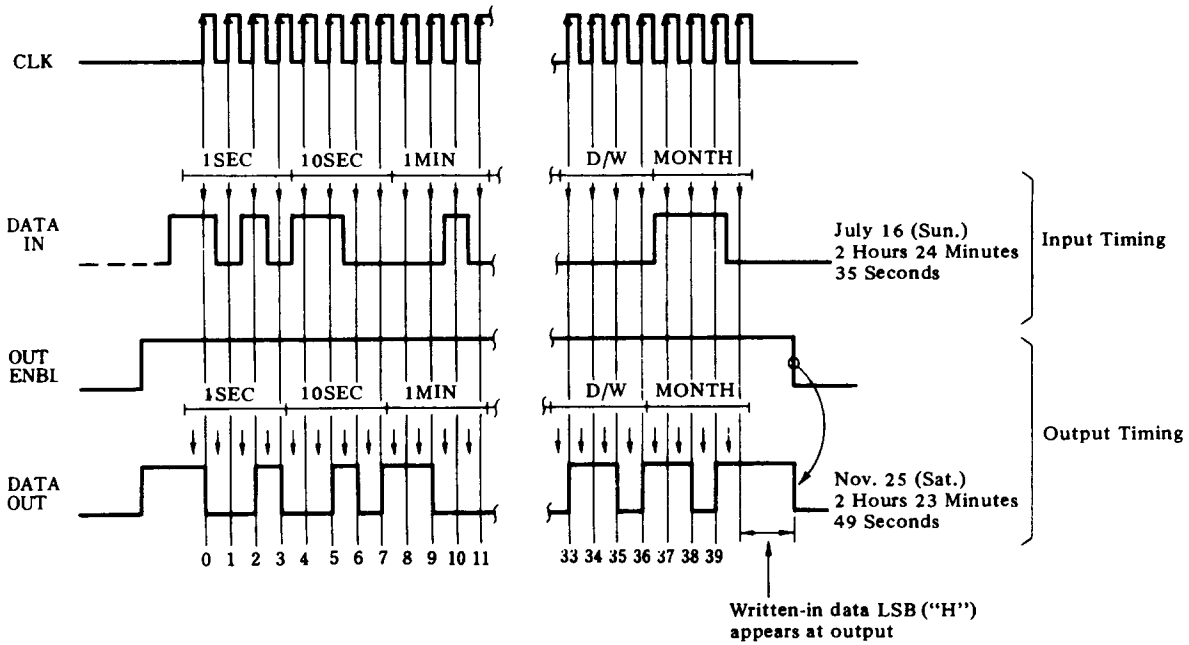


Fig. C-19 μPD1990AC Data Input/Output Timing Diagram

(5) MC14412 (MODEM)

Fig. C-22 shows the MODEM in a system application. The data to be transmitted is presented in serial format to the modulator for conversion to FSK signals for transmission over the telephone network. The modulator output is buffered/amplified before dividing the 600 ohm telephone line.

The FSK signal from the remote MODEM is received via the telephone line and filtered to remove extraneous signals such as the local Transmit Carrier. This filtering can be either a bandpass which passes only the desired band of frequencies or a notch which rejects the known interfering signal. The desired signal is then limited to preserve the axis crossings and fed to the demodulator where the data is recovered from the received FSK carrier.

Pin Functions

Symbol	Function
TYPE	The Type input selects either the U.S. or C.C.I.T.T. operational frequencies for both transmitting and receiving data. When the Type input = "1", the U.S. standard is selected and when the Type input = "0", the C.C.I.T.T. standard is selected.
Tx Data	Transmit Data is the binary information input. Data entered for transmission is modulated using FSK techniques. When operating the U.S. standard (TYPE = "1") a logic "1" input level represents a Mark or when operating in the C.C.I.T.T. standard (TYPE = "0") a logic "1" input level represents a Mark.
Tx Car	The Transmit Carrier is a digital-synthesized sine wave derived from a 1.0 MHz oscillator reference. The frequency characteristics are as follows:

United States Standard — TYPE = "1"
Transmit Frequency — ECHO = "0"

Mode	Tx Data	Tx Car
Originate "1"	Mark "1"	1270 Hz
Originate "1"	Space "0"	1070 Hz
Answer "0"	Mark "1"	2225 Hz
Answer "0"	Space "0"	2025 Hz

C.C.I.T.T. Standard — TYPE = "0"
Transmit Frequency — ECHO = "0"

Mode	Tx Data	Tx Car
Channel "1"	Mark "1"	980 Hz
No. 1 "1"	Space "0"	1180 Hz
Channel "0"	Mark "1"	1650 Hz
No. 2 "0"	Space "0"	1850 Hz

Echo Suppressor — TYPE = "0"
Disable Tone — ECHO = "1"

Mode	Tx Data	Tx Car
Chan. No. 2 "0"	"1"	2100 Hz

Symbol	Function
Tx Enable	The transmit carrier output is enabled when the Tx Enable input = "1". No output tone can be transmitted when Tx enable = "0".
MODE	The Mode input selects the pair of transmitting and receive frequencies used during modulation and demodulation. When mode = "1", the U.S. originate mode is selected (Type input = "1") or the C.C.I.T.T. channel No. 1 (Type = "0"). When Mode = "0", the U.S. answer mode is selected (Type = "1") or the C.C.I.T.T. channel No. 2 (type input = "0").
ECHO	When the Echo input = "1" (Type = "0", Mode = "0", Tx Data = "1") the demodulator will transmit a 2100 Hz tone for the disabling line echo suppressors. During normal data transmission, this input should be low = "0".
Rx Data	The Receive Data output is the digital data resulting from demodulating the Receive Carrier.
Rx Car	The Receive Carrier is the FSK input to the demodulator. This input must have either CMOS or TTL compatible logic level input (see TTL pull up disable) at a duty cycle of 50% ± 4%, that is a square wave resulting from a signal limiter.
Rx Rate	The demodulator has been optimized for signal to noise performance at 200, 300, and 600 bps. The Receive Carrier must change frequency for more than half of the selected data rate period before the Receive Data output will change.

Data Rate	Rx rate	Type
0–200 bps	"1"	"0"
0–300 bps	"1"	"1"
0–600 bps	"0"	"1"

SELF TEST	When a high level (ST = "1") is placed on this input, the demodulator is switched to the modulator frequency.
Reset	This input is provided to decrease the test time of the chip. In normal operation, this input may be used to disable the demodulator (Reset = "1") – otherwise it should be tied low = "0".
Osc in, Osc out	A 1.0 MHz crystal is required to utilize the on chip oscillator. A 1.0 MHz square wave clock can also be applied to the Osc in input to satisfy the clock requirement. When utilizing the 1.0 MHz crystal, external parastic capacitance, including crystal shunt capacitance, must be < 9 pF at the crystal input.

TTLD

To improve TTL interface compatibility, all of the inputs to the MODEM have controllable P-channel devices which act as pull-up registors when TTLD input is low ("0"). When the input is taken high ("1") the pull up is disabled, thus reducing power dissipation when interfacing with CMOS.

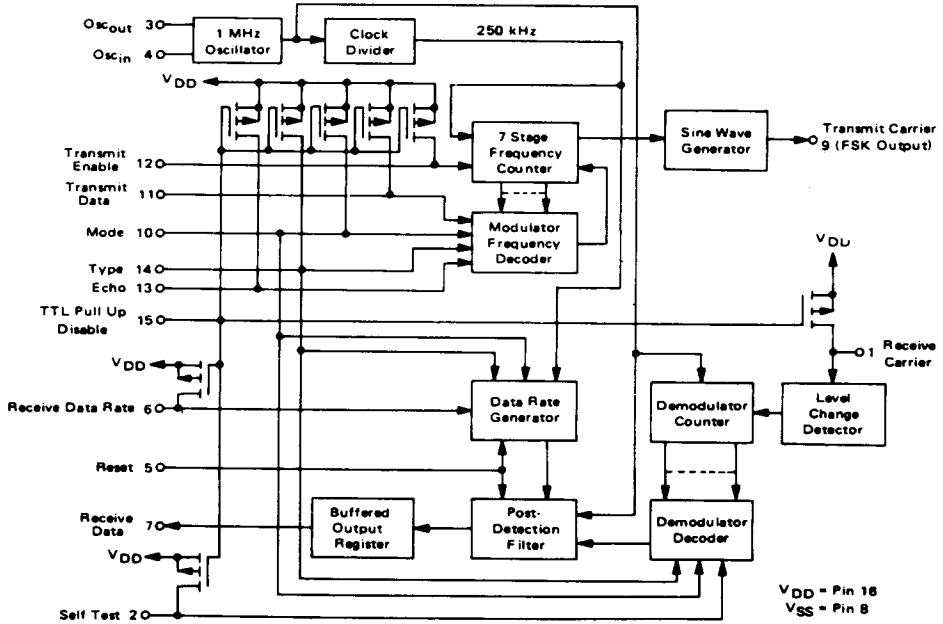


Fig. C-20 MC14412 System Block Diagram

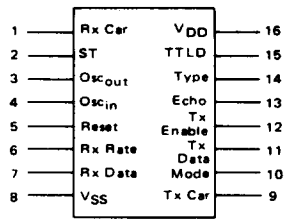
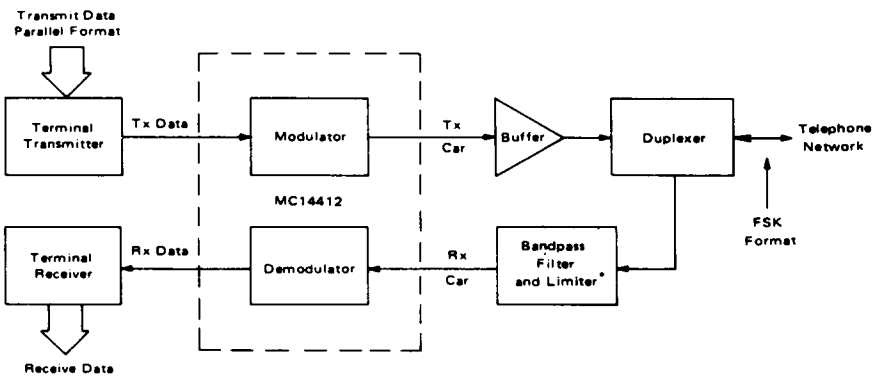


Fig. C-21 MC14412 Pin Layout



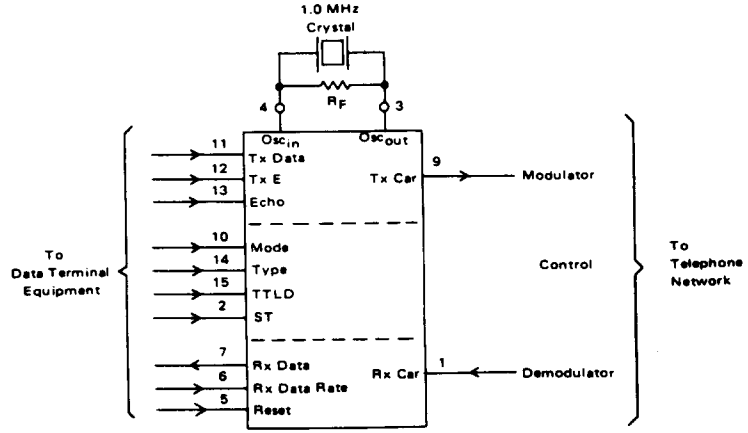


Fig. C-23 MC14412 Input Output Signals

(6) TC5518BF-25 (RAM)

The TC5518BF-25 is a 16384-bit high speed and low power fully static Random Access Memory organized as 2048 words by 8 bits. This IC has two chip enable inputs, $\overline{CE_1}$ and $\overline{CE_2}$, which are used for device selection and can be used in order to achieve the minimum standby current mode easily for battery back up.

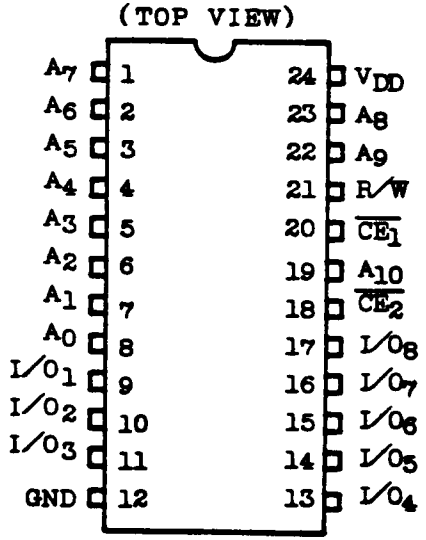


Fig. C-24 TC5518BF-25 Pin Layout

Pin Name	Description
$A_0 \sim A_{10}$	Address Inputs
R/W	Read/Write Control Input
CE_1, CE_2	Chip Enable Inputs
$I/O_1 \sim I/O_8$	Data Input/Output
GND	Ground

Table C-6 TC5518BF-25 Pin Assignment

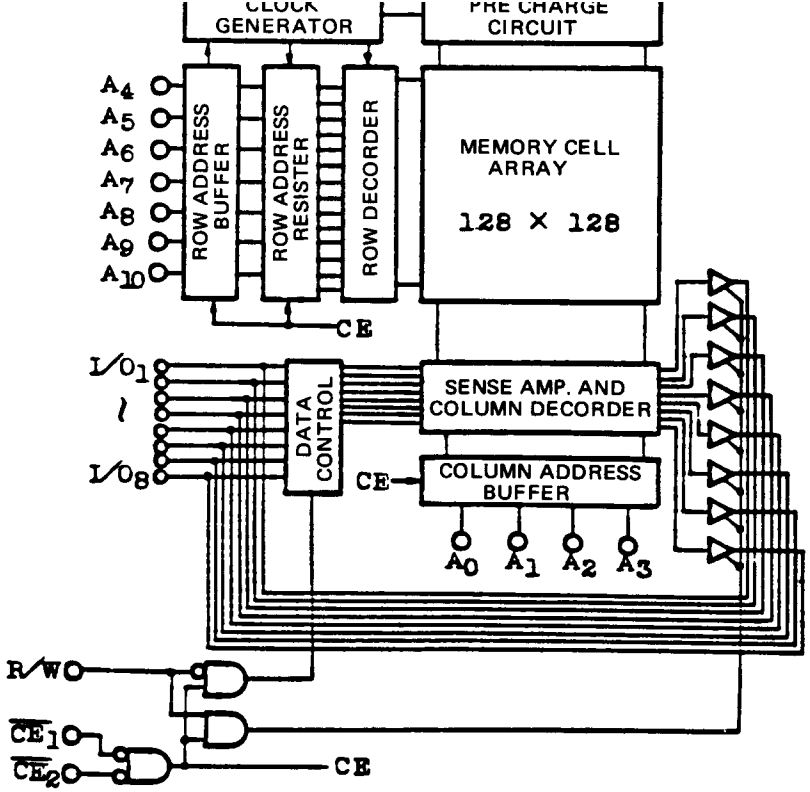
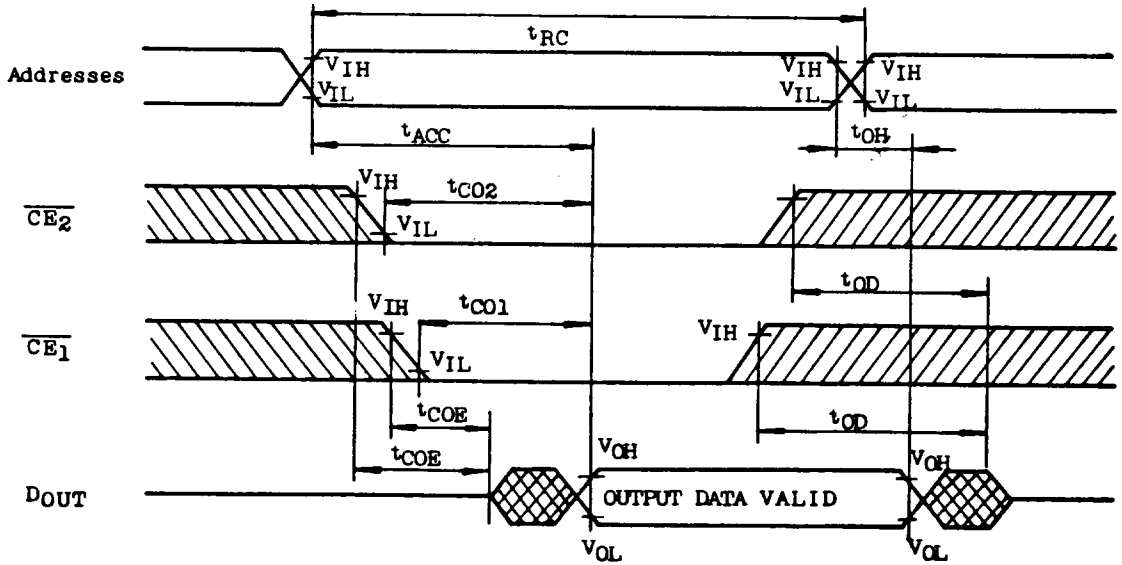
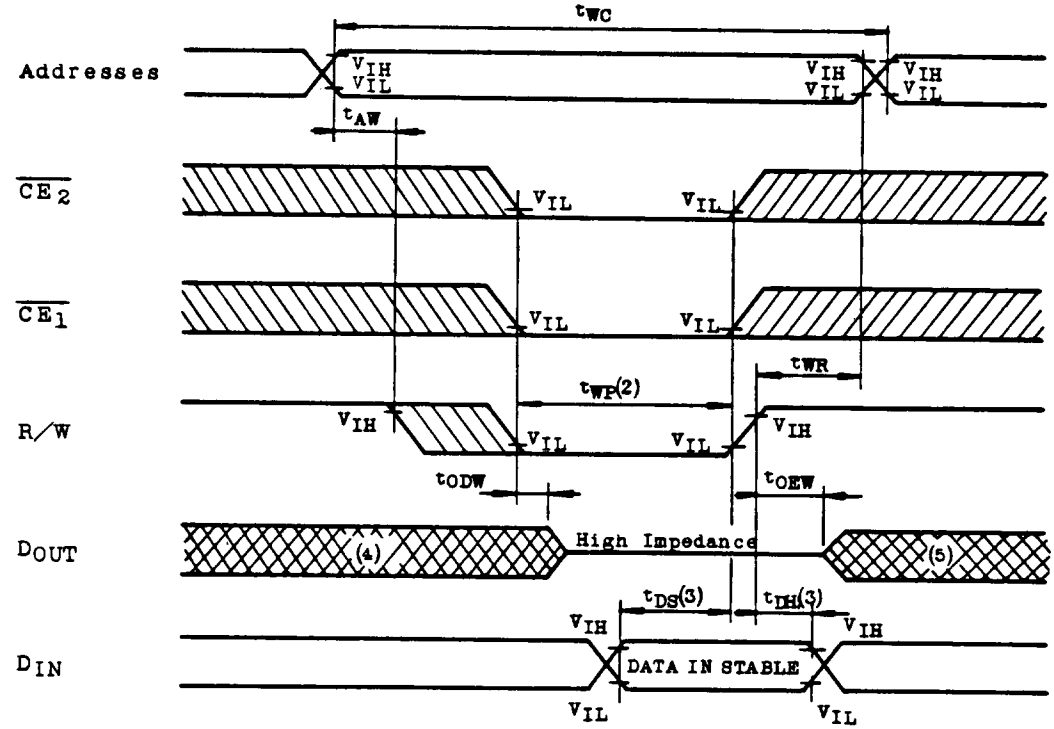
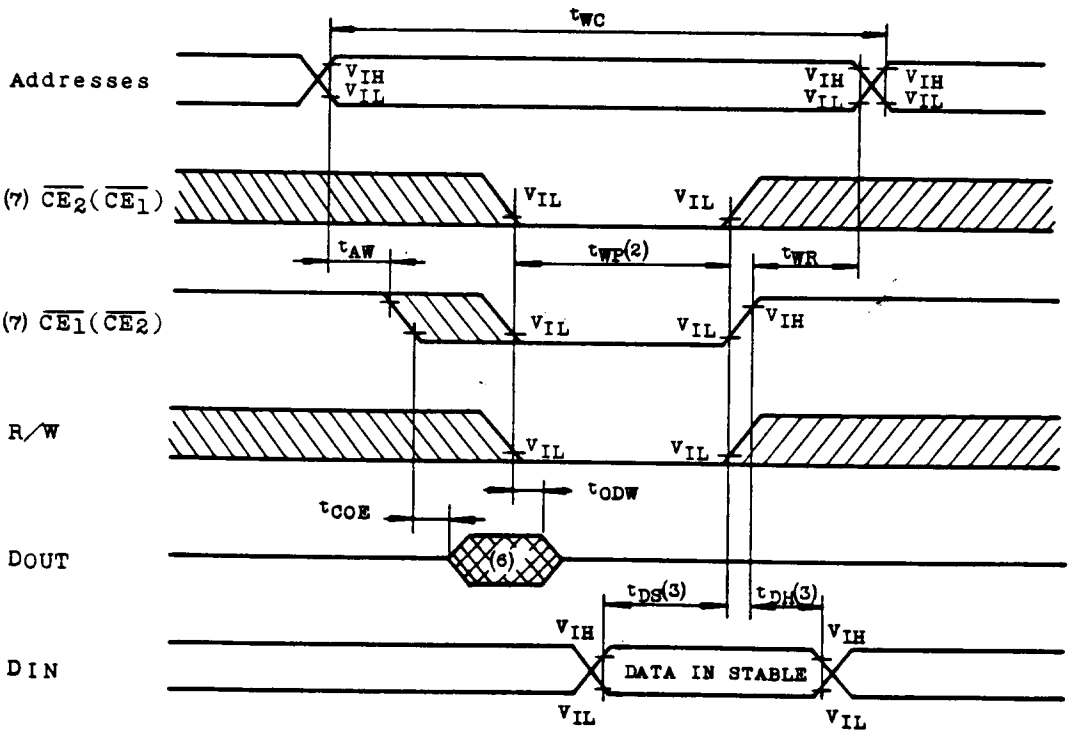


Fig. C-25 TC5518BF-25 Block Diagram





Write Cycle 2.



(7) LH-535618 (ROM)

The LH-535618 is a static mask Read Only Memory organized as 32768 words by 8 bits, fabricated with a silicon-gate CMOS process.

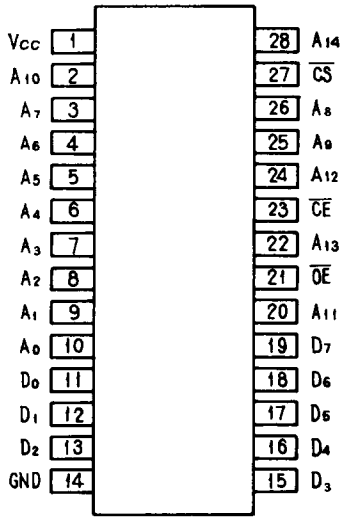


Fig. C-28 LH-535618 Pin Layout

Pin Name	Description
$A_0 \sim A_{14}$	Address Inputs
CS	Chip Select Input
CE	Chip Enable Input
OE	Output Enable Input
$D_0 \sim D_7$	Data Outputs
Vcc	Power Supply

Table C-7 LH-535618 Pin Assignment

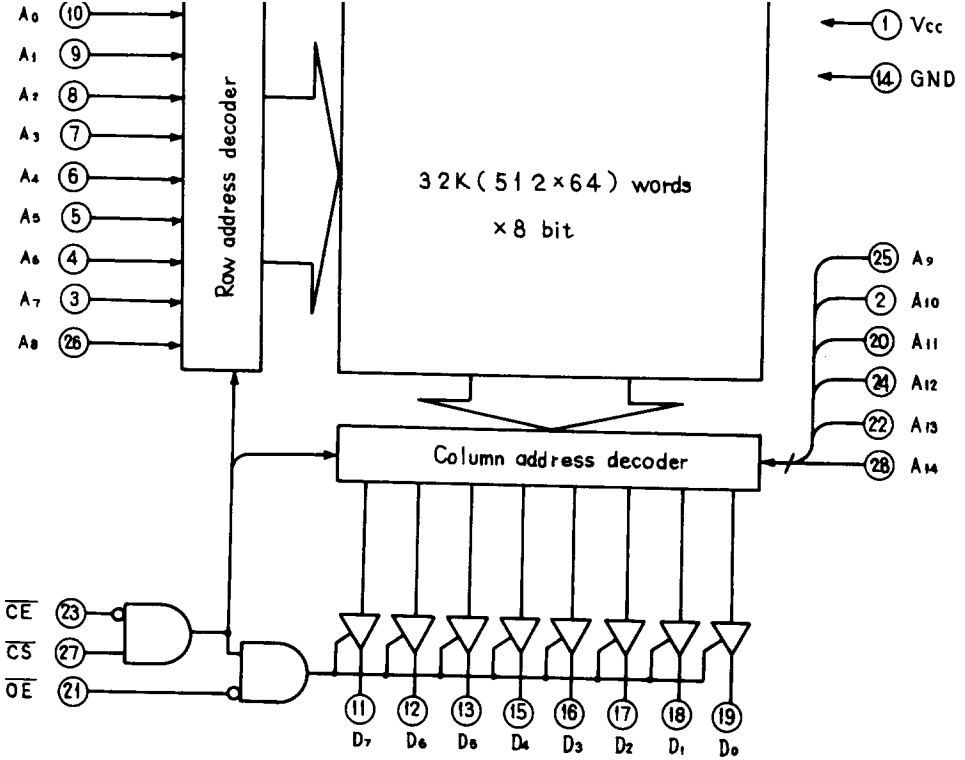
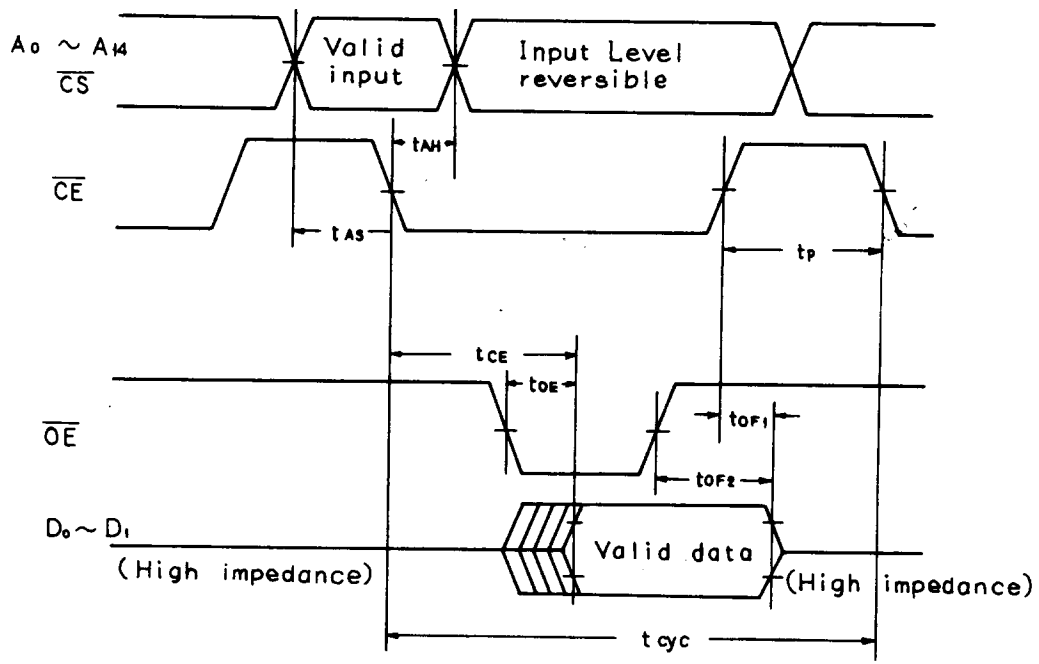


Fig. C-29 LH-535618 Block Diagram



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