BIO – 1 BUFFERED INTERFACE BOARD

FOR S–100 SYSTEMS

USER'S MANUAL

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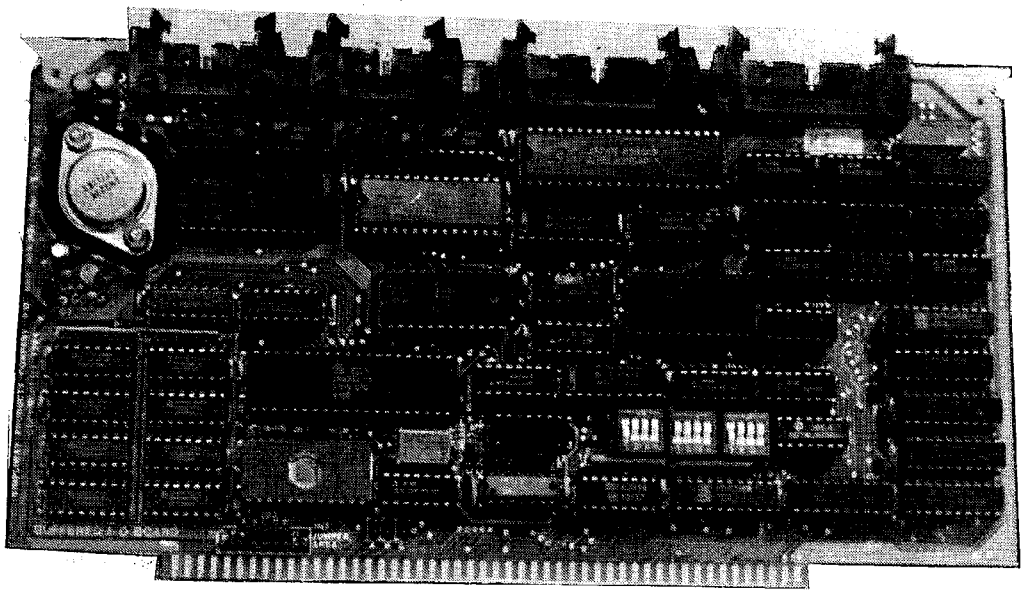
FRONT COVER: The front cover was printed on an Epson MX-80 line printer, using a program that generates characters on a dot-by-dot basis. The program takes two minutes to compute the dot pattern, and without the BIO-1, aprox. 8 minutes to print (4 MHz system). The host computer becomes dedicated to this task for this time. But with the BIO-1, this print time is reduced to about 4 minutes. The whole data file is down loaded to the BIO-1 64 Kbyte ram, and the host is released.

Please note:

The BIO-1 is a somewhat complex product, and its construction should not be attempted by those without some previous experience in assembling and testing circuits of similar complexity. Should you feel it is too difficult a project, please feel free to return the complete un-assembled product for a cash refund, after obtaining prior permission from SPC.

B I O - 1

S-100 BUFFERED INTERFACE BOARD



THE FEATURES of the BIO-1 ARE:

-- Two BUFFERED RS-232 Serial ports
-- TWO BUFFERED Parallel ports, with handshaking
(one input & one output port)
-- Buffer areas in ram are DYNAMICALLY ALLOCATED
-- All 4 I/O ports are buffered simultaniously
-- One PROGRAMABLE TIMER under system control
-- Programable baud rates from 110 to 19,200 baud
-- 3 serial printer protocols: XON/XOFF, ETB/ACK, & EXT/ACK
-- 16 Bit I/O port addressing
-- I/O port address switch selectable to any group of 16
-- Independent Vector interrupts
-- Space compression in printer buffer mode
-- 64 Kbytes of buffer ram on board ('4164's , 200 ns.)
-- Expandable to 256 KBYTES with NO HARDWARE MODS
-- Ideal for multi-user systems
-- Easy to adapt software; source code is included
-- All functions of the board are under software control
-- Uses only EASY-TO-GET parts

BIO-1 DETAILED PRODUCT DESCRIPTION

The BIO-1 Buffered Interface Board provides complete I/O to peripheral devices, such as serial or parallel line printers, display terminals, modems, keyboards, etc. The parallel output port can also be used for control functions. The MOST IMPORTANT FEATURE of this board is its 64 Kbyte buffer ram and Z80 CPU, which allows the host computer to down load as many as three files to the 1 parallel, and 2 serial output ports. The board will automatically allocate a portion of this ram to each file, as determined by the size of file (up to the 64K/256K limit). It then will continue to simultaneously communicate with each of the peripheral devices, independent of the host system, and thus frees the host of this overhead.

The serial ports support the standard 6-wire RS-232 interfacing for bi-directional I/O. The baud rates of each port is programmable form the host, in 8 speeds from 110 to 19,200 baud. Three handshake protocols are supported; XON/XOFF, ETX/ACK, and ETB/ACK. A break signal may also be sent and received.

The programable timer can be set and triggered by the system, or triggered by an external gate signal, and its time-out will cause an interrupt to the host system. Full extended addressing is supported, as defined by the IEEE-696 S-100 Standard. Interrupts are handled by user strapped vector interrupt lines (VIO-7) or the main interupt line.

As an aid in hardware interfacing, an adapter board is available, the BI/O-IB. With a DB-25 connector, this board mounts to an opening in the rear panel of your computer. A ribbon cable then extends back to the proper port of the BI/O-1, connectorized at both ends. The same PC board can function as either a serial or parallel interconnect, depending on how (and which) parts are inserted. When wired for serial operation, pull-up resistors and jumpers are provided to simplify the definition of the handshake protocol, and whether the I/O device is a "receiver" or "transmitter".

The buffer consists of 8, 4164 ram devices for 51 Kbytes of useable buffer. However, the BIO-1 will accept the new 41256 rams, WITHOUT modifiation to the board, or the addition of piggy-backed boards. Therefore, you can upgrade to 256 Kbytes of buffer, when the price and availability of these rams improve. The software presently provided only accomodates one page (64 Kbytes) of on-board memory.

The FR4 PC board is of high quality, with plated thru holes, solder plated runners, solder masks on both sides, a component side legend, and gold plating on the 100 contact S-100 edge connector.

A UTILITY Program is also available to allow you to modify the BIO-1 at any time to meet new system requirements. Some of the commands are: Change baud rate of either serial port, buffering on/off, printer despool control, copy/clear buffer, page pause, space compression control, hand-shake protocols, and much more. This program runs under CP/M (tm), and is supplied with the source code, as well as the source and data for the on-board eprom.

Specifications subject to change without notice.

ASSEMBLY INSTRUCTIONS

Start by obtaining a small needle nose pliers and wire cutter, a screwdriver, a flat work surface, and a strong light. A rosen core solder is mandatory for printed circuit work, and the thinner .032 diameter type is preferred. Use a 25-40 watt soldering iron with a small chisel or pencil tip. Apply the iron to the circuit pad to be soldered, apply the solder to the pad, touching the iron as well, and add enough solder to wet the tip and pad. Hold the iron on long enough to cause the solder to bubble down into the plated thru hole. If not enough heat is used, flux may form around the component lead and leave an intermittant or cold solder joint. If too much heat is used, the foil pad will lift off the board, and the component may be damaged as well.

The general procedure is to start with those components that have the lowest profile (height), then add the next lowest parts, etc., until all the components are soldered. The component side of the board has the component legend. Insert the leads of the component into the correct holes as shown by the legend (and printed component placement guide), seat the part as close to the board as possible, and bend the leads over at about a 45 degree angle. Then solder as described above and clip the leads as close as possible to the board. The recommended assembly order follows:

[] First, examine the board for visible shorts. If possible, use an ohmmeter to check for shorts between address lines, data lines, between +5 v. and ground (ie: pins 14 and 7 at one of the 14 pin IC sockets), and between pins 1 & 50 on the edge connector.

[] Insert all 1/4 watt resistors:

[]	R1	330 ohm	(orange-orange-brown)
[]	R2,R3	560 ohm	(green-blue-brown)

[] Turn the board over, lay it on a flat surface and then solder all resistors.

[] Insert all IC sockets, noting the proper position of pin 1 on each (usually a notch in the plastic). Sockets should not be used for switches S1, S2, and S3. Place a heavy cardboard (the back of a clip-board does nicely) over the sockets, and carefully turn the sandwich over to expose the solder tails of the sockets. Solder only opposite pins of each socket (ie: pins 1 & 8 on a 14 pin socket). Now the board can be lifted without the sockets falling out. Re-heat each joint, forcing the socket down against the board to seat it properly. All this is to insure the sockets won't tear foil loose when the IC's are inserted.

[] After this, the rest of the pins on the sockets can be soldered. Be careful not to get solder bridges to adjacent runners.

[] Insert and solder the 79L12 regulator, Q2. Observe the marking on the board.

[] Insert and solder all disk ceramic capacitors:

[]	Unmarked ovals	0.01 uF, 25 v. +80/-20
[]	C2, C4, C5, C8, C9	0.01 uF, 25 v. +80/-20
[]	C1	33 pF, 25 v. +/- 10% NPO

[] Insert and solder the tantalum capacitors, noting the polarity sign (+) marked on the board:

[]	C3, C4, C7, C10	10 uF, 20 v. +/- 20%

[] Insert and solder the resistor packs. Note that pin 1 on each part faces in the same direction as the IC sockets:

[]	RP1,2,3	22 ohm, 4 per pack
[]	RP4, 5	10 kohm, 7 per pack

[] Insert and solder the 16 and 26 pin I/O sockets J1 - J4.

[] Mount Q1, the LM323, 5 volt regulator and heatsink, using 2 screws, lock washers, and nuts. Do not use an insulator under the device, but a very thin coating of heat conducting grease (Wakefield) between the device flange and the heatsink is quite desirable. The heads of the screws should be located on the solder side of the board, and care should be taken to not over-tighten them. Now solder the leads of Q1.

[] Bend the leads of the crystal at 90 degrees, taking care not to stress the points where the leads enter the bottom of the crystal case. Insert and solder. A small piece of double-sided foam tape makes an excellent retainer and shock mount.

[] Insert and solder the jumper options as described in the JUMPER SET-UP section below. If .025 inch jumper pins are desired, they should be inserted at this time. Only jumpers JU2 and JU3 (A thru E, and the 9 VI lines) need pins, as all the other jumper options are pre-wired with foil traces on the solder side of the board for the normal installation.

[] Insert and solder switch block S1. Also insert S2 and S3 if extended I/O addressing will be used.

NOTE: If extended addressing will not be used, U37 and RP5 may also be omitted. The foil trace at JU10-A should be cut, and re-wired to position B.

[] Perform a thorough visual check of the board under a strong light to locate and clear any solder bridges between adjacent pads.

[] Insert board into host system and apply power. Observe that +5 volts appears on each IC socket pin as described in the parts listing. Also check that +5 volts appears on pin 1 of each serial port socket, pin 25 of each parallel port socket, and that there is -12 volts on pin 1 of IC's U2 & U4.

[] Turn off the power, remove the board from the system, and with the board lying on a conductive, grounded surface, insert all IC's into their sockets, using the component placement guide and parts list. Take extreme care to insert each IC in the correct direction, and to observe that none of the leads of the IC's fold up under the body (a very common occurance, and VERY hard to see!).

***** SPECIAL NOTES *****

The following parts are static sensitive devices:

U5	8255A	Programmable Peripheral Interface
U9 & U10	8251A	Programmable Communication Interface
U18	8253	Programmable Interval Timer
U26	Z80	C.P.U.
U31	2716 (2732)	R.O.M.'s
U44 - U51	4164 (41256)	R.A.M.'s

STATIC PREVENTITIVE measures MUST be employed.

[] By this time, you should have prepared (or purchased) the program rom, "ROM 1". Insert this as well.

[] Replace the board into the system, apply power, and using a thumb or forefinger, quickly check the body of each part for overheating. Only the regulator Q1 should get noticeably warm after a minute or so. If any other part gets very warm, the part may be defective or inserted wrong. Turn the power off immediately and correct this!

[] Remove the power, and proceed to the Board Jumper Set-up section.

The BIO-1 should be working properly when all these checks have been successfully completed. A trouble-shooting chart is included in this document to assist in locating some hardware faults. We recognize that it may be difficult to diagnose faults on a product of this type, since the program cannot be modified directly by the host system to assist in isolating problem areas.

If a problem occurs that seems to defy easy solution, PLEASE, PLEASE call or write us. If you find a solution to a problem, again, let us know about it, as we may be able to pass it along to others similarly troubled.

Buffered I/O Board Jumper Set-up

1. System Clock using a 3.6864 MHz crystal:

   Connect JU2-A for 3.6864 MHz operation.

   Connect JU2-B for 1.8432 MHz operation.

   Remember, if you wish to use 3.6864 MHz, the following IC's must be capable of this speed: Z80A, 2716-1, 8251, 8253, 8255, and the 4164's/41256's (200 nS).

2. Board Address Selection

   Switch blocks SW1, SW2, and SW3 select the board address. The address maybe on any boundary of 16. This ranges from 0 to FFF0H.

   Switch "on" is a logical "0".
   Switch "off" is a logical "1".

   Looking directly at the board, the switches have the following meaning.

SW1	SW2	SW3
A4 A5 A6 A7	A8 A9 A10 A11	A12 A13 A14 A15

   For example, the address 15D0H would look like this:

SW1 "D"	SW2 "5"	SW3 "1"
off-on-off-off	off-on-off-on	off-on-on-on
1 0 1 1	1 0 1 0	1 0 0 0

   Some older cpu boards cannot generate a 16 bit I/O extended address. If this is true on your board, cut the plated jumper JU10-A and connect JU10-B.

3. Reset Mode

   The board, as supplied, is reset only by POC* (pin 99 of the S100 bus). By cutting the plated jumper JU1-C, and connecting JU1-B, RESET* (pin 75) can be used. I/O CLEAR (pin 54) can be used by connecting JU1-A instead of JU1-B.

4. Interrupts and Vectored Interrupts

Jumpers for input interrupts from the three input ports (serial A, serial B, parallel A) and the timer are provided. The interrupt jumper holes are marked INT, and VI0 to VI7. The input ports are marked:

A - timer
B - DO NOT USE
C - parallel A
D - serial B
E - serial A

5. External Timer Gate

An external timer gate can be used if the plating jumper JU9 is cut, and an external gate source connected to the hole marked EXT. GATE. A low (0 volts) at this point will inhibit the count, and a high (5 volts) will enable the count.

NOTE: When the timer times-out, only an interupt can be generated - no data is output to the S-100 data bus.

Buffered I/O board Opcodes

All of the following opcodes are used by writing to the command port XXX2H.

Example:

```
      cmdport   equ  12H  ;set address of command port

b1200:  mvi a,13H     ;set opcode for Serial B to 1200 baud.
        out cmdport   ;send opcode to buffered I/O board.
        ret           ;return to system
```

1. Baud Rate

This opcode selects the baud rates for the serial ports. The table below lists the opcode numbers for Serial ports A and B.

Baud	Serial A	Serial B
110	00H	10H
300	01H	11H
600	02H	12H
1200	03H	13H
2400	04H	14H
4800	05H	15H
9600	06H	16H
19200	07H	17H

The default baud rates are 9600 baud for serial A and 300 baud for serial B.

2. Counter Functions

The spare timer in the 8253 IC has been set up to generate an interrupt after a 16 bit binary number has been counted down to zero by the on-board clock (1.8432 MHz). Opcodes have been provided to load a 16 bit binary number, start the counter, and reset the counter. To determine the 16 bit binary number, use the following formula:

binary number (HEX) = desired time (in Sec.) x 1,843,200
or N = T x 1,843,200

The minimum time that should be used is 100 microseconds and the maximum is 35.5 milliseconds.

example: 1 mSec. x 1,843,200 = 1843 decmal (rounded off)

1843 D = 0733 H and 07 H = MSB, 33 H = LSB

A. Loading Counter

To load the counter, a proper sequence must be followed in order to insure correct board operation, and a good count. The "set counter" opcode must be followed by the least significant byte (LSB) of the count, and then by the most signifcant byte (MSB) of the count. If any other command opcodes are sent to the buffered I/O board before the squence is finished, those opcodes will be interpreted as the count number.

NOTE: Loading the counter does NOT reset the interrupt. However, starting the counter does reset the interrupt.

The "set counter" opcode is listed below:

20H	Set counter period.	The next two bytes following
xxH	LSB count	this opcode will be loaded
xxH	MSB count	into the counter.

B. Start Counter

The counter is started after receiving the opcode:

21H	Start count	An interrupt will be generated at the end of the count.

C. Reset Counter

The interrupt line is reset after the "reset counter" opcode has been received. Its code is listed below:

22H	Reset Counter	Resets Interrupt line & readies counter for next count.

3. Despool Functions

The despool functions are only active on output ports. The default is OFF for all functions.

A. Buffer Hold

When this function is activated, data that has been sent to the output port is saved (see B below). This allows the use of the copy buffer function. This function should only be activated when an output is to be copied. Failure to do so will use up the buffer memory.

Serial A	Serial B	Parallel B	
40H	50H	60H	Buffer hold on.
41H	51H	61H	Buffer hold off.

B. Copy Buffer

Copy buffer will RESEND to the output port, all the data stored in the buffer after "Buffer Hold" was activated. If "Buffer Hold" is not active this opcode will be ignored.

Serial A	Serial B	Parallel B	
42H	52H	62H	Copy Buffer

C. Clear Buffer

The Clear Buffer command will destroy the contents of the output buffer. The contents of an input buffer cannot be cleared.

Serial A	Serial B	Parallel B	
43H	53H	63H	Clear Output Buffer

D. Page Pause

Page pause is used for single sheet printing. After the "page pause on" command has been given, the output buffer will stop sending data to the peripheral when a Form Feed control character is found (0CH) in the data to be outputed. The output buffer will not resume sending any data until the "next page" command is given. Page pause may be turned off by using the "page pause off" command.

"Immediate pause" will stop the output buffer from sending any more data. This action is immediate and does not wait for a form feed. Sending of data will resume when the "next page" comand is given.

Serial A	Serial B	Parallel B	
44H	54H	64H	Page Pause on
45H	55H	65H	Page pause off
46H	56H	66H	Immediate pause
47H	57H	67H	Next Page

E. Space Compression

When space compression is activated consectutive spaces are stored in one byte. Up to 127 spaces may be stored in one memory location. The most significant bit (D7) is used as a space flag; if it is detected on any output data received from the host, it is assumed to be a graphics character, and not an ASCII character, and space compres sion will be automaticly turned off. Therefore, ASCII data sent to the board should not use parity, and D7 should be zero.

Serial A	Serial B	Parallel B	
48H	58H	68H	Space compression on
49H	59H	69H	Space compression off

F. Output Buffer Disable

This opcode sets the buffered I/O board in no-buffering mode. In this mode, data that is output to the board will be sent directly to the peripheral. Input data is always buffered and cannot be changed.

Serial A	Serial B	Parallel B	
4AH	5AH	6AH	No Output Buffering
4BH	5BH	6BH	Output Buffering on

4. Protocal Functions

A. Break

In RS-232 systems, a break is a constant logical 0 for more than one character length. Break is not an ASCII character and thus requires special handling.

Breaks can be immediately sent through the serial ports. Once a break is turned on it can only be turned off by the break-off code. Received breaks can be detected by monitoring the MSB of the Buffer Status Port (xxx7), NOT the Command Port.

Serial A	Serial B	
80H	90H	Break on
81H	91H	Break off

B. Handshake Protocals

XON/XOFF, ETX/ACK, and ETB/ACK protocals are supported. XON/XOFF is supported for both input and output.

Serial A	Serial B	
82H	92H	XON/XOFF on
83H	93H	ETX/ACK on
84H	94H	ETB/ACK on
85H	95H	All Protocals off

C. XON/XOFF

Whenever XOFF is sent by a peripheral, the buffered I/O board will stop sending data untill XON is received from the peripheral. Conversely, if an input buffer is filled by the peripheral, the buffered I/O board will generate an XOFF. When the buffer has free space, the XON will be sent to the peripheral.

D. ETX/ACK and ETB/ACK

Using these protocols, the buffered I/O board will send 64 data bytes to the peripheral, and then send a ETX or ETB control character. The buffered I/O board will wait for an ACK control character from the peripheral, and then send the next 64 characters. If there are less than 64 characters in the buffer, ETX or ETB will be sent after the last character.

5. Reset

The reset opcode will force the buffered I/O board to its powered-up conditions. This means the all buffers will be cleared, default baud rates set, and all functions set to their default condition.

FFH	Reset

S100 to Buffered I/O Board Handshaking.

A. Port Designations

The board has 10 I/O ports on the S100 bus. The board may be addressed on any boundry of 16, from 000XH to FFFXH. There is one input/output S100 logical port pair for each physical serial I/O port. The parallel-in and parallel-out physical ports each have one S100 port. In addition, there is one S100 command port and two S100 board status ports. List below are the port assignments. Ports xxx9 to xxxF are not used, although xxx9 is dedicated to the BIO-1 and must not be used for any other board in the system.

xxx0	I/O port status Byte
xxx1	Serial A input port
xxx2	Command Port
xxx3	Serial B input port
xxx4	Serial A output port
xxx5	Parallel A input port
xxx6	Serial B output port
xxx7	Break/Full Buffer status port
xxx8	Parallel B output port
xxx9	dedicated - don't use

B. Status Ports

1. Break/Full Buffer Status port (xxx7)

This status port should be checked before sending any data to an I/O port. This port shows which output buffers are full, since data sent to a full buffer will be discarded. This port also shows the input break status of the two serial ports. The bits in the port have the following meaning. Data bits D3,D4, & D5 are not used.

Bit	State	
D0	0	Serial A ouptut buffer NOT full
	1	Serial A output buffer FULL
D1	0	Serial B output buffer NOT full
	1	Serial B output buffer FULL
D2	0	Parallel B output buffer NOT full
	1	Parallel B output buffer FULL
D6	0	Serial B no break
	1	Serial B break received
D7	0	Serial A no break
	1	Serial A break received

2. I/O port status Byte (xxx0)

This port shows which I/O ports are ready for service.

Bit	Status	
D0	0	port xxx1 Serial A input has data for host
	1	port xxx1 Serial A NOT ready
D1	0	port xxx3 Serial B input has data for host
	1	port xxx3 Serial B NOT ready
D2	0	port xxx5 Parallel A input has data for host
	1	port xxx5 Parallel A NOT ready
D4	0	all output ports: xxx2 Command, xxx4 Serial A, xxx6 Serial B, xxx8 Parallel B are ready for data from host
	1	all output ports xxx2,4,6,8 NOT ready

D3, D5, D6, & D7 are not used.

C. Typical Service Routines

1. Input routine using Serial A:

```
;
           sainmask  equ  1          ;serial A input mask
           portstatus equ xxx0       ;
           sainport  equ xxx1        ;serial A input port
;
;
conin:     in   portstatus           ;get status byte
           ani  sainmask             ;mask bit for serial a
           jnz  conin                ;wait till ready
;
           in   sainport             ;get data from port
           ani  7fh                  ;strip parity
           ret
;
```

2. Output routine using Serial A

```
;
           bufferstatus equ xxx7     ;
           bufmask      equ 1        ;
           outmask      equ 10h      ;
           portstatus   equ xxx0     ;
           saoutport    equ xxx4     ;
;
```

```
(continuing;)

;
;CHECK PORT STATUS FIRST!!!
;
conout:   in    portstatus          ;get status byte
          ani   outmask             ;mask bit for inputs
          jnz   conout              ;wait till not full
;
;CHECK BUFFER FULL STATUS SECOND!!!
;
          in    bufferstatus        ;get buffer status
          ani   bufmask             ;mask bit for serial a
          jnz   conout              ;wait till not full
;
;THEN SEND THE DATA
;
          mov   a,c                 ;get data
          out   saoutport           ;send it
          ret
;
```

Note: It is important to remember that the port status should be checked BEFORE the buffer-full status. Failure to do this will result in lost data when a buffer fills up !!!

Connecting Peripherals to The Buffered I/O board

Please refer to the schematic for pin numbers.

1. Serial Ports

The serial ports use RS 232 output and input driver IC's. A logic HIGH is +5 Volts, and a logic LOW is -12 Volts. There are six signal lines used, with their functions and uses listed below:

TX — Serial data from Buffered I/O board to peripheral.

RX — Serial data from peripheral to Buffered I/O board.

RTS — Request to send - Output always HIGH.

CTS — Clear to send - Input needs to be HIGH to enable TX If not used by peripheral, tie CTS to RTS.

DSR — Data Set Ready - Output. HIGH means board is ready for next transmission. LOW means last transmission is being serviced, or the buffer is full.

DTR — Data Terminal Ready - Input needs to be HIGH to enable TX. If not used by peripheral, tie to RTS.

2. Parallel Input

The parallel input port uses 5 volt logic, and has 8 data lines and 2 handshake lines. The data lines of the peripheral should be connected to data lines of the port, along with the two handshake lines, Strobe and Acknowledge. A negative going pulse on the Strobe line will latch the data in the port. The Acknowledge line will go HIGH after data is strobed in, and go LOW after the data is serviced.

3. Parallel Output

The parallel output port also uses 5 volt logic, and has 8 data and 2 handshake lines. The data lines of the peripheral should be connected to data lines of the port, and the two handshake lines (Strobe and Acknowledge) should also be connected to their respective lines. When new data is present the Strobe line goes LOW. The Strobe will stay LOW until the peripheral pulls the Acknowledge line LOW. If the peripheral does not have an Acknowledge line, the Strobe line should be tied to the Acknowledge line.

NOTE: The Simpliway Products Co. BIO-IB Interconnect board is useful in making these connections. Refer to the pricing sheet for more information, or contact SPC.

Buffered I/O Board Theory of Operation

A. General

The Buffered I/O Board is designed to be a general purpose buffer between the peripheral and the host computer. This frees the host from waiting for a peripheral (e.g. printer) to be ready for the next byte. Conversely, a peripheral (e.g. modem) can dump its data at full speed without fear of the host losing any data.

The board itself is a self contained computer system with I/O to both the host computer and peripherals. The heart of the system is a Z80 uP with 2k of ROM and 64K of RAM. The peripheral I/O is handled by the low cost Intel I/O IC's, the 8251, 8253, and 8255.

B. S100 to Z80 interface.

IC's, U-36 & U-37 are comparitors which match the address selected by switches SW 1, 2, and 3, with the address on the S100 buss. SW 2 and SW 3 select the extended I/O address, and SW 1 selects the most significant nibble of the 8 bit standard I/O address. The least significant nibble is used to select the 10 I/O ports on the board. One half of U-28 is used to buffer lines A0 to A3. U-21 is the port decoder which is enabled if there is an address match from U-36 and U-37, and the presence of SIN or SOUT.

If A0 to A3 is a 2, 4, 6, 8, or 9, and PWR* is active, the buss data is latched in U-38, and the port address is latched in U-12. This method of input into the board saves the hardware of having a I/O latch for 5 input ports. When this port is loaded by the host, the Z80, U-26, is interrupted via the interrupt priority IC, U-19. The Z80 then reads the latched address and routes the data accordingly.

If A0 to A3 is a 0, 1, 3, 5, or 7, and DBIN is active, the port data is put out on the S100 buss. IC's that hold port data are: U-2, U-3, U-4, U-5, and U-6.

The board port status is read through port 0, while Buffer status is read through port 7. Port status is stored in flip-flop's in U-13 and U-35. They set and reset the port being accessed by the Z80 or by the host.

C. Z80 to the internal I/O System

The Z80 accesses its I/O ports through address decoders U-27 and U-20. The Z80 reads the status of the S100 ports through U-28. The status of the I/O IC's is read from their own status registers.

The Z80 addresses the ROM through the address decoder made up of OR gates in U-7 & U-6. The ROM occupies the first 2K of the memory space (2716 rom, version 1.x software). This decoder also disables RAM addressing to prevent buss contention between the ROM and RAM.

The rest of the memory space is made up of 64k DRAM's. The flip-flop U-50 controls the RAS and CAS sequence to the DRAM'S. IC's U-16 & U-17 multiplex the address to the DRAM'S. The refreshing is done via the refresh line from the Z80, which prevents CAS from being activated during a memory refresh. (41256's must be the type that use RAS-before-CAS refresh).

All inputs to the board, whether from a peripheral or the host, are serviced by interrupts. The priority interrupt controller U-19 arbitrates the interrupts to the Z80. When an interrupt is received, the controller, via the buffer U-11, places the address of the interrupt on the buss during the interrupt acknowledge. This vectors the Z80 to the correct service routine. The priority is in the following order:

1. Host, 2. Serial A, 3. Serial B, 4. Parallel A.

D. Internal I/O's to the Peripheral's

The two serial ports use the INTEL 8251A ACIA's. For details on their operation please refer to Intel data sheets. The The 8251A's, U-9 & U-10, drive standard RS 232 drivers U-1 & U-3 (1489) for input, and U-2 & U-4 (1488) for output. The handshake functions DTR, DSR, RTS, and CTS are supported by both hardware and software. The 'A' version is needed for proper BREAK function operation.

The two parallel ports use the INTEL 8255 P.I.O., U-5. For details on its operation, again please refer to INTEL data sheets. Port A is configured for input, with two hand shake lines; one is Data Strobe, and the other is Data Buffer Full. Port B is simularly configured for output, and also has two hand-shake lines; one is Data Strobe, and the other is Acknowledge. Of the remaining I/O ports, two are used for interrupting the Z80, and the last two are reserved for future use (banked memory using 41256's).

One-half of the timer IC, an INTEL 8253 TIMER, is used as the baud rate generator for the two serial ports. The remaining half of U-18 is used as an independent program able timer, with interrrupt to the host. The gate which controls the count can be accesed for external use. For details on its operation please refer to INTEL data sheets, and the previous section on BIO-1 Opcodes.

SOFTWARE OVERVIEW

The following two programs are useful in checking the performance of the BIO-1, or trouble-shooting. Besides checking memory, the signal paths to and from the S100 bus and peripherals can be observed with a logic probe or oscilloscope. This should be done whenever the user suspects that a problem may not just involve memory. The user simply programs either program into a spare 2716 eprom, starting at address 0000H. Execution starts whenever there is a system hardware reset.

"BUFFER.ASM" is the main program for the BIO-1 eprom, 'ROM-1'. This is version 2.x, and it only supports 64 kbytes of un-banked ram. The source code is provided with this manual as a separate document, but for convienence, a disk is available from SPC that contains the HEX, COM, and ASM files to aid in programming/modification. At a future time, a second version to handle 256 Kbyte of on-board banked memory (using a 2732 eprom) will be offered.

```
0000      ;
0000      ;
0000      ;
0000      ; 'BUFFERED I/O BOARD MEMORY EXERCISE PROGRAM 9/20/84'
0000           ;
0000      ;    This program exercises memory to help with touble-
0000      ;    shooting the memory circuits.  As with the
0000      ;    MEMBUF.Z80 program, this program is placed in an
0000      ;    eprom, and used in place of the BUFFER.COM routine.
0000      ;
0000      ;         ORG      0000H
0000      ;
0000 210008    START:  LD       HL,800H     ;LOAD HL WITH TOP OF MEMORY
0003 110100            LD       DE,1        ;LOAD DE FOR 1 WITH ADD
0006 3E55              LD       A,55H       ;LOAD SOME DATA
0008           ;
0008 77        LOOP:   LD       (HL),A      ;EXERCISE (FOR WRITE USE
0009                                        ; LD    A,(HL))
0009 19                ADD      HL,DE       ;INCREMENT POINTER
000A 38F4              JR       C,START     ;IF > FFFFH START OVER
000C 18FA              JR       LOOP        ;DO NEXT ADDRESS
0000                   END


0008 LOOP     0000 START

00 ERRORS
```

```
0000                    ;
0000                    ;
0000                    ;           TITLE 'BUFFERED I/O MEMORY TEST  9/20/84'
0000                    ;
0000                    ;   This program is a simple memory test to insure that
0000                    ;   the memory address and refresh hardware is functioning
0000                    ;   correctly.
0000                    ;
0000                    ;   The program will alternately load memory with AAH and 55H.
0000                    ;   If an error is found, the error info is put in the I/O ports:
0000                    ;   The bad data in port 1 (serial A input - xxx1),
0000                    ;   the high address in port 3 (serial B input - xxx3),
0000                    ;   and the low address in port 5 (parallel A input - xxx5).
0000                    ;   Then the Z80 is halted.  The user, with the aid of his
0000                    ;   system monitor program or a short program he/she has
0000                    ;   written, queries these ports, using any necessary opcodes.
0000                    ;
0000                    ;BEGINING OF PROGRAM
0000                    ;
0000                            ORG     0000H
0000                    ;
0000 110100             START:  LD      DE,1            ;LOAD DE WITH 1 FOR ADD
0003 210008                     LD      HL,800H         ;LOAD HL WITH START OF MEMORY
0006 36AA               NEXT1:  LD      (HL),0AAH       ;PUT AAH IN MEMORY
0008 19                         ADD     HL,DE           ;INCREMENT POINTER
0009 30FB                       JR      NC,NEXT1        ;IF NOT > FFFFH THEN DO AGAIN
000B                    ;
000B 210008                     LD      HL,800H         ;LOAD HL WITH START OF MEMORY
000E 7E                 NEXT2:  LD      A,(HL)          ;GET BYTE IN MEMORY
000F FEAA                       CP      0AAH            ;IS IT AAH????
0011 201C                       JR      NZ,ERROR        ;NO - SEND ERROR
0013 19                         ADD     HL,DE           ;YES - INCREMENT POINTER
0014 30F8                       JR      NC,NEXT2        ;IF NOT > FFFFH THEN DO AGAIN
0016                    ;
0016 110100                     LD      DE,1            ;LOAD DE WITH 1 FOR ADD
0019 210008                     LD      HL,800H         ;LOAD HL WITH START OF MEMORY
001C 3655               NEXT3:  LD      (HL),055H       ;PUT 55H IN MEMORY
001E 19                         ADD     HL,DE           ;INCREMENT POINTER
001F 30FB                       JR      NC,NEXT3        ;IF NOT > FFFFH THEN DO AGAIN
0021                    ;
0021 210008                     LD      HL,800H         ;LOAD HL WITH START OF MEMORY
0024 7E                 NEXT4:  LD      A,(HL)          ;GET BYTE IN MEMORY
0025 FE55                       CP      055H            ;IS IT 55H????
0027 2006                       JR      NZ,ERROR        ;NO - SEND ERROR
0029 19                         ADD     HL,DE           ;YES - INCREMENT POINTER
002A 30F8                       JR      NC,NEXT4        ;IF NOT > FFFFH THEN DO AGAIN
002C C30000                     JP      START           ;DO FOREVER
002F                    ;
002F                    ;       SEND ERROR ADDRESS
002F D341               ERROR:  OUT     (41H),A         ;PUT DATA IN PORT 1
0031 7C                         LD      A,H
0032 D342                       OUT     (42H),A         ;PUT ERROR ADDR H IN PORT 3
0034 7D                         LD      A,L
0035 D343                       OUT     (43H),A         ;PUT ERROR ADDR L IN PORT 5
0037 76                         HALT                    ;STOP FOR ERROR
0038                    ;
0000                            END


002F ERROR    0006 NEXT1    000E NEXT2
001C NEXT3    0024 NEXT4    0000 START


00 ERRORS
```

Despool Setup

A despool program, called "DESPOOL.COM" is available in disk format from SPC. It is a menu driven utility to assist the user in controlling output to a printer, and allows easy modification of the default parameters of the BIO-1. Please refer to pricing info page. As it is written in the 'C' language, and requires a specific compiler, the source will not be offered.

In order for the Buffered I/O board utility to work in your system, a setup file must be made. The file must be named BUF.DTA, and must reside on the currently logged disk. The file contains the port address of the Buffered I/O Board, and attributes about the CRT terminal you are using. The file must be arranged in the following manner:

1. All numbers in the file must be decimal, and separated by commas.

2. The first number is the base address of your Buffered I/O Board, in decimal. For example, if the setting of SW 1 on the board is 10H, the first number should be 16.

   NOTE: If extended I/O addressing is needed, the HOST hardware and/or software that defines which block the BIO-1 is in will need modifcation.

3. The next two numbers are the clear screen code for your CRT. If there is only one byte in your clear-screen code, then the second number should be zero.

4. The next two numbers are the cursor position codes for your CRT / Terminal. If there is only one byte in your cursor position code, then the second number should be zero.

5. The next number is the cusor offset, typically 32 .

6. The last character is an ASCII 'Y', if the column in the cursor position is first, and 'N' if the row is first.

Example for a Televidio 910/920

```
16,26,00,27,61,32,Y
 |  |  |  |  |  |  |__Y for column first
 |  |  |  |  |  |_____Cursor offset is 32
 |  |  |  |__|________Cursor position is "ESC ="
 |  |__|_____________Clear screen is "ctl Z"
 |________________Board address is 10H
```

Troubleshooting Guide

Always check for:

1. Bad solder joints
2. Bad sockets.
3. IC's inserted wrong or inserted backwards.
4. No DC voltages or shorts.
5. Folded IC pin under socket.
6. All capacitors inserted, and with correct polarity.

Problem	Probable Cause
1. Rom program not executing.	a. Bad Prom ; U-17. b. Prom addressing circuits not working; U-6, U-7. c. Ram not working; U-44 to U-51. d. Clock not working; U-34, U-35. e. Reset circuits not working; U-32, U-34.
2. Ram not functioning	a. Bad DRAM U-s 44-51. b. Refresh circuits not working; U-25, U-25, U-14. c. Prom addressing circuits not working; U-6, U-7, U-25. d. Address multiplexing not working U-16, U-17.
3. No Interrupts	a. Bad priority U-19. b. Bad driver U-11. c. Bad interrupt add. ckt. U-22.
4. S100 interface not functioning.	a. Bad status flip-flops; U-13, U-35. b. I/O drivers bad; U-39, U-43. c. I/O receivers bad; U-38, U-12, U-28. d. Bad address decoding; U-'s 36, 37, 32, 21, 23, 30, 29, 45, 22, 14, 6, 25, 34, 24, 28.
5. Serial port not functioning	a. CTS not "HI". b. Bad interrupt circuits U-19. c. Bad address ciruits U-20, U-27. d. Check lines to connector. e. Bad Timer U-18. f. Bad serial ACIA; U-9, U-10. g. Bad Reset circuit; U-34. h. Bad line drivers; U-1 to U-4
6. Parallel port not functioning.	a. Bad interrupt circuits U- 19. b. Bad address circuits; U-20, U-27 c. Check lines to connector. d. Bad parallel PIA; U-5. e. Bad Reset circuit; U-34.
7. Timer not working.	a. Bad address cicuits; U-20, U-27. b. Bad clock circuit; U-18.

Parts list for Buffered I/O Board Ver 1.0 7-27-84

IC # (U-)	PART NUMBER	DESCRIPTION	STRAPPED PINS 5V	GND	12V
1	1489	RS232 LN-RX	14	7	
2	1488	RS232 LN-TX	14	7	1
3	1489	RS232 LN-RX	14	7	
4	1488	RS232 LN-TX	14	7	1
5	8255	PIO	26	7	
6	74SL32	QUAD OR	14	7	
7	74SL32	QUAD OR	14	7	
8	74LS153	DUAL 4 LINE MUX	16	8	
9	8251A	ACIA	26	4	
10	8251A	ACIA	26	4	
11	74LS244	OCT INVERTER	20	10	
12	74LS373	OCT LATCH	20	10	
13	74LS279	HEX R-S FLIP FLOP	16	8	
14	74LS02	QUAD NOR	14	7	
15	74LS74	DUAL D-FLIP FLOP	14	7	
16	74LS157	QUAD 2-BIT MUX	16	8	
17	74LS157	QUAD 2-BIT MUX	16	8	
18	8253	TIMER	24	12	
19	74LS148	PRIORITY DECODER	16	8	
20	74LS138	8 TO 1 DECODER	16	8	
21	74LS154	16 TO 1 DECODER	24	12	
22	74SL32	QUAD OR	14	7	
23	74LS30	8-IN NAND	14	7	
24	74LS14	HEX INVERTER SMTGR	14	7	
25	74LS14	HEX INVERTER SMTGR	14	7	
26	Z80	CPU	11	28	
27	74LS138	8 TO 1 DECODER	16	8	
28	74LS244	OCT INVERTER	20	10	
29	74SL32	QUAD OR	14	7	
30	74SL32	QUAD OR	14	7	
31 *	2716	EPROM (ROM 1)	24	12	
32	74LS14	HEX INVERTER SMTGR	14	7	
33	74LS05	HEX INVERTER OC	14	7	
34	7404	HEX INVERTER	14	7	
35	74LS74	DUAL D-FLIP FLOP	14	7	
36	74LS85	4-BIT COMP	16	8	
37	74LS682	8-BIT COMP	20	10	
38	74LS373	OCT LATCH	20	10	
39	74LS240	OCT BUFFER	20	10	
40	74LS373	OCT LATCH	20	10	
41	74LS373	OCT LATCH	20	10	
42	74LS373	OCT LATCH	20	10	
43	74LS373	OCT LATCH	20	10	
44	4164	64K DRAM	8	16	
45	4164	64K DRAM	8	16	
46	4164	64K DRAM	8	16	
47	4164	64K DRAM	8	16	
48	4164	64K DRAM	8	16	
49	4164	64K DRAM	8	16	
50	4164	64K DRAM	8	16	
51	4164	64K DRAM	8	16	

* AVAILABLE PRE-PROGRAMMED FROM THE SIMPLIWAY CO.
NOTE: Use single supply, 5 volt type only.

QTY	DESCRIPTION	QTY	DESCRIPTION	QTY	DESCRIPTION
2	1489	2	74LS157	1	74LS85
2	1488	1	8253 Intel	1	74LS682
1	8255 Intel	1	74LS148	1	74LS240
5	74LS32	2	74LS138	1	74LS153
1	74LS154	2	8251A Intel	1	74LS30
2	74LS244	3	74LS14	6	74LS373
1	Z80A Zilog	1	74LS279	1	74LS05
1	74LS02	2	74LS74	1	7404
1	2716-1 (350 nS)			8	4164 (41256 ~)

\# Extended addressing only ~ Block memory only

QTY	DESCRIPTION Miscellaneous Parts
1	Q1, REGULATOR, LM323, 5v, 3a TO3 CASE
1	* HEAT SINK THERMALLOY #6013-B
18	14 PIN SOCKET
16	16 PIN SOCKET
10	20 PIN SOCKET
3	24 PIN SOCKET
2	28 PIN SOCKET
2	40 PIN SOCKET
2 EA.	16 & 26 PIN RIBBON CONNECTOR SOCKETS; 2 rows, .10" centers, .025" square post AMP : 746101-3 (16 pin), 746101-6 (26 pin) DIGI-KEY: R215-ND (16 pin), R227-ND (26 pin) MOLEX: A6797-16A (10-55-2161) (16 pin) A6797-26A (10-55-2261) (26 pin)
1	PIN HEADER STRIP, 36 pins per strip, 1 row, .10" centers, .025" square post A-P Products: 929834-01-36 or equiv.
3	SHORTING JUMPERS, A-P Products # 925250-R
38	.01uF Capacitor, Disk Ceramic, 25V, +80/-20%
4	15uF Tantalum Capacitor, 20V +/- 20%
1	30 pF Capacitor, Disk Ceramic, 25V, +/- 10% ,NPO
2	560 OHMS 1/4W 5% carbon film preferred
1	330 OHMS 1/4W 5% carbon film preferred
2	10K OHMS Resistor pack, 10%, 7 per pack DALE : MPS08A-01-103J ALLEN-BRADLEY : 708A103 BOURNES : 4608X-101-103
3	22 OHM Resistor pack, 10%, 4 per pack DALE : MPS08A-03-220-J ALLEN-BRADLEY : 708B220 BOURNES : 4608X-102-220
1	* CRYSTAL: 3.6864 MHz, HC-18 case, 32 pF, series
1	Q2, REGULATOR, -12.0 VOLTS, MC79L12 OR EQUIV.
3	DIP SWITCH, 4 position
2 EA.	6-32 X 3/8" ROUND HEAD MACHINE SCREW, NUT, LOCKWASHER
2	Ejectors Scanbe, Inc. # S-203 or equiv. (Optional)

* AVAILABLE FROM THE SIMPLIWAY CO.

QUICK REFERENCE CHART

COMMAND SUMMARY FOR BIO-1 BUFFERED INTERFACE BOARD 10-30-84

SOFTWARE VERSION 2.0 07/13/84

****

BAUD RATE	SERIAL A	SERIAL B
110	00H	10H
300	01H	11H
600	02H	12H
1,200	03H	13H
2,400	04H	14H
4,800	05H	15H
9,600	06H	16H
19,200	07H	17H

PROTOCOL FUNCTIONS	SER A	SER B
BREAK ON	80H	90H
BREAK OFF	81H	91H
XON/XOFF	82H	92H
ETX/ACK	83H	93H
ETB/ACK	84H	94H
ALL PROTOCOLS OFF	85H	95H

DESPOOL FUNCTIONS	SER A	SER B	PAR B
BUFFER HOLD ON	40H	50H	60H
BUFFER HOLD OFF	41H	51H	61H
COPY BUFFER	42H	52H	62H
CLEAR BUFFER	43H	53H	63H
PAGE PAUSE ON	44H	54H	64H
PAGE PAUSE OFF	45H	55H	65H
IMMEDIATE PAUSE	46H	56H	66H
NEXT PAGE	47H	57H	67H
SPACE COMPRESSION ON	48H	58H	68H
SPACE COMPRESSION OFF	49H	59H	69H
BUFFERING OFF	4AH	5AH	6AH
BUFFERING ON	4BH	5BH	6BH

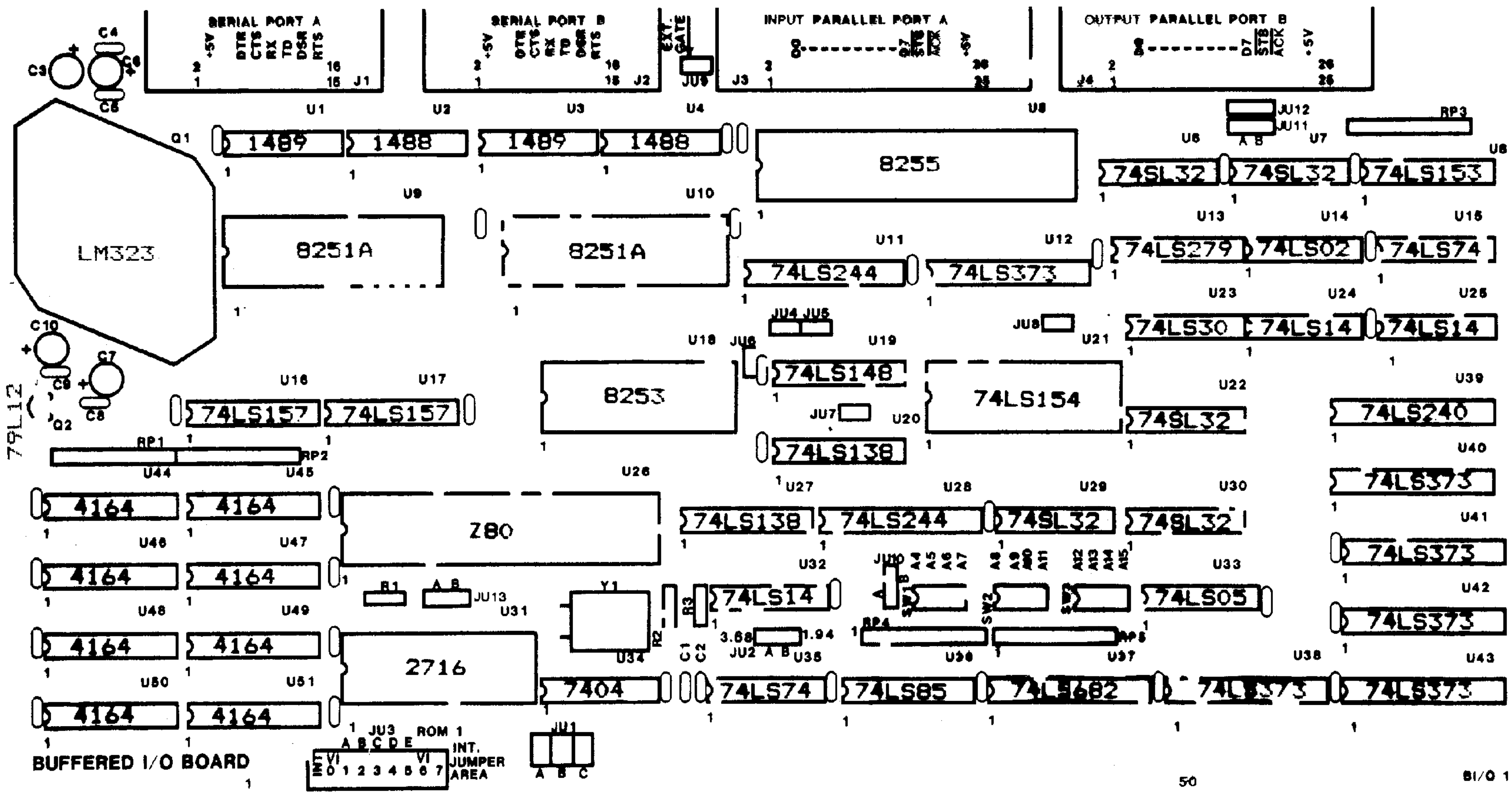
COUNTER FUNCTIONS	
SET PERIOD,	20H
LSB COUNT,	XXH
MSB COUNT	XXH
N(d)=T(sec) x 1,843,200	
START COUNT	21H
RESET COUNT	22H
SOFTWARE RESET	FFH

S100 I/O Port designations

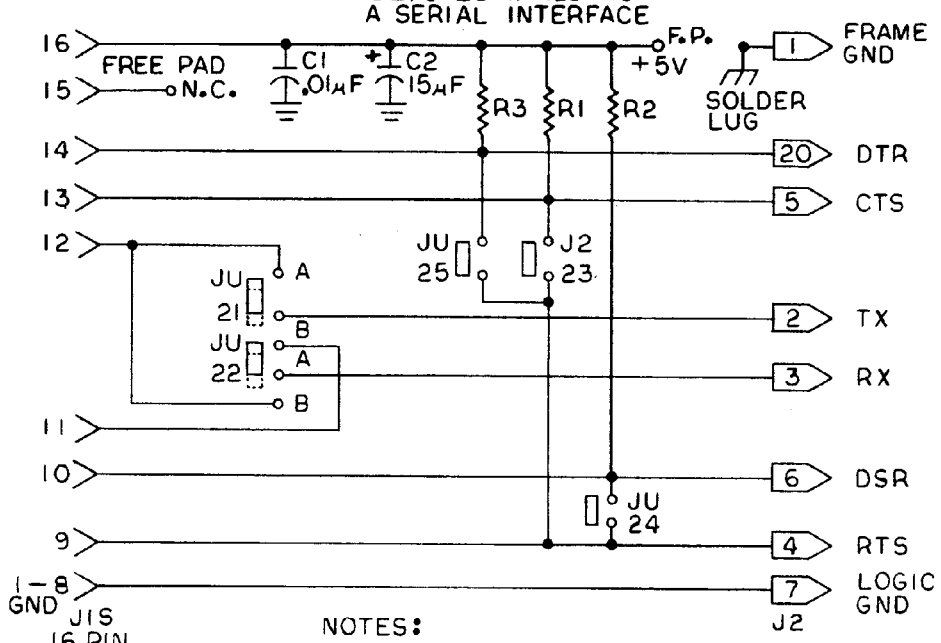
xxx0	I/O port status byte	xxx5	Parallel A input port
xxx1	Serial A input port	xxx6	Serial B output port
xxx2	Command Port	xxx7	Break/Full Buffer status port
xxx3	Serial B input port	xxx8	Parallel B output port
xxx4	Serial A output port	xxx9	dedicated - don't use

Status Ports

Bit	State	Break/Full Status port (xxx7)	I/O port status Byte (xxx0)
D0	0	Ser A ouptut buffer NOT full	port xxx1 Ser A input has data
	1	Ser A output buffer FULL	port xxx1 Ser A NOT ready
D1	0	Ser B output buffer NOT full	port xxx3 Ser B input has data
	1	Ser B output buffer FULL	port xxx3 Ser B NOT ready
D2	0	Parallel B out buf NOT full	port xxx5 Par A input has data
	1	Parallel B output buf FULL	port xxx5 Parallel A NOT ready
D4	0	N/A	all output ports ready for data: xxx2 Command, xxx4 Ser A, xxx6 Ser B, xxx8 Parallel B
	1	N/A	output ports xxx2,4,6,8 NOT ready
D5	1/0	not used	not used
D6	0	Serial B no break	Note: It is important to remember that the port status should be checked BEFORE the buffer-full status. Failure to do this will result in lost data when a buffer fills up !!!
	1	Serial B break received	
D7	0	Serial A no break	
	1	Serial A break received	


SERIAL PORT A
+5V DTR CTS RX TD DSR RTS
J1
SERIAL PORT B
J2
EXT. GATE
JU9
INPUT PARALLEL PORT A
J3
OUTPUT PARALLEL PORT B
J4
LM323
79L12
1489
1488
8251A
8255
74SL32
74LS153
74LS279
74LS02
74LS74
74LS244
74LS373
74LS30
74LS14
8253
74LS148
74LS154
74LS138
74LS157
74LS240
4164
Z80
2716
7404
74LS74
74LS85
74LS682
74LS05
Y1
ROM 1
INT. JUMPER AREA
BUFFERED I/O BOARD
50
BI/O 1

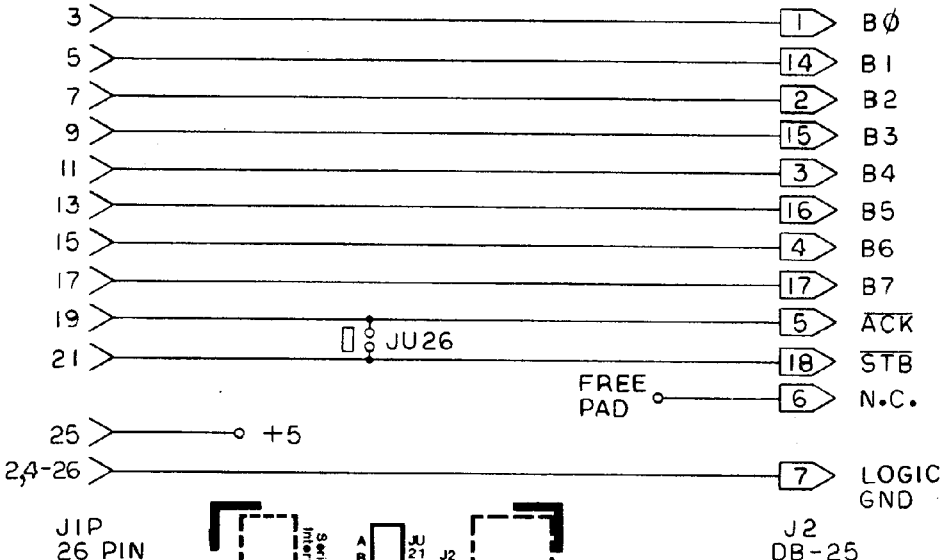
BI/O-IB WIRED AS A SERIAL INTERFACE

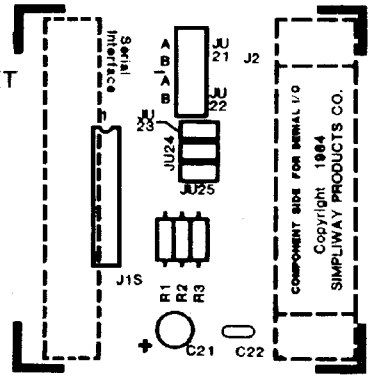


NOTES:

1. CONNECTOR PIN NUMBERING AS SEEN FROM COMPONENT SIDE OF BOARD
2. R1-R3 = 2.2K TO 10KΩ, 1/4 W, 5%

BI/O-IB WIRED AS A PARALLEL INTERFACE





TITLE	INTERCONNECT BD 1/1
DATE 10/28/84	DRAWN J.A.
SCALE ~	CHECKED
APPROVED	DRG NO. BIO-IB
Simpliway Products Company	

SERIAL SIDE LEGEND

Assembly Instructions for the BIO-IB Interconnect Board

The BIO-IB is an adapter board used as an aid in hardware interfacing. With a DB-25 connector, this board mounts to an opening in the rear panel of your computer. A ribbon cable then extends back to the proper port of the BI/O-1, connectorized at both ends. The same PC board can function as either a serial or parallel interconnect, depending on how (and which) parts are inserted. When wired for serial operation, pull-up resistors and jumpers are provided to simplify the definition of the handshake protocol, and whether the I/O device is a "receiver" or "transmitter". When wired for parallel operation, a jumper (JU 26) may be installed to connect the STB* to ACK* lines, if the peripheral does not provide the acknowledge.

SERIAL CONNECTION

First check the board on both sides visually and with an ohmmeter for shorts between runners. The component side is the side marked "Component Side for Serial I/O". Insert the following parts:

- [ ] R1, R2, R3 Resistor, 1 Kohm, 1/4 W., 5%, carbon film
- [ ] C1 Capacitor, .01 uF, 25 V., +80/-20 %, ceramic disc
- [ ] C2 Capacitor, 15 uF, 16 V., +/- 20%, Al. electrolytic
  NOTE: Observe polarity as marked on board!!

The parts above are needed only if the peripheral requires pull-up resistors on the DTR, CTS, & DSR lines.

- [ ] Pin header strips, 1 row, .01" centers, .025" square post
  JU 21,22 -- 1 strip of 5 pins
  JU 23-25 -- 3 strips of 2 pins each

JU 21 & 22 allow the sense for the TX & RX lines to be easly reversed, depending on whether the peripheral is defined as the 'transmitter' or 'receiver' (see EIA RS-232 spec).

JU 23, 24, & 25 allow the use of RTS to provide the strobe signal for the DTR, CTS, and/or DSR lines, as an alternative to the pull-up resistors. (Refer to schematic on other side of these instructions.)

- [ ] J1S DIP IC Socket, 16 pin
- [ ] J2 Connector, P.C. mount, DB 25 style, rt. angle, female
  AMP # 206584-1 or equiv.
- [ ] 4 ea. Mounting hardware: screw, 4-40 x 3/8", nut, lockwasher
- [ ] 5 Shorting jumpers, as required

PARALLEL CONNECTION

Insert the following parts on the side marked "Parallel Interface":

- [ ] Pin header strip, as above,
  J1P 2 rows 13 pins JU 26 1 row of 2 pins
- [ ] J2 Connector, P.C. mount, DB 25 style, right angle pins male or female, as required
- [ ] Hardware, as above

CONNECTOR ASSEMBLIES

Serial Interface: 2 Ft., 16 conductor ribbon cable, .050" spacing
1 16 pin DIP plug A-P # 925120-16-R
1 26 pin IDC plug A-P # 925110-26-R

Parallel Interface: 2 Ft., 26 conductor ribbon cable, as above
2 26 pin IDC plug, as above

ORDERING INFORMATION Oct. 10, 1984

TO ORDER -- Please check the items desired:

PROTOTYPING BOARD price information:

PTB-1 with documentation

[]	Bare board	$ 67.50
[]	Complete kit	$ 89.50
[]	Assembled and tested	$ 95.00
[]	Complete instruction manual (Refundable with PTB-1 purchase)	$ 5.00

<><><><><><><><><><><><><><><><><><><><><><><><><><><><><><><><><>

BUFFERED I/O BOARD price information:

BI/O-1 with documentation and ROM 1 source code.

[]	Bare board with heat-sink	$ 59.95
[]	Complete kit, 64K, WITH eprom & source	$289.00
[]	Assembled and soldered, but WITHOUT ic's or eprom. You use your own, and test it.	$159.00
[]	Assembled and tested, with 64 Kbyte of ram, 3.62 MHz crystal, and source code.	$325.00

BI/O Interface board. This board mounts to the rear panel of your computer via a DB-25 connector. It may be wired for serial or parallel port operation

[]	BI/O I-B, bare board w/documentation	$ 9.95
[]	Complete kit, serial or parallel oper.	$ 25.00
[]	Assembled and tested, serial operation	$ 35.00
[]	Assembled and tested, parallel operation	$ 30.00

Miscellaneous

[]	Serial cable assembly for BI/O I-B, 1.5 ft.	$ 10.95
[]	Parallel cable assembly as above	$ 8.95
[]	ROM 1 programmed eprom, 350 nS, with source	$ 30.00
[]	Crystal, 3.6282 MHz.	$ 7.00
[]	I-C set with programmed eprom	$145.50

Documentation

[]	Complete instruction manual, less source code	$ 5.00
[]	Source code for ROM 1	$ 15.00
	(Both above refundable with BI/O-1 purchase)	
[]	Source code for Utility Program below	$ 20.00
[]	Disk, containing the source and data files for the eprom, ROM 1, and a utility program for easy formatting of the BI/O-1 for your system (8" ss,sd)	$ 35.00

Please add $3.00 for shipping & handling (or $1.50 for documentation only) 3.00

TOTAL _______

(Please add to SUB-TOTAL on other side)

<Ordering information continued on other side>

ORDERING INFORMATION CONTINUED

VDB-A2 Video Board can be ordered in 3 ways:

[ ]	Bare board with standard 24 x 80 source code, includes heat sink and phono connector.	$ 49.50
[ ]	Complete kit less crystal & eproms (Order eproms & crystal to match Rel #, below)	197.50
[ ]	Assembled & soldered, but WITHOUT IC's/eproms you get your own & test. (state crystal Freq)	$182.50

VDB-A2 Assembled and tested, with programmed eproms

[ ]	With standard 24 x 80 source code	$269.00
[ ]	With VIDSTAR (Wordstar/dBase II) source code	279.00
[ ]	With VIDSTAR 25th line non-scrolling, status "VIDSTAR" emulates the Televideo 920 terminal!	285.00

ROM 1 Pre-programmed eproms for above source code

[ ]	Release 1.x : 24 lines x 80 characters, std.	18.50
[ ]	Release 3.x : VIDSTAR for Wordstar / dBASE II	28.50
[ ]	Release 4.x : VIDSTAR 25th line non-scrolling	32.50

Character Generator eproms, 2716, 450 nS (ok at 4 MHz)

[ ]	ROM 2 Std. alpha-numeric, 5 x 7 matrix & 1-c	18.50
[ ]	ROM 3 Graphics, Greek, & Potpourri (no source)	18.50

Source and Data on 8" SSSD CP/M(tm) Disc (inc ROM 2)

[ ]	Release 1.x : 24 lines x 80 characters, std.	8.50
[ ]	Release 3.x : VIDSTAR for Wordstar / dBASE II	22.75
[ ]	Release 4.x : VIDSTAR with 25th line nonscroll	27.75

Crystals, HC-18 size, wire leads, for Rel's 1.x & 3.x

[ ]	13.628 MHz crystal (60 Hz. - USA)	18.9kHz	7.00
[ ]	11.357 MHz crystal (50 Hz. - foreign)	18.9kHz	9.00

For Rel. 2.x (obsolete) and 4.x only :

[ ]	11.340 MHz crystal (60 Hz. - USA)	15.7kHz	6.00
[ ]	9.4500 MHz crystal (50 Hz. - foreign)	15.7kHz	9.00

Miscellaneous

[ ]	Serial Keyboard port adapter **	T.B.A.
[ ]	Trim-pot set (2 - 20kohm, 1 - 5kohm)	4.50
[ ]	8275 CRT controller IC	27.75
[ ]	Complete set of IC's & Q1, less eproms	73.00

Documentation		Complete	source only
[ ]	Release 1.x,	10.00 *	5.00
[ ]	Release 3.x,	15.00	11.00
[ ]	Release 4.x,	20.00	15.00
[ ]	No source list	5.00 *	-----

(* Refundable with VDB-A purchase) _____

Please add $3.00 for shipping & handling 3.00
(or $1.50 for documentation only) SUB-TOTAL _____

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