DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD70208H, 70216H

V40HL™, V50HL™
16/8, 16-BIT MICROPROCESSOR

DESCRIPTION

The μPD70208H (V40HL) is a high-speed, low-power 16-/8-bit microprocessor based on the μPD70208 (V40™) with 16-bit architecture, 8-bit data bus, and general-purpose peripheral functions.

The μPD70216H (V50HL) is a high-speed, low-power 16-bit microprocessor based on the μPD70216 (V50™) with 16-bit architecture, 16-bit data bus, and general-purpose peripheral functions.

The V40HL and V50HL offer 20 MHz operation, and in addition to the conventional standby functions, also allows the clock to be stopped by the use of fully static internal circuitry, thus achieving greatly reduced power consumption. It is also capable of 3 V operation in addition to the previous 5 V operation, making it ideally suited to battery driven systems.

Details are given in the following manuals. Be sure to read when carrying out design work.

- **V40HL, V50HL User's Manual – Hardware (U11610E)**
- **16-bit V series™ User's Manual – Instruction (U11301J: Japanese version)**

FEATURES

- High-speed, low-power version of V40 and V50
- High-performance CPU (V20™/V30™ software compatible)
  - Minimum instruction execution time: 100 ns (20 MHz, 5 V)
    200 ns (10 MHz, 3 V)
  - Memory addressing space: 1M bytes
  - High-speed multiply/divide instructions: 0.95 to 2.8 μs (20 MHz, 5 V)
    1.9 to 5.6 μs (10 MHz, 3 V)
  - Maskable (ICU) & non-maskable (NMI) interrupt inputs
  - μPD8080AF emulation function
  - Standby functions, clock stoppage capability
- Standard peripheral LSI functions on chip
  - Clock generator (CG)
  - Programmable wait control unit (WCU)
  - Refresh control unit (REFU)
  - Timer/counter unit (TCU) ··· μPD71054 subset
  - Serial control unit (SCU) ··· μPD71051 subset
  - Interrupt control unit (ICU) ··· μPD71059 subset
  - DMA control unit (DMAU) ··· μPD71071/71037 subset (functions of either selectable)
- Operating frequency: 10/12.5/16/20 MHz (at 5 V, with 20/25/32/40 MHz supplied externally)
  5/6.25/8/10 MHz (at 3 V, with 10/12.5/16/20 MHz supplied externally)

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Printed in Japan

The mark ★ shows the the major revised points.

ORDERING INFORMATION

(1) V40HL

Part Number	Package	Max. Operating Frequency (MHz)
μPD70208HGF-10-3B9	80-pin plastic QFP (14 × 20 mm) (Resin thickness 2.7 mm)	10
μPD70208HGF-12-3B9	80-pin plastic QFP (14 × 20 mm) (Resin thickness 2.7 mm)	12.5
μPD70208HGF-16-3B9	80-pin plastic QFP (14 × 20 mm) (Resin thickness 2.7 mm)	16
μPD70208HGF-20-3B9	80-pin plastic QFP (14 × 20 mm) (Resin thickness 2.7 mm)	20
μPD70208HGK-10-9EU	80-pin plastic TQFP (Fine pitch) (12 × 12 mm) (Resin thickness 1.0 mm)	10
μPD70208HGK-12-9EU	80-pin plastic TQFP (Fine pitch) (12 × 12 mm) (Resin thickness 1.0 mm)	12.5
μPD70208HGK-16-9EU	80-pin plastic TQFP (Fine pitch) (12 × 12 mm) (Resin thickness 1.0 mm)	16
μPD70208HGK-20-9EU	80-pin plastic TQFP (Fine pitch) (12 × 12 mm) (Resin thickness 1.0 mm)	20
μPD70208HLP-10	68-pin plastic QFJ (950 × 950 mil)	10
μPD70208HLP-12	68-pin plastic QFJ (950 × 950 mil)	12.5
μPD70208HLP-16	68-pin plastic QFJ (950 × 950 mil)	16
μPD70208HLP-20	68-pin plastic QFJ (950 × 950 mil)	20

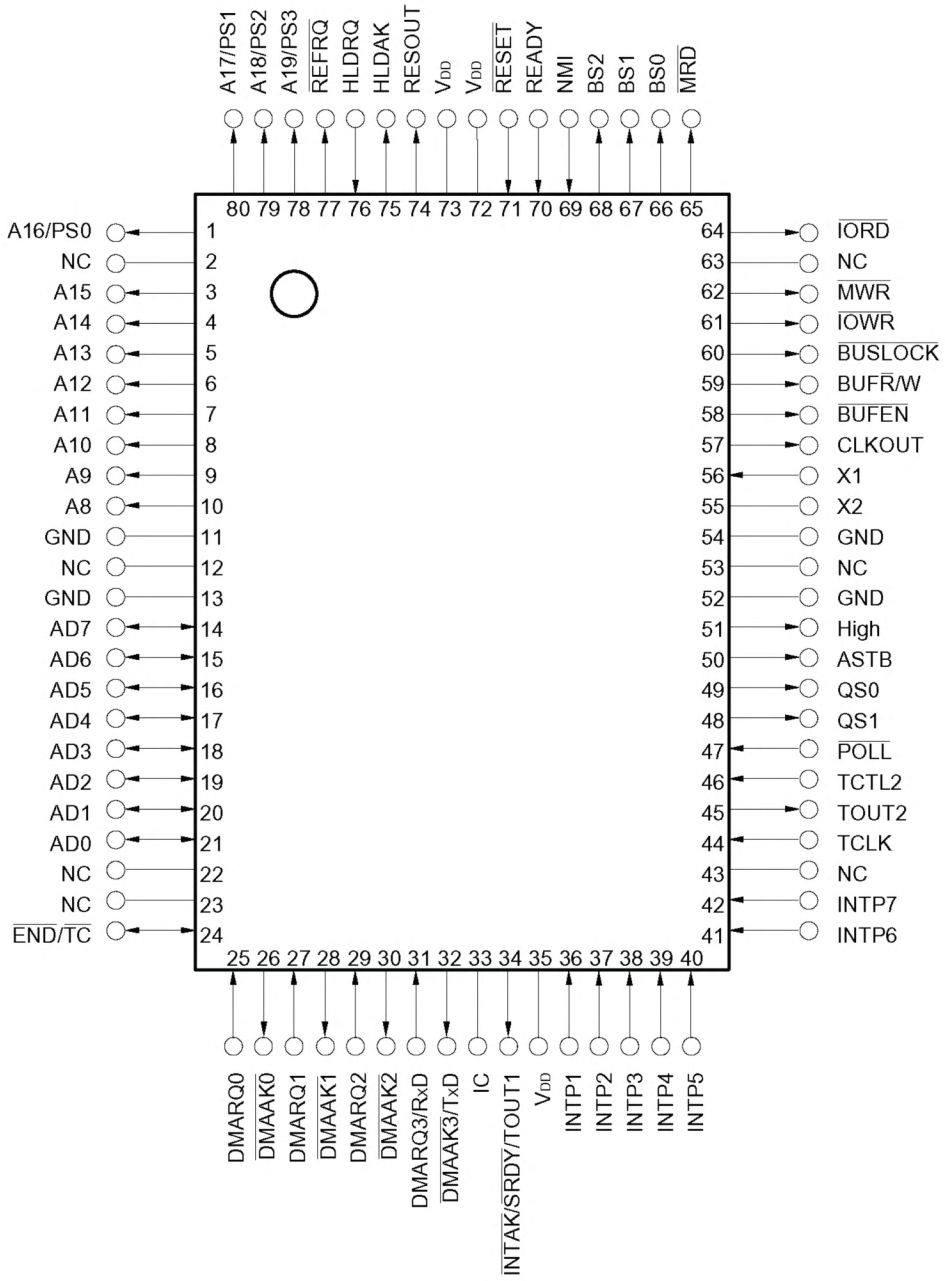
(2) V50HL

Part Number	Package	Max. Operating Frequency (MHz)
μPD70216HGF-10-3B9	80-pin plastic QFP (14 × 20 mm) (Resin thickness 2.7 mm)	10
μPD70216HGF-12-3B9	80-pin plastic QFP (14 × 20 mm) (Resin thickness 2.7 mm)	12.5
μPD70216HGF-16-3B9	80-pin plastic QFP (14 × 20 mm) (Resin thickness 2.7 mm)	16
μPD70216HGF-20-3B9	80-pin plastic QFP (14 × 20 mm) (Resin thickness 2.7 mm)	20
μPD70216HGK-10-9EU	80-pin plastic TQFP (Fine pitch) (12 × 12 mm) (Resin thickness 1.0 mm)	10
μPD70216HGK-12-9EU	80-pin plastic TQFP (Fine pitch) (12 × 12 mm) (Resin thickness 1.0 mm)	12.5
μPD70216HGK-16-9EU	80-pin plastic TQFP (Fine pitch) (12 × 12 mm) (Resin thickness 1.0 mm)	16
μPD70216HGK-20-9EU	80-pin plastic TQFP (Fine pitch) (12 × 12 mm) (Resin thickness 1.0 mm)	20
μPD70216HLP-10	68-pin plastic QFJ (950 × 950 mil)	10
μPD70216HLP-12	68-pin plastic QFJ (950 × 950 mil)	12.5
μPD70216HLP-16	68-pin plastic QFJ (950 × 950 mil)	16
μPD70216HLP-20	68-pin plastic QFJ (950 × 950 mil)	20

PIN CONFIGURATION (Top View)

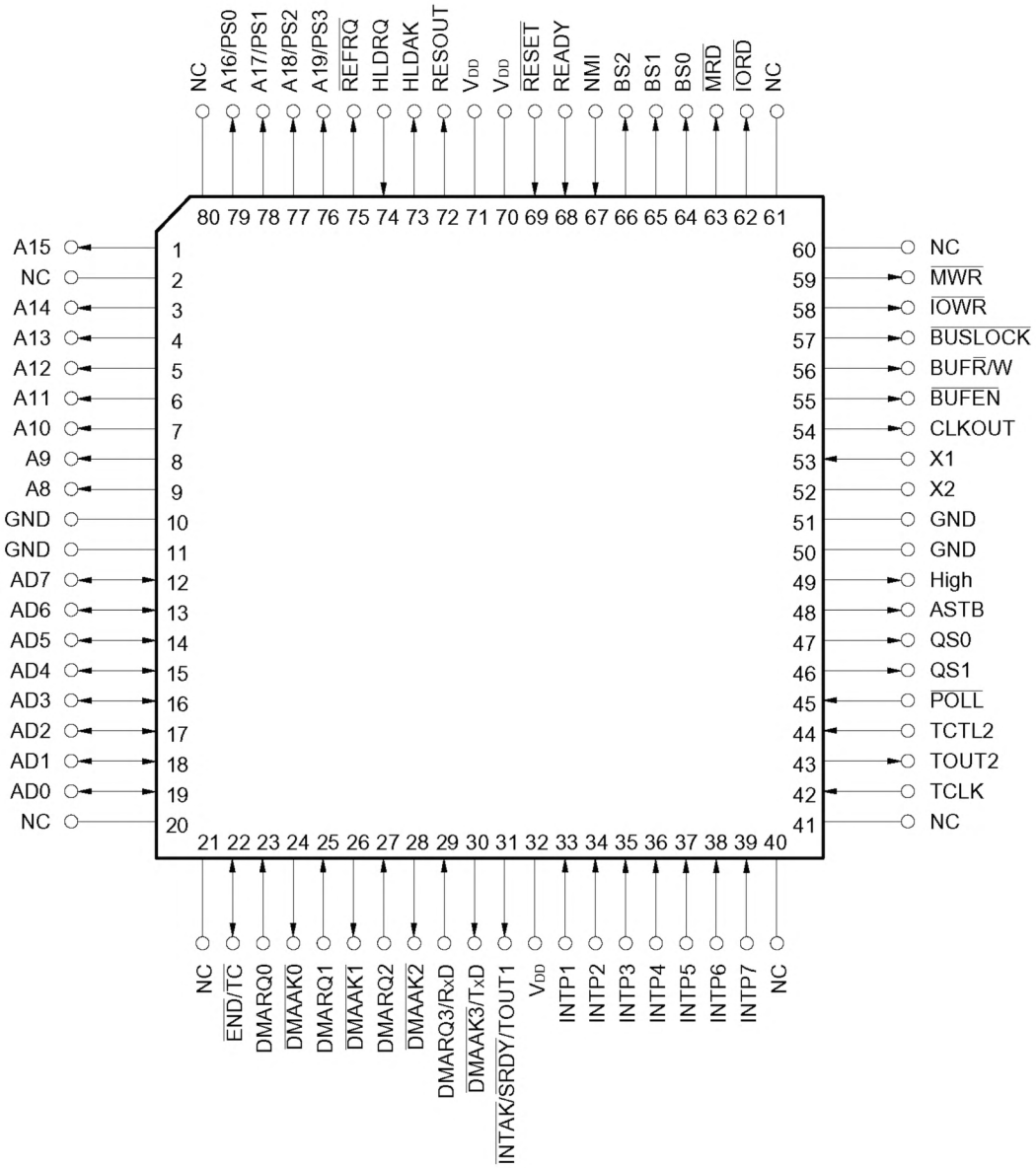
(1) V40HL

- **80-pin Plastic QFP (14 × 20 mm)**
  μPD70208HGF-10-3B9
  μPD70208HGF-12-3B9
  μPD70208HGF-16-3B9
  μPD70208HGF-20-3B9

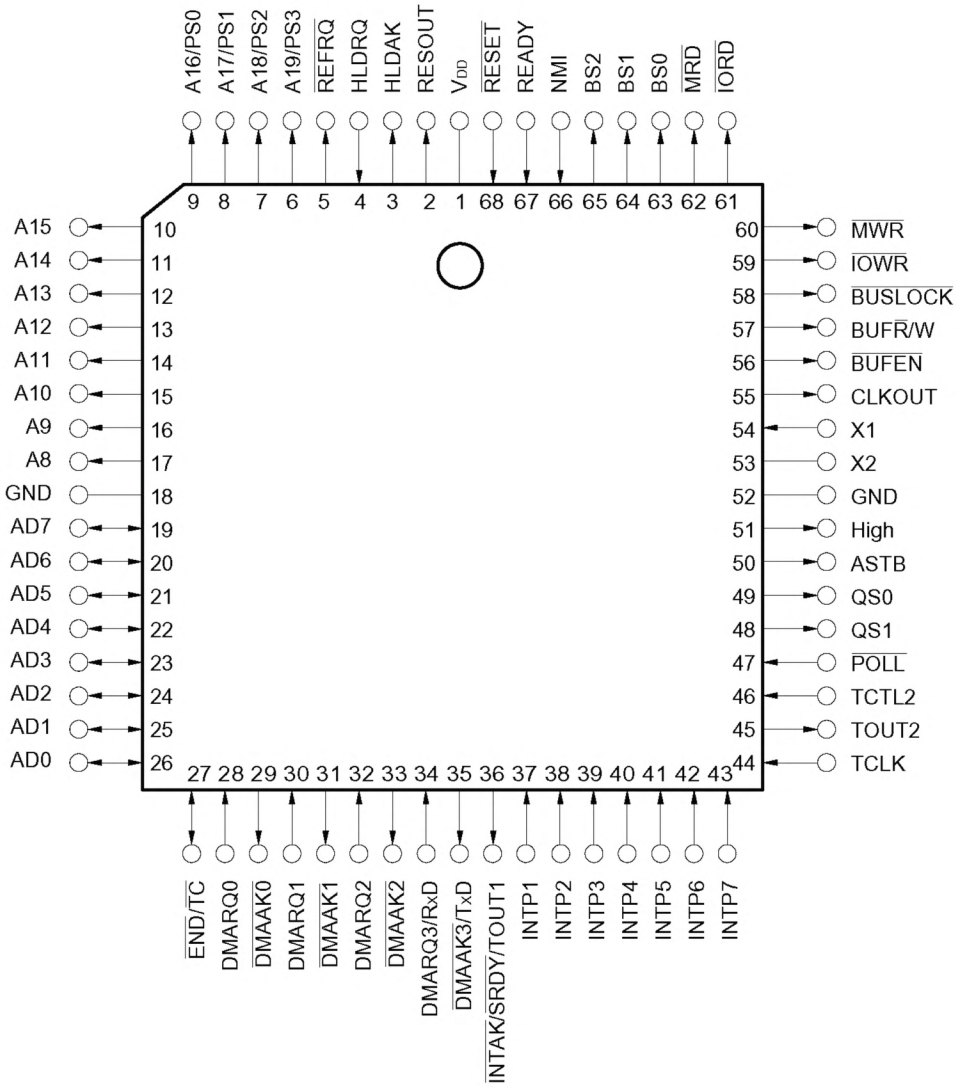


Caution Leave IC pin open.

- **80-pin Plastic TQFP (Fine pitch) (12 × 12 mm)**
  μPD70208HGK-10-9EU
  μPD70208HGK-12-9EU
  μPD70208HGK-16-9EU
  μPD70208HGK-20-9EU



- **68-pin Plastic QFJ (950 × 950 mil)**
  μPD70208HLP-10
  μPD70208HLP-12
  μPD70208HLP-16
  μPD70208HLP-20



(2) V50HL

- 80-pin Plastic QFP (14 × 20 mm)
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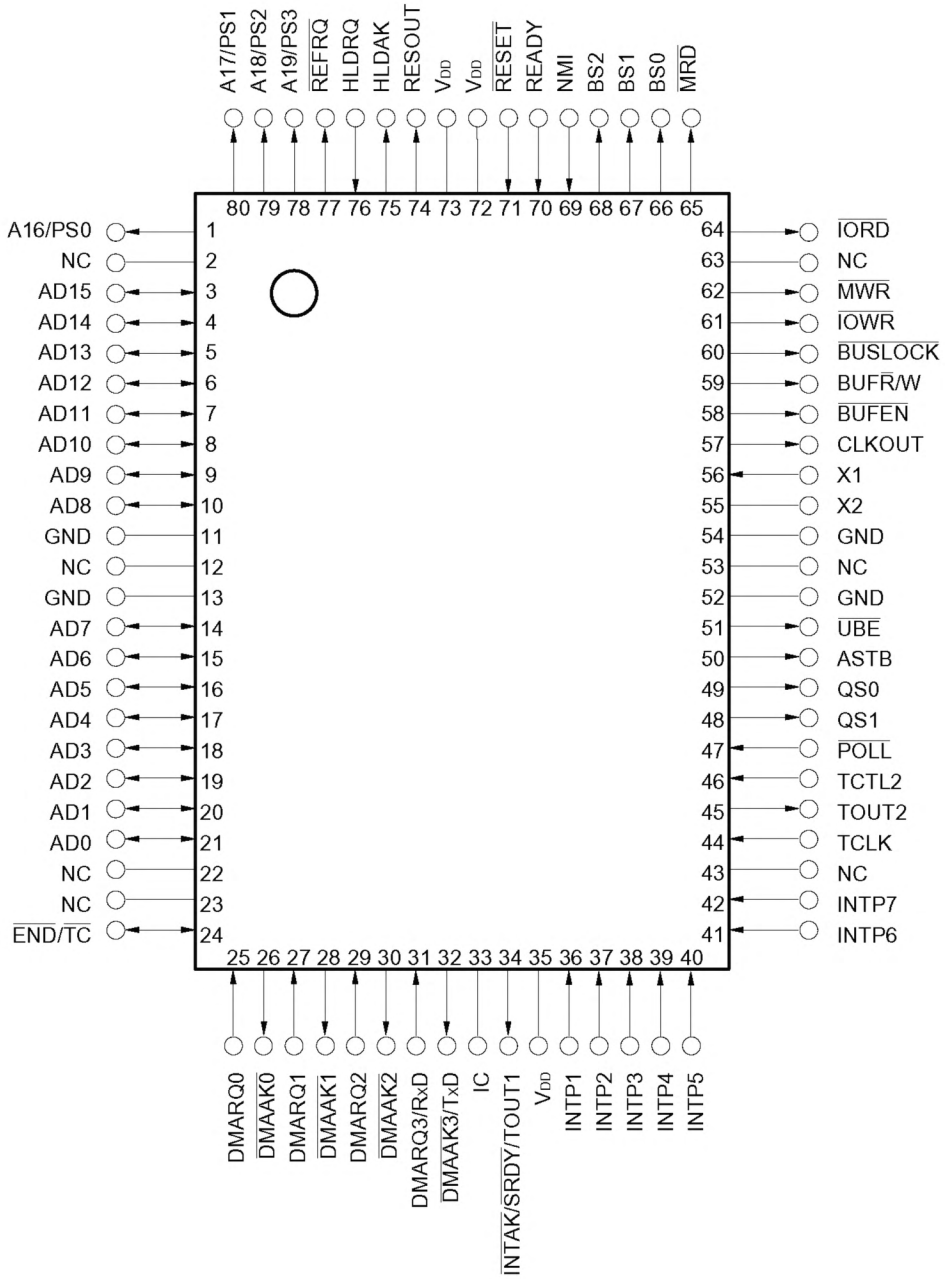
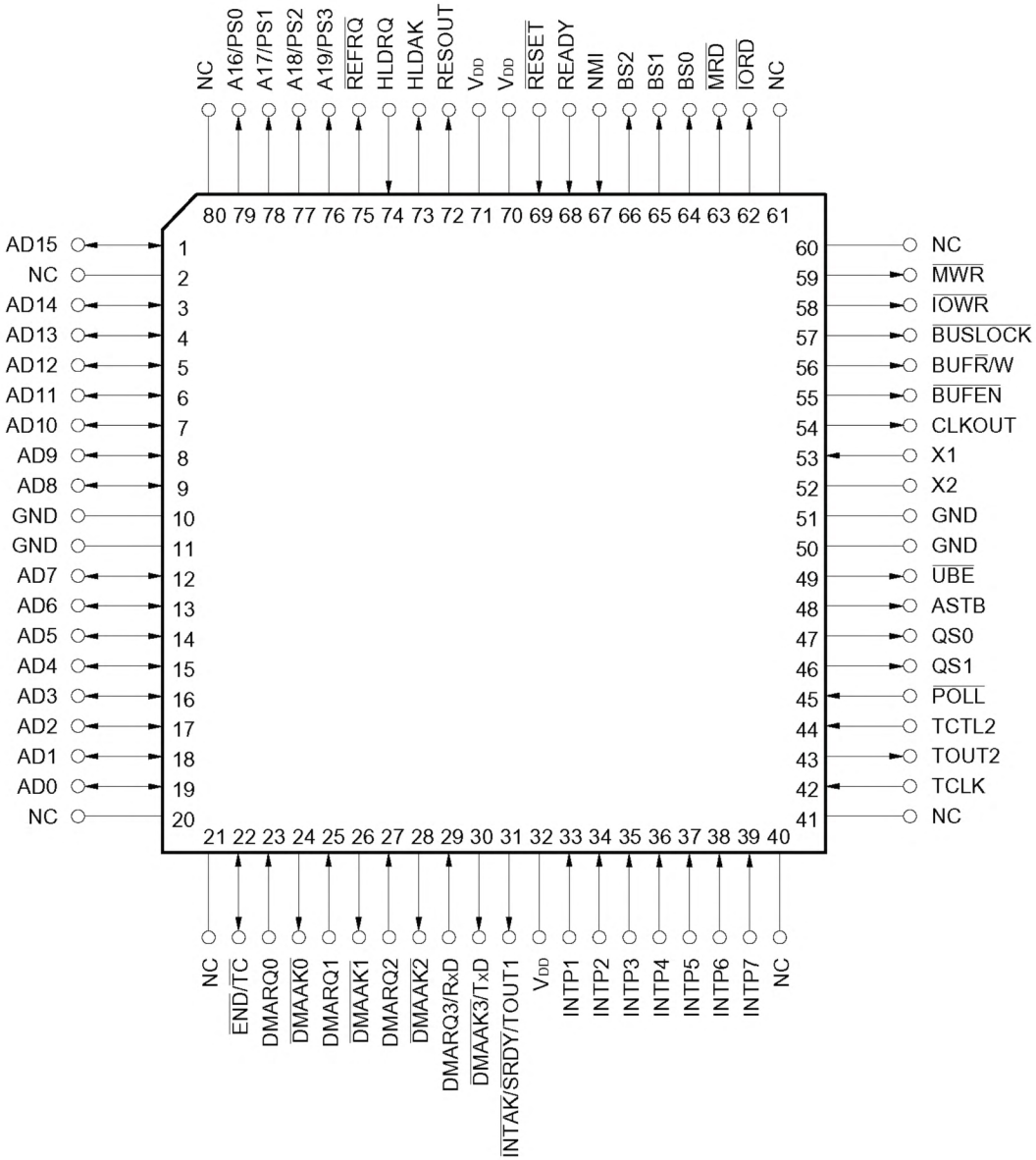
  μPD70216HGF-12-3B9
  μPD70216HGF-16-3B9
  μPD70216HGF-20-3B9

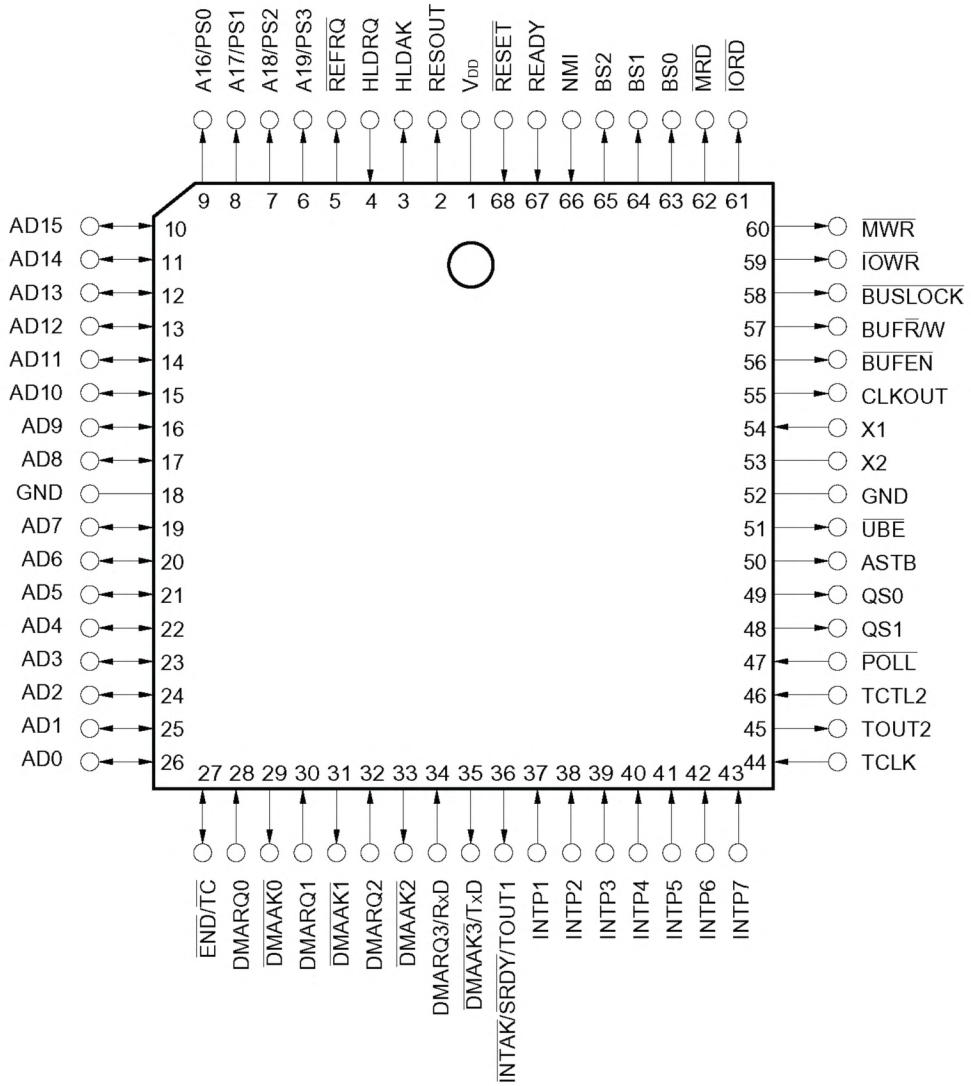


Caution Leave IC pin open.

- **80-pin Plastic TQFP (Fine pitch) (12 × 12 mm)**
  μPD70216HGK-10-9EU
  μPD70216HGK-12-9EU
  μPD70216HGK-16-9EU
  μPD70216HGK-20-9EU



- **68-pin Plastic QFJ (950 × 950 mil)**
  μPD70216HLP-10
  μPD70216HLP-12
  μPD70216HLP-16
  μPD70216HLP-20

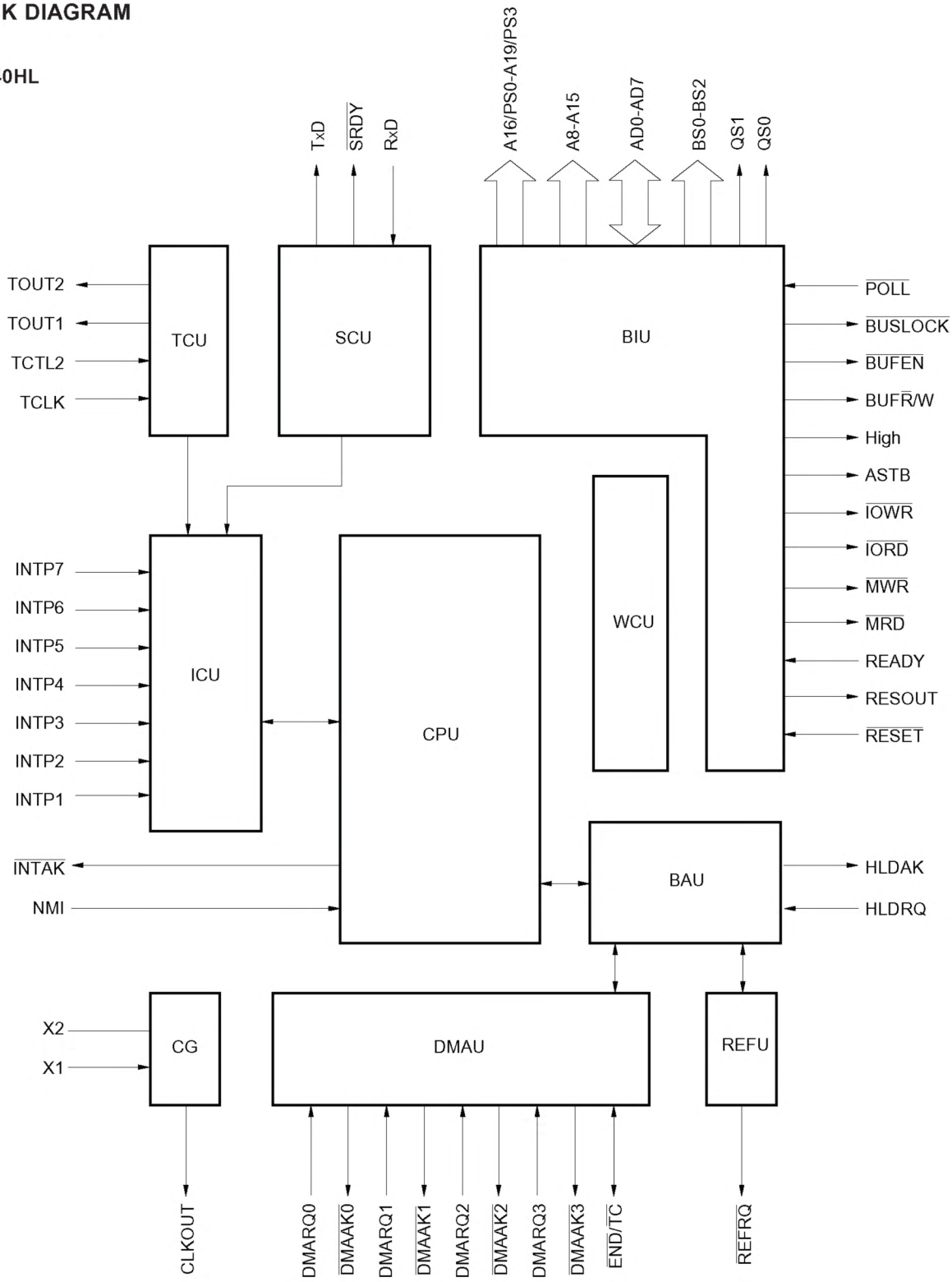


PIN NAMES

A8-A15	:	Address Bus
A16/PS0-A19/PS3	:	Address/Processor Status
AD0-AD15	:	Address Bus/Data Bus
ASTB	:	Address Strobe
BS0-BS2	:	Bus Status
$\overline{\text{BUFEN}}$	:	Buffer Enable
BUF$\overline{\text{R}}$/W	:	Buffer Read/Write
$\overline{\text{BUSLOCK}}$	:	Bus Lock
CLKOUT	:	Clock Output
$\overline{\text{DMAAK0}}$-$\overline{\text{DMAAK2}}$	:	DMA Acknowledge
$\overline{\text{DMAAK3}}$/TxD	:	DMA Acknowledge/Transmit Data
DMARQ0-DMARQ2	:	DMA Request
DMARQ3/RxD	:	DMA Request/Receive Data
$\overline{\text{END}}$/$\overline{\text{TC}}$	:	End/Terminal Count
GND	:	Ground
High	:	High Level Output
HLDAK	:	Hold Acknowledge
HLDRQ	:	Hold Request
IC	:	Internally Connected
$\overline{\text{INTAK}}$/$\overline{\text{SRDY}}$/TOUT1	:	Interrupt Acknowledge/Serial Ready/Timer Output 1
INTP1-INTP7	:	Interrupt Request from Peripherals
$\overline{\text{IORD}}$	:	I/O Read
$\overline{\text{IOWR}}$	:	I/O Write
$\overline{\text{MRD}}$	:	Memory Read
$\overline{\text{MWR}}$	:	Memory Write
NC	:	No Connection
NMI	:	Non-Maskable Interrupt Request
$\overline{\text{POLL}}$	:	Poll
QS0, QS1	:	Queue Status
READY	:	Ready
$\overline{\text{REFRQ}}$	:	Refresh Request
$\overline{\text{RESET}}$	:	Reset
RESOUT	:	Reset Output
TCLK	:	Timer Clock
TCTL2	:	Timer Control 2
TOUT2	:	Timer Output 2
$\overline{\text{UBE}}$	:	Upper Byte Enable
V_{DD}	:	Power Supply
X1, X2	:	Crystal

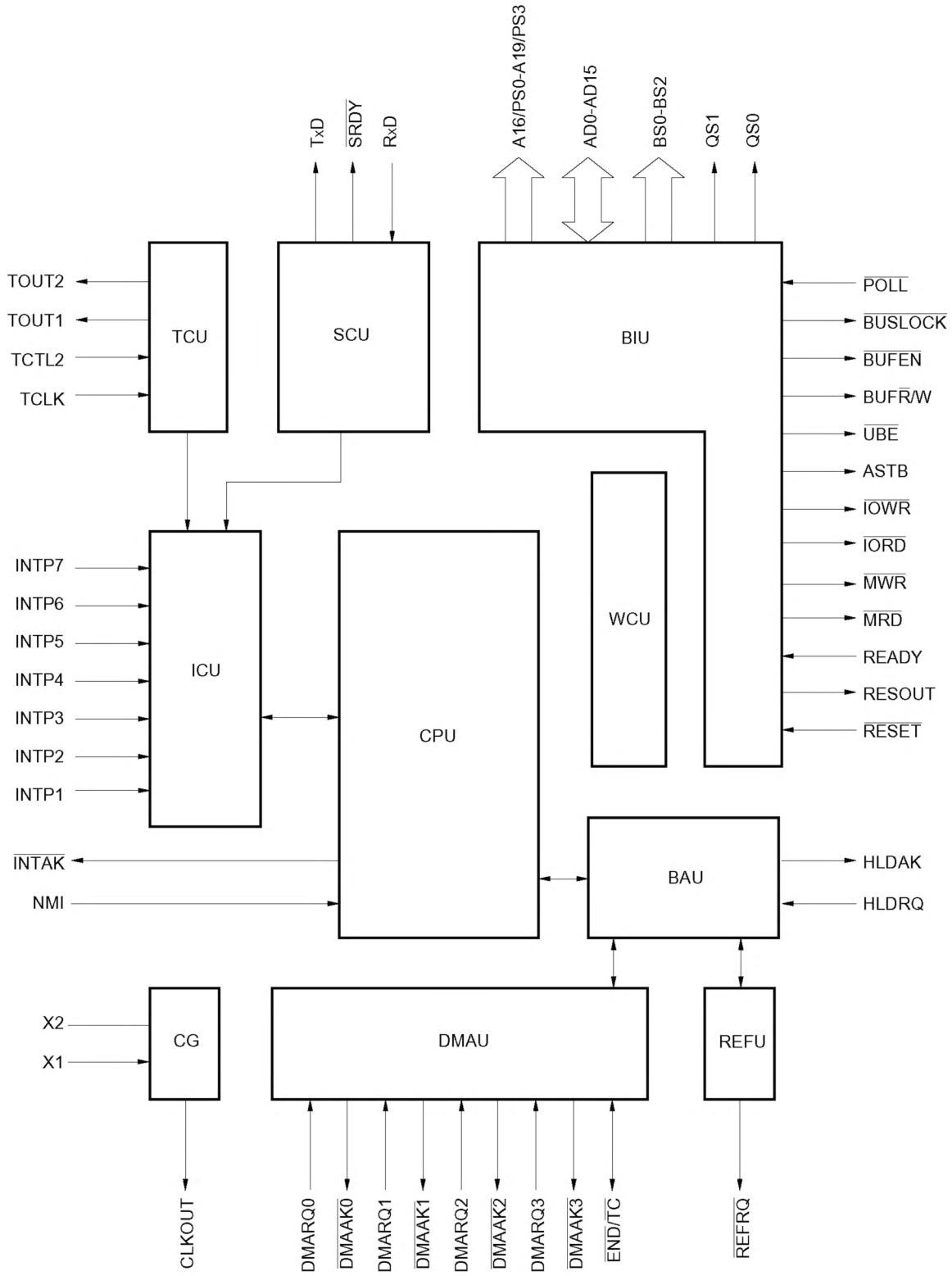
BLOCK DIAGRAM

(1) V40HL



CPU : Central Processing Unit
CG : Clock Generator
BIU : Bus Interface Unit
BAU : Bus Arbitration Unit
WCU : Wait Control Unit
REFU : Reflesh Control Unit
TCU : Timer/Count Unit
SCU : Serial Control Unit
ICU : Interrupt Control Unit
DMAU : DMA Control Unit

(2) V50HL


A16/PS0-A19/PS3
AD0-AD15
BS0-BS2
QS1
QS0
TxD
SRDY
RxD
TOUT2
TOUT1
TCTL2
TCLK
TCU
SCU
BIU
POLL
BUSLOCK
BUFEN
BUFR/W
UBE
ASTB
IOWR
IORD
MWR
MRD
READY
RESOUT
RESET
INTP7
INTP6
INTP5
INTP4
INTP3
INTP2
INTP1
ICU
CPU
WCU
INTAK
NMI
BAU
HLDAK
HLDRQ
X2
X1
CG
DMAU
REFU
CLKOUT
DMARQ0
DMAAK0
DMARQ1
DMAAK1
DMARQ2
DMAAK2
DMARQ3
DMAAK3
END/TC
REFRQ

DIFFERENCES FROM V40 AND V50

Item		V40HL, V50HL	V40, V50
Operating supply voltage		3 V, 5 V	5 V
Operating frequency	V_{DD} = 5 V	MAX. : 10, 12.5, 16, 20 MHz MIN. : DC	MAX. : 8, 10 MHz MIN. : 2 MHz
	V_{DD} = 3 V	MAX. : 5, 6.25, 8, 10 MHz MIN. : DC	No operation
Clock generator (CG)		Variable scaling factor	Fixed scaling factor
		Variable instruction cycle time	Fixed instruction cycle time
		Maximum input frequency: 40 MHz	Maximum input frequency: 20 MHz
Internal I/O relocation function		Switchable 8-bit boundary or 16-bit boundary relocation function	V40: Relocation possible on 8-bit boundary V50: Relocation possible on 16-bit boundary
Wait control unit (WCU)		Memory space: 5 divisions[Note 1]	Memory space: 3 divisions
		I/O space: 3 divisions[Note 2]	I/O space: Not divided
Refresh control unit (REFU)		Refresh address: 16 bits	Refresh address: 9 bits
		$\overline{\text{REFRQ}}$ extended timing supported	No $\overline{\text{REFRQ}}$ extended timing
Serial control unit (SCU)		Dedicated baud rate generator incorporated	No dedicated baund rate generator incorporated
DMA control unit (DMAU)		μPD71071/71037 subset (either function selectable)	μPD71071 subset
Standby functions		HALT mode, STOP mode	HALT mode only

Notes 1. Divided into 3 when a reset is performed.

2. Not divided when a reset is performed.

CONTENTS

1. PIN FUNCTIONS

1.1 LIST OF PIN FUNCTIONS

Pin Name	Input/Output	Function
AD0 to AD15[Note 1, 3]	3-state I/O	Time-division address/data bus
AD0 to AD7[Note 2, 3]	3-state I/O	Time-division address/data bus
A8 to A15[Note 2, 3]	3-state output	Address bus
A16/PS0 to A19/PS3[Note 3]	3-state output	Time-division address/processor status
$\overline{\text{REFRQ}}$	Output	Refresh request
HLDRQ	Input	Bus hold request
HLDAK	Output	Bus hold acknowledge
$\overline{\text{RESET}}$	Input	Reset
RESOUT	Output	System reset output
READY	Input	Bus cycle end
NMI	Input	Non-maskable interrupt
$\overline{\text{MRD}}$[Note 3]	3-state output	Memory read strobe
$\overline{\text{MWR}}$[Note 3]	3-state output	Memory read strobe
$\overline{\text{IORD}}$[Note 3]	3-state output	I/O read strobe
$\overline{\text{IOWR}}$[Note 3]	3-state output	I/O write strobe
ASTB	Output	Address strobe
$\overline{\text{UBE}}$[Note 1, 3]	3-state output	Data bus upper byte enable
High[Note 2]	3-state output	High level output
$\overline{\text{BUSLOCK}}$[Note 3]	3-state output	Bus lock
$\overline{\text{POLL}}$	Input	Floating-point operation processor polling
BUF$\overline{\text{R}}$/W[Note 3]	3-state output	Buffer read/write
$\overline{\text{BUFEN}}$[Note 3]	3-state output	Buffer enable
X1	Input	Crystal/external clock
X2	—	
CLKOUT	Output	Clock output
BS0 to BS2[Note 3]	3-state output	Bus status
QS0, QS1	Output	Queue status
TOUT2	Output	Timer 2 output
TCTL2	Input	Timer 2 control
TCLK	Input	Timer clock
INTP1 to INTP7	Input	Maskable interrupts
$\overline{\text{INTAK}}$/$\overline{\text{SRDY}}$/TOUT1	Output	Interrupt acknowledge/serial reception ready/timer 1 output

Notes 1. V50HL only

2. V40HL only

3. These pins are provided with a latch. Therefore, when they go into a high-impedance state, they hold the status before the high-impedance state until driven by an external device. It is not necessary to pull up or down the data bus. To invert the level of the pin that goes into a high-impedance state by an external device, a drive current higher than the latch invert current (I_{ILH}, I_{ILL}) is necessary.

Pin Name	Input/Output	Function
$\overline{\text{DMAAK3}}$/TxD	Output	DMA acknowledge 3/serial transmit data
DMARQ3/RxD	Input	DMA request 3/serial receive data
$\overline{\text{DMAAK0}}$ to $\overline{\text{DMAAK2}}$	Output	DMA acknowledge
DMARQ0 to DMARQ2	Input	DMA request
$\overline{\text{END}}$/$\overline{\text{TC}}$	I/O	DMA service forcible termination/DMA service completion
V_{DD}	—	Positive power supply pin
GND	—	Ground potential pin
IC	—	Internal connection pin (External connection impossible)

1.2 PROCESSING OF UNUSED PINS

Table 1-1 shows the processing (recommended connection) of the unused pins. Use of a resistor with a resistance of 1 to 10 kΩ is recommended to connect these pins to V_{DD} or GND via resistor.

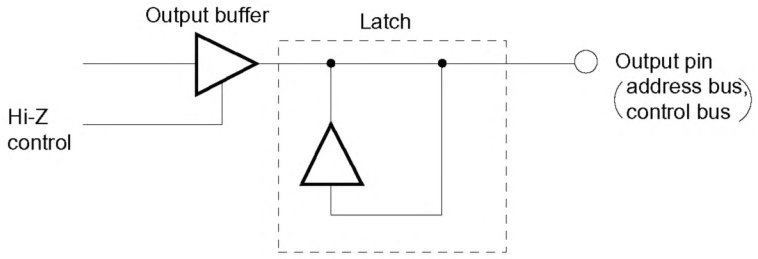
Table 1-1. Processing of Unused Pins

Pin Name	Input/Output	Recommended Connection
AD0 to AD15 Note 1	3-state I/O	Open
AD0 to AD7 Note 2	3-state I/O	
A8 to A15 Note 2	3-state output	
A16/PS0 to A19/PS3	3-state output	
$\overline{\text{REFRQ}}$	Output	
HLDRQ	Input	Connect to GND via resistor
HLDAK	Output	Open
RESOUT	Output	Open
READY	Input	Connect to V_{DD} via resistor
NMI	Input	Connect to GND via resistor
$\overline{\text{MRD}}$	3-state output	Open
$\overline{\text{MWR}}$	3-state output	
$\overline{\text{IORD}}$	3-state output	
$\overline{\text{IOWR}}$	3-state output	
ASTB	Output	
$\overline{\text{UBE}}$ Note 1	3-state output	
High Note 2	Output	
$\overline{\text{BUSLOCK}}$	3-state output	
$\overline{\text{POLL}}$	Input	Connect to GND via resistor
BUF$\overline{\text{R}}$/W	3-state output	Open
$\overline{\text{BUFEN}}$	3-state output	
CLKOUT	Output	Open
BS0 to BS2	3-state output	
QS0, QS1	Output	
TOUT2	Output	
TCTL2	Input	Connect to GND via resistor
TCLK	Input	
INTP1 to INTP7	Input	Open
$\overline{\text{INTAK}}$/$\overline{\text{SRDY}}$/TOUT1	Output	
$\overline{\text{DMAAK3}}$/TxD	Output	
DMARQ3/RxD	Input	Connect to GND via resistor
$\overline{\text{DMAAK0}}$ to $\overline{\text{DMAAK2}}$	Output	Open
DMARQ0 to DMARQ2	Input	Connect to GND via resistor
$\overline{\text{END}}$/$\overline{\text{TC}}$	I/O	Individually connect to V_{DD} via resistor

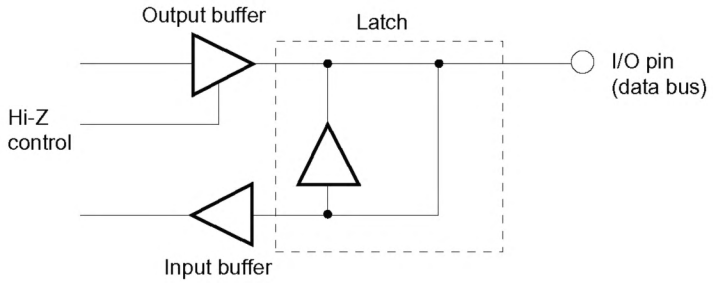
Notes 1. V50HL only
2. V40HL only

Remark The circuit configuration of the latch is as illustrated below. To invert the level of the pin with a latch, a drive current higher than the latch invert current is necessary.

(1) Output pin



(2) I/O pin



2. MEMORY AND I/O CONFIGURATION

2.1 MEMORY SPACE

The V40HL and V50HL can access a 1M-byte (512K-word) memory space.

Figure 2-1. Memory Map

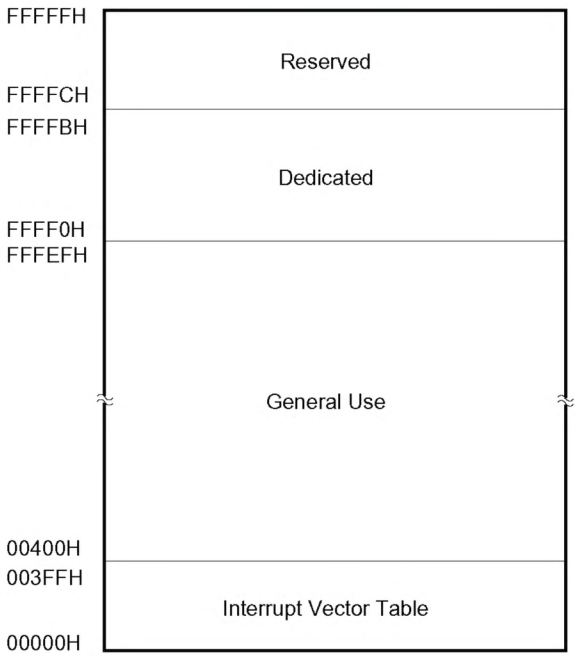


Figure 2-2. Interface with Memory (1/2)

(a) V40HL

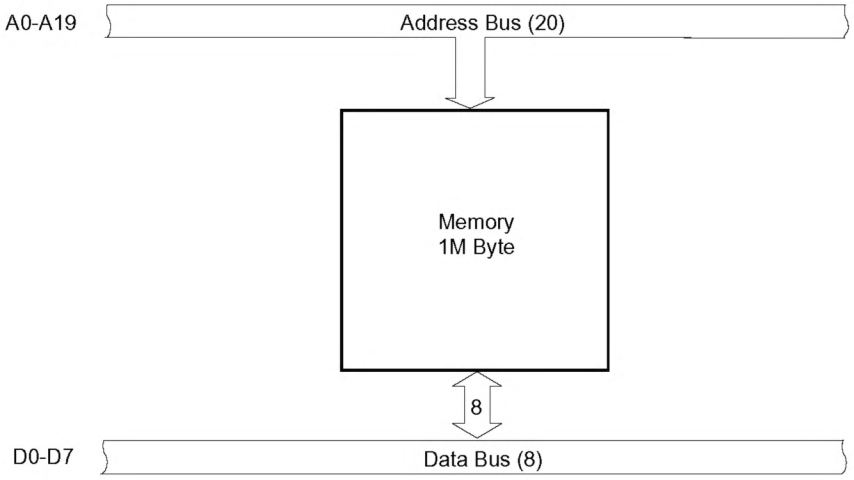
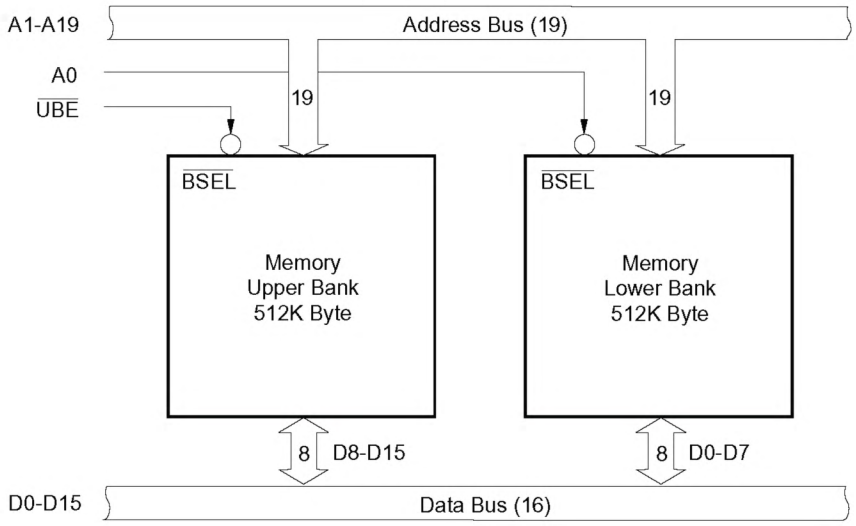


Figure 2-2. Interface with Memory (2/2)

(b) V50HL



2.2 I/O SPACE

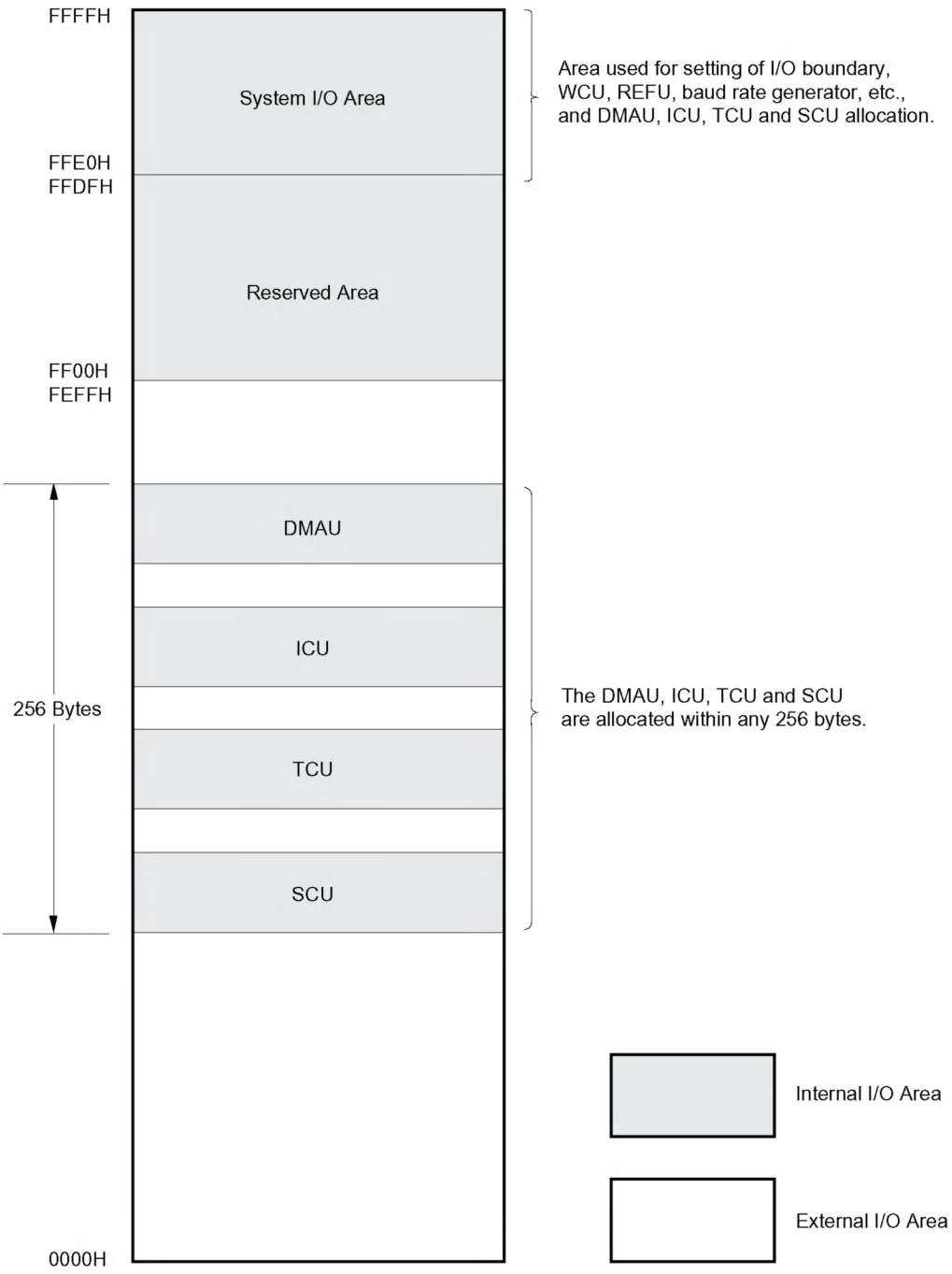
In the V40HL and V50HL, I/Os up to 64K bytes (32K words) can be accessed in an area independent of the memory.

The various on-chip peripheral LSIs are set by accessing the system I/O area.

Extended functions added to those of the V40 and V50 are mapped onto unused V40 and V50 registers and the reserved area.

The I/O map is shown in Figure 2-3.

Figure 2-3. I/O Map



3. CPU

The CPU has the same functions as the V20HL™ and V30HL™. In hardware terms, there are some changes regarding the use of the bus with on-chip peripherals, but in software terms the CPU is fully compatible.

The internal block diagram of the CPU is shown in Figure 3-1.

Figure 3-1. Internal Block Diagram of CPU (1/2)

(a) V40HL

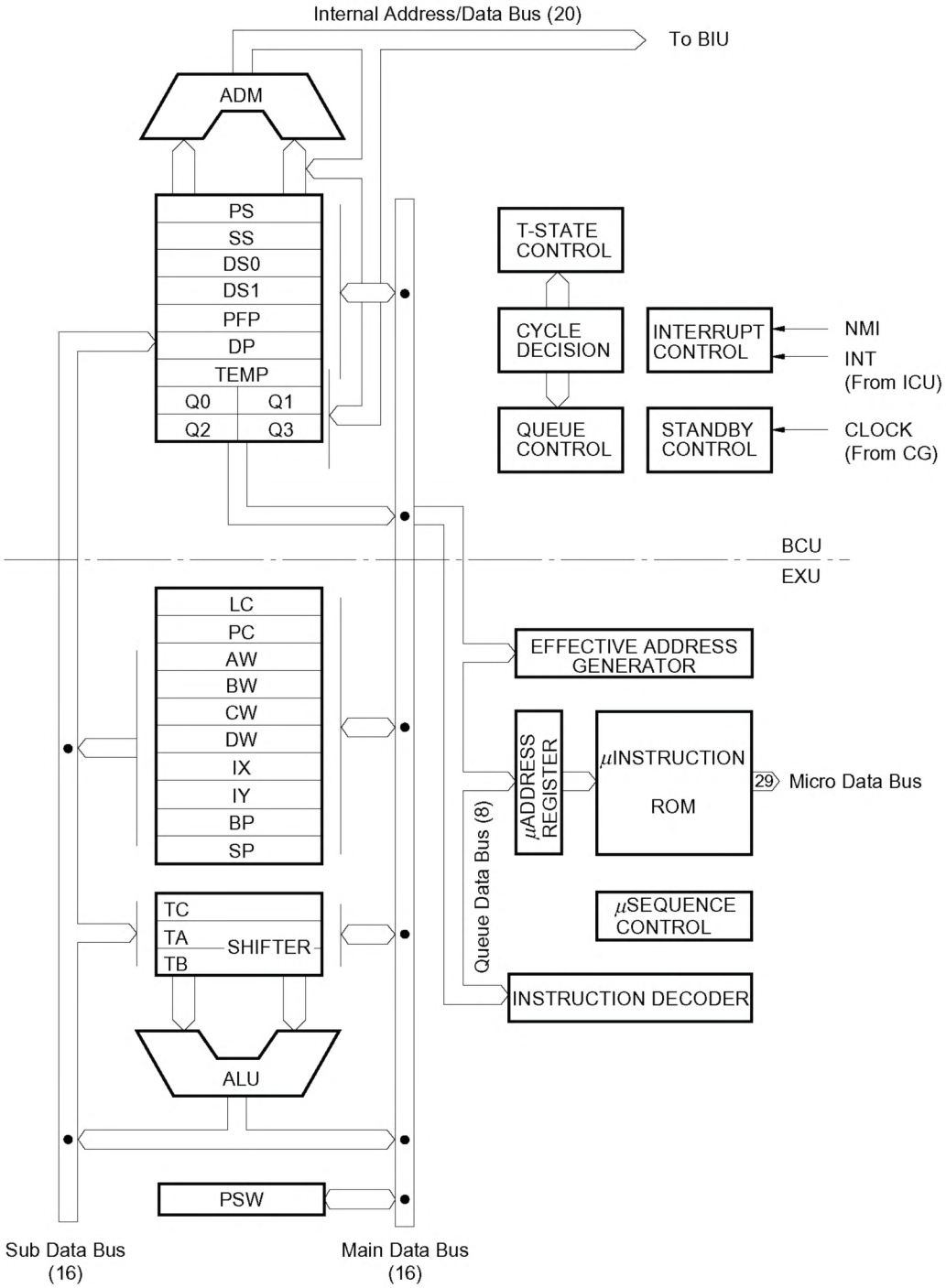
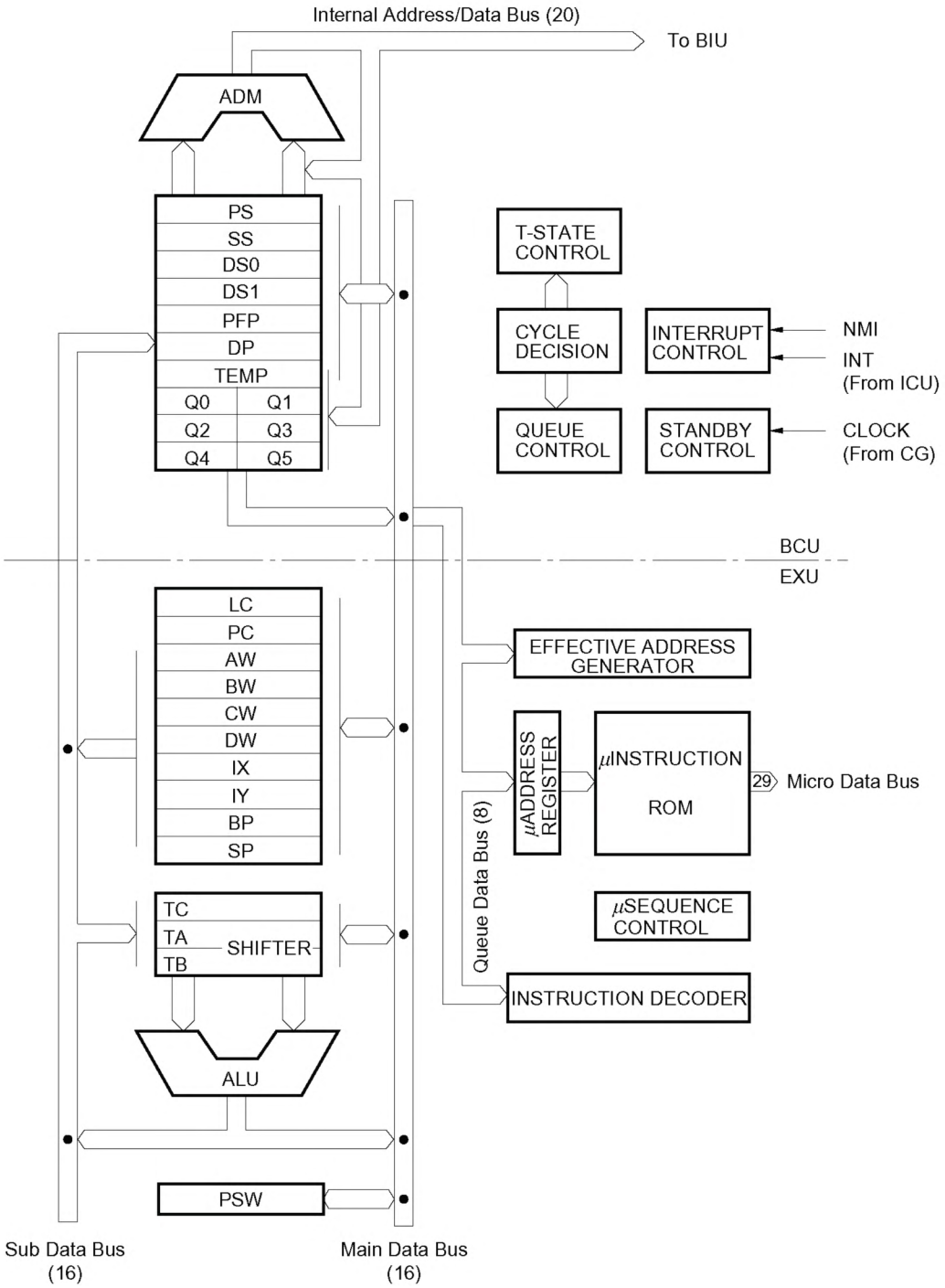


Figure 3-1. Internal Block Diagram of CPU (2/2)

(b) V50HL

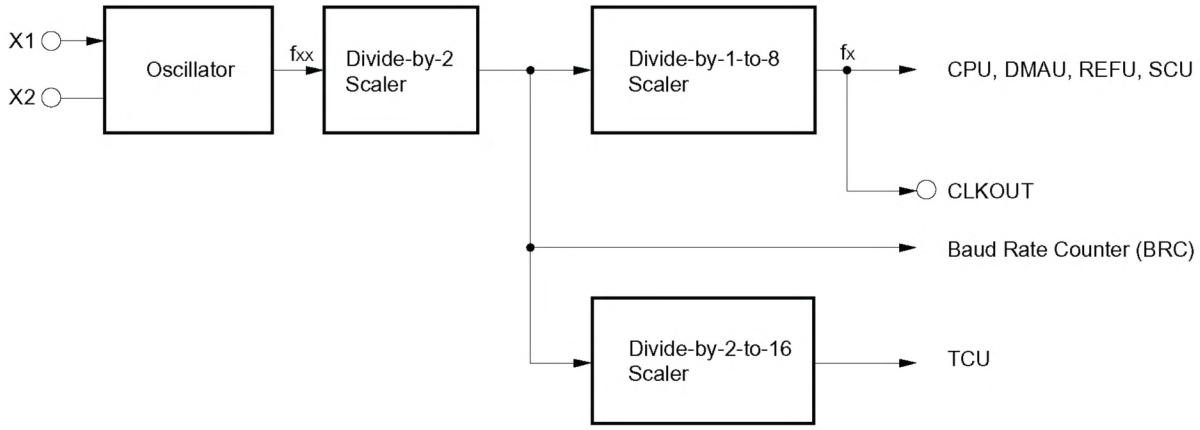


4. CG (CLOCK GENERATOR)

The CG generates a clock at a frequency of 1/2, 1/4, 1/8 or 1/16 that of the crystal and oscillator connected to the X1 and X2 pins, supplies it as the CPU operating clock and outputs it externally as the CLKOUT pin output.

The interrupt cycle time can be changed according to the oscillator scaling factor. The scaling factor can be set by a system I/O area register.

Figure 4-1. Internal Block Diagram of CG

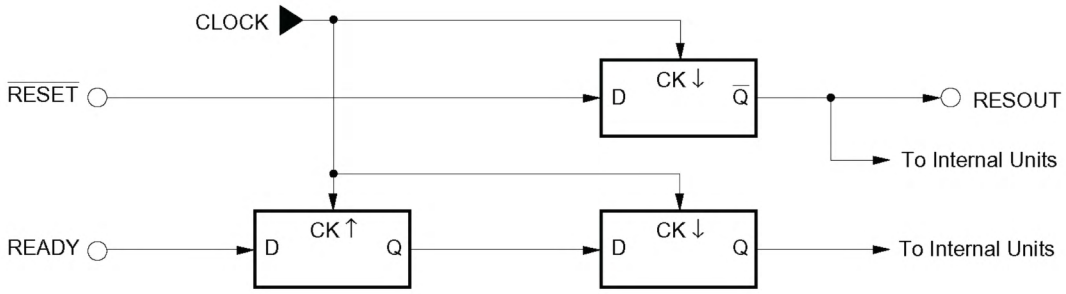


5. BIU (BUS INTERFACE UNIT)

The BIU controls the data bus, address bus and control bus pins. These buses are used by the CPU, DMAU (DMA control unit) and REFU (refresh control unit).

The BIU synchronizes the $\overline{\text{RESET}}$ input signal and READY input signal using the CLOCK signal generated by the clock generator (CG). In addition to being supplied to the inside of the V40HL and V50HL, the synchronized reset signal is also output externally from the RESOUT pin. The synchronized READY signal is supplied to the internal CPU, DMAU and REFU.

Figure 5-1. $\overline{\text{RESET}}$ and READY Signal Synchronization



6. BAU (BUS ARBITRATION UNIT)

The BAU performs bus arbitration among bus masters.
A list of bus masters (units which can acquire the bus) is shown below.

Table 6-1. Bus Masters

Bus Master	Bus Cycle
CPU	Program fetch, data read/write
DMAU	DMA cycle
REFU	Refresh cycle
External bus master (HLDRQ pin input)	Bus cycle driven by external device

The relative priorities of the bus masters are shown below.

High — CPU (when BUSLOCK prefix is used)
↕ REFU (highest priority: when given number of requests are reached)
DMAU
HLDRQ pin
CPU (normal CPU cycle)
Low — REFU (lowest priority: cycle steal)

BAU bus arbitration is performed as follows.
A bus master such as the CPU, DMAU, REFU, etc., incorporated in the V40HL and V50HL normally release the bus at the end of the bus cycle currently being executed, as shown in Figure 6-1. However, in the case of a bus master connected to the HLDRQ pin, or cascaded external DMA controllers, for instance, the situation is as shown in Figure 6-2. The V40HL and V50HL request return of the bus by inactivating the acknowledge signal (HLDAK), and on receiving this request, the external bus master holding the bus should release the bus by dropping the bus hold request signal (HLDRQ). The V40HL and V50HL-internal bus master with the highest priority is kept waiting until the bus hold request signal is dropped. This is called a bus wait operation.

Figure 6-1. Internal Bus Cycles

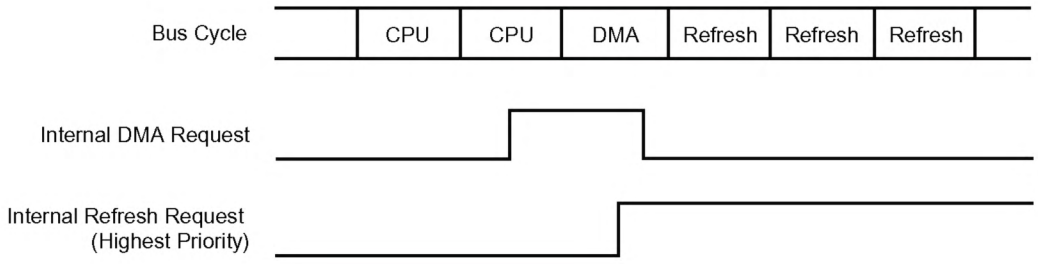
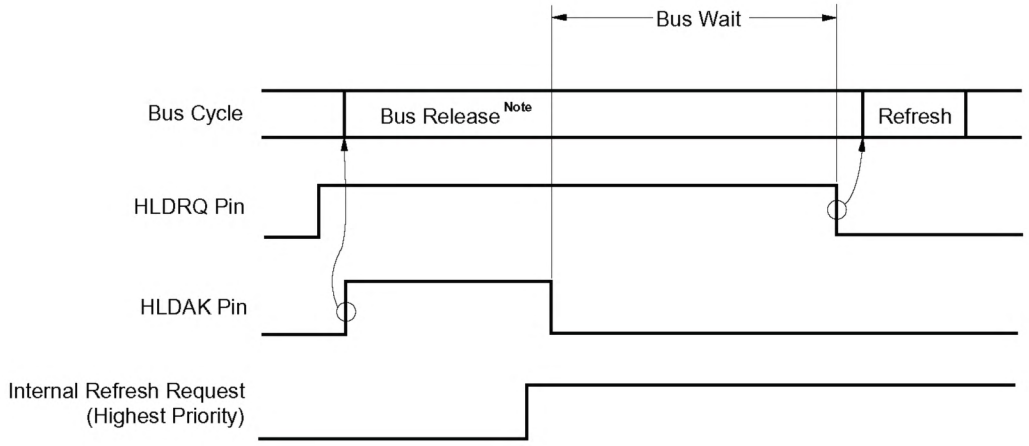


Figure 6-2. Bus Wait Operation



Note The period in which the external bus master which has been given the bus after its release by the V40HL and V50HL can use the bus.

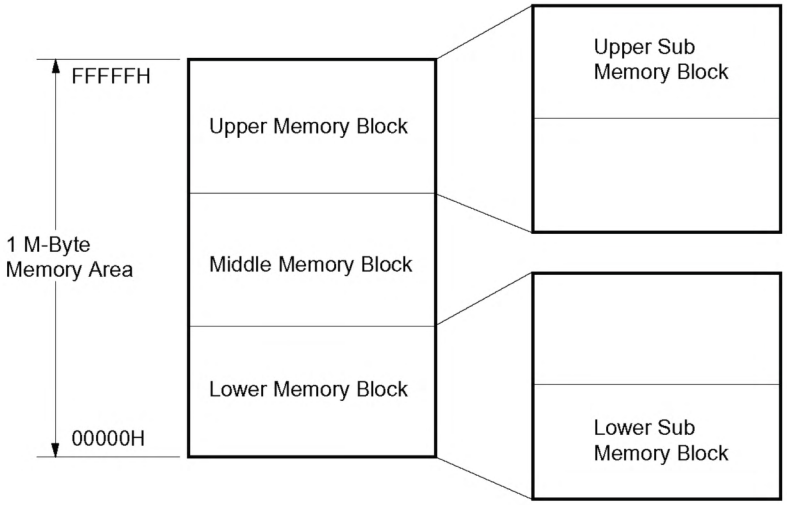
7. WCU (WAIT CONTROL UNIT)

The WCU has the function of automatically inserting a wait state (TW) of 0 to 3 clock cycles in a CPU, DMAU or REFU bus cycle.

7.1 FEATURES

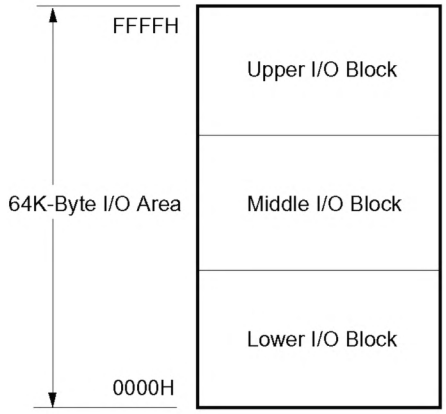
- Automatic setting of 0 to 3 waits for a CPU memory bus cycle
- 1M-byte memory space can be divided into 5
- 64K-byte I/O space can be divided into 3
- Automatic setting of 0 to 3 waits for an external I/O cycle
- Automatic setting of 0 to 3 waits for a DMA cycle
- Automatic setting of 0 to 3 waits for a refresh cycle
- Same as V40 and V50 directly after a reset (memory space divided into 3, no division of I/O space)

Figure 7-1. Example of Memory Space Division



Remark The division specification and the size of each block are set by means of a system I/O area register.

Figure 7-2. Example of I/O Space Division

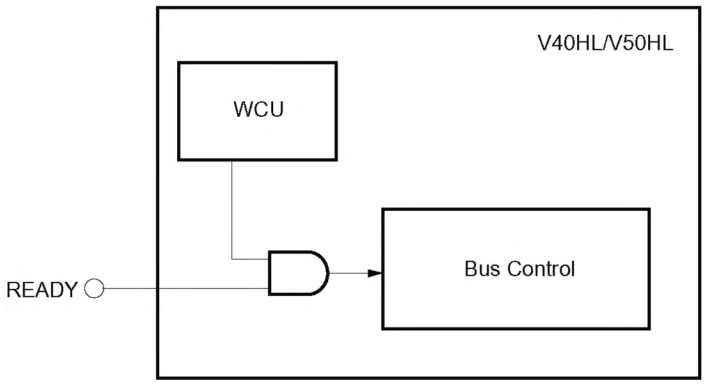


Remark The division specification and the size of each block are set by means of a system I/O area register.

7.2 RELATION BETWEEN WCU AND READY PIN

When wait cycles exceeding 3 clock cycles are necessary, the WCU and the READY signal pin can be used in combination. The number of wait cycles specified by the WCU set value or the number of wait cycles under READY control, whichever is larger, is inserted.

Figure 7-3. WCU and READY Control



8. REFU (REFRESH CONTROL UNIT)

The REFU generates refresh cycles required for refreshing of external DRAM. Refresh enabling/disabling and the refresh interval can be set programmably.

8.1 FEATURES

- Lowest-priority refreshing/highest-priority refreshing
- 7-refresh queue
- 16-bit refresh address
- $\overline{\text{REFRQ}}$ extended timing supported ($\overline{\text{REFRQ}}$ active from T1 state)

8.2 REFRESH OPERATIONS

The REFU has two priorities. Normally, it has the lowest priority, and a refresh cycle cannot be started unless the bus is completely idle. However, if there are 7 or more pending refresh requests, it is given the highest priority, and it requests the bus master holding the bus to relinquish it. (See **6. BAU**.)

The refresh address is output on A0 to A15. Every refresh cycle the refresh address is incremented by 1 (for the V40HL) or by 2 (for the V50HL), and the next refresh address is generated.

In a refresh cycle, a low-level signal is output on the low address pins (A16 to A19).

This refresh address is not affected by a reset. When the device is powered on, the refresh address is undefined.

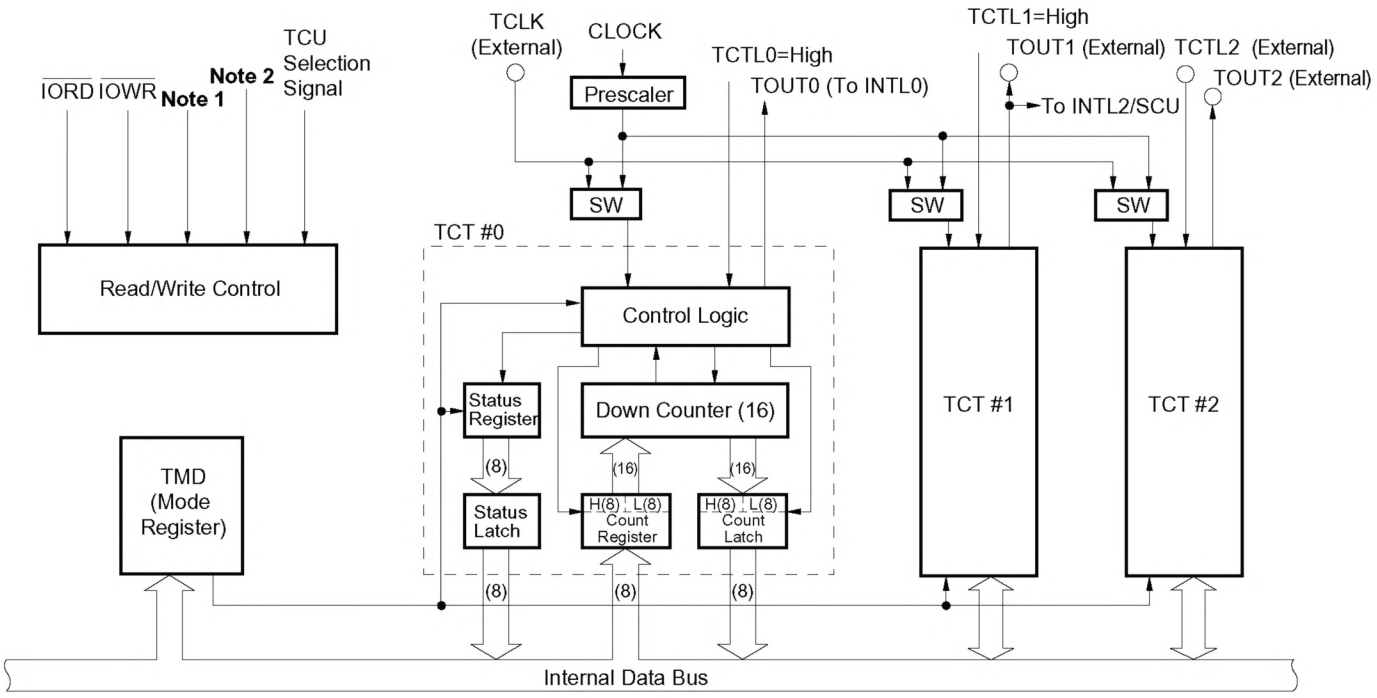
9. TCU (TIMER/COUNTER UNIT)

The TCU incorporates 3 counters, and can be used as a timer, event counter, rate generator, etc. Functionally it is a subset of the μPD71054.

9.1 FEATURES

- 3 × 16-bit counters
- Six programmable count modes
- Binary/BCD count
- Multiple latch command
- Choice of two input clocks: internal/external

9.2 TCU INTERNAL BLOCK DIAGRAM



Notes 1. A0 or A1 (Set by a system I/O area register)

2. A1 or A2 (Set by a system I/O area register)

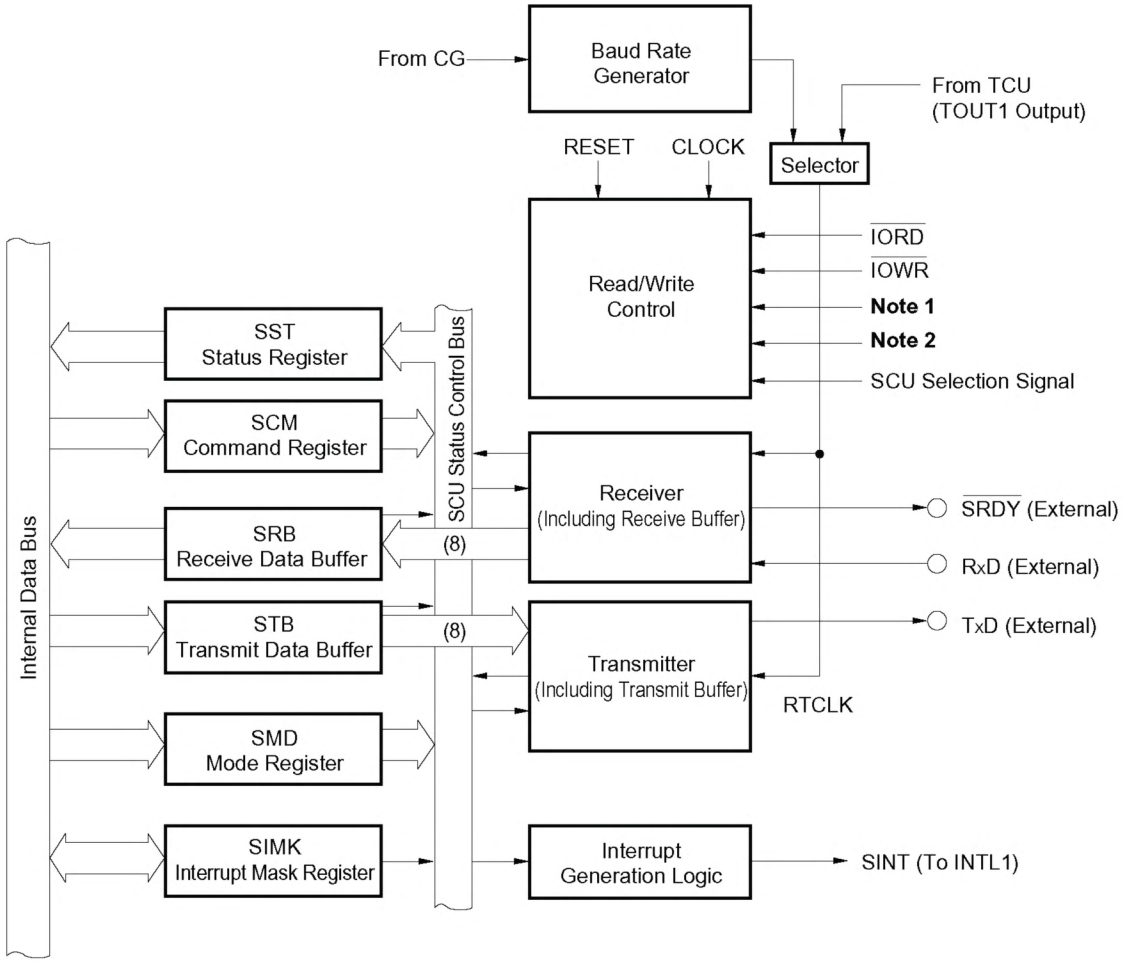
10. SCU (SERIAL CONTROL UNIT)

The SCU performs control of serial communication (asynchronous). Its functions are a subset of the μPD71051 excluding synchronous communication. Also, what was the control word register in the μPD71051 has been divided into two: a command register and a mode register.

10.1 FEATURES

- Dedicated baud rate generator incorporated (using internal clock)
- Asynchronous serial communication
- Clock rate: baud rate × 16, × 64
- Baud rate: DC – 500 kbps
- Character length: 7/8 bits
- Transmit stop bits: 1/2 bits
- Break transmission
- Automatic break detection
- Full-duplex double-buffer system
- Parity addition/checking
- Error detection: parity, overrun, framing
- Interrupt generation maskable

10.2 SCU INTERNAL BLOCK DIAGRAM



Notes 1. A0 or A1 (Set by a system I/O area register)

2. A1 or A2 (Set by a system I/O area register)

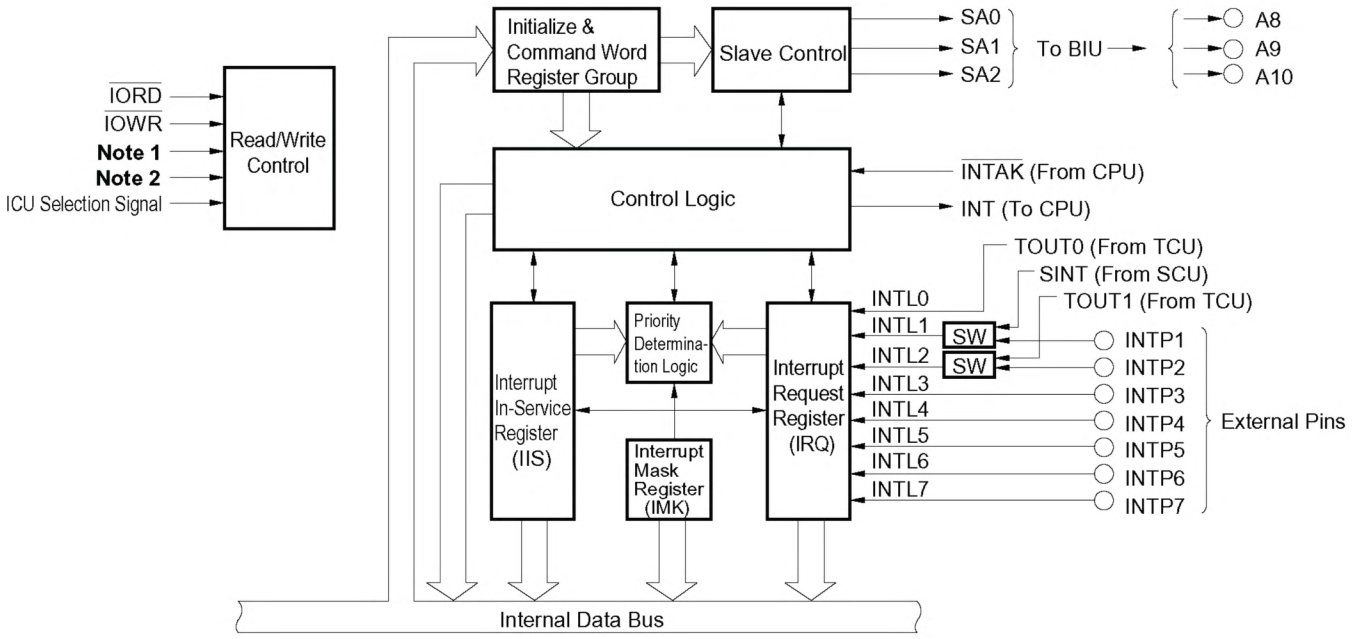
11. ICU (INTERRUPT CONTROL UNIT)

The ICU arbitrates among up to 8 interrupt requests (maskable interrupts) generated inside and outside the V40HL and V50HL, and transfers one of them to the CPU. The ICU functions comprise the functions of the V40HL and V50HL minus those functions not required by the V40HL and V50HL.

11.1 FEATURES

- 8 interrupt inputs
- μPD71059 cascading possible
- Edge- or level-triggered request input
  (input from internally connected TCU is edge-triggered only)
- Interrupt requests individually maskable
- Programmable interrupt request priority order
- Polling operation capability

11.2 ICU INTERNAL BLOCK DIAGRAM



Notes 1. A0 or A1 (Set by a system I/O area register)

2. A1 or A2 (Set by a system I/O area register)

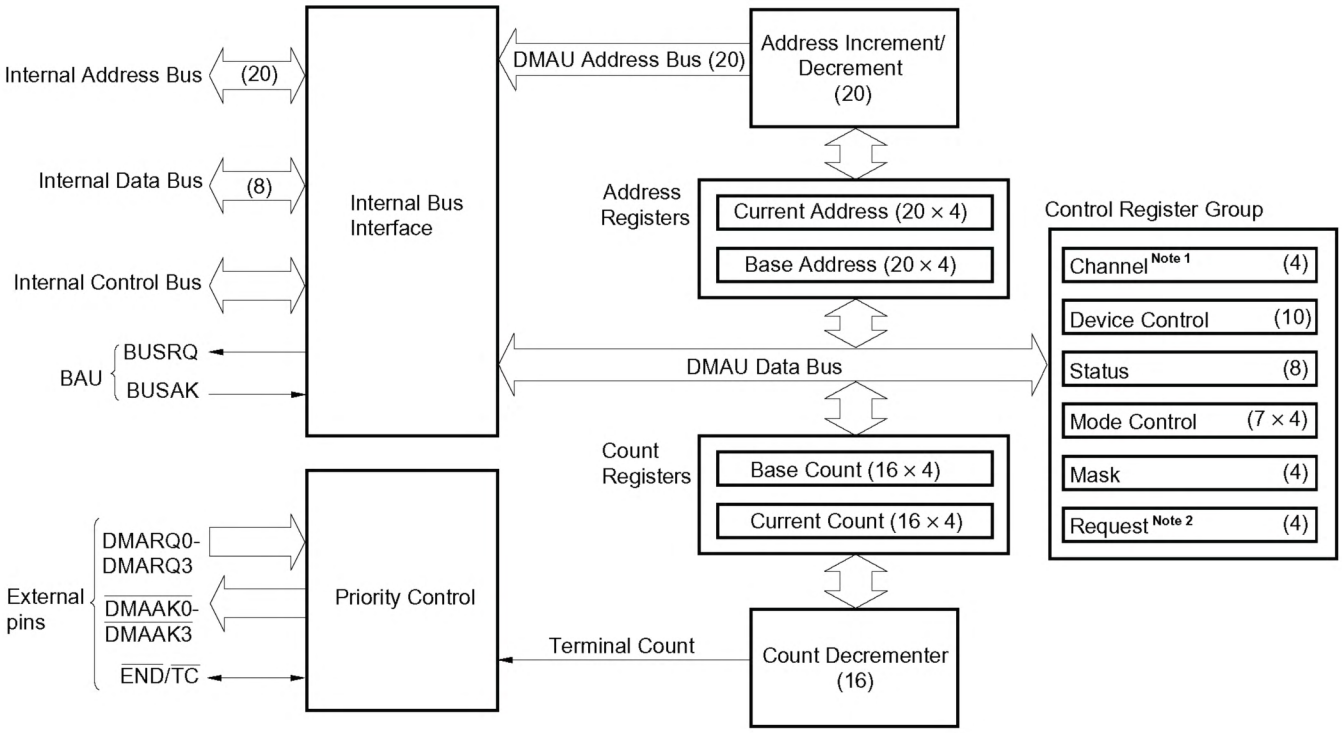
12. DMAU (DMA CONTROL UNIT)

The DMAU has 4 DMA channels, and provides the functions (subset) of two LSIs, the μPD71071 and μPD71037.

12.1 FEATURES

- Two operating modes (μPD71071 mode, μPD71037 mode)
- 20-bit address register
- 16-bit count register
- Four independent DMA channels
- Byte transfer/word transfer selectable
- Three transfer modes (settable on an individual channel basis)
  Single transfer mode, demand transfer mode, block transfer mode
- Two bus modes (common to all channels: in μPD71037 mode, bus release mode only)
  Bus release mode
  Bus hold mode
- DMA requests maskable on an individual channel basis
- Auto initialization function
- Transfer address increment/decrement
- Two channel priority systems (fixed priority/rotating priority)
- $\overline{TC}$ output at end of transfer
- Forced termination of service by $\overline{END}$ input
- Cascading capability

12.2 DMAU INTERNAL BLOCK DIAGRAM



Notes 1. In μPD71071 mode
2. In μPD71037 mode

13. STANDBY FUNCTIONS

The V40HL and V50HL have two modes, the HALT mode and STOP mode, as standby functions.

(1) HALT mode

When the HALT instruction is executed, the clock to internal CPU circuitry (excluding the HALT mode release circuit) is stopped.

(2) STOP mode

When the HALT instruction is executed, all clocks to the CPU and internal I/Os are stopped.
STOP mode should be used when a resonator is connected to the X1 and X2 pins.

Remark Switching between HALT mode and STOP mode is performed by setting a system I/O area register.

14. RESET OPERATION

When the $\overline{\text{RESET}}$ pin is driven low and this level is held for 4 clock cycles or more from the fall of the signal, the CPU and on-chip peripheral LSIs are reset.

When the $\overline{\text{RESET}}$ pin subsequently returns to the high level, the CPU begins an instruction prefetch from address FFFF0H.

When the V40HL and V50HL are reset, its status is fully compatible with the V40 and V50.

Extended functions added to those of the V40 and V50 are mapped onto unused V40 and V50 registers and the reserved area.

Table 14-1 shows the main statuses of the on-chip peripheral LSIs when a reset is performed.

Table 14-1. Main Statuses of On-Chip Peripheral LSIs After Reset

WCU	Memory, external I/O, DMA & refresh : 3-wait insertion Upper & lower memory blocks : set to 512 KB
REFU	Refresh cycle : set to 72 clock cycles Refresh enabling/disabling : not affected by reset
SCU	Baud rate : x 64 Character : 7 bits Parity : None Stop bits : 1 bit Break detection : None
DMAU	μPD71071 mode Demand mode Auto initialization disabled Verify transfer, byte transfer Bus release mode DMA enabled

Caution When a reset is performed, the SCU, TCU, ICU and DMAU cannot be used.

15. INSTRUCTION SET

Table 15-1. Operand Type Legend

Identifier	Description
reg	8/16-bit general register (destination register in an instruction using two 8/16-bit general registers)
reg'	Source register in an instruction using two 8/16-bit general registers
reg8	8-bit general register (destination register in an instruction using two 8-bit general registers)
reg8'	Source register in an instruction using two 8-bit general registers
reg16	16-bit general register (destination register in an instruction using two 16-bit general registers)
reg16'	Source register in an instruction using two 16-bit general registers
dmem	8/16-bit memory location
mem	8/16-bit memory location
mem8	8-bit memory location
mem16	16-bit memory location
mem32	32-bit memory location
imm	Constant in range 0 to FFFFH
imm3	Constant in range 0 to 7
imm4	Constant in range 0 to FH
imm8	Constant in range 0 to FFH
imm16	Constant in range 0 to FFFFH
acc	Accumulator AW or AL
sreg	Segment register
src-table	Name of 256-byte conversion translation table
src-block	Name of block addressed by register IX
dst-block	Name of block addressed by register IY
near-proc	Procedure in current program segment
far-proc	Procedure in a different program segment
near-label	Label in current program segment
short-label	Label in range –128 to +127 bytes from end of instruction
far-label	Label in a different program segment
memptr16	Word containing location offset in a different program segment to which control is to be shifted and segment base address
memptr32	Doubleword containing location offset in a different program segment to which control is to be shifted and segment base address
regptr16	General register containing location offset in a different program segment to which control is to be shifted
pop-value	Number of bytes to be removed from stack (0 to 64K, normally an even number)
fp-op	Immediate value which identifies external floating-point operation coprocessor operation code
R	Register set

Table 15-2. Operation Code Legend

Identifier	Description
W	Byte/word specification bit (0: byte, 1: word). However, when s =1, byte data of sign extension is 16-bit operand if W = 1.
reg	Register field (000 to 111)
reg'	Register field (000 to 111) (source register in instruction which uses two registers)
mem	Memory field (000 to 111)
mod	Mode field (00 to 10)
s	Sign-extended specification bit (0: without sign extension, 1: with sign extension)
X, XXX, YYY, ZZZ	Data used to determine external floating-point coprocessor operation code

Table 15-3. Operand Description Legend

Identifier	Description
AW	Accumulator (16-bit)
AH	Accumulator (high-order byte)
AL	Accumulator (low-order byte)
BW	Register BW (16-bit)
CW	Register CW (16-bit)
CL	Register CL (low-order byte)
DW	Register DW (16-bit)
BP	Base pointer (16-bit)
SP	Stack pointer (16-bit)
PC	Program counter (16-bit)
PSW	Program status word (16-bit)
IX	Index register (source) (16-bit)
IY	Index register (destination) (16-bit)
PS	Program segment register (16-bit)
SS	Stack segment register (16-bit)
DS0	Data segment 0 register (16-bit)
DS1	Data segment 1 register (16-bit)
AC	Auxiliary carry flag
CY	Carry flag
P	Parity flag
S	Sign flag
Z	Zero flag
DIR	Direction flag
IE	Interrupt enable flag
V	Overflow flag
BRK	Break flag
MD	Mode flag
(…)	Contents of memory indicated by contents of ( )
disp	Displacement (8/16-bit)
ext-disp8	16 bits with 8-bit displacement sign-extended
temp	Temporary register (8/16/32-bit)
TA	Temporary register A (16-bit)
TB	Temporary register B (16-bit)
TC	Temporary register C (16-bit)
tmpcy	Temporary carry flag (1-bit)
seg	Immediate segment data (16-bit)
offset	Immediate offset data (16-bit)
←	Transfer direction
+	Addition
–	Subtraction
×	Multiplication
÷	Division
%	Modulo
∧	Logical product
∨	Logical sum
∀	Exclusive logical sum
××H	Two-digit hexadecimal number
××××H	Four-digit hexadecimal number

Table 15-4. Flag Operation Legend

Identifier	Description
(Blank)	No change
0	Cleared to 0
1	Set to 1
×	Set or cleared depending upon result
U	Undefined
R	Previously saved value is restored

Table 15-5. Memory Addressing

mem \ mod	00	01	10
000	BW + IX	BW + IX + disp 8	BW + IX + disp 16
001	BW + IY	BW + IY + disp 8	BW + IY + disp 16
010	BP + IX	BP + IX + disp 8	BP + IX + disp 16
011	BP + IY	BP + IY + disp 8	BP + IY + disp 16
100	IX	IX + disp 8	IX + disp 16
101	IY	IY + disp 8	IY + disp 16
110	DIRECT ADDRESS	BP + disp 8	BP + disp 16
111	BW	BW + disp 8	BW + disp 16

Table 15-6. 8/16-Bit General Register Selection

reg, reg'	W=0	W=1
000	AL	AW
001	CL	CW
010	DL	DW
011	BL	BW
100	AH	SP
101	CH	BP
110	DH	IX
111	BH	IY

Table 15-7. Segment Register Selection

sreg	
00	DS1
01	PS
10	SS
11	DS0

The instruction set is shown in tabular form on the following pages.

Clock cycle shown in table is the time required for execution of instruction by the execution unit and is based on the following conditions.

- Prefetch time and wait time for using bus, etc. are not included.
- 0 wait is assumed for memory access. That is, the clock number of one bus cycle is four clock cycle.
- 0 wait is assumed for I/O access.
- Primitive block transfer instruction and primitive input/output instruction is included repeat prefixes.

The number of clock cycle of instruction with byte processing and word processing (with W bit) is shown as the followings.

(1) V40HL

On the left of "/" : The value corresponding to byte processing (W= 0) or word processing (W = 1) of even address

On the right of "/": The value corresponding to word processing (W =1) of odd address

For the clock of block transfer related instruction of V40HL, see **Table 15-8**.

Table 15-8. Number of Clock Cycles in Block Transfer Related Instruction (V40HL)

Instruction	Number of Clock Cycles	
	Byte Processing (W = 0)	Word Processing (W = 1)
MOVBK	9 + 8 × rep (9)	9 + 16 × rep (17)
CMPBK	7 + 14 × rep (13)	7 + 22 × rep (21)
CMPM	7 + 10 × rep (7)	7 + 14 × rep (11)
LDM	7 + 9 × rep (7)	7 + 13 × rep (11)
STM	5 + 4 × rep (5)	5 + 8 × rep (9)
INM	9 + 8 × rep (10)	9 + 16 × rep (18)
OUTM	9 + 8 × rep (10)	9 + 16 × rep (18)

Remark The figures in parentheses apply to one-time processing only.

(2) V50HL

On the left of "/" : The value corresponding to byte processing (W= 0) or word processing (W = 1) of even address

On the right of "/" : The value corresponding to word processing (W =1) of odd address

For the clock of block transfer related instruction of V50HL, see **Table 15-9**.

Table 15-9. Number of Clock Cycles in Block Transfer Related Instruction V50HL (1/2)

Instruction	Number of Clock Cycles			
	Byte Processing (W = 0)	Word Processing (W = 1)		
		Odd/Odd Address	Odd/Even Address	Even/Even Address
MOVBK	9 + 8 × rep (9)	9 + 16 × rep (17)	9 + 12 × rep (13)	9 + 8 × rep (9)
CMPBK	7 + 14 × rep (13)	7 + 22 × rep (21)	7 + 18 × rep (17)	7 + 14 × rep (13)
INM	9 + 8 × rep (10)	9 + 16 × rep (18)	9 + 12 × rep (14)	9 + 8 × rep (10)
OUTM	9 + 8 × rep (10)	9 + 16 × rep (18)	9 + 12 × rep (14)	9 + 8 × rep (10)

Remark The figures in parentheses apply to one-time processing only.

Table 15-9. Number of Clock Cycles in Block Transfer Related Instruction (V50HL) (2/2)

Instruction	Number of Clock Cycles		
	Byte Processing (W = 0)	Word Processing (W = 1)	
		Odd Address	Even Address
CMPM	7 + 10 × rep (7)	7 + 14 × rep (11)	7 + 10 × rep (7)
LDM	7 + 9 × rep (7)	7 + 13 × rep (11)	7 + 9 × rep (7)
STM	5 + 4 × rep (5)	5 + 8 × rep (9)	5 + 4 × rep (5)

Remark The figures in parentheses apply to one-time processing only.

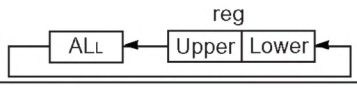
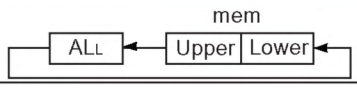
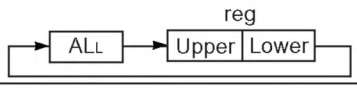
Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
Data transfer instructions	MOV	reg, reg'	1 0 0 0 1 0 1 W	1 1 reg reg'	2	2	2	reg ← reg'
		mem, reg	1 0 0 0 1 0 0 W	mod reg mem	2-4	7/11	7/11	(mem) ← reg
		reg, mem	1 0 0 0 1 0 1 W	mod reg mem	2-4	10/14	10/14	reg ← (mem)
		mem, imm	1 1 0 0 0 1 1 W	mod 0 0 0 mem	3-6	9/13	9/13	(mem) ← imm
		reg, imm	1 0 1 1 W reg		2-3	4	4	reg ← imm
		acc, dmem	1 0 1 0 0 0 0 W		3	10/14	10/14	If W=0: AL ← (dmem) If W=1: AH ← (dmem + 1), AL ← (dmem)
		dmem, acc	1 0 1 0 0 0 1 W		3	9/13	9/13	If W=0: (dmem) ←AL If W=1: (dmem + 1) ← AH, (dmem) ←AL
		sreg, reg16	1 0 0 0 1 1 1 0	1 1 0 sreg reg	2	2	2	sreg ← reg16 sreg:SS, DS0
		sreg, mem16	1 0 0 0 1 1 1 0	mod 0 sreg mem	2-4	14	10/14	sreg ← (mem16) sreg:SS, DS0
		reg16, sreg	1 0 0 0 1 1 0 0	1 1 0 sreg reg	2	2	2	reg16 ← sreg
		mem16, sreg	1 0 0 0 1 1 0 0	mod 0 sreg mem	2-4	12	8/12	(mem16) ← sreg
		DS0, reg16, mem32	1 1 0 0 0 1 0 1	mod reg mem	2-4	25	17/25	reg16← (mem32) DS0 ← (mem32 + 2)
		DS1, reg16, mem32	1 1 0 0 0 1 0 0	mod reg mem	2-4	25	17/25	reg16 ← (mem32) DS1 ← (mem32 + 2)
		AH, PSW	1 0 0 1 1 1 1 1		1	2	2	AH ← S, Z, ×, AC, ×, P, ×, CY
		PSW, AH	1 0 0 1 1 1 1 0		1	3	3	S, Z, ×, AC, ×, P, ×, CY← AH
	LDEA	reg16, mem16	1 0 0 0 1 1 0 1	mod reg mem	2-4	4	4	reg16 ←mem16
	TRANS	src-table	1 1 0 1 0 1 1 1		1	9	9	AL← (BW + AL)
	XCH	reg, reg'	1 0 0 0 0 1 1 W	1 1 reg reg'	2	3	3	reg ↔ reg'
		mem, reg reg, mem	1 0 0 0 0 1 1 W	mod reg mem	2-4	13/21	13/21	(mem) ↔ reg
		AW, reg16 reg16, AW	1 0 0 1 0 reg		1	3	3	AW ↔ reg16

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
Repeat prefixes	REPC		0 1 1 0 0 1 0 1		1	2	2	While CW ≠ 0, the following byte primitive block tra instruction is executed and CW is decremented (– If there is a pending interrupt, it is serviced. If CY ≠ 1 the loop is exited.
	REPNC		0 1 1 0 0 1 0 0		1	2	2	Same as above If CY ≠ 0 the loop is exited.
	REP REPE REPZ		1 1 1 1 0 0 1 1		1	2	2	While CW ≠ 0, the following byte primitive block tra instruction is executed and CW is decremented (– If there is a pending interrupt, it is serviced. If the primitive block transfer instruction is CMPBK CMPM and Z ≠ 1 the loop is exited.
	REPNE REPNZ		1 1 1 1 0 0 1 0		1	2	2	Same as above If Z ≠ 0 the loop is exited.
Primitive block transfer instructions	MOVBK	dst-block, src-block	1 0 1 0 0 1 0 W		1	See **Table 15-8**	See **Table 15-9**	If W = 0: (IY) ← (IX) DIR = 0 : IX ← IX + 1, IY ← IY + 1 DIR = 1 : IX ← IX – 1, IY ← IY – 1 If W = 1: (IY + 1, IY) ← (IX + 1, IX) DIR = 0 : IX ← IX + 2, IY ← IY + 2 DIR = 1 : IX ← IX – 2, IY ← IY – 2
	CMPBK	src-block, dst-block	1 0 1 0 0 1 1 W		1	See **Table 15-8**	See **Table 15-9**	If W = 0: (IX) – (IY) DIR = 0 : IX ← IX + 1, IY ← IY + 1 DIR = 1 : IX ← IX – 1, IY ← IY – 1 If W = 1: (IX + 1, IX) – (IY + 1, IY) DIR = 0 : IX ← IX + 2, IY ← IY + 2 DIR = 1 : IX ← IX – 2, IY ← IY – 2
	CMPM	dst-block	1 0 1 0 1 1 1 W		1	See **Table 15-8**	See **Table 15-9**	If W = 0: AL – (IY) DIR = 0 : IY ← IY + 1; DIR = 1 : IY ← IY – 1 If W = 1: AW – (IY + 1, IY) DIR = 0 : IY ← IY + 2; DIR = 1 : IY ← IY – 2
	LDM	src-block	1 0 1 0 1 1 0 W		1	See **Table 15-8**	See **Table 15-9**	If W = 0: AL ← (IX) DIR = 0 : IX ← IX + 1; DIR = 1 : IX ← IX – 1 If W = 1: AW ← (IX + 1, IX) DIR = 0 : IX + 2; DIR = 1 : IX ← IX – 2
	STM	dst-block	1 0 1 0 1 0 1 W		1	See **Table 15-8**	See **Table 15-9**	If W = 0: (IY) ← AL DIR = 0 : IY ← IY + 1; DIR = 1 : IY ← IY – 1 If W = 1: (IY + 1, IY) ← AW DIR = 0 : IY ← IY + 2; DIR = 1 : IY ← IY – 2

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
Bit field manipulation instructions	INS	reg8, reg8'	0 0 0 0 1 1 1 1	0 0 1 1 0 0 0 1	3	35-133	31-117/	16-bit field ← AW
			1 1 reg' reg				35-133	
		reg8, imm4	0 0 0 0 1 1 1 1	0 0 1 1 1 0 0 1	4	35-133	31-117/	16-bit field ← AW
			1 1 0 0 0 reg				35-133	
	EXT	reg8, reg8'	0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	3	34-59	26-55/	AW ← 16-bit field
			1 1 reg' reg				34-59	
		reg8, imm4	0 0 0 0 1 1 1 1	0 0 1 1 1 0 1 1	4	34-59	26-55/	AW ← 16-bit field
			1 1 0 0 0 reg				34-59	
Input/output instructions	IN	acc, imm8	1 1 1 0 0 1 0 W		2	9/13	9/13[Note]	If W = 0: AL ← (imm8) If W = 1: AH ← (imm8 + 1), AL ← (imm8)
		acc, DW	1 1 1 0 1 1 0 W		1	8/12	8/12[Note]	If W = 0: AL ← (DW) If W = 1: AH ← (DW + 1), AL ← (DW)
	OUT	imm8, acc	1 1 1 0 0 1 1 W		2	8/12	8/12[Note]	If W = 0: (imm8) ← AL If W = 1: (imm8 + 1) ← AH, (imm8) ← AL
		DW, acc	1 1 1 0 1 1 1 W		1	8/12	8/12[Note]	If W = 0: (DW) ← AL If W = 1: (DW + 1) ← AH, (DW) ← AL
Primitive input/output instructions	INM	dst-block, DW	0 1 1 0 1 1 0 W		1	See **Table 15-8**	See **Table 15-9**	If W = 0: (IY) ← (DW) DIR = 0 : IY ← IY + 1 ; DIR = 1 : IY ← IY – 1 If W = 1: (IY + 1, IY) ← (DW + 1, DW) DIR = 0 : IY ← IY + 2 ; DIR = 1 : IY ← IY – 2
	OUTM	DW, src-block	0 1 1 0 1 1 1 W		1	See **Table 15-8**	See **Table 15-9**	If W = 0: (DW) ← (IX) DIR = 0 : IX ← IX + 1 ; DIR = 1 : IX ← IX – 1 If W = 1: (DW + 1, DW) ← (IX + 1, IX) DIR = 0 : IX ← IX + 2 ; DIR = 1 : IX ← IX – 2

Note In case of IN/OUT instruction to internal DMAU, the number of word processing clock cycles applied is always that to the right

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
Addition/subtraction instructions	ADD	reg, reg'	0 0 0 0 0 0 1 W	1 1 reg reg'	2	2	2	reg ← reg + reg'
		mem, reg	0 0 0 0 0 0 0 W	mod reg mem	2-4	13/21	13/21	(mem) ← (mem) + reg
		reg, mem	0 0 0 0 0 0 1 W	mod reg mem	2-4	10/14	10/14	reg ← reg + (mem)
		reg, imm	1 0 0 0 0 0 s W	1 1 0 0 0 reg	3-4	4	4	reg ← reg + imm
		mem, imm	1 0 0 0 0 0 s W	mod 0 0 0 mem	3-6	15/23	15/23	(mem) ← (mem) + imm
		acc, imm	0 0 0 0 0 1 0 W		2-3	4	4	If W = 0: AL ← AL + imm If W = 1: AW ← AW + imm
	ADDC	reg, reg'	0 0 0 1 0 0 1 W	1 1 reg reg'	2	2	2	reg ← reg + reg'+ CY
		mem, reg	0 0 0 1 0 0 0 W	mod reg mem	2-4	13/21	13/21	(mem) ← (mem) + reg + CY
		reg, mem	0 0 0 1 0 0 1 W	mod reg mem	2-4	10/14	10/14	reg ← reg + (mem) + CY
		reg, imm	1 0 0 0 0 0 s W	1 1 0 1 0 reg	3-4	4	4	reg ← reg + imm + CY
		mem, imm	1 0 0 0 0 0 s W	mod 0 1 0 mem	3-6	15/23	15/23	(mem) ← (mem) + imm + CY
		acc, imm	0 0 0 1 0 1 0 W		2-3	4	4	If W = 0: AL ← AL + imm + CY If W = 1: AW ← AW + imm + CY
	SUB	reg, reg'	0 0 1 0 1 0 1 W	1 1 reg reg'	2	2	2	reg ← reg – reg'
		mem, reg	0 0 1 0 1 0 0 W	mod reg mem	2-4	13/21	13/21	(mem) ← (mem) – reg
		reg, mem	0 0 1 0 1 0 1 W	mod reg mem	2-4	10/14	10/14	reg ← reg – (mem)
		reg, imm	1 0 0 0 0 0 s W	1 1 1 0 1 reg	3-4	4	4	reg ← reg – imm
		mem, imm	1 0 0 0 0 0 s W	mod 1 0 1 mem	3-6	15/23	15/23	(mem) ← (mem) – imm
		acc, imm	0 0 1 0 1 1 0 W		2-3	4	4	If W = 0: AL ← AL – imm If W = 1: AW ← AW – imm
	SUBC	reg, reg'	0 0 0 1 1 0 1 W	1 1 reg reg'	2	2	2	reg ← reg – reg'– CY
		mem, reg	0 0 0 1 1 0 0 W	mod reg mem	2-4	13/21	13/21	(mem) ← (mem) – reg – CY
		reg, mem	0 0 0 1 1 0 1 W	mod reg mem	2-4	10/14	10/14	reg ← reg – (mem) – CY
		reg, imm	1 0 0 0 0 0 s W	1 1 0 1 1 reg	3-4	4	4	reg ← reg – imm – CY
		mem, imm	1 0 0 0 0 0 s W	mod 0 1 1 mem	3-6	15/23	15/23	(mem) ← (mem) – imm – CY
		acc, imm	0 0 0 1 1 1 0 W		2-3	4	4	If W = 0: AL ← AL – imm – CY If W = 1: AW ← AW imm– CY

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
BCD operation instructions	ADD4S		0 0 0 0 1 1 1 1	0 0 1 0 0 0 0 0	2	19 × n + 7	19 × n + 7	dst BCD string ← dst BCD string + src BCD string*
	SUB4S		0 0 0 0 1 1 1 1	0 0 1 0 0 0 1 0	2	19 × n + 7	19 × n + 7	dst BCD string ← dst BCD string – src BCD string*
	CMP4S		0 0 0 0 1 1 1 1	0 0 1 0 0 1 1 0	2	19 × n + 7	19 × n + 7	dst BCD string – src BCD string*
	ROL4	reg8	0 0 0 0 1 1 1 1 1 1 0 0 0 reg	0 0 1 0 1 0 0 0	3	13	13	
		mem8	0 0 0 0 1 1 1 1 mod 0 0 0 mem	0 0 1 0 1 0 0 0	3-5	25	25	
	ROR4	reg8	0 0 0 0 1 1 1 1 1 1 0 0 0 reg	0 0 1 0 1 0 1 0	3	17	17	
		mem8	0 0 0 0 1 1 1 1 mod 0 0 0 mem	0 0 1 0 1 0 1 0	3-5	29	29	
Increment/decrement instructions	INC	reg8	1 1 1 1 1 1 1 0	1 1 0 0 0 reg	2	2	2	reg8 ← reg8 + 1
		mem	1 1 1 1 1 1 1 W	mod 0 0 0 mem	2-4	13/21	13/21	(mem) ← (mem) + 1
		reg16	0 1 0 0 0 reg		1	2	2	reg16 ← reg16 + 1
	DEC	reg8	1 1 1 1 1 1 1 0	1 1 0 0 1 reg	2	2	2	reg8 ← reg8 – 1
		mem	1 1 1 1 1 1 1 W	mod 0 0 1 mem	2-4	13/21	13/21	(mem) ← (mem) – 1
		reg16	0 1 0 0 1 reg		1	2	2	reg16 ← reg16 – 1

n: 1/2 the number of BCD digits

* The number of BCD digits is given by the CL register: a value between 1 a

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
Multiplication instructions	MULU	reg8	1 1 1 1 0 1 1 0	1 1 1 0 0 reg	2	21-22	21-22	AW ← AL × reg8 AH = 0: CY ← 0, V ← 0 AH ≠ 0: CY ← 1, V ← 1
		mem8	1 1 1 1 0 1 1 0	mod 1 0 0 mem	2-4	26-27	26-27	AW ← AL × (mem8) AH = 0: CY ← 0, V ← 0 AH ≠ 0: CY ← 1, V ← 1
		reg16	1 1 1 1 0 1 1 1	1 1 1 0 0 reg	2	29-30	29-30	DW, AW ← AW × reg16 DW = 0: CY ← 0, V ← 0 DW ≠ 0: CY ← 1, V ← 1
		mem16	1 1 1 1 0 1 1 1	mod 1 0 0 mem	2-4	38-39	34-35/ 38-39	DW, AW ← AW × (mem16) DW = 0: CY ← 0, V ← 0 DW ≠ 0: CY ←1, V ← 1
	MUL	reg8	1 1 1 1 0 1 1 0	1 1 1 0 1 reg	2	33-39	33-39	AW ←AL × reg8 AH = AL sign extension: CY ← 0, V ← 0 AH ≠ AL sign extension: CY ← 1, V ← 1
		mem8	1 1 1 1 0 1 1 0	mod 1 0 1 mem	2-4	38-44	38-44	AW ← AL × (mem8) AH = AL sign extension: CY ← 0, V ← 0 AH ≠ AL sign extension: CY ← 1, V ← 1
		reg16	1 1 1 1 0 1 1 1	1 1 1 0 1 reg	2	41-47	41-47	DW, AW ← AW × reg16 DW = AW sign extension: CY ← 0, V ← 0 DW ≠ AW sign extension: CY ← 1, V ← 1
		mem16	1 1 1 1 0 1 1 1	mod 1 0 1 mem	2-4	50-56	46-52/ 50-56	DW, AW ← AW × (mem16) DW = AW sign extension: CY ← 0, V ← 0 DW ≠ AW sign extension: CY ← 1, V ← 1
		reg16, (reg16',)[Note] imm8	0 1 1 0 1 0 1 1	1 1 reg reg'	3	28-34	28-34	reg16 ← reg16' × imm8 Product ≤ 16 bits : CY ← 0, V ← 0 Product > 16 bits : CY ← 1, V ← 1
		reg16, mem16, imm8	0 1 1 0 1 0 1 1	mod reg mem	3-5	37-43	33-39/ 37-43	reg16 ← (mem16) × imm8 Product ≤ 16 bits : CY ← 0, V ← 0 Product > 16 bits : CY ← 1, V ← 1
		reg16, (reg16',)[Note] imm16	0 1 1 0 1 0 0 1	1 1 reg reg'	4	36-42	36-42	reg16 ← reg16' × imm16 Product ≤ 16 bits : CY ← 0, V ← 0 Product > 16 bits : CY ← 1, V ← 1
		reg16, mem16, imm16	0 1 1 0 1 0 0 1	mod reg mem	4-6	45-51	41-47/ 45-51	reg16 ← (mem16) × imm16 Product ≤ 16 bits : CY ← 0, V ← 0 Product > 16 bits : CY ← 1, V ← 1

Note The 2nd operand can be omitted, in which case the same register as the 1st operand is taken as being specified.

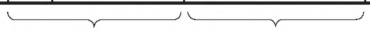
Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
Unsigned division instructions	DIVU	reg8	1 1 1 1 0 1 1 0	1 1 1 1 0 reg	2	19	19	temp ← AW If temp ÷ reg8 ≤ FFH AH ← temp%reg8, AL ←temp ÷ reg8 If temp ÷ reg8 > FFH TA ← (001H, 000H), TC ← (003H, 002H) SP ← SP – 2, (SP + 1, SP) ← PSW, IE ← 0, BRK SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP – 2, (SP + 1, SP) ← PC, PC ← TA
		mem8	1 1 1 1 0 1 1 0	mod 1 1 0 mem	2-4	24	24	temp ← AW If temp ÷ (mem8) ≤ FFH AH ← temp%(mem8), AL ←temp ÷ (mem8) If temp ÷ (mem8) > FFH TA ← (001H, 000H), TC ← (003H, 002H) SP ← SP – 2, (SP + 1, SP) ← PSW, IE ← 0, BRK SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP – 2, (SP + 1, SP) ← PC, PC ← TA
		reg16	1 1 1 1 0 1 1 1	1 1 1 1 0 reg	2	25	25	temp ← DW, AW If temp ÷ reg16 ≤ FFFFH DW ← temp%reg16, AW ←temp ÷ reg16 If temp ÷ reg16 > FFFFH TA ← (001H, 000H), TC ← (003H, 002H) SP ← SP – 2, (SP + 1, SP) ← PSW, IE ← 0, BRK SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP – 2, (SP + 1, SP) ← PC, PC ← TA
		mem16	1 1 1 1 0 1 1 1	mod 1 1 0 mem	2-4	34	30/34	temp ← DW, AW If temp ÷ (mem16) ≤ FFFFH DW ← temp%(mem16), AW ←temp ÷ (mem16) If temp ÷ (mem16) > FFFFH TA ← (001H, 000H), TC ← (003H, 002H) SP ← SP – 2, (SP + 1, SP) ← PSW, IE ← 0, BRK SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP – 2, (SP + 1, SP) ← PC, PC ← TA

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
Signed division instructions	DIV	reg8	1 1 1 1 0 1 1 0	1 1 1 1 1 reg	2	29-34	29-34	temp ← AW If temp ÷ reg8 > 0 and temp ÷ reg8 ≤ 7FH or temp ÷ reg8 < 0 and temp ÷ reg8 > 0 – 7FH –1 AH ← temp%reg8, AL ← temp ÷ reg8 If temp ÷ reg8 > 0 and temp ÷ reg8 > 7FH or temp ÷ reg8 < 0 and temp ÷ reg8 ≤ 0 – 7FH –1 TA ← (001H, 000H), TC ← (003H, 002H) SP ← SP – 2, (SP + 1, SP) ← PSW, IE ← 0, BRK SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP – 2, (SP + 1, SP) ← PC, PC ← TA
		mem8	1 1 1 1 0 1 1 0	mod 1 1 1 mem	2-4	34-39	34-39	temp ← AW If temp ÷ (mem8) > 0 and temp ÷ (mem8) ≤ 7FH or temp ÷ (mem8) < 0 and temp ÷ (mem8) > 0 – 7F AH ← temp%(mem8), AL ← temp ÷(mem8) If temp ÷ (mem8) > 0 and temp ÷ (mem8) > 7FH or temp ÷ (mem8) < 0 and temp ÷ (mem8) ≤ 0 – 7F TA ← (001H, 000H), TC ← (003H, 002H) SP ← SP – 2, (SP + 1, SP) ← PSW, IE ← 0, BRK SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP – 2, (SP + 1, SP) ← PC, PC ← TA
		reg16	1 1 1 1 0 1 1 1	1 1 1 1 1 reg	2	38-43	38-43	temp ← DW, AW If temp ÷ reg16 > 0 and temp ÷ reg16 ≤ 7FFFH or temp ÷ reg16 < 0 and temp ÷ reg16 > 0 – 7FFFH DW ← temp%reg16, AW ← temp ÷ reg16 If temp ÷ reg16 > 0 and temp ÷ reg16 > 7FFFH or temp ÷ reg16 < 0 and temp ÷ reg16 ≤ 0 – 7FFFH TA ← (001H, 000H), TC ← (003H, 002H) SP ← SP – 2, (SP + 1, SP) ← PSW, IE ← 0, BRK SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP – 2, (SP + 1, SP) ← PC, PC ← TA
		mem16	1 1 1 1 0 1 1 1	mod 1 1 1 mem	2-4	47-52	43-48/ 47-52	temp ← DW, AW If temp ÷ (mem16) > 0 and temp ÷ (mem16) ≤ 7FF or temp ÷ (mem16) < 0 and temp ÷ (mem16) > 0 – –1 DW ← temp%(mem16), AW ← temp ÷ (mem16) If temp ÷ (mem16) > 0 and temp ÷ (mem16) > 7FF or temp ÷ (mem16) < 0 and temp ÷ (mem16) ≤ 0 – –1 TA ← (001H, 000H), TC ← (003H, 002H) SP ← SP – 2, (SP + 1, SP) ← PSW, IE ← 0, BRK

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
BCD adjustment instructions	ADJBA		0 0 1 1 0 1 1 1		1	7	7	If AL ∧ 0FH > 9 or AC = 1: AL ← AL + 6 AH ← AH + 1, AC ← 1, CY ← AC, AL ← AL ∧ 0FH
	ADJ4A		0 0 1 0 0 1 1 1		1	3	3	If AL ∧ 0FH > 9 or AC = 1 AL ← AL + 6, CY ← CY ∨ AC , AC← 1 If AL > 9FH or CY = 1 AL ← AL + 60H, CY ← 1
	ADJBS		0 0 1 1 1 1 1 1		1	7	7	If AL ∧ 0FH > 9 or AC = 1 AL ← AL – 6, AH ← AH – 1 , AC← 1 CY ← AC, AL ← AL ∧ 0FH
	ADJ4S		0 0 1 0 1 1 1 1		1	3	3	If AL ∧ 0FH > 9 or AC = 1 AL ← AL –6, CY ← CY ∨ AC , AC← 1 If AL > 9FH or CY = 1 AL ← AL – 60H, CY ← 1
Data conversion instructions	CVTBD		1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0	2	15	15	AH ← AL ÷ 0AH, AL ← AL%0AH
	CVTDB		1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0	2	7	7	AL ← AH × 0AH + AL, AH ← 0
	CVTBW		1 0 0 1 1 0 0 0		1	2	2	If AL < 80H: AH ← 0, otherwise: AH ← FFH
	CVTWL		1 0 0 1 1 0 0 1		1	4-5	4-5	If AW < 8000H: DW ← 0, otherwise: DW ← FFFFH
Comparison instructions	CMP	reg, reg'	0 0 1 1 1 0 1 W	1 1 reg reg'	2	2	2	reg – reg'
		mem, reg	0 0 1 1 1 0 0 W	mod reg mem	2-4	10/14	10/14	(mem) – reg
		reg, mem	0 0 1 1 1 0 1 W	mod reg mem	2-4	10/14	10/14	reg – (mem)
		reg, imm	1 0 0 0 0 0 s W	1 1 1 1 1 reg	3-4	4	4	reg – imm
		mem, imm	1 0 0 0 0 0 s W	mod 1 1 1 mem	3-6	12/16	12/16	(mem) – imm
		acc, imm	0 0 1 1 1 1 0 W		2-3	4	4	If W = 0: AL – imm If W = 1: AW – imm
Complement operation instructions	NOT	reg	1 1 1 1 0 1 1 W	1 1 0 1 0 reg	2	2	2	reg ← $\overline{\text{reg}}$
		mem	1 1 1 1 0 1 1 W	mod 0 1 0 mem	2-4	13/21	13/21	(mem) ← $\overline{\text{(mem)}}$
	NEG	reg	1 1 1 1 0 1 1 W	1 1 0 1 1 reg	2	2	2	reg ← $\overline{\text{reg}}$ + 1
		mem	1 1 1 1 0 1 1 W	mod 0 1 mem	2-4	13/21	13/21	(mem) ← $\overline{\text{(mem)}}$ + 1

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
Logical operation instructions	TEST	reg, reg'	1 0 0 0 0 1 0 W	1 1 reg' reg	2	2	2	reg ∧ reg'
		mem, reg reg, mem	1 0 0 0 0 1 0 W	mod reg mem	2-4	9/13	9/13	(mem) ∧ reg
		reg, imm	1 1 1 1 0 1 1 W	1 1 0 0 0 reg	3-4	4	4	reg ∧ imm
		mem, imm	1 1 1 1 0 1 1 W	mod 0 0 0 mem	3-6	10/14	10/14	(mem) ∧ imm
		acc, imm	1 0 1 0 1 0 0 W		2-3	4	4	If W = 0: AL ∧ imm8 If W = 1: AW ∧ imm16
	AND	reg, reg'	0 0 1 0 0 0 1 W	1 1 reg reg'	2	2	2	reg ← reg ∧ reg'
		mem, reg	0 0 1 0 0 0 0 W	mod reg mem	2-4	13/21	13/21	(mem) ← (mem) ∧ reg
		reg, mem	0 0 1 0 0 0 1 W	mod reg mem	2-4	10/14	10/14	reg ← reg ∧ (mem)
		reg, imm	1 0 0 0 0 0 0 W	1 1 1 0 0 reg	3-4	4	4	reg ← reg ∧ imm
		mem, imm	1 0 0 0 0 0 0 W	mod 1 0 0 mem	3-6	15/23	15/23	(mem) ← (mem) ^ imm
		acc, imm	0 0 1 0 0 1 0 W		2-3	4	4	If W = 0: AL ← AL ∧ imm8 If W = 1: AW ← AW ^ imm16
	OR	reg, reg'	0 0 0 0 1 0 1 W	1 1 reg reg'	2	2	2	reg ← reg ∨ reg'
		mem, reg	0 0 0 0 1 0 0 W	mod reg mem	2-4	13/21	13/21	(mem) ← (mem) ∨ reg
		reg, mem	0 0 0 0 1 0 1 W	mod reg mem	2-4	10/14	10/14	reg ← reg ∨ (mem)
		reg, imm	1 0 0 0 0 0 0 W	1 1 0 0 1 reg	3-4	4	4	reg ← reg ∨ imm
		mem, imm	1 0 0 0 0 0 0 W	mod 0 0 1 mem	3-6	15/23	15/23	(mem) ← (mem) ∨ imm
		acc, imm	0 0 0 0 1 1 0 W		2-3	4	4	If W = 0: AL ← AL ∨ imm8 If W = 1: AW ← AW ∨ imm16
	XOR	reg, reg'	0 0 1 1 0 0 1 W	1 1 reg reg'	2	2	2	reg ← reg ⊻ reg'
		mem, reg	0 0 1 1 0 0 0 W	mod reg mem	2-4	13/21	13/21	(mem) ← (mem) ⊻ reg
		reg, mem	0 0 1 1 0 0 1 W	mod reg mem	2-4	10/14	10/14	reg ← reg ⊻ (mem)
		reg, imm	1 0 0 0 0 0 0 W	1 1 1 1 0 reg	3-4	4	4	reg ← reg ⊻ imm
		mem, imm	1 0 0 0 0 0 0 W	mod 1 1 0 mem	3-6	15/23	15/23	(mem) ← (mem) ⊻ imm
		acc, imm	0 0 1 1 0 1 0 W		2-3	4	4	If W = 0: AL ← AL ⊻ imm8 If W = 1: AW ← AW ⊻ imm16

Instruction Group	Mnemonic	Operand(s)	Operation Code 7 6 5 4 3 2 1 0	Operation Code 7 6 5 4 3 2 1 0	Bytes	Clock Cycles V40HL	Clock Cycles V50HL	Operation
Bit manipulation instructions	TEST1	reg8, CL	0 0 0 1 0 0 0 0	1 1 0 0 0 reg	3	3	3	reg8 bit NO.CL = 0 : Z ← 1 reg8 bit NO.CL = 1 : Z ← 0
		mem8, CL	0 0 0 0	mod 0 0 0 mem	3-5	7	7	(mem8) bit NO.CL = 0 : Z← 1 (mem8) bit NO.CL = 1 : Z← 0
		reg16, CL	0 0 0 1	1 1 0 0 0 mem	3	3	3	reg16 bit NO.CL = 0 : Z ← 1 reg16 bit NO.CL = 1 : Z ← 0
		mem16, CL	0 0 0 1	mod 0 0 0 mem	3-5	11	7/11	(mem16) bit NO.CL = 0 : Z← 1 (mem16) bit NO.CL = 1 : Z← 0
		reg8, imm3	1 0 0 0	1 1 0 0 0 reg	4	4	4	reg8 bit NO.imm3 = 0 : Z ← 1 reg8 bit NO.imm3 = 1 : Z ← 0
		mem8, imm3	1 0 0 0	mod 0 0 0 mem	4-6	8	8	(mem8) bit NO.imm3 = 0 : Z← 1 (mem8) bit NO.imm3 = 1 : Z← 0
		reg16, imm4	1 0 0 1	1 1 0 0 0 reg	4	4	4	reg16 bit NO.imm4 = 0 : Z ← 1 reg16 bit NO.imm4 = 1 : Z ← 0
		mem16, imm4	1 0 0 1	mod 0 0 0 mem	4-6	12	8/12	(mem16) bit NO.imm4 = 0 : Z← 1 (mem16) bit NO.imm4 = 1 : Z← 0
	NOT1	reg8, CL	0 1 1 0	1 1 0 0 0 reg	3	4	4	reg8 bit NO.CL← $\overline{\text{reg8 bit NO.CL}}$
		mem8, CL	0 1 1 0	mod 0 0 0 mem	3-5	10	10	(mem8) bit NO.CL← $\overline{\text{(mem8) bit NO.CL}}$
		reg16, CL	0 1 1 1	1 1 0 0 0 reg	3	4	4	reg16 bit NO.CL← $\overline{\text{reg16 bit NO.CL}}$
		mem16, CL	0 1 1 1	mod 0 0 0 mem	3-5	18	10/18	(mem16) bit NO.CL← $\overline{\text{(mem16) bit NO.CL}}$
		reg8, imm3	1 1 1 0	1 1 0 0 0 reg	4	5	5	reg8 bit NO.imm3← $\overline{\text{reg8 bit NO.imm3}}$
		mem8, imm3	1 1 1 0	mod 0 0 0 mem	4-6	11	11	(mem8) bit NO.imm3← $\overline{\text{(mem8) bit NO.imm3}}$
		reg16, imm4	1 1 1 1	1 1 0 0 0 reg	4	5	5	reg16 bit NO.imm4← $\overline{\text{reg16 bit NO.imm4}}$
		mem16, imm4	1 1 1 1	mod 0 0 0 mem	4-6	19	11/19	(mem16) bit NO.imm4← $\overline{\text{(mem16) bit NO.imm4}}$



* 1st byte = 0FH

	NOT1	CY	1 1 1 1 0 1 0 1		1	2	2	CY← $\overline{\text{CY}}$

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
Bit manipulation instructions	CLR1	reg8, CL	0 0 0 1 0 0 1 0	1 1 0 0 0 reg	3	5	5	reg8 bit NO.CL ← 0
		mem8, CL	0 0 1 0	mod 0 0 0 mem	3-5	11	11	(mem8) bit NO.CL ← 0
		reg16, CL	0 0 1 1	1 1 0 0 0 mem	3	5	5	reg16 bit NO.CL ← 0
		mem16, CL	0 0 1 1	mod 0 0 0 mem	3-5	19	11/19	(mem16) bit NO.CL ← 0
		reg8, imm3	1 0 1 0	1 1 0 0 0 reg	4	6	6	reg8 bit NO.imm3 ← 0
		mem8, imm3	1 0 1 0	mod 0 0 0 mem	4-6	12	12	(mem8) bit NO.imm3 ← 0
		reg16, imm4	1 0 1 1	1 1 0 0 0 reg	4	6	6	reg16 bit NO.imm4 ← 0
		mem16, imm4	1 0 1 1	mod 0 0 0 mem	4-6	20	12/20	(mem16) bit NO.imm4 ← 0
	SET1	reg8, CL	0 1 0 0	1 1 0 0 0 reg	3	4	4	reg8 bit NO.CL ← 1
		mem8, CL	0 1 0 0	mod 0 0 0 mem	3-5	10	10	(mem8) bit NO.CL ← 1
		reg16, CL	0 1 0 1	1 1 0 0 0 reg	3	4	4	reg16 bit NO.CL ← 1
		mem16, CL	0 1 0 1	mod 0 0 0 mem	3-5	18	10/18	(mem16) bit NO.CL ← 1
		reg8, imm3	1 1 0 0	1 1 0 0 0 reg	4	5	5	reg8 bit NO.imm3 ← 1
		mem8, imm3	1 1 0 0	mod 0 0 0 mem	4-6	11	11	(mem8) bit NO.imm3 ← 1
		reg16, imm4	1 1 0 1	1 1 0 0 0 reg	4	5	5	reg16 bit NO.imm4 ← 1
		mem16, imm4	1 1 0 1	mod 0 0 0 mem	4-6	19	11/19	(mem16) bit NO.imm4 ← 1

2nd byte* 3rd byte*

* 1st byte = 0FH

	CLR1	CY	1 1 1 1 1 0 0 0		1	2	2	CY ← 0
		DIR	1 1 1 1 1 1 0 0		1	2	2	DIR ← 0
	SET1	CY	1 1 1 1 1 0 0 1		1	2	2	CY ← 1
		DIR	1 1 1 1 1 1 0 1		1	2	2	DIR ← 1

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
Shift instructions	SHL	reg, 1	1 1 0 1 0 0 0 W	1 1 1 0 0 reg	2	6	6	CY ← reg MSB, reg ← reg × 2 If reg MSB ≠ CY: V ← 1 If reg MSB = CY: V ← 0

		mem, 1	1 1 0 1 0 0 0 W	mod 1 0 0 mem	2-4	13/21	13/21	CY ← (mem) MSB, (mem) ← (mem) × 2
								If (mem) MSB ≠ CY: V ← 1
								If (mem) MSB = CY: V ← 0

		reg, CL	1 1 0 1 0 0 1 W	1 1 1 0 0 reg	2	7 + n	7 + n	temp ← CL, while temp ≠0 the following operation are re CY ← reg MSB, reg ← reg × 2 temp ← temp – 1
		mem, CL	1 1 0 1 0 0 1 W	mod 1 0 0 mem	2-4	16/24 + n	16/24 + n	temp ← CL, while temp ≠0 the following operation are re CY ← (mem) MSB, (mem) ← (mem) × 2 temp ← temp – 1
		reg, imm8	1 1 0 0 0 0 0 W	1 1 1 0 0 reg	3	7 + n	7 + n	temp ← imm8, while temp ≠ 0 the following operati repeated: CY ← reg MSB, reg← reg × 2 temp ← temp – 1
		mem, imm8	1 1 0 0 0 0 0 W	mod 1 0 0 mem	3-5	16/24 + n	16/24 + n	temp ← imm8, while temp ≠ 0 the following operati repeated: CY ← (mem) MSB, (mem) ← (mem) × 2 temp ← temp – 1

n: Number of shifts

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
Shift instructions	SHR	reg, 1	1 1 0 1 0 0 0 W	1 1 1 0 1 reg	2	6	6	CY ← reg LSB, reg ← reg ÷ 2 If reg MSB ≠ bit after reg MSB : V ← 1 If reg MSB = bit after reg MSB : V ← 0

		mem, 1	1 1 0 1 0 0 0 W	mod 1 0 1 mem	2-4	13/21	13/21	CY ← (mem) LSB, (mem) ← (mem) ÷ 2
								If (mem) MSB ≠ bit after (mem) MSB : V ← 1
								If (mem) MSB = bit after (mem) MSB : V ← 0

		reg, CL	1 1 0 1 0 0 1 W	1 1 1 0 1 reg	2	7 + n	7 + n	temp ← CL, while temp ≠ 0 the following operat repeated: CY ← reg LSB, reg ← reg ÷ 2 temp ← temp – 1
		mem, CL	1 1 0 1 0 0 1 W	mod 1 0 1 mem	2-4	16/24 + n	16/24 + n	temp ← CL, while temp ≠ 0 the following operat repeated: CY ← (mem) LSB, (mem) ← (mem) ÷ 2 temp ← temp – 1
		reg, imm8	1 1 0 0 0 0 0 W	1 1 1 0 1 reg	3	7 + n	7 + n	temp ← imm8, while temp ≠ 0 the following operati repeated: CY ← reg LSB, reg ← reg ÷ 2 temp ← temp – 1
		mem, imm8	1 1 0 0 0 0 0 W	mod 1 0 1 mem	3-5	16/24 + n	16/24 + n	temp ← imm8, while temp ≠ 0 the following operati repeated: CY ← (mem) LSB,(mem) ← (mem) ÷ 2 temp ← temp – 1

n: Number of shifts

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
	SHRA	reg, 1	1 1 0 1 0 0 0 W	1 1 1 1 1 reg	2	6	6	CY ← reg LSB, reg ← reg ÷ 2, V ← 0 MSB of operand is unchanged.
		mem, 1	1 1 0 1 0 0 0 W	mod 1 1 1 mem	2-4	13/21	13/21	CY ← (mem) LSB,(mem) ← (mem) ÷ 2, V ← 0 MSB of operand is unchanged.
		reg, CL	1 1 0 1 0 0 1 W	1 1 1 1 1 reg	2	7 + n	7 + n	temp ← CL, while temp ≠ 0 the following operat repeated: CY ← reg LSB, reg ← reg ÷ 2 temp ← temp – 1, MSB of operand is unchanged.
		mem, CL	1 1 0 1 0 0 1 W	mod 1 1 1 mem	2-4	16/24 + n	16/24 + n	temp ← CL, while temp ≠ 0 the following operat repeated: CY ← (mem) LSB, (mem) ← (mem) ÷ 2 temp ← temp – 1, MSB of operand is unchanged.
		reg, imm8	1 1 0 0 0 0 0 W	1 1 1 1 1 reg	3	7 + n	7 + n	temp ← imm8, while temp ≠ 0 the following operati repeated: CY ← reg LSB, reg ← reg ÷ 2 temp ← temp – 1, MSB of operand is unchanged.
		mem, imm8	1 1 0 0 0 0 0 W	mod 1 1 1 mem	3-5	16/24 + n	16/24 + n	temp ← imm8, while temp ≠ 0 the following operati repeated: CY ← (mem) LSB,(mem) ← (mem) ÷ 2 temp ← temp – 1, MSB of operand is unchanged.

n: Number of shifts

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
Rotate instructions	ROL	reg, 1	1 1 0 1 0 0 0 W	1 1 0 0 0 reg	2	6	6	CY ← reg MSB, reg ← reg × 2 + CY reg MSB ≠ CY : V ← 1 reg MSB = CY : V ← 0
		mem, 1	1 1 0 1 0 0 0 W	mod 0 0 0 mem	2-4	13/21	13/21	CY ← (mem) MSB, (mem) ← (mem) × 2 + CY (mem) MSB ≠ CY : V ← 1 (mem) MSB = CY : V ← 0
		reg, CL	1 1 0 1 0 0 1 W	1 1 0 0 0 reg	2	7 + n	7 + n	temp ← CL, while temp ≠ 0 the following operati repeated: CY ← reg MSB, reg ← reg × 2 + CY temp ← temp – 1
		mem, CL	1 1 0 1 0 0 1 W	mod 0 0 0 mem	2-4	16/24 + n	16/24 + n	temp ← CL, while temp ≠ 0 the following operati repeated: CY ← (mem) MSB, (mem) ← (mem) × 2 + CY temp ← temp – 1
		reg, imm8	1 1 0 0 0 0 0 W	1 1 0 0 0 reg	3	7 + n	7 + n	temp ← imm8, while temp ≠ 0 the following operati repeated: CY ← reg MSB, reg ← reg × 2 + CY temp ← temp – 1
		mem, imm8	1 1 0 0 0 0 0 W	mod 0 0 0 mem	3-5	16/24 + n	16/24 + n	temp ← imm8, while temp ≠ 0 the following operati repeated: CY ← (mem) MSB, (mem) ← (mem) × 2 + CY temp ← temp – 1

n: Number of shifts

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
Rotate instructions	ROR	reg, 1	1 1 0 1 0 0 0 W	1 1 0 0 1 reg	2	6	6	CY ← reg LSB, reg← reg ÷ 2 reg MSB ← CY reg MSB ≠ bit after reg MSB : V ← 1 reg MSB = bit after reg MSB : V ← 0
		mem, 1	1 1 0 1 0 0 0 W	mod 0 0 1 mem	2-4	13/21	13/21	CY ← (mem) LSB, (mem) ← (mem) ÷ 2 (mem) MSB ← CY (mem) MSB ≠ bit after (mem) MSB : V ← 1 (mem) MSB = bit after (mem) MSB : V ← 0
		reg, CL	1 1 0 1 0 0 1 W	1 1 0 0 1 reg	2	7 + n	7 + n	temp ← CL, while CL ≠ 0 the following operations are r CY ← reg LSB, reg ← reg ÷ 2 reg MSB ← CY temp ← temp – 1
		mem, CL	1 1 0 1 0 0 1 W	mod 0 0 1 mem	2-4	16/24 + n	16/24 + n	temp ← CL, while CL ≠ 0 the following operations are r CY ← (mem) LSB,(mem) ← (mem) ÷ 2 (mem) MSB ← CY temp ← temp – 1
		reg, imm8	1 1 0 0 0 0 0 W	1 1 0 0 1 reg	3	7 + n	7 + n	temp ← imm8, while CL ≠ 0 the following operat repeated: CY ← reg LSB,reg ← reg ÷ 2 reg MSB ← CY temp ← temp – 1
		mem, imm8	1 1 0 0 0 0 0 W	mod 0 0 1 mem	3-5	16/24 + n	16/24 + n	temp ← imm8, while CL ≠ 0 the following operat repeated: CY ← (mem) LSB,(mem) ← (mem) ÷ 2 (mem) MSB ← CY temp ← temp – 1

n: Number of shifts

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
Rotate instructions	ROLC	reg, 1	1 1 0 1 0 0 0 W	1 1 0 1 0 reg	2	6	6	tmpcy ← CY, CY ← reg MSB reg ← reg × 2 + tmpcy reg MSB ≠ CY : V ← 1 reg MSB = CY : V ← 0
		mem, 1	1 1 0 1 0 0 0 W	mod 0 1 0 mem	2-4	13/21	13/21	tmpcy ← CY, CY ← (mem) MSB (mem)← (mem) × 2 + tmpcy (mem) MSB ≠ CY : V ← 1 (mem) MSB = CY : V ← 0
		reg, CL	1 1 0 1 0 0 1 W	1 1 0 1 0 reg	2	7 + n	7 + n	temp ← CL, while CL ≠ 0 the following operations peated: tmpcy← CY, CY ← reg MSB reg ← reg × 2 + tmpcy temp ← temp – 1
		mem, CL	1 1 0 1 0 0 1 W	mod 0 1 0 mem	2-4	16/24 + n	16/24 + n	temp ← CL, while CL ≠ 0 the following operations are re tmpcy ← CY, CY ← (mem) MSB (mem) ← (mem) × 2 + tmpcy temp ← temp – 1
		reg, imm8	1 1 0 0 0 0 0 W	1 1 0 1 0 reg	3	7 + n	7 + n	temp ← imm8, while CL ≠ 0 the following operati repeated: tmpcy ← CY, CY ← reg MSB reg ← reg × 2 + tmpcy temp ← temp – 1
		mem, imm8	1 1 0 0 0 0 0 W	mod 0 1 0 mem	3-5	16/24 + n	16/24 + n	temp ← imm8, while CL ≠ 0 the following operati repeated: tmpcy ← CY, CY ← (mem) MSB (mem) ← (mem) × 2 + tmpcy temp ← temp – 1

n: Number of shifts

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
Rotate instructions	RORC	reg, 1	1 1 0 1 0 0 0 W	1 1 0 1 1 reg	2	6	6	tmpcy ← CY, CY ← reg LSB reg ← reg ÷ 2 reg MSB ← tmpcy reg MSB ≠ bit after reg MSB : V ← 1 reg MSB = bit after reg MSB : V ← 0
		mem, 1	1 1 0 1 0 0 0 W	mod 0 1 1 mem	2-4	13/21	13/21	tmpcy ← CY, CY ← (mem) LSB (mem) ← (mem) ÷ 2 (mem) MSB ← tmpcy (mem) MSB ≠ bit after (mem) MSB : V ← 1 (mem) MSB = bit after (mem) MSB : V ← 0
		reg, CL	1 1 0 1 0 0 1 W	1 1 0 1 1 reg	2	7 + n	7 + n	temp ← CL, while CL ≠ 0 the following operations are re tmpcy ← CY, CY ← reg LSB reg ← reg ÷ 2 reg MSB ← tmpcy temp ← temp – 1
		mem, CL	1 1 0 1 0 0 1 W	mod 0 1 1 mem	2-4	16/24 + n	16/24 + n	temp ← CL, while CL ≠ 0 the following operations are re tmpcy ← CY, CY ← (mem) LSB (mem) ← (mem) ÷ 2 (mem) MSB ← tmpcy temp ← temp – 1
		reg, imm8	1 1 0 0 0 0 0 W	1 1 0 1 1 reg	3	7 + n	7 + n	temp ←imm8, while CL ≠ 0 the following operat repeated: tmpcy ← CY, CY ← reg LSB reg ← reg ÷ 2 reg MSB ← tmpcy temp ← temp – 1
		mem, imm8	1 1 0 0 0 0 0 W	mod 0 1 1 mem	3-5	16/24 + n	16/24 + n	temp ← imm8, while CL ≠ 0 the following operat repeated: tmpcy ← CY, CY ← (mem) LSB (mem) ← (mem) ÷ 2 (mem) MSB ← tmpcy temp ← temp – 1

n: Number of shifts

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
Subroutine control instructions	CALL	near-proc	1 1 1 0 1 0 0 0		3	20	16/20	SP ← SP – 2, (SP + 1, SP) ← PC PC ← PC + disp
		regptr16	1 1 1 1 1 1 1 1	1 1 0 1 0 reg	2	18	14/18	SP ← SP – 2, (SP + 1, SP) ← PC PC ← regptr16
		memptr16	1 1 1 1 1 1 1 1	mod 0 1 0 mem	2-4	31	23/31	TA ← (memptr16) SP ← SP – 2, (SP + 1, SP) ← PC, PC ← TA
		far-proc	1 0 0 1 1 0 1 0		5	29	21/29	SP ← SP – 2, (SP + 1, SP) ← PS, PS ← seg SP ← SP – 2, (SP + 1, SP) ← PC, PC ← offset
		memptr32	1 1 1 1 1 1 1 1	mod 0 1 1 mem	2-4	47	31/47	TA ← (memptr32),TB ← (memptr32 + 2) SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TB SP ← SP – 2, (SP + 1, SP) ← PC, PC ← TA
	RET		1 1 0 0 0 0 1 1		1	19	15/19	PC ← (SP + 1, SP) SP ← SP + 2
		pop-value	1 1 0 0 0 0 1 0		3	24	20/24	PC ← (SP + 1, SP) SP ← SP + 2, SP ← SP + pop-value
			1 1 0 0 1 0 1 1		1	29	21/29	PC ← (SP + 1, SP) PS ← (SP + 3, SP + 2) PS ← SP + 4
		pop-value	1 1 0 0 1 0 1 0		3	32	24/32	PC ← (SP + 1, SP) PS ← (SP + 3, SP + 2) SP ← SP + 4, SP ← SP + pop-value

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
Stack manipulation instructions	PUSH	mem16	1 1 1 1 1 1 1 1	mod 1 1 0 mem	2-4	23	15/23	SP ← SP – 2 (SP + 1, SP) ← (mem16)
		reg16	0 1 0 1 0 reg		1	10	6/10	SP ← SP – 2 (SP + 1, SP) ← reg16
		sreg	0 0 0 sreg 1 1 0		1	10	6/10	SP ← SP – 2 (SP + 1, SP) ← sreg
		PSW	1 0 0 1 1 1 0 0		1	10	6/10	SP ← SP – 2 (SP + 1, SP) ← PSW
		R	0 1 1 0 0 0 0 0		1	65	33/65	Push registers on the stack
		imm8	0 1 1 0 1 0 1 0		2	9	5/9	SP ← SP – 2 (SP + 1, SP) ← imm8, sign of extension
		imm16	0 1 1 0 1 0 0 0		3	10	6/10	SP ← SP – 2 (SP + 1, SP) ← imm16
	POP	mem16	1 0 0 0 1 1 1 1	mod 0 0 0 mem	2-4	24	16/24	(mem16) ← (SP + 1, SP) SP ← SP + 2
		reg16	0 1 0 1 1 reg		1	12	8/12	reg16← (SP + 1, SP) SP ← SP + 2
		sreg	0 0 0 sreg 1 1 1		1	12	8/12	sreg← (SP + 1, SP) SP ← SP + 2 sreg : SS, DS0, DS1
		PSW	1 0 0 1 1 1 0 1		1	12	8/12	PSW← (SP + 1, SP) SP ← SP + 2
		R	0 1 1 0 0 0 0 1		1	75	43/75	Pop registers from the stack
	PREPARE	imm16, imm8	1 1 0 0 1 0 0 0		4	**Note 1**	**Note 2**	Prepare New Stack Frame
	DISPOSE		1 1 0 0 1 0 0 1		1	10	6/10	Dispose of Stack Frame

Notes 1. If imm8 = 0 16

If imm8 ≥ 1 21 + 16 (imm8 – 1)

2. If imm8 = 0 12/16

If imm8 ≥ 1 {17 + 8 (imm8 – 1)} / {21 + 16 (imm8 – 1)}

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
Branch instructions	BR	near-label	1 1 1 0 1 0 0 1		3	13	13	PC ← PC+ dsip
		short-label	1 1 1 0 1 0 1 1		2	12	12	PC ← PC+ ext-disp8
		regptr16	1 1 1 1 1 1 1 1	1 1 1 0 0 reg	2	11	11	PC ← regptr16
		memptr16	1 1 1 1 1 1 1 1	mod 1 0 0 mem	2-4	23	19/23	PC ← (memptr16)
		far-label	1 1 1 0 1 0 1 0		5	15	15	PS ← seg PC ← offset
		memptr32	1 1 1 1 1 1 1 1	mod 1 0 1 mem	2-4	34	26/34	PS ← (memptr32 + 2) PC ← (memptr32)

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles[Note]		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
Conditional branch instructions	BV	short-label	0 1 1 1 0 0 0 0		2	14/4	14/4	if V = 1 PC ← PC + ext-disp8
	BNV	short-label	0 0 0 1		2	14/4	14/4	if V = 0 PC ← PC + ext-disp8
	BC BL	short-label	0 0 1 0		2	14/4	14/4	if CY = 1 PC ← PC + ext-disp8
	BNC BNL	short-label	0 0 1 1		2	14/4	14/4	if CY = 0 PC ← PC + ext-disp8
	BE BZ	short-label	0 1 0 0		2	14/4	14/4	if Z = 1 PC ← PC + ext-disp8
	BNE BNZ	short-label	0 1 0 1		2	14/4	14/4	if Z = 0 PC ← PC + ext-disp8
	BNH	short-label	0 1 1 0		2	14/4	14/4	if CY ∨ Z = 1 PC ← PC + ext-disp8
	BH	short-label	0 1 1 1		2	14/4	14/4	if CY ∨ Z = 0 PC ← PC + ext-disp8
	BN	short-label	1 0 0 0		2	14/4	14/4	if S = 1 PC ← PC + ext-disp8
	BP	short-label	1 0 0 1		2	14/4	14/4	if S = 0 PC ← PC + ext-disp8
	BPE	short-label	1 0 1 0		2	14/4	14/4	if P = 1 PC ← PC + ext-disp8
	BPO	short-label	1 0 1 1		2	14/4	14/4	if P = 0 PC ← PC + ext-disp8
	BLT	short-label	1 1 0 0		2	14/4	14/4	if S ⊻ V = 1 PC ← PC + ext-disp8
	BGE	short-label	1 1 0 1		2	14/4	14/4	if S ⊻ V = 0 PC ← PC + ext-disp8
	BLE	short-label	1 1 1 0		2	14/4	14/4	if (S ⊻ V) ∨ Z = 1 PC ← PC + ext-disp8
	BGT	short-label	1 1 1 1		2	14/4	14/4	if (S ⊻ V) ∨ Z = 0 PC ← PC + ext-disp8
	DBNZNE	short-label	1 1 1 0 0 0 0 0		2	14/5	14/5	CW = CW – 1 if Z = 0 and CW ≠ 0 PC ← PC + ext-disp8
	DBNZE	short-label	1 1 1 0 0 0 0 1		2	14/5	14/5	CW = CW – 1 if Z = 1 and CW ≠ 0 PC ← PC + ext-disp8
	DBNZ	short-label	1 1 1 0 0 0 1 0		2	13/5	13/5	CW = CW – 1 if CW ≠ 0 PC ← PC + ext-disp8
	BCWZ	short-label	1 1 1 0 0 0 1 1		2	13/5	13/5	if CW = 0 PC ← PC + ext-disp8

Note Condition determination: true/false

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
Interrupt instructions	BRK	3	1 1 0 0 1 1 0 0		1	50	38/50	TA ← (00DH, 00CH), TC ← (00FH, 00EH) SP ← SP – 2, (SP + 1, SP) ← PSW, IE ← 0, BRK SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP – 2, (SP + 1, SP) ← PC, PC ← TA
		imm8 (= 3)	1 1 0 0 1 1 0 1		2	50	38/50	TA ← (4 n + 1, 4n), TC ← (4n + 3, 4n + 2) n = imm SP ← SP – 2, (SP + 1, SP) ← PSW, IE ← 0, BRK SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP – 2, (SP + 1, SP) ← PC, PC ← TA
	BRKV		1 1 0 0 1 1 1 0		1	**Note 1**	**Note 2**	If V = 1 TA ← (011H, 010H), TC ← (013H, 012H) SP ← SP – 2, (SP + 1, SP) ← PSW, IE ← 0, BRK SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP – 2, (SP + 1, SP) ← PC, PC ← TA
	RETI		1 1 0 0 1 1 1 1		1	39	27/39	PC ← (SP + 1, SP), PS ← (SP + 3, SP + 2), PSW ← (SP + 5, SP + 4), SP ← SP + 6
	BRKEM	imm8	0 0 0 0 1 1 1 1	1 1 1 1 1 1 1 1	3	50	38/50	TA ← (4 n + 1, 4n), TC ← (4n + 3, 4n + 2) n = imm SP ← SP – 2, (SP + 1, SP) ← PSW, MD ← 0 MD is set to write enabled SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP – 2, (SP + 1, SP) ← PC, PC ← TA
	CHKIND	reg16, mem32	0 1 1 0 0 0 1 0	mod reg mem	2-4	**Note 3**	**Note 4**	If (mem32) > reg16 or (mem32 + 2) < reg16 TA ← (015H, 014H), TC ← (017H, 016H) SP ← SP – 2, (SP + 1, SP) ← PSW, IE ← 0, BRK SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP – 2, (SP + 1, SP) ← PC, PC ← TA

Notes 1. When V = 1: 52
When V = 0: 3

2. When V = 1: 40/52
When V = 0: 3

3. When interrupt condition is established : 72 to 75
When interrupt condition is not established : 25

4. When interrupt condition is established : (52 to 55)/(72 to 75)
When interrupt condition is not established : 17/25

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
CPU control instructions	HALT		1 1 1 1 0 1 0 0		1	2	2	CPU Halt
	POLL		1 0 0 1 1 0 1 1		1	2 + 5n	2 + 5n	Poll and wait n: Number of times $\overline{\text{POLL}}$ pin is sar
	DI		1 1 1 1 1 0 1 0		1	2	2	IE ← 0
	EI		1 1 1 1 1 0 1 1		1	2	2	IE ← 1
	BUSLOCK		1 1 1 1 0 0 0 0		1	2	2	Bus Lock Prefix
	FPO1	fp-op	1 1 0 1 1 X X X	1 1 Y Y Y Z Z Z	2	2	2	No Operation
		fp-op, mem	1 1 0 1 1 X X X	mod Y Y Y mem	2-4	14	10/14	data bus ← (mem)
	FPO2	fp-op	0 1 1 0 0 1 1 X	1 1 Y Y Y Z Z Z	2	2	2	No Operation
		fp-op, mem	0 1 1 0 0 1 1 X	mod Y Y Y mem	2-4	14	10/14	data bus ← (mem)
	NOP		1 0 0 1 0 0 0 0		1	3	3	No Operation

	*		0 0 1 sreg 1 1 0		1	2	2	Segment override prefix

* DS0:, DS1:, PS:, and SS:.

Instruction Group	Mnemonic	Operand(s)	Operation Code		Bytes	Clock Cycles		Operation
			7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		V40HL	V50HL	
8080	RETEM		1 1 1 0 1 1 0 1	1 1 1 1 1 1 0 1	2	39	27/39	PC ← (SP + 1, SP), PS ← (SP + 3, SP + 2), PSW ← (SP + 5, SP + 4), SP ← SP + 6, MD is se disabled
	CALLN	imm8	1 1 1 0 1 1 0 1	1 1 1 0 1 1 0 1	3	58	38/58	TA ← (4n + 1, 4n), TC ← (4n + 3, 4n + 2) n = in SP ← SP – 2, (SP + 1, SP) ← PSW, MD ← 1 SP ← SP – 2, (SP + 1, SP) ← PS, PS ← TC SP ← SP – 2, (SP + 1, SP) ← PC, PC ← TA

16. ELECTRICAL SPECIFICATIONS

Applied standard

The electrical characteristics shown below are applied to devices other than the old models conforming to K mask.

Therefore, these characteristics are different from those conforming to the K mask. For the electrical characteristics of the K mask, consult NEC.

"Others" in the table below means products conforming to the masks other than E, P, X, and M (but conforming to the L, F mask).

16.1 AT 5 V OPERATION

OPERATING RANGE

	E, P, X, M Mask Model	Others
μPD70208H, 70216H-10/12/16	V_{DD} = 5 V ±10%	
μPD70208H, 70216H-20	—	V_{DD} = 5 V ±5%

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Test Conditions	Rating	Unit
Supply voltage	V_{DD}		–0.5 to +7.0	V
Input voltage	V_I	V_{DD} = 5 V ±10% (μPD70208H, 70216H-10/12/16) V_{DD} = 5 V ±5% (μPD70208H, 70216H-20)	–0.5 to V_{DD} + 0.3	V
Clock input voltage	V_K		–0.5 to V_{DD} + 1.0	V
Output voltage	V_O		–0.5 to V_{DD} + 0.3	V
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Cautions 1. Do not directly connect the output pins of two or more IC products and do not directly connect the output pins to V_{DD} or V_{CC} and GND. However, open-drain pins or open-collector pins may be connected directly. Moreover, an external circuit whose timing is designed to avoid output collision can be connected to pins that go into a high-impedance state.

2. If even one of the above parameters exceeds the absolute maximum rating even momentarily, the quality of the program may be degraded. Absolute maximum ratings, therefore, are the values exceeding which the product may be physically damaged. Use the program keeping all the parameters within these rated values.

The standards and conditions shown in DC and AC Characteristics below specify the range within which the normal operation of the product is guaranteed.

DC CHARACTERISTICS

(T_A = –40 to +85 °C, V_{DD} = 5 V ±10% (μPD70208H, 70216H-10/12/16), V_{DD} = 5 V ±5% (μPD70208H, 70216H-20))

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH}	E, P, X, M masks	Except $\overline{RESET}$	2.2		V_{DD}+0.3	V
			$\overline{RESET}$	0.8 V_{DD}		V_{DD}+0.3	
		Others	Except $\overline{RESET}$, INTP1 to INTP7	2.2		V_{DD}+0.3	
			$\overline{RESET}$	0.8 V_{DD}		V_{DD}+0.3	
			INTP1 to INTP7	2.4		V_{DD}+0.3	
Input voltage low	V_{IL}	Except $\overline{RESET}$		–0.5		+0.8	V
		$\overline{RESET}$		–0.5		0.2V_{DD}	
Clock input voltage high	V_{KH}			3.9		V_{DD}+1.0	V
Clock input voltage low	V_{KL}			–0.5		+0.6	V
Output voltage high	V_{OH}	I_{OH} = –2.5 mA		0.7 V_{DD}			V
		I_{OH} = –100 μA		V_{DD} – 0.4			
Output voltage low	V_{OL}	Except $\overline{END}/\overline{TC}$: I_{OL} = 2.5 mA				0.4	V
		$\overline{END}/\overline{TC}$: I_{OL} = 5.0 mA					
Input leak current high	I_{LIH}	$V_I = V_{DD}$				10	μA
Input leak current low	I_{LIL}	Except INTP: V_I = 0 V				–10	μA
INTP input current low	I_{LIPL}	INTP input: V_I = 0 V				–300	μA
Output leak current high	I_{LOH}	$V_O = V_{DD}$				10	μA
Output leak current low	I_{LOL}	V_O = 0 V				–10	μA
Latch leak current high	I_{LLH}	V_I = 3.0 V		–50		–300	μA
Latch leak current low	I_{LLL}	V_I = 0.8 V		50		300	μA
Latch inversion current (L → H)	I_{ILH}					400	μA
Latch inversion current (H → L)	I_{ILL}					–400	μA
Supply current[Note]	I_{DD}	E, P, X, M masks	On operation		5.5 f_X	9.0 f_X	mA
			On standby (HALT)		1.5 f_X	2.5 f_X	
			On standby (STOP)			50	μA
		Others	On operation		4.5 f_X	6.0 f_X	mA
			On standby (HALT)		1.5 f_X	2.2 f_X	
			On standby (STOP)			50	μA

Note The unit of constant values (1.5, 2.2, 2.5, 4.5, 5.5, 6.0 and 9.0) is mA/MHz.

CAPACITANCE (T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz			10	pF
Input/output capacitance	C_{IO}	0 V other than test pin.			15	pF

AC CHARACTERISTICS

(1) μPD70208H, 70216H-10/12/16 (T_A = –40 to +85 °C, V_{DD} = 5 V ±10%) (1/3)

Output Pin Load Capacitance: C_L = 100 pF

Parameter		Symbol		μPD70208H-10 μPD70216H-10		μPD70208H-12 μPD70216H-12		μPD70208H-16 μPD70216H-16		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
External clock input cycle		<1>	t_{CYX}	50	DC	40	DC	31.25	DC	ns
External clock input high-level width (V_{KH}=3.0 V)		<2>	t_{XXH}	19		14		12		ns
External clock input low-level width (V_{KL}=1.5 V)		<3>	t_{XXL}	19		14		12		ns
External clock input rise time (1.5→3.0 V)		<4>	t_{XR}		5		5		5	ns
External clock input fall time (3.0→1.5 V)		<5>	t_{XF}		5		5		5	ns
Clock output cycle		<6>	t_{CYK}	100	DC	80	DC	62.5	DC	ns
Clock output high-level width (V_{OH}=3.0 V)		<7>	t_{KKH}	0.5t_{CYK}–5		0.5t_{CYK}–5		0.5t_{CYK}–5		ns
Clock output low-level width (V_{OL}=1.5 V)		<8>	t_{KKL}	0.5t_{CYK}–5		0.5t_{CYK}–5		0.5t_{CYK}–5		ns
Clock output rise time (1.5→3.0 V)		<9>	t_{KR}		5		5		5	ns
Clock output fall time (3.0→1.5 V)		<10>	t_{KF}		5		5		5	ns
CLKOUT delay time (vs. external clock)		<11>	t_{DXK}		40		35		20	ns
Input rise time (except external clock) (0.8→2.2 V)		<12>	t_{IR}		15		15		15	ns
Input fall time (except external clock) (2.2→0.8 V)		<13>	t_{IF}		10		10		10	ns
Output rise time (except CLKOUT) (0.8→2.2 V)	E, P, X, M masks	<14>	t_{OR}		15		15		15	ns
	Others				10		10		10	ns
Output fall time (except CLKOUT) (2.2→0.8 V)		<15>	t_{OF}		10		10		10	ns
$\overline{\text{RESET}}$ setup time (vs. CLKOUT↓)**Note 1**		<16>	t_{SRESK}	20		20		20		ns
$\overline{\text{RESET}}$ hold time (vs. CLKOUT↓)**Note 1**		<17>	t_{HKRES}	25		25		15		ns
RESOUT output delay time (vs. CLKOUT↓)		<18>	t_{DKRES}	5	50	5	40	5	30	ns
READY inactive setup time (vs. CLKOUT↑)		<19>	t_{SRYLK}	15		10		7		ns
READY inactive hold time (vs. CLKOUT↑)		<20>	t_{HKRYL}	20		15		15		ns
READY active setup time (vs. CLKOUT↑)		<21>	t_{SRYHK}	15		10		7		ns
READY active hold time (vs. CLKOUT↑)		<22>	t_{HKRYH}	20		20		15		ns
NMI setup time (vs. CLKOUT↑)		<23>	t_{SNMIK}	15		15		15		ns
POLL setup time (vs. CLKOUT↑)		<24>	t_{SPOLK}	20		20		20		ns
Data setup time (vs. CLKOUT↓)		<25>	t_{SDK}	15		10		7		ns
Data hold time (vs. CLKOUT↓)		<26>	t_{HKD}	5		5		5		ns
CLKOUT → address delay time**Note 2**		<27>	t_{DKA}	5	50	5	40	5	28	ns
★ CLKOUT → address hold time		<28>	t_{HKA}	5		5		5		ns
CLKOUT↓ → PS delay time		<29>	t_{DKP}	5	50	5	40	5	30	ns
CLKOUT↓ → PS float delay time		<30>	t_{FKP}	5	50	5	40	5	30	ns
Address setup time (vs. ASTB↓)		<31>	t_{SAST}	t_{KKL}–20		t_{KKL}–10		t_{KKL}–10		ns
CLKOUT↓ → address float delay time**Note 3**		<32>	t_{FKA}	t_{HKA}	50	t_{HKA}	40	t_{HKA}	30	ns
CLKOUT↓ → ASTB↑ delay time		<33>	t_{DKSTH}		40		30		25	ns

Notes 1. When reset with the minimum pulse width or when guaranteeing the RESOUT output timing.

2. Specifications also corresponding to the QS0, QS1, and $\overline{\text{BUSLOCK}}$ signals, and A16/PS0-A19/PS3, $\overline{\text{UBE}}$, $\overline{\text{BUFEN}}$, BUF$\overline{\text{R}}$/W, $\overline{\text{MRD}}$, $\overline{\text{IORD}}$, $\overline{\text{MWR}}$, $\overline{\text{IOWR}}$, and BS0-BS2 signals at HLDRQ/HLDAK timing.

3. Specifications also corresponding to the A16/PS0-A19/PS3, $\overline{\text{UBE}}$, $\overline{\text{BUFEN}}$, BUF$\overline{\text{R}}$/W, $\overline{\text{MRD}}$, $\overline{\text{IORD}}$, $\overline{\text{MWR}}$, $\overline{\text{IOWR}}$, and BS0-BS2 signals at HLDRQ/HLDAK timing.

(1) μPD70208H, 70216H-10/12/16 (T_A = –40 to +85 °C, V_{DD} = 5 V ±10%) (2/3)

Output Pin Load Capacitance: C_L = 100 pF

Parameter		Symbol		μPD70208H-10 μPD70216H-10		μPD70208H-12 μPD70216H-12		μPD70208H-16 μPD70216H-16		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
CLKOUT↑ → ASTB↓ delay time		<34>	t_{DKSTL}		45		35		30	ns
ASTB high-level width		<35>	t_{STST}	t_{KKL}–10		t_{KKL}–10		t_{KKL}–10		ns
ASTB↓ → address hold time		<36>	t_{HSTA}	t_{KKH}–20		t_{KKH}–10		t_{KKH}–10		ns
CLKOUT → control 1[Note 1] delay time		<37>	t_{DKCT1}	5	60	5	50	5	40	ns
CLKOUT → control 2[Note 2] delay time		<38>	t_{DKCT2}	5	55	5	45	5	35	ns
Address float → $\overline{RD}$↓ delay time		<39>	t_{DAFRL}	0		0		0		ns
CLKOUT↓ → $\overline{RD}$↓ delay time		<40>	t_{DKRL}	5	65	5	50	5	40	ns
CLKOUT↓ → $\overline{RD}$↑ delay time		<41>	t_{DKRH}	5	60	5	45	5	35	ns
$\overline{RD}$↑ → address delay time		<42>	t_{DRHA}	t_{CYK}–40		t_{CYK}–20		t_{CYK}–10		ns
$\overline{RD}$ low-level width		<43>	t_{RR}	2t_{CYK}–40		2t_{CYK}–20		2t_{CYK}–20		ns
$\overline{BUFEN}$↑ → BUF$\overline{R}$/W delay time (read cycle)		<44>	t_{DBECT}	t_{KKL}–20		t_{KKL}–10		t_{KKL}–10		ns
CLKOUT↓ → data output delay time		<45>	t_{DKD}	5	55	5	40	5	30	ns
CLKOUT↓ → data float delay time		<46>	t_{FKD}	5	55	5	40	5	30	ns
$\overline{WR}$ low-level width		<47>	t_{WW}	2t_{CYK}–40		2t_{CYK}–20		2t_{CYK}–20		ns
$\overline{WR}$↑ → $\overline{BUFEN}$↑ or BUF$\overline{R}$/W↓ (write cycle)		<48>	t_{DWCT}	t_{KKL}–20		t_{KKL}–10		t_{KKL}–10		ns
CLKOUT↑ → BS↓ delay time		<49>	t_{DKBL}	5	55	5	40	5	30	ns
CLKOUT↓ → BS↑ delay time		<50>	t_{DKBH}	5	55	5	40	5	30	ns
HLDRQ setup time (vs. CLKOUT↓)		<51>	t_{SHQK}	15		10		7		ns
CLKOUT↓ → HLDAK delay time		<52>	t_{DKHA}	5	60	5	50	5	40	ns
CLKOUT↑ → $\overline{DMAAK}$ delay time		<53>	t_{DKHDA}	5	55	5	45	5	35	ns
CLKOUT↓ → $\overline{DMAAK}$ delay time (cascade mode)		<54>	t_{DKLDA}	5	80	5	70	5	55	ns
$\overline{WR}$ low-level width (DMA cycle)	DMA extended write	<55>	t_{WW1}	2t_{CYK}–40		2t_{CYK}–20		2t_{CYK}–20		ns
	DMA normal write	<56>	t_{WW2}	t_{CYK}–40		t_{CYK}–20		t_{CYK}–15		ns
$\overline{RD}$↓, $\overline{WR}$↓ delay time (vs. $\overline{DMAAK}$↓)		<57>	t_{DDARW}	t_{KKH}–30		t_{KKH}–20		t_{KKH}–15		ns
$\overline{DMAAK}$↑ delay time (vs. $\overline{RD}$↑)		<58>	t_{DRHDAH}	t_{KKL}–30		t_{KKL}–20		t_{KKL}–15		ns
$\overline{RD}$↑ delay time (vs. $\overline{WR}$↑)		<59>	t_{DWHRH}	3		3		3		ns
$\overline{TC}$ output delay time (vs. CLKOUT↑)		<60>	t_{DKTCL}		55		45		35	ns
$\overline{TC}$ OFF delay time (vs. CLKOUT↑)		<61>	t_{DKTCF}		55		45		35	ns
$\overline{TC}$ low-level width		<62>	t_{TCTCL}	t_{CYK}–15		t_{CYK}–10		t_{CYK}–10		ns
$\overline{TC}$ pull-up delay time (vs. CLKOUT↑)		<63>	t_{DKTCH}		**Note 3**		**Note 4**		**Note 4**	ns
$\overline{END}$ setup time (vs. CLKOUT↑)		<64>	t_{SEDK}	30		25		20		ns
$\overline{END}$ low-level width		<65>	t_{EDEDL}	80		65		50		ns
DMARQ setup time (vs. CLKOUT↑)		<66>	t_{SDQK}	30		20		15		ns
INTPn low-level width		<67>	t_{IPIPL}	80		80		80		ns
RxD setup time (vs. SCU internal clock↓)		<68>	t_{SRX}	500		500		500		ns

Notes 1. $\overline{MWR}$ and $\overline{IOWR}$ signals in DMA cycle

2. $\overline{MWR}$ and $\overline{IOWR}$ signals in CPU cycles and $\overline{BUFEN}$, BUF$\overline{R}$/W, $\overline{INTAK}$ and $\overline{REFRQ}$ signals.

3. t_{KKH} + 2t_{CYK} – 10 (Reference value when a 1.1-kΩ pull-up resistor is connected.)

4. t_{KKH} + 2t_{CYK} – 5 (Reference value when a 1.1-kΩ pull-up resistor is connected.)

(1) μPD70208H, 70216H-10/12/16 (T_A = –40 to +85 °C, V_{DD} = 5 V ±10%) (3/3)

Output Pin Load Capacitance: C_L = 100 pF

Parameter	Symbol		μPD70208H-10 μPD70216H-10		μPD70208H-12 μPD70216H-12		μPD70208H-16 μPD70216H-16		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
RxD hold time (vs. SCU internal clock↓)	<69>	t_{HRX}	500		500		500		ns
CLKOUT↓ → $\overline{\text{SRDY}}$ delay time	<70>	t_{DKSR}		100		100		100	ns
TOUT1↓ → TxD delay time	<71>	t_{DTX}		200		200		200	ns
TCTL2 setup time (vs. CLKOUT↓)	<72>	t_{SGK}	40		40		40		ns
TCTL2 setup time (vs. TCLK↑)	<73>	t_{SGTK}	40		40		40		ns
TCTL2 hold time (vs. CLKOUT↓)	<74>	t_{HKG}	80		80		80		ns
TCTL2 hold time (vs. TCLK↑)	<75>	t_{HTKG}	40		40		40		ns
TCTL2 high-level width	<76>	t_{GGH}	40		40		40		ns
TCTL2 low-level width	<77>	t_{GGL}	40		40		40		ns
TOUT output delay time (vs. CLKOUT↓)	<78>	t_{DKTO}		150		150		150	ns
TOUT output delay time (vs. TCLK↓)	<79>	t_{DTKTO}		100		100		100	ns
TOUT output delay time (vs. TCTL2↓)	<80>	t_{DGTO}		90		90		90	ns
TCLK rise time	<81>	t_{TKR}		25		25		25	ns
TCLK fall time	<82>	t_{TKF}		25		25		25	ns
TCLK high-level width	<83>	t_{TKTKH}	45		40		30		ns
TCLK low-level width	<84>	t_{TKTKL}	45		40		30		ns
TCLK cycle	<85>	t_{CYTK}	100	DC	80	DC	62.5	DC	ns
Access interval[Note 1]	<86>	t_{AI}	$2t_{CYK}$–40		$2t_{CYK}$–25		$2t_{CYK}$–20		ns
$\overline{\text{REFRQ}}$↑ delay time (vs. $\overline{\text{MRD}}$↑)[Note 2]	<87>	t_{DRQHRH}	t_{KKL}–30		t_{KKL}–15		t_{KKL}–10		ns
$\overline{\text{RESET}}$ pulse width[Note 3]	<88>	t_{WRESL}	$4t_{CYK}$		$4t_{CYK}$		$4t_{CYK}$		ns

Notes 1. Specification to guarantee read/write recovery time for I/O device.

2. Specification to guarantee that $\overline{\text{REFRQ}}$↑ is always later than $\overline{\text{MRD}}$↑.
Only guaranteed when the EREF bit of the SCTL register is 0.

3. When using internal clock generator by connecting a resonator to the X1 and X2 pins, the oscillation stabilization time must be added at power-ON. Because the oscillation stabilization time varies depending on the characteristics of the resonator and oscillator used, evaluate the oscillation stabilization time with the resonator and oscillator actually used.

(2) μPD70208H, 70216H-20 (T_A = –40 to +85 °C, V_{DD} = 5 V ±5%) (1/3)

Output Pin Load Capacitance: C_L = 100 pF

Parameter		Symbol	μPD70208H-20 μPD70216H-20		Unit
			MIN.	MAX.	
External clock input cycle	<1>	t_{CYX}	25	DC	ns
External clock input high-level width (V_{KH}=3.0 V)	<2>	t_{XXH}	10		ns
External clock input low-level width (V_{KL}=1.5 V)	<3>	t_{XXL}	10		ns
External clock input rise time (1.5→3.0 V)	<4>	t_{XR}		5	ns
External clock input fall time (3.0→1.5 V)	<5>	t_{XF}		5	ns
Clock output cycle	<6>	t_{CYK}	50	DC	ns
Clock output high-level width (V_{OH}=3.0 V)	<7>	t_{KKH}	0.5t_{CYK}–5		ns
Clock output low-level width (V_{OL}=1.5 V)	<8>	t_{KKL}	0.5t_{CYK}–5		ns
Clock output rise time (1.5→3.0 V)	<9>	t_{KR}		5	ns
Clock output fall time (3.0→1.5 V)	<10>	t_{KF}		5	ns
CLKOUT delay time (vs. external clock)	<11>	t_{DXK}		20	ns
Input rise time (except external clock) (0.8→2.2 V)	<12>	t_{IR}		15	ns
Input fall time (except external clock) (2.2→0.8 V)	<13>	t_{IF}		10	ns
Output rise time (except CLKOUT) (0.8→2.2 V)	<14>	t_{OR}		10	ns
Output fall time (except CLKOUT) (2.2→0.8 V)	<15>	t_{OF}		10	ns
$\overline{\text{RESET}}$ setup time (vs. CLKOUT↓)**Note 1**	<16>	t_{SRESK}	20		ns
$\overline{\text{RESET}}$ hold time (vs. CLKOUT↓)**Note 1**	<17>	t_{HKRES}	10		ns
RESOUT output delay time (vs. CLKOUT↓)	<18>	t_{DKRES}	5	25	ns
READY inactive setup time (vs. CLKOUT↑)	<19>	t_{SRYLK}	7		ns
READY inactive hold time (vs. CLKOUT↑)	<20>	t_{HKRYL}	10		ns
READY active setup time (vs. CLKOUT↑)	<21>	t_{SRYHK}	7		ns
READY active hold time (vs. CLKOUT↑)	<22>	t_{HKRYH}	10		ns
NMI setup time (vs. CLKOUT↑)	<23>	t_{SNMIK}	10		ns
POLL setup time (vs. CLKOUT↑)	<24>	t_{SPOLK}	20		ns
Data setup time (vs. CLKOUT↓)	<25>	t_{SDK}	7		ns
Data hold time (vs. CLKOUT↓)	<26>	t_{HKD}	5		ns
CLKOUT → address delay time**Note 2**	<27>	t_{DKA}	5	25	ns
★ CLKOUT → address hold time	<28>	t_{HKA}	5		ns
CLKOUT ↓ → PS delay time	<29>	t_{DKP}	5	30	ns
CLKOUT ↓ → PS float delay time	<30>	t_{FKP}	5	30	ns
Address setup time (vs. ASTB↓)	<31>	t_{SAST}	t_{KKL}–10		ns
CLKOUT ↓ → address float delay time**Note 3**	<32>	t_{FKA}	t_{HKA}	25	ns
CLKOUT ↓ → ASTB ↑ delay time	<33>	t_{DKSTH}		20	ns
CLKOUT ↑ → ASTB ↓ delay time	<34>	t_{DKSTL}		20	ns
ASTB high-level width	<35>	t_{STST}	t_{KKL}–10		ns

Notes 1. When reset with the minimum pulse width or when guaranteeing the RESOUT output timing.

2. Specifications also corresponding to the QS0, QS1, and $\overline{\text{BUSLOCK}}$ signals, and A16/PS0-A19/PS3, $\overline{\text{UBE}}$, $\overline{\text{BUFEN}}$, BUF$\overline{\text{R}}$/W, $\overline{\text{MRD}}$, $\overline{\text{IORD}}$, $\overline{\text{MWR}}$, $\overline{\text{IOWR}}$, and BS0-BS2 signals at HLDRQ/HLDAK timing.

3. Specifications also corresponding to the A16/PS0-A19/PS3, $\overline{\text{UBE}}$, $\overline{\text{BUFEN}}$, BUF$\overline{\text{R}}$/W, $\overline{\text{MRD}}$, $\overline{\text{IORD}}$, $\overline{\text{MWR}}$, $\overline{\text{IOWR}}$, and BS0-BS2 signals at HLDRQ/HLDAK timing.

(2) μPD70208H, 70216H-20 (T_A = –40 to +85 °C, V_{DD} = 5 V ±5%) (2/3)

Output Pin Load Capacitance: C_L = 100 pF

Parameter		Symbol		μPD70208H-20 μPD70216H-20 MIN.	μPD70208H-20 μPD70216H-20 MAX.	Unit
ASTB ↓ → address hold time		<36>	t_{HSTA}	t_{KKH}–10		ns
CLKOUT → control 1[Note 1] delay time		<37>	t_{DKCT1}	5	25	ns
CLKOUT → control 2[Note 2] delay time		<38>	t_{DKCT2}	5	30	ns
Address float → $\overline{RD}$ ↓ delay time		<39>	t_{DAFRL}	0		ns
CLKOUT ↓ → $\overline{RD}$ ↓ delay time		<40>	t_{DKRL}	5	25	ns
CLKOUT ↓ → $\overline{RD}$ ↑ delay time		<41>	t_{DKRH}	5	28	ns
$\overline{RD}$ ↑ → address delay time		<42>	t_{DRHA}	t_{CYK}–5		ns
$\overline{RD}$ low-level width		<43>	t_{RR}	2t_{CYK}–15		ns
$\overline{BUFEN}$ ↑ → BUF$\overline{R}$/W delay time (read cycle)		<44>	t_{DBECT}	t_{KKL}–10		ns
CLKOUT ↓ → data output delay time		<45>	t_{DKD}	5	25	ns
CLKOUT ↓ → data float delay time		<46>	t_{FKD}	5	25	ns
$\overline{WR}$ low-level width		<47>	t_{WW}	2t_{CYK}–15		ns
$\overline{WR}$ ↑ → $\overline{BUFEN}$ ↑ or BUF$\overline{R}$/W ↓ (write cycle)		<48>	t_{DWCT}	t_{KKL}–10		ns
CLKOUT ↑ → BS ↓ delay time		<49>	t_{DKBL}	5	30	ns
CLKOUT ↓ → BS ↑ delay time		<50>	t_{DKBH}	5	25	ns
HLDRQ setup time (vs. CLKOUT ↓)		<51>	t_{SHQK}	7		ns
CLKOUT ↓ → HLDAK delay time		<52>	t_{DKHA}	5	25	ns
CLKOUT ↑ → $\overline{DMAAK}$ delay time		<53>	t_{DKHDA}	5	25	ns
CLKOUT ↓ → $\overline{DMAAK}$ delay time (cascade mode)		<54>	t_{DKLDA}	5	45	ns
$\overline{WR}$ low-level width (DMA cycle)	DMA extended write	<55>	t_{WW1}	2t_{CYK}–15		ns
	DMA normal write	<56>	t_{WW2}	t_{CYK}–15		ns
$\overline{RD}$ ↓, $\overline{WR}$ ↓ delay time (vs. $\overline{DMAAK}$ ↓)		<57>	t_{DDARW}	t_{KKH}–10		ns
$\overline{DMAAK}$ ↑ delay time (vs. $\overline{RD}$ ↑)		<58>	t_{DRHDAH}	t_{KKL}–10		ns
$\overline{RD}$ ↑ delay time (vs. $\overline{WR}$ ↑)		<59>	t_{DWHRH}	3		ns
$\overline{TC}$ output delay time (vs. CLKOUT ↑)		<60>	t_{DKTCL}		25	ns
$\overline{TC}$ OFF delay time (vs. CLKOUT ↑)		<61>	t_{DKTCF}		25	ns
$\overline{TC}$ low-level width		<62>	t_{TCTCL}	t_{CYK}–10		ns
$\overline{TC}$ pull-up delay time (vs. CLKOUT ↑)		<63>	t_{DKTCH}		**Note 3**	ns
$\overline{END}$ setup time (vs. CLKOUT ↑)		<64>	t_{SEDK}	20		ns
$\overline{END}$ low-level width		<65>	t_{EDEDL}	40		ns
DMARQ setup time (vs. CLKOUT ↑)		<66>	t_{SDQK}	10		ns
INTPn low-level width		<67>	t_{IPIPL}	60		ns
RxD setup time (vs. SCU internal clock ↓)		<68>	t_{SRX}	500		ns
RxD hold time (vs. SCU internal clock ↓)		<69>	t_{HRX}	500		ns
CLKOUT ↓ → $\overline{SRDY}$ delay time		<70>	t_{DKSR}		100	ns

Notes 1. $\overline{MWR}$ and $\overline{IOWR}$ signals in DMA cycle

2. $\overline{MWR}$ and $\overline{IOWR}$ signals in $\overline{BUFEN}$, BUF$\overline{R}$/W, $\overline{INTAK}$, $\overline{REFRQ}$, and CPU cycles

3. t_{KKH} + 2t_{CYK} – 5 (reference value when a 1.1-kΩ pull-up resistor is connected)

(2) μPD70208H, 70216H-20 (T_A = –40 to +85 °C, V_{DD} = 5 V ±5%) (3/3)

Output Pin Load Capacitance: C_L = 100 pF

Parameter	Symbol		μPD70208H-20 μPD70216H-20		Unit
			MIN.	MAX.	
TOUT1 ↓ → TxD delay time	<71>	t_{DTX}		200	ns
TCTL2 setup time (vs. CLKOUT ↓)	<72>	t_{SGK}	40		ns
TCTL2 setup time (vs. TCLK ↑)	<73>	t_{SGTK}	40		ns
TCTL2 hold time (vs. CLKOUT ↓)	<74>	t_{HKG}	80		ns
TCTL2 hold time (vs. TCLK ↑)	<75>	t_{HTKG}	40		ns
TCTL2 high-level width	<76>	t_{GGH}	40		ns
TCTL2 low-level width	<77>	t_{GGL}	40		ns
TOUT output delay time (vs. CLKOUT ↓)	<78>	t_{DKTO}		150	ns
TOUT output delay time (vs. TCLK ↓)	<79>	t_{DTKTO}		100	ns
TOUT output delay time (vs. TCTL2 ↓)	<80>	t_{DGTO}		90	ns
TCLK rise time	<81>	t_{TKR}		25	ns
TCLK fall time	<82>	t_{TKF}		25	ns
TCLK high-level width	<83>	t_{TKTKH}	23		ns
TCLK low-level width	<84>	t_{TKTKL}	23		ns
TCLK cycle	<85>	t_{CYTK}	50	DC	ns
Access interval[Note 1]	<86>	t_{AI}	$2t_{CYK}$–15		ns
$\overline{\text{REFRQ}}$ ↑ delay time (vs. $\overline{\text{MRD}}$ ↑)[Note 2]	<87>	t_{DRQHRH}	t_{KKL}–10		ns
$\overline{\text{RESET}}$ pulse width[Note 3]	<88>	t_{WRESL}	$4t_{CYK}$		ns

Notes 1. This rating is to guarantee the read/write recovery time for the I/O device.

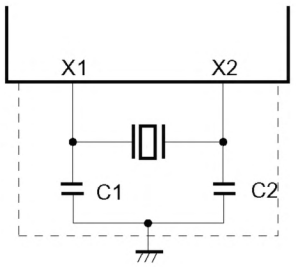
2. This rating is to guarantee that $\overline{\text{REFRQ}}$ ↑ is always behind $\overline{\text{MRD}}$ ↑, and guaranteed only when the EREF bit of the STCL register is 0.

3. When using internal clock generator by connecting a resonator to the X1 and X2 pins, the oscillation stabilization time must be added at power-ON. Because the oscillation stabilization time varies depending on the characteristics of the resonator and oscillator used, evaluate the oscillation stabilization time with the resonator and oscillator actually used.

RECOMMENDED OSCILLATOR

The clock input circuits (1) and (2) shown below are recommended.

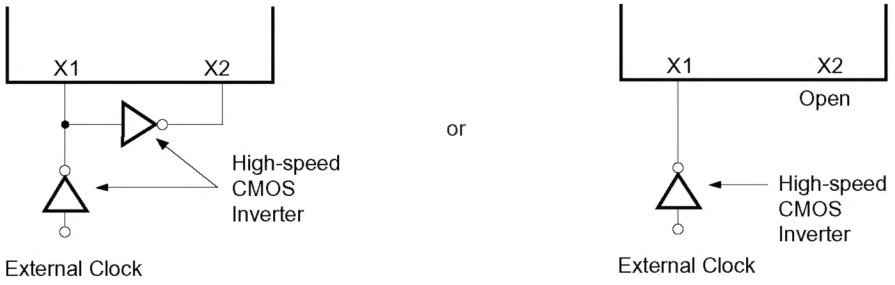
(1) Ceramic resonator connection (T_A = –40 to +85 °C, V_{DD} = 5 V ±10% (μPD70208H, 70216H-10/12/16), V_{DD} = 5 V ±5% (μPD70208H, 70216H-20))



Cautions
1. **The oscillator should be as close as possible to the X1 and X2 pins.**
2. **No other signal lines should pass through the area enclosed in dashed line.**
3. **For matching between V40HL, V50HL and resonator, the efficient evaluation should be carried out.**
4. **The values of the oscillator constants C1 and C2 depend on the characteristics of the resonator used. Evaluate them with the resonator actually used.**

Manufacturer	Frequency (f_{XX}) [MHz]	Product Name	Recommended Constant	
			C1 [pF]	C2 [pF]
Murata Mfg. Co., Ltd.	40	CSA40.00MXZ040	3	3
	32	CSA32.00MXZ040	5	5
	25	CSA25.00MXZ040	5	5
	20	CSA20.00MXZ040	10	10
TDK Corp.	32	FCR32.0M2G	5	5
	25	FCR25.0M2G	5	5
	20	FCR20.0M2G	10	10

(2) External clock input



Caution The high-speed CMOS inverter should be as close as possible to the X1 and X2 pins.

16.2 AT 3 V OPERATION

OPERATING RANGE

	E, P, X, M Masks	Others
μPD70208H, 70216H-10/12/16	V_{DD} = 3 V ±10%	
μPD70208H, 70216H-20	—	V_{DD} = 3 V ±10%

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Test Conditions	Rating	Unit
Supply voltage	V_{DD}		–0.5 to +7.0	V
Input voltage	V_I	V_{DD} = 3 V ±10%	–0.5 to V_{DD} + 0.3	V
Clock input voltage	V_K		–0.5 to V_{DD} + 1.0	V
Output voltage	V_O		–0.5 to V_{DD} + 0.3	V
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Cautions 1. Do not directly connect the output pins of two or more IC products and do not directly connect the output pins to V_{DD} or V_{CC} and GND. However, open-drain pins or open-collector pins may be connected directly. Moreover, an external circuit whose timing is designed to avoid output collision can be connected to pins that go into a high-impedance state.

2. If even one of the above parameters exceeds the absolute maximum rating even momentarily, the quality of the program may be degraded. Absolute maximum ratings, therefore, are the values exceeding which the product may be physically damaged. Use the program keeping all the parameters within these rated values.

The standards and conditions shown in DC and AC Characteristics below specify the range within which the normal operation of the product is guaranteed.

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 3 V ±10%)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH}	Except $\overline{RESET}$		0.7 V_{DD}		V_{DD}+0.3	V
		$\overline{RESET}$		0.8 V_{DD}		V_{DD}+0.3	
Input voltage low	V_{IL}	Except $\overline{RESET}$		–0.5		0.2 V_{DD}	V
		$\overline{RESET}$					
Clock input voltage high	V_{KH}			0.8 V_{DD}		V_{DD}+0.5	V
Clock input voltage low	V_{KL}			–0.5		0.2 V_{DD}	V
Output voltage high	V_{OH}	I_{OH} = –2.5 mA		0.7 V_{DD}			V
		I_{OH} = –100 μA		V_{DD} – 0.4			
Output voltage low	V_{OL}	Except $\overline{END}/\overline{TC}$: I_{OL} = 2.5 mA				0.4	V
		$\overline{END}/\overline{TC}$: I_{OL} = 5.0 mA					
Input leak current high	I_{LIH}	V_I = V_{DD}				10	μA
Input leak current low	I_{LIL}	V_I = 0 V : Except INTP				–10	μA
INTP input current low	I_{LIPL}	V_I = 0 V : INTP input				–300	μA
Output leak current high	I_{LOH}	V_O = V_{DD}				10	μA
Output leak current low	I_{LOL}	V_O = 0 V				–10	μA
Latch leak current high	I_{LLH}	V_I = 3.0 V		–50		–300	μA
Latch leak current low	I_{LLL}	V_I = 0.8 V		50		300	μA
Latch inversion current (L → H)	I_{ILH}					400	μA
Latch inversion current (H → L)	I_{ILL}					–400	μA
Supply current[Note]	I_{DD}	E, P, X, M masks	On Operation		3.0 f_X	5.5 f_X	mA
			On standby (HALT)		0.9 f_X	1.5 f_X	
			On standby (STOP)			30	μA
		Others	On Operation		2.5 f_X	4.0 f_X	mA
			On standby (HALT)		0.9 f_X	1.5 f_X	
			On standby (STOP)			30	μA

Note The unit of constant values (0.9, 1.5, 2.5, 3.0, 4.0 and 5.5) is mA/MHz.

CAPACITANCE (T_A = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz			10	pF
Input/output capacitance	C_{IO}	0 V other than test pin.			15	pF

AC CHARACTERISTICS

(1) μPD70208H, 70216H-10/12/16 (T_A = –40 to +85 °C, V_{DD} = 3 V ±10%) (1/3)

Output Pin Load Capacitance: C_L = 100 pF

	Parameter	Symbol		μPD70208H-10 μPD70216H-10		μPD70208H-12 μPD70216H-12		μPD70208H-16 μPD70216H-16		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
	External clock input cycle	<1>	t_{CYX}	100	DC	83	DC	62.5	DC	ns
	External clock input high-level width (V_{KH}=0.8 V_{DD})	<2>	t_{XXH}	40		30		20		ns
	External clock input low-level width (V_{KL}=0.2 V_{DD})	<3>	t_{XXL}	40		30		20		ns
	External clock input rise time (0.2 V_{DD}→0.8 V_{DD})	<4>	t_{XR}		10		10		10	ns
	External clock input fall time (0.8 V_{DD}→0.2 V_{DD})	<5>	t_{XF}		10		10		10	ns
	Clock output cycle	<6>	t_{CYK}	200	DC	166	DC	125	DC	ns
	Clock output high-level width (V_{OH}=0.7 V_{DD})	<7>	t_{KKH}	0.5t_{CYK}–7		0.5t_{CYK}–7		0.5t_{CYK}–7		ns
	Clock output low-level width (V_{OL}=0.2 V_{DD})	<8>	t_{KKL}	0.5t_{CYK}–7		0.5t_{CYK}–7		0.5t_{CYK}–7		ns
	Clock output rise time (0.2 V_{DD}→0.7 V_{DD})	<9>	t_{KR}		7		7		7	ns
	Clock output fall time (0.7 V_{DD}→0.2 V_{DD})	<10>	t_{KF}		7		7		7	ns
	CLKOUT delay time (vs. external clock)	<11>	t_{DXK}		75		65		55	ns
	Input rise time (except external clock) (0.2 V_{DD}→0.7 V_{DD})	<12>	t_{IR}		20		20		20	ns
	Input fall time (except external clock) (0.7 V_{DD}→0.2 V_{DD})	<13>	t_{IF}		12		12		12	ns
	Output rise time (except CLKOUT) (0.2 V_{DD}→0.7 V_{DD})	<14>	t_{OR}		20		20		20	ns
	Output fall time (except CLKOUT) (0.7 V_{DD}→0.2 V_{DD})	<15>	t_{OF}		12		12		12	ns
	$\overline{\text{RESET}}$ setup time (vs. CLKOUT↓)Note 1	<16>	t_{SRESK}	25		25		25		ns
	$\overline{\text{RESET}}$ hold time (vs. CLKOUT↓)Note 1	<17>	t_{HKRES}	35		35		35		ns
	RESOUT output delay time (vs. CLKOUT↓)	<18>	t_{DKRES}	5	80	5	70	5	60	ns
	READY inactive setup time (vs. CLKOUT↑)	<19>	t_{SRYLK}	20		20		15		ns
	READY inactive hold time (vs. CLKOUT↑)	<20>	t_{HKRYL}	30		30		25		ns
	READY active setup time (vs. CLKOUT↑)	<21>	t_{SRYHK}	20		20		15		ns
	READY active hold time (vs. CLKOUT↑)	<22>	t_{HKRYH}	30		30		25		ns
	NMI setup time (vs. CLKOUT↑)	<23>	t_{SNMIK}	15		15		15		ns
	POLL setup time (vs. CLKOUT↑)	<24>	t_{SPOLK}	20		20		20		ns
	Data setup time (vs. CLKOUT↓)	<25>	t_{SDK}	20		20		15		ns
	Data hold time (vs. CLKOUT↓)	<26>	t_{HKD}	5		5		5		ns
	CLKOUT → address delay timeNote 2	<27>	t_{DKA}	5	75	5	65	5	55	ns
★	CLKOUT → address hold time	<28>	t_{HKA}	5		5		5		ns
	CLKOUT↓ → PS delay time	<29>	t_{DKP}	5	80	5	70	5	60	ns
	CLKOUT↓ → PS float delay time	<30>	t_{FKP}	5	80	5	70	5	60	ns
	Address setup time (vs. ASTB↓)	<31>	t_{SAST}	t_{KKL}–30		t_{KKL}–30		t_{KKL}–30		ns
	CLKOUT↓ → address float delay timeNote 3	<32>	t_{FKA}	5	80	5	70	5	60	ns
	CLKOUT↓ → ASTB↑ delay time	<33>	t_{DKSTH}	5	65	5	55	5	45	ns
	CLKOUT↑ → ASTB↓ delay time	<34>	t_{DKSTL}	5	70	5	60	5	50	ns
	ASTB high-level width	<35>	t_{STST}	t_{KKL}–10		t_{KKL}–10		t_{KKL}–10		ns

Notes 1. When reset with the minimum pulse width or when guaranteeing the RESOUT output timing.

2. Specifications also corresponding to the QS0, QS1, and $\overline{\text{BUSLOCK}}$ signals, and A16/PS0-A19/PS3, $\overline{\text{UBE}}$, $\overline{\text{BUFEN}}$, BUF$\overline{\text{R}}$/W, $\overline{\text{MRD}}$, $\overline{\text{IORD}}$, $\overline{\text{MWR}}$, $\overline{\text{IOWR}}$, and BS0-BS2 signals at HLDRQ/HLDAK timing.

3. Specifications also corresponding to the A16/PS0-A19/PS3, $\overline{\text{UBE}}$, $\overline{\text{BUFEN}}$, BUF$\overline{\text{R}}$/W, $\overline{\text{MRD}}$, $\overline{\text{IORD}}$, $\overline{\text{MWR}}$, $\overline{\text{IOWR}}$, and BS0-BS2 signals at HLDRQ/HLDAK timing.

(1) μPD70208H, 70216H-10/12/16 (T_A = –40 to +85 °C, V_{DD} = 3 V ±10%) (2/3)

Output Pin Load Capacitance: C_L = 100 pF

Parameter		Symbol		μPD70208H-10 μPD70216H-10		μPD70208H-12 μPD70216H-12		μPD70208H-16 μPD70216H-16		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
ASTB↓ → address hold time		<36>	t_{HSTA}	t_{KKH}–30		t_{KKH}–30		t_{KKH}–20		ns
CLKOUT → control 1[Note 1] delay time		<37>	t_{DKCT1}	5	90	5	80	5	70	ns
CLKOUT → control 2[Note 2] delay time		<38>	t_{DKCT2}	5	80	5	70	5	60	ns
Address float → $\overline{RD}$↓ delay time		<39>	t_{DAFRL}	0		0		0		ns
CLKOUT↓ → $\overline{RD}$↓ delay time		<40>	t_{DKRL}	5	95	5	85	5	75	ns
CLKOUT↓ → $\overline{RD}$↑ delay time		<41>	t_{DKRH}	5	90	5	80	5	70	ns
$\overline{RD}$↑ → address delay time		<42>	t_{DRHA}	t_{CYK}–70		t_{CYK}–60		t_{CYK}–50		ns
$\overline{RD}$ low-level width		<43>	t_{RR}	2t_{CYK}–70		2t_{CYK}–60		2t_{CYK}–50		ns
$\overline{BUFEN}$↑ → BUF$\overline{R}$/W delay time (read cycle)		<44>	t_{DBECT}	t_{KKL}–30		t_{KKL}–30		t_{KKL}–20		ns
CLKOUT↓ → data output delay time		<45>	t_{DKD}	5	80	5	70	5	60	ns
CLKOUT↓ → data float delay time		<46>	t_{FKD}	5	80	5	70	5	60	ns
$\overline{WR}$ low-level width		<47>	t_{WW}	2t_{CYK}–50		2t_{CYK}–50		2t_{CYK}–40		ns
$\overline{WR}$↑ → $\overline{BUFEN}$↑ or BUF$\overline{R}$/W↓ (write cycle)		<48>	t_{DWCT}	t_{KKL}–30		t_{KKL}–30		t_{KKL}–20		ns
CLKOUT↑ → BS↓ delay time		<49>	t_{DKBL}	5	80	5	70	5	60	ns
CLKOUT↓ → BS↑ delay time		<50>	t_{DKBH}	5	80	5	70	5	60	ns
HLDRQ setup time (vs. CLKOUT↓)		<51>	t_{SHQK}	25		25		20		ns
CLKOUT↓ → HLDAK delay time		<52>	t_{DKHA}	5	90	5	80	5	70	ns
CLKOUT↑ → $\overline{DMAAK}$ delay time		<53>	t_{DKHDA}	5	80	5	70	5	60	ns
CLKOUT↓ → $\overline{DMAAK}$ delay time (cascade mode)		<54>	t_{DKLDA}	5	110	5	100	5	90	ns
$\overline{WR}$ low-level width (DMA cycle)	DMA extended write	<55>	t_{WW1}	2t_{CYK}–50		2t_{CYK}–50		2t_{CYK}–40		ns
	DMA normal write	<56>	t_{WW2}	t_{CYK}–50		t_{CYK}–50		t_{CYK}–40		ns
$\overline{RD}$↓ $\overline{WR}$↓ delay time (vs. $\overline{DMAAK}$↓)		<57>	t_{DDARW}	t_{KKH}–40		t_{KKH}–40		t_{KKH}–30		ns
$\overline{DMAAK}$↑ delay time (vs. $\overline{RD}$↑)		<58>	t_{DRHDAH}	t_{KKL}–40		t_{KKL}–40		t_{KKL}–30		ns
$\overline{RD}$↑ delay time (vs. $\overline{WR}$↑)		<59>	t_{DWHRH}	5		5		5		ns
$\overline{TC}$ output delay time (vs. CLKOUT↑)		<60>	t_{DKTCL}	5	80	5	70	5	60	ns
$\overline{TC}$ OFF delay time (vs. CLKOUT↑)		<61>	t_{DKTCF}	5	80	5	70	5	60	ns
$\overline{TC}$ low-level width		<62>	t_{TCTCL}	t_{CYK}–25		t_{CYK}–25		t_{CYK}–15		ns
$\overline{TC}$ pull-up delay time (vs. CLKOUT↑)		<63>	t_{DKTCH}		**Note 3**		**Note 4**		**Note 4**	ns
$\overline{END}$ setup time (vs. CLKOUT↑)		<64>	t_{SEDK}	45		40		35		ns
$\overline{END}$ low-level width		<65>	t_{EDEDL}	140		120		100		ns
DMARQ setup time (vs. CLKOUT↑)		<66>	t_{SDQK}	45		40		35		ns
INTPn low-level width		<67>	t_{IPIPL}	100		100		100		ns
RxD setup time (vs. SCU internal clock↓)		<68>	t_{SRX}	1000		1000		1000		ns
RxD hold time (vs. SCU internal clock↓)		<69>	t_{HRX}	1000		1000		1000		ns
CLKOUT↓ → $\overline{SRDY}$ delay time		<70>	t_{DKSR}		150		150		150	ns

Notes 1. $\overline{MWR}$ and $\overline{IOWR}$ signals in DMA cycle

2. $\overline{MWR}$ and $\overline{IOWR}$ signals in CPU cycles and $\overline{BUFEN}$, BUF$\overline{R}$/W, $\overline{INTAK}$ and $\overline{REFRQ}$ signals.

3. t_{KKH} + 2t_{CYK} – 20 (Reference value when a 1.1-kΩ pull-up resistor is connected)

4. t_{KKH} + 2t_{CYK} – 10 (Reference value when a 1.1-kΩ pull-up resistor is connected)

(1) μPD70208H, 70216H-10/12/16 (T_A = –40 to +85 °C, V_{DD} = 3 V ±10%) (3/3)

Output Pin Load Capacitance: C_L = 100 pF

Parameter	Symbol		μPD70208H-10 μPD70216H-10		μPD70208H-12 μPD70216H-12		μPD70208H-16 μPD70216H-16		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
TOUT1↓→ TxD delay time	<71>	t_{DTX}		500		500		500	ns
TCTL2 setup time (vs. CLKOUT↓)	<72>	t_{SGK}	50		50		50		ns
TCTL2 setup time (vs. TCLK↑)	<73>	t_{SGTK}	50		50		50		ns
TCTL2 hold time (vs. CLKOUT↓)	<74>	t_{HKG}	100		100		100		ns
TCTL2 hold time (vs. TCLK↑)	<75>	t_{HTKG}	50		50		50		ns
TCTL2 high-level width	<76>	t_{GGH}	50		50		50		ns
TCTL2 low-level width	<77>	t_{GGL}	50		50		50		ns
TOUT output delay time (vs. CLKOUT↓)	<78>	t_{DKTO}		200		200		200	ns
TOUT output delay time (vs. TCLK↓)	<79>	t_{DTKTO}		150		150		150	ns
TOUT output delay time (vs. TCTL2↓)	<80>	t_{DGTO}		120		120		120	ns
TCLK rise time	<81>	t_{TKR}		25		25		25	ns
TCLK fall time	<82>	t_{TKF}		25		25		25	ns
TCLK high-level width	<83>	t_{TKTKH}	60		55		50		ns
TCLK low-level width	<84>	t_{TKTKL}	60		55		50		ns
TCLK cycle	<85>	t_{CYTK}	200	DC	166	DC	125	DC	ns
Access interval[Note 1]	<86>	t_{AI}	$2t_{CYK}$–70		$2t_{CYK}$–60		$2t_{CYK}$–50		ns
$\overline{\text{REFRQ}}$↑ delay time (vs. $\overline{\text{MRD}}$↑)[Note 2]	<87>	t_{DRQHRH}	t_{KKL}–50		t_{KKL}–40		t_{KKL}–30		ns
$\overline{\text{RESET}}$ pulse width[Note 3]	<88>	t_{WRESL}	$4t_{CYK}$		$4t_{CYK}$		$4t_{CYK}$		ns

Notes 1. Specification to guarantee read/write recovery time for I/O device.

2. Specification to guarantee that $\overline{\text{REFRQ}}$↑ is always later than $\overline{\text{MRD}}$↑.
Only guaranteed when the EREF bit of the SCTL register is 0.

3. When using internal clock generator by connecting a resonator to the X1 and X2 pins, the oscillation stabilization time must be added at power-ON. Because the oscillation stabilization time varies depending on the characteristics of the resonator and oscillator used, evaluate the oscillation stabilization time with the resonator and oscillator actually used.

(2) μPD70208H, 70216H-20 (T_A = –40 to +85 °C, V_{DD} = 3 V ±10%) (1/3)

Output Pin Load Capacitance: C_L = 100 pF

	Parameter	Symbol		μPD70208H-20 μPD70216H-20		Unit
				MIN.	MAX.	
	External clock input cycle	<1>	t_{CYX}	50	DC	ns
	External clock input high-level width (V_{KH}=0.8 V_{DD})	<2>	t_{XXH}	19		ns
	External clock input low-level width (V_{KL}=0.2 V_{DD})	<3>	t_{XXL}	19		ns
	External clock input rise time (0.2 V_{DD}→0.8 V_{DD})	<4>	t_{XR}		5	ns
	External clock input fall time (0.8 V_{DD}→0.2 V_{DD})	<5>	t_{XF}		5	ns
	Clock output cycle	<6>	t_{CYK}	100	DC	ns
	Clock output high-level width (V_{OH}=0.7 V_{DD})	<7>	t_{KKH}	0.5t_{CYK}–7		ns
	Clock output low-level width (V_{OL}=0.2 V_{DD})	<8>	t_{KKL}	0.5t_{CYK}–7		ns
	Clock output rise time (0.2 V_{DD}→0.7 V_{DD})	<9>	t_{KR}		7	ns
	Clock output fall time (0.7 V_{DD}→0.2 V_{DD})	<10>	t_{KF}		7	ns
	CLKOUT delay time (vs. external clock)	<11>	t_{DXK}		45	ns
	Input rise time (except external clock) (0.2 V_{DD}→0.7 V_{DD})	<12>	t_{IR}		15	ns
	Input fall time (except external clock) (0.7 V_{DD}→0.2 V_{DD})	<13>	t_{IF}		10	ns
	Output rise time (except CLKOUT) (0.2 V_{DD}→0.7 V_{DD})	<14>	t_{OR}		15	ns
	Output fall time (except CLKOUT) (0.7 V_{DD}→0.2 V_{DD})	<15>	t_{OF}		10	ns
	$\overline{\text{RESET}}$ setup time (vs. CLKOUT↓)**Note 1**	<16>	t_{SRESK}	25		ns
	$\overline{\text{RESET}}$ hold time (vs. CLKOUT↓)**Note 1**	<17>	t_{HKRES}	25		ns
	RESOUT output delay time (vs. CLKOUT↓)	<18>	t_{DKRES}	5	50	ns
	READY inactive setup time (vs. CLKOUT↑)	<19>	t_{SRYLK}	15		ns
	READY inactive hold time (vs. CLKOUT↑)	<20>	t_{HKRYL}	20		ns
	READY active setup time (vs. CLKOUT↑)	<21>	t_{SRYHK}	15		ns
	READY active hold time (vs. CLKOUT↑)	<22>	t_{HKRYH}	20		ns
	NMI setup time (vs. CLKOUT↑)	<23>	t_{SNMIK}	15		ns
	POLL setup time (vs. CLKOUT↑)	<24>	t_{SPOLK}	20		ns
	Data setup time (vs. CLKOUT↓)	<25>	t_{SDK}	15		ns
	Data hold time (vs. CLKOUT↓)	<26>	t_{HKD}	5		ns
	CLKOUT → address delay time**Note 2**	<27>	t_{DKA}	5	50	ns
★	CLKOUT → address hold time	<28>	t_{HKA}	5		ns
	CLKOUT ↓ → PS delay time	<29>	t_{DKP}	5	50	ns
	CLKOUT ↓ → PS float delay time	<30>	t_{FKP}	5	50	ns
	Address setup time (vs. ASTB↓)	<31>	t_{SAST}	t_{KKL}–20		ns
	CLKOUT ↓ → address float delay time**Note 3**	<32>	t_{FKA}	t_{HKA}	50	ns
	CLKOUT ↓ → ASTB ↑ delay time	<33>	t_{DKSTH}		40	ns
	CLKOUT ↑ → ASTB ↓ delay time	<34>	t_{DKSTL}		45	ns
	ASTB high-level width	<35>	t_{STST}	t_{KKL}–10		ns

Notes 1. When reset with the minimum pulse width or when guaranteeing the RESOUT output timing.

2. Specifications also corresponding to the QS0, QS1, and $\overline{\text{BUSLOCK}}$ signals, and A16/PS0-A19/PS3, $\overline{\text{UBE}}$, $\overline{\text{BUFEN}}$, BUF$\overline{\text{R}}$/W, $\overline{\text{MRD}}$, $\overline{\text{IORD}}$, $\overline{\text{MWR}}$, $\overline{\text{IOWR}}$, and BS0-BS2 signals at HLDRQ/HLDAK timing.

3. Specifications also corresponding to the A16/PS0-A19/PS3, $\overline{\text{UBE}}$, $\overline{\text{BUFEN}}$, BUF$\overline{\text{R}}$/W, $\overline{\text{MRD}}$, $\overline{\text{IORD}}$, $\overline{\text{MWR}}$, $\overline{\text{IOWR}}$, and BS0-BS2 signals at HLDRQ/HLDAK timing.

(2) μPD70208H, 70216H-20 (T_A = –40 to +85 °C, V_{DD} = 3 V ±10%) (2/3)

Output Pin Load Capacitance: C_L = 100 pF

Parameter		Symbol		μPD70208H-20 μPD70216H-20		Unit
				MIN.	MAX.	
ASTB ↓ → address hold time		<36>	t_{HSTA}	t_{KKH}–20		ns
CLKOUT → control 1[Note 1] delay time		<37>	t_{DKCT1}	5	60	ns
CLKOUT → control 2[Note 2] delay time		<38>	t_{DKCT2}	5	55	ns
Address float → $\overline{RD}$ ↓ delay time		<39>	t_{DAFRL}	0		ns
CLKOUT ↓ → $\overline{RD}$ ↓ delay time		<40>	t_{DKRL}	5	65	ns
CLKOUT ↓ → $\overline{RD}$ ↑ delay time		<41>	t_{DKRH}	5	60	ns
$\overline{RD}$ ↑ → address delay time		<42>	t_{DRHA}	t_{CYK}–40		ns
$\overline{RD}$ low-level width		<43>	t_{RR}	2t_{CYK}–40		ns
$\overline{BUFEN}$ ↑ → BUF$\overline{R}$/W delay time (read cycle)		<44>	t_{DBECT}	t_{KKL}–20		ns
CLKOUT ↓ → data output delay time		<45>	t_{DKD}	5	55	ns
CLK$\overline{OUT}$ ↓ → data float delay time		<46>	t_{FKD}	5	55	ns
$\overline{WR}$ low-level width		<47>	t_{WW}	2t_{CYK}–40		ns
$\overline{WR}$ ↑ → $\overline{BUFEN}$ ↑ or BUF$\overline{R}$/W ↓ (write cycle)		<48>	t_{DWCT}	t_{KKL}–20		ns
CLKOUT ↑ → BS ↓ delay time		<49>	t_{DKBL}	5	55	ns
CLKOUT ↓ → BS ↑ delay time		<50>	t_{DKBH}	5	55	ns
HLDRQ setup time (vs. CLKOUT ↓)		<51>	t_{SHQK}	15		ns
CLKOUT ↓ → HLDAK delay time		<52>	t_{DKHA}	5	60	ns
CLKOUT ↑ → $\overline{DMAAK}$ delay time		<53>	t_{DKHDA}	5	55	ns
CLKOUT ↓ → $\overline{DMAAK}$ delay time (cascade mode)		<54>	t_{DKLDA}	5	80	ns
$\overline{WR}$ low-level width (DMA cycle)	DMA extended write	<55>	t_{WW1}	2t_{CYK}–40		ns
	DMA normal write	<56>	t_{WW2}	t_{CYK}–40		ns
$\overline{RD}$ ↓, $\overline{WR}$ ↓ delay time (vs. $\overline{DMAAK}$ ↓)		<57>	t_{DDARW}	t_{KKH}–30		ns
$\overline{DMAAK}$ ↑ delay time (vs. $\overline{RD}$ ↑)		<58>	t_{DRHDAH}	t_{KKL}–30		ns
$\overline{RD}$ ↑ delay time (vs. $\overline{WR}$ ↑)		<59>	t_{DWHRH}	3		ns
$\overline{TC}$ output delay time (vs. CLKOUT ↑)		<60>	t_{DKTCL}		55	ns
$\overline{TC}$ OFF delay time (vs. CLKOUT ↑)		<61>	t_{DKTCF}		55	ns
$\overline{TC}$ low-level width		<62>	t_{TCTCL}	t_{CYK}–15		ns
$\overline{TC}$ pull-up delay time (vs. CLKOUT ↑)		<63>	t_{DKTCH}		**Note 3**	ns
$\overline{END}$ setup time (vs. CLKOUT ↑)		<64>	t_{SEDK}	30		ns
END low-level width		<65>	t_{EDEDL}	80		ns
DMARQ setup time (vs. CLKOUT ↑)		<66>	t_{SDQK}	30		ns
INTPn low-level width		<67>	t_{IPIPL}	80		ns
RxD setup time (vs. SCU internal clock ↓)		<68>	t_{SRX}	500		ns
RxD hold time (vs. SCU internal clock ↓)		<69>	t_{HRX}	500		ns
CLKOUT ↓ → $\overline{SRDY}$ delay time		<70>	t_{DKSR}		100	ns

Notes 1. $\overline{MWR}$ and $\overline{IOWR}$ signals in DMA cycle

2. $\overline{MWR}$ and $\overline{IOWR}$ signals in CPU cycles and $\overline{BUFEN}$, BUF$\overline{R}$/W, $\overline{INTAK}$ and $\overline{REFRQ}$ signals.

3. t_{KKH} + 2t_{CYK} – 10 (reference value when a 1.1-kΩ pull-up resistor is connected)

(2) μPD70208H, 70216H-20 (T_A = –40 to +85 °C, V_{DD} = 3 V ±10%) (3/3)

Output Pin Load Capacitance: C_L = 100 pF

Parameter	Symbol		μPD70208H-20 μPD70216H-20		Unit
			MIN.	MAX.	
TOUT1 ↓ → TxD delay time	<71>	t_{DTX}		200	ns
TCTL2 setup time (vs. CLKOUT ↓)	<72>	t_{SGK}	40		ns
TCTL2 setup time (vs. TCLK ↑)	<73>	t_{SGTK}	40		ns
TCTL2 hold time (vs. CLKOUT ↓)	<74>	t_{HKG}	80		ns
TCTL2 hold time (vs. TCLK ↑)	<75>	t_{HTKG}	40		ns
TCTL2 high-level width	<76>	t_{GGH}	40		ns
TCTL2 low-level width	<77>	t_{GGL}	40		ns
TOUT output delay time (vs. CLKOUT ↓)	<78>	t_{DKTO}		150	ns
TOUT output delay time (vs. TCLK ↓)	<79>	t_{DTKTO}		100	ns
TOUT output delay time (vs. TCTL2 ↓)	<80>	t_{DGTO}		90	ns
TCLK rise time	<81>	t_{TKR}		25	ns
TCLK fall time	<82>	t_{TKF}		25	ns
TCLK high-level width	<83>	t_{TKTKH}	45		ns
TCLK low-level width	<84>	t_{TKTKL}	45		ns
TCLK cycle	<85>	t_{CYTK}	100	DC	ns
Access interval[Note 1]	<86>	t_{AI}	$2t_{CYK}$–40		ns
$\overline{\text{REFRQ}}$ ↑ delay time (vs. $\overline{\text{MRD}}$ ↑)[Note 2]	<87>	t_{DRQHRH}	t_{KKL}–30		ns
$\overline{\text{RESET}}$ pulse width[Note 3]	<88>	t_{WRESL}	$4t_{CYK}$		ns

Notes 1. This rating is to guarantee the read/write recovery time for the I/O device.

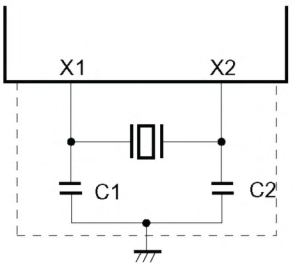
2. This rating is to guarantee that $\overline{\text{REFRQ}}$ ↑ is always behind $\overline{\text{MRD}}$ ↑, and is guaranteed only when the EREF bit of the STCL register is 0.

3. When using internal clock generator by connecting a resonator to the X1 and X2 pins, the oscillation stabilization time must be added at power-ON. Because the oscillation stabilization time varies depending on the characteristics of the resonator and oscillator used, evaluate the oscillation stabilization time with the resonator and oscillator actually used.

RECOMMENDED OSCILLATOR

The clock input circuits (1) and (2) shown below are recommended.

(1) Ceramic resonator connection (T_A = –40 to +85 °C, V_{DD} = 3 V ±10%[Note])

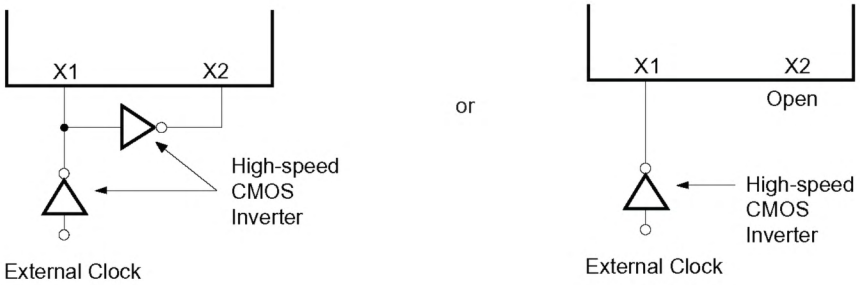


Cautions
1. **The oscillator should be as close as possible to the X1 and X2 pins.**
2. **No other signal lines should pass through the area enclosed in dashed line.**
3. **V40HL, V50HL and resonator matching requires careful evaluation.**
4. **The values of the oscillator constants C1 and C2 depend on the characteristics of the resonator used. Evaluate them with the resonator actually used.**

Manufacturer	Frequency (fxx) [MHz]	Product Name	Recommended Constant	
			C1 [pF]	C2 [pF]
Murata Mfg. Co., Ltd.	20	CSA20.00MXZ040[Note]	10	10
	16	CSA16.00MXZ040	15	15
		CSA16.00MXW0C3	–	–
	12.5	CSA12.5MTZ	30	30
		CSA12.5MTW	–	–
	10	CSA10.0MTZ	30	30
		CST10.0MXW	–	–
TDK Corp.	20	FCR20.0M2G	10	10
	16	FCR16.0M2G	15	15
	10	FCR10.0MC	–	–

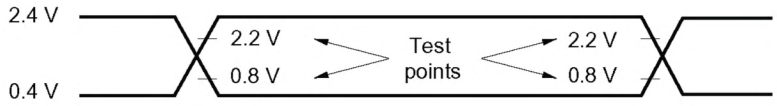
Note Use the CAS20.00MXZ040 within the range of V_{DD} = 2.9 to 3.3 V.

(2) External clock input

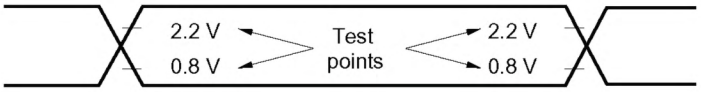


Caution The high-speed CMOS inverter should be as close as possible to the X1 and X2 pins.

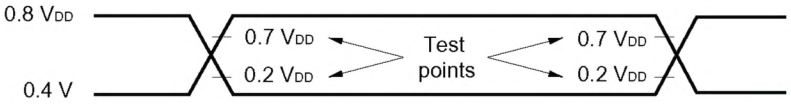
AC Test Input Waveform (Except X1 and X2) (at 5 V operation)



AC Test Output Test Points (at 5 V operation)

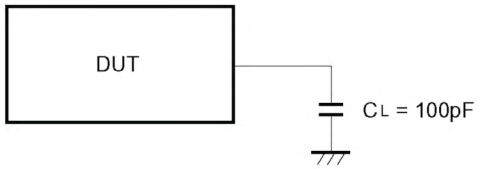


AC Test Input Waveform (Except X1 and X2) (at 3 V operation)



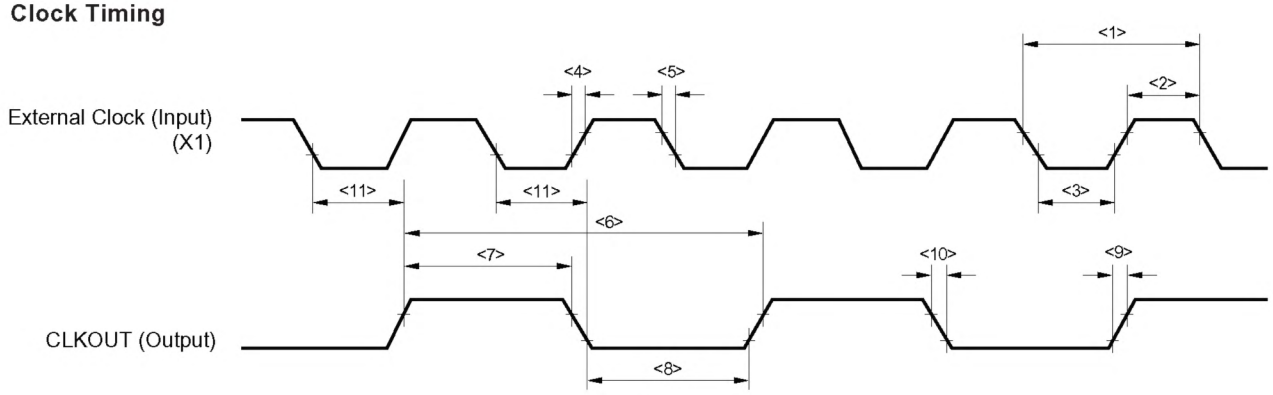
AC Test Output Waveform (at 3 V operation)

Load Conditions

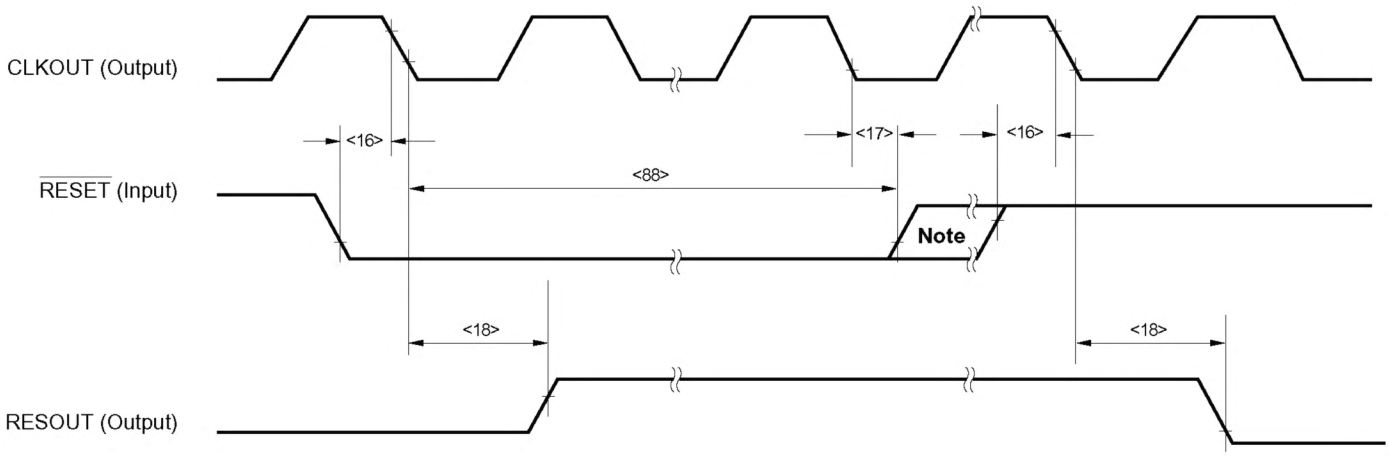


Caution If the load capacitance exceeds 100 pF due to the configuration of the circuit, the load capacitance of this device should be reduced to 100 pF or less by insertion of a buffer, etc.

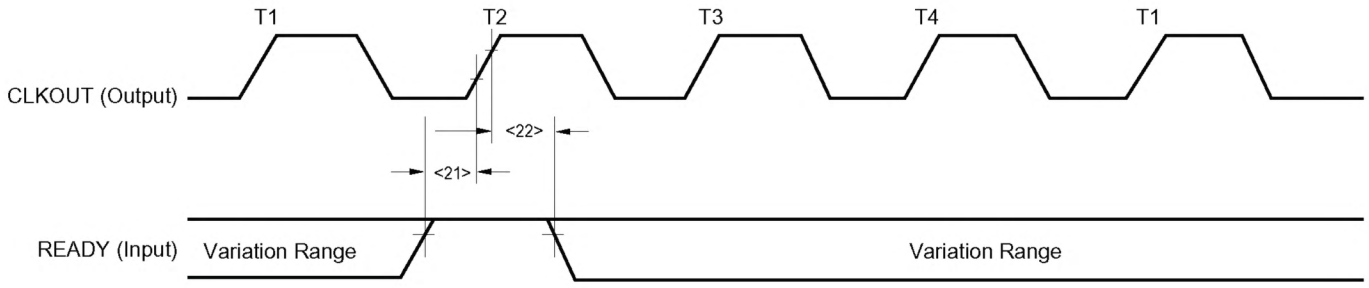
Clock Timing



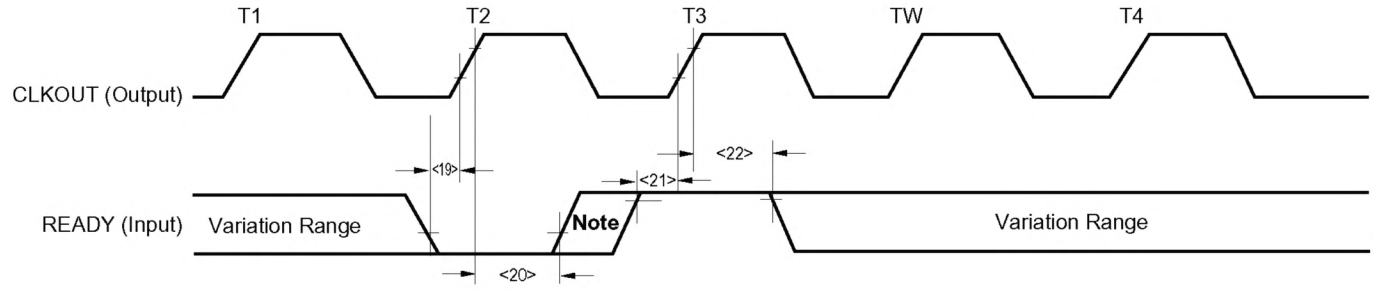
Reset Timing



Ready Timing (1)

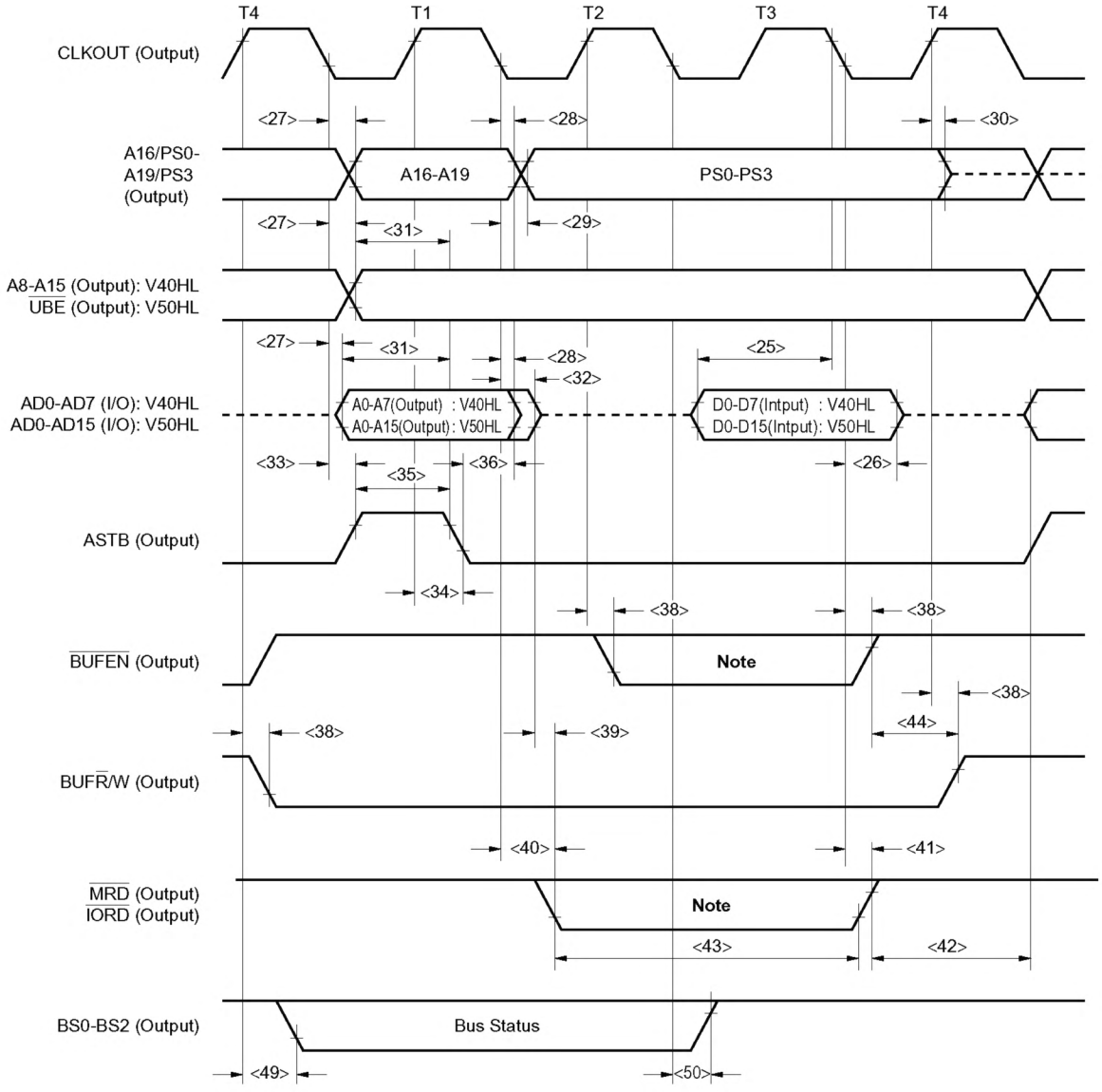


Ready Timing (2)



Note Variation range

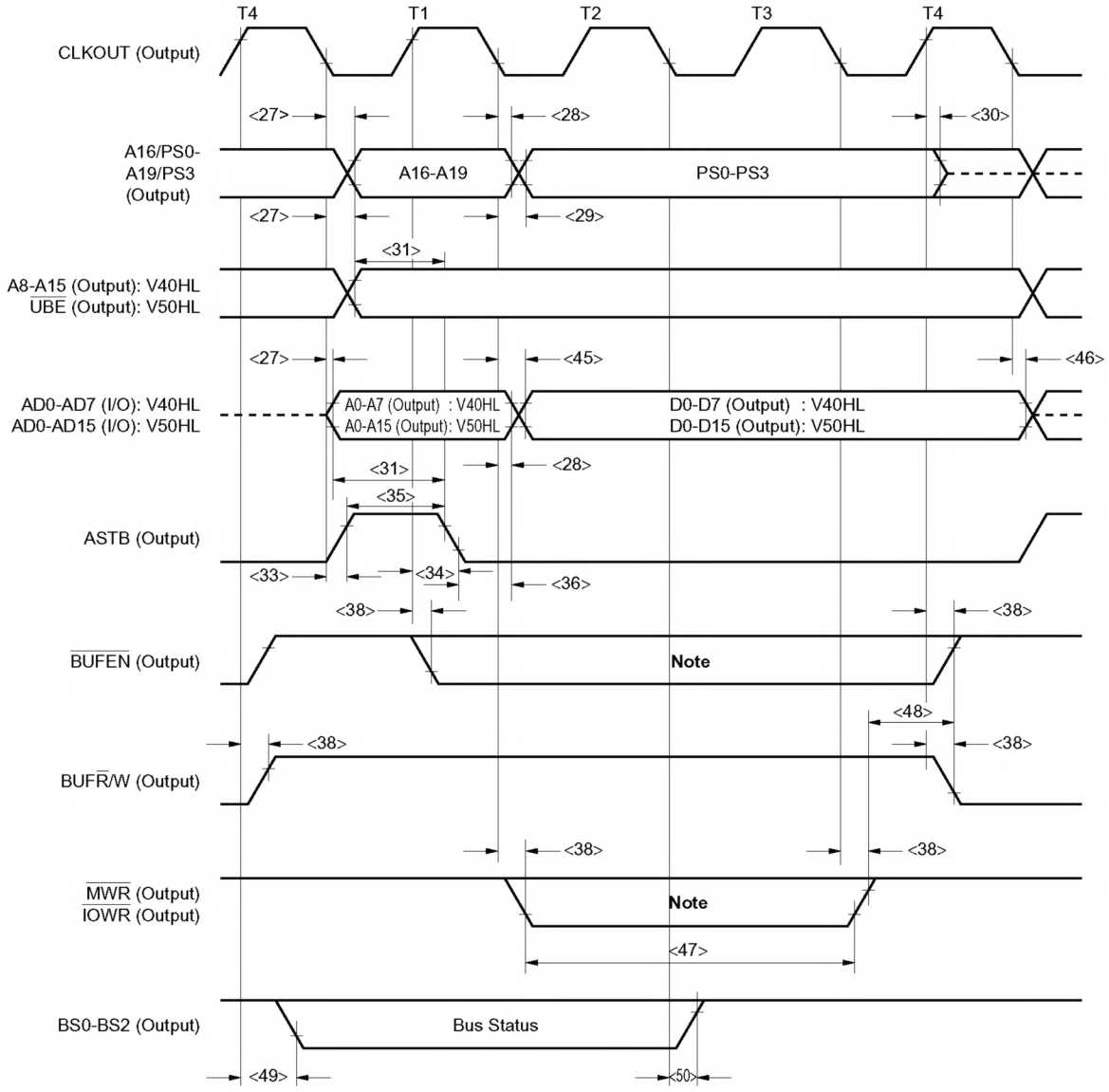
Read Timing



Note High-level signal is output in case of internal access.

Remark A dashed line indicates high impedance.

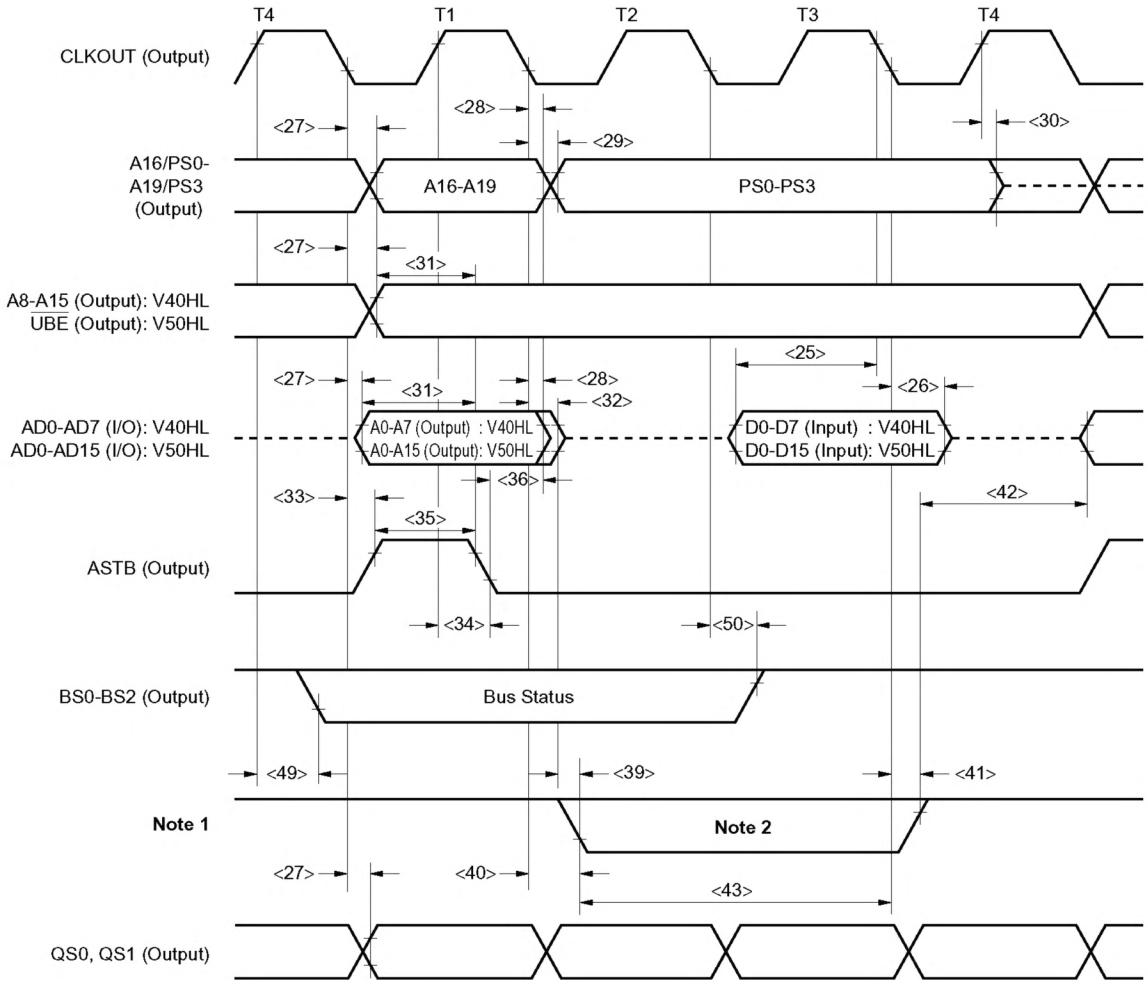
Write Timing



Note High-level signal is output in case of internal access.

Remark A dashed line indicates high impedance.

Status Timing

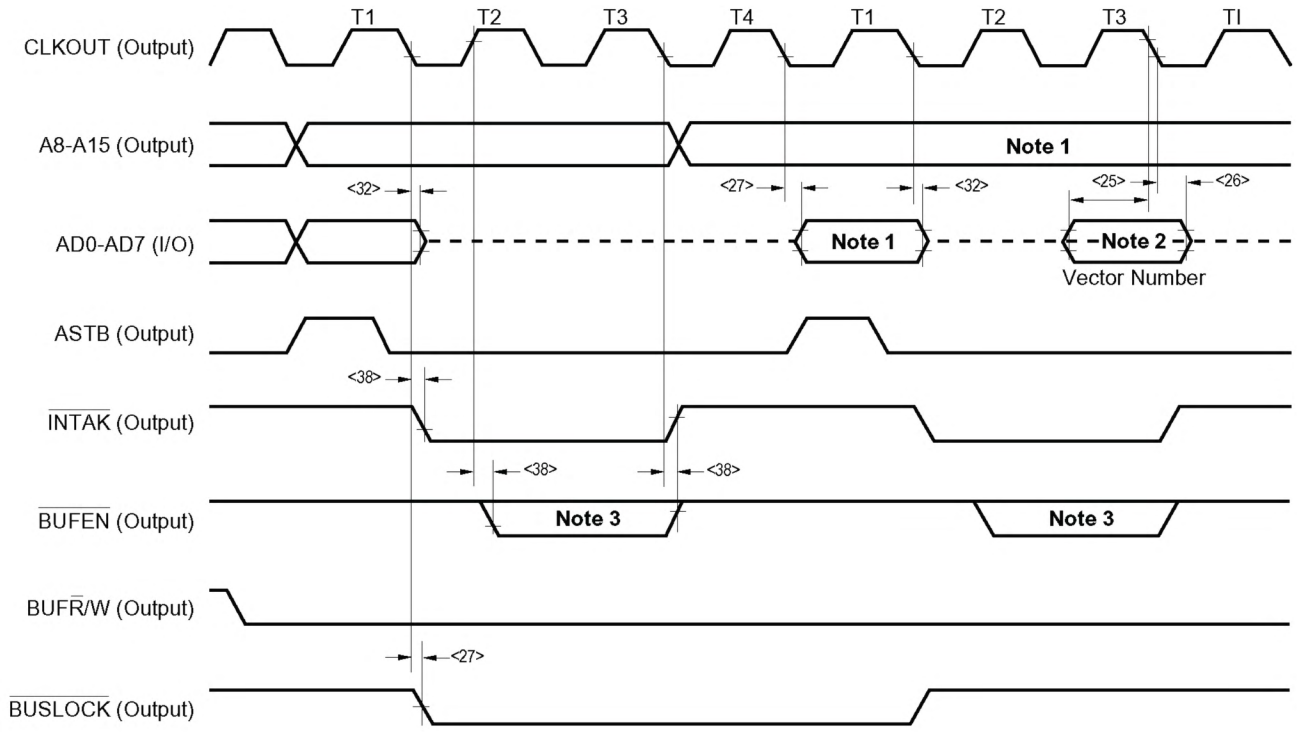


Notes 1. $\overline{\text{MRD}}$, $\overline{\text{IORD}}$, $\overline{\text{MWR}}$, $\overline{\text{IOWR}}$ (all output)

2. High-level signal is output in case of internal access.

Remark A dashed line indicates high impedance.

Interrupt Acknowledge Timing (V40HL)



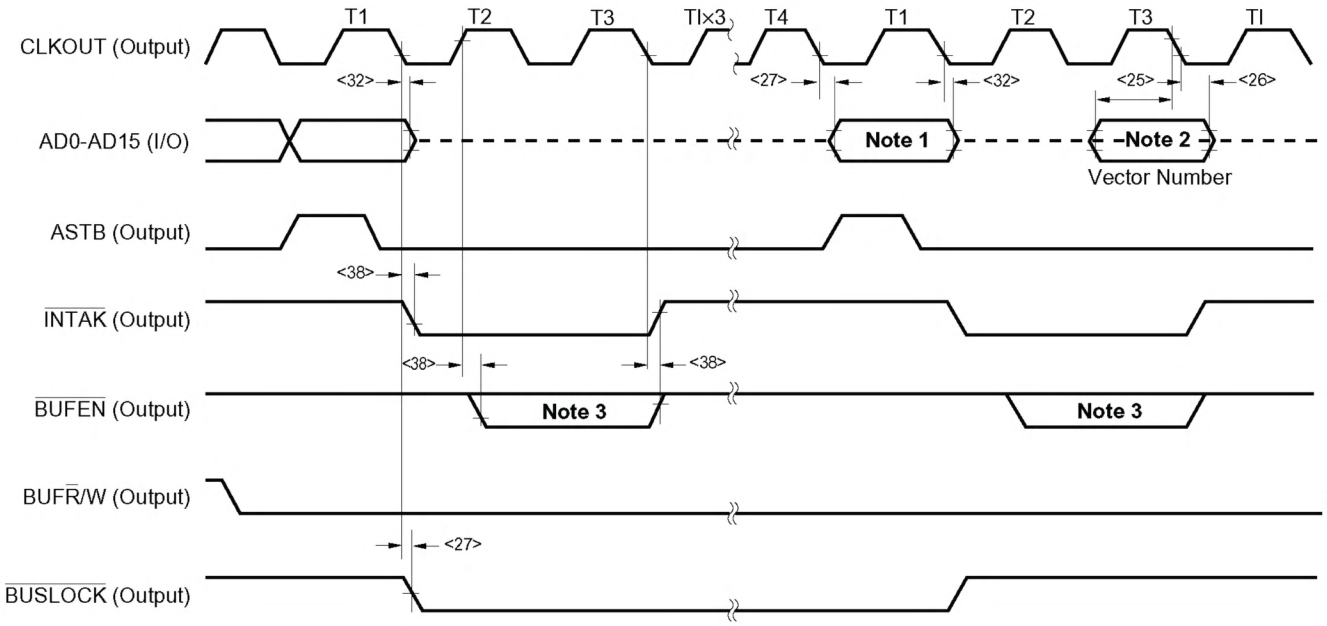
Notes 1. Slave address in case of interrupt from external μPD71059.
Invalid data in case of interrupt from internal ICU.

2. Data read as vector address in case of interrupt from external μPD71059.
High impedance in case of interrupt from internal ICU.

3. Low-level output in case of interrupt from external μPD71059.
High-level output in case of interrupt from internal ICU.

Remark A dashed line indicates high impedance.

Interrupt Acknowledge Timing (V50HL)



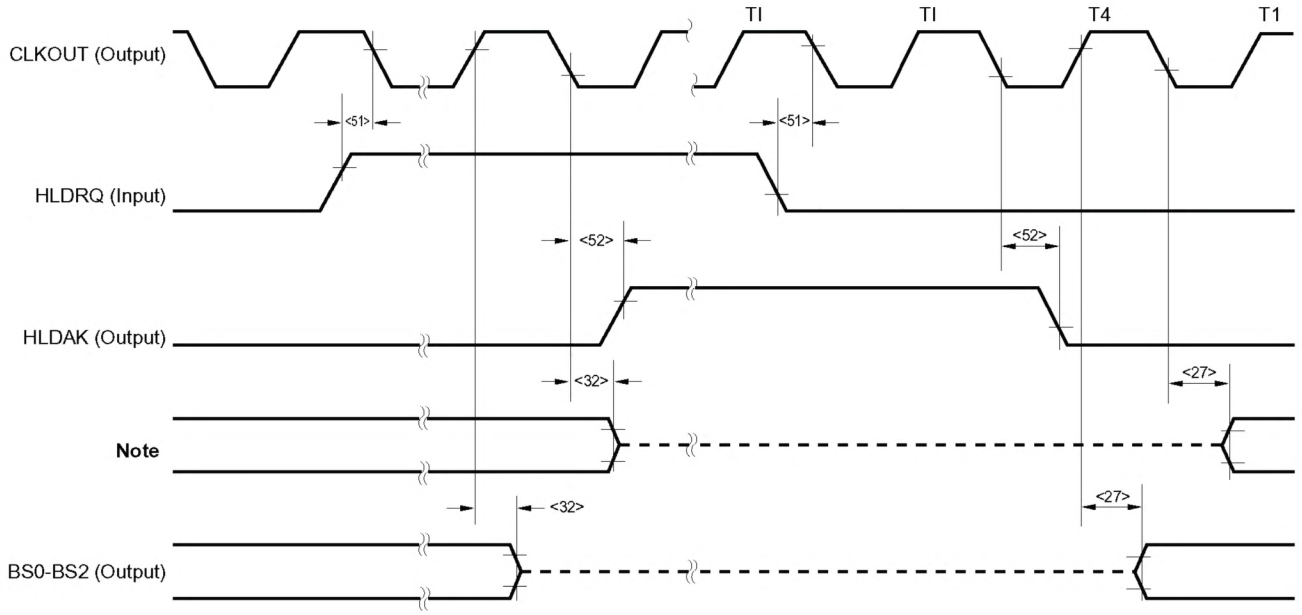
Notes 1. Slave address in case of interrupt from external μPD71059.
Invalid data in case of interrupt from internal ICU.

2. Data read as vector address in case of interrupt from external μPD71059.
High impedance in case of interrupt from internal ICU.

3. Low-level output in case of interrupt from external μPD71059.
High-level output in case of interrupt from internal ICU.

Remark A dashed line indicates high impedance.

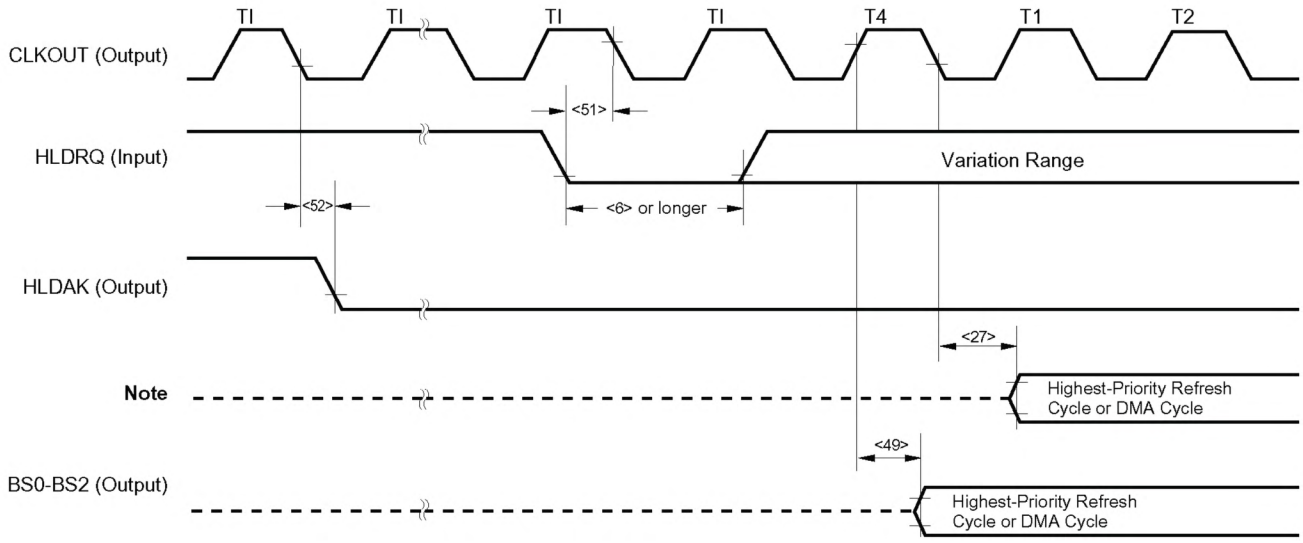
HLDRQ/HLDAK Timing (1)



Note A16/PS0 to A19/PS3, $\overline{UBE}$, $\overline{BUFEN}$, BUF$\overline{R}$/W, $\overline{MRD}$, $\overline{IORD}$, $\overline{MWR}$, $\overline{IOWR}$ (all output): V40HL, V50HL
A8-A15 (output): V40HL AD0-AD7 (input/output): V40HL AD0-AD15 (input/output) V50HL

Remark A dashed line indicates high impedance.

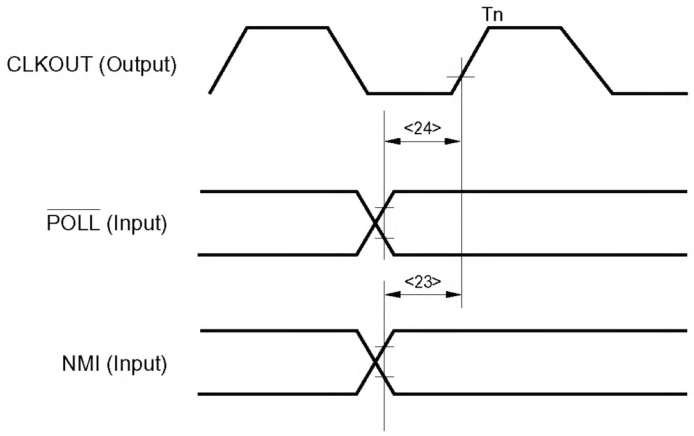
HLDRQ/HLDAK Timing (2)



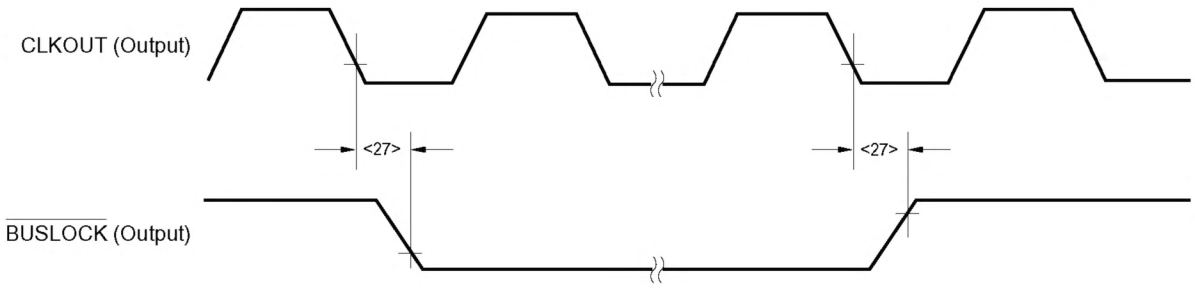
Note A16/PS0 to A19/PS3, $\overline{UBE}$, $\overline{BUFEN}$, BUF$\overline{R}$/W, $\overline{MRD}$, $\overline{IORD}$, $\overline{MWR}$, $\overline{IOWR}$ (all output): V40HL, V50HL
A8-A15 (output): V40HL AD0-AD7 (input/output): V40HL AD0-AD15 (input/output) V50HL

Remark A dashed line indicates high impedance.

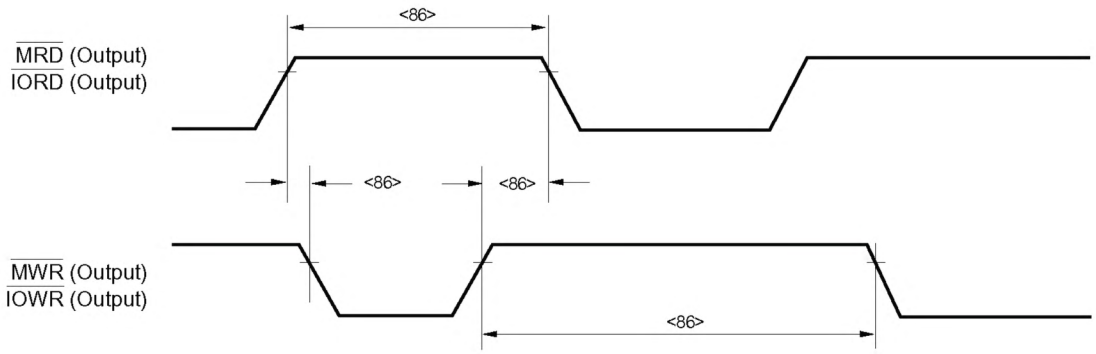
$\overline{\text{POLL}}$, NMI Input Timing



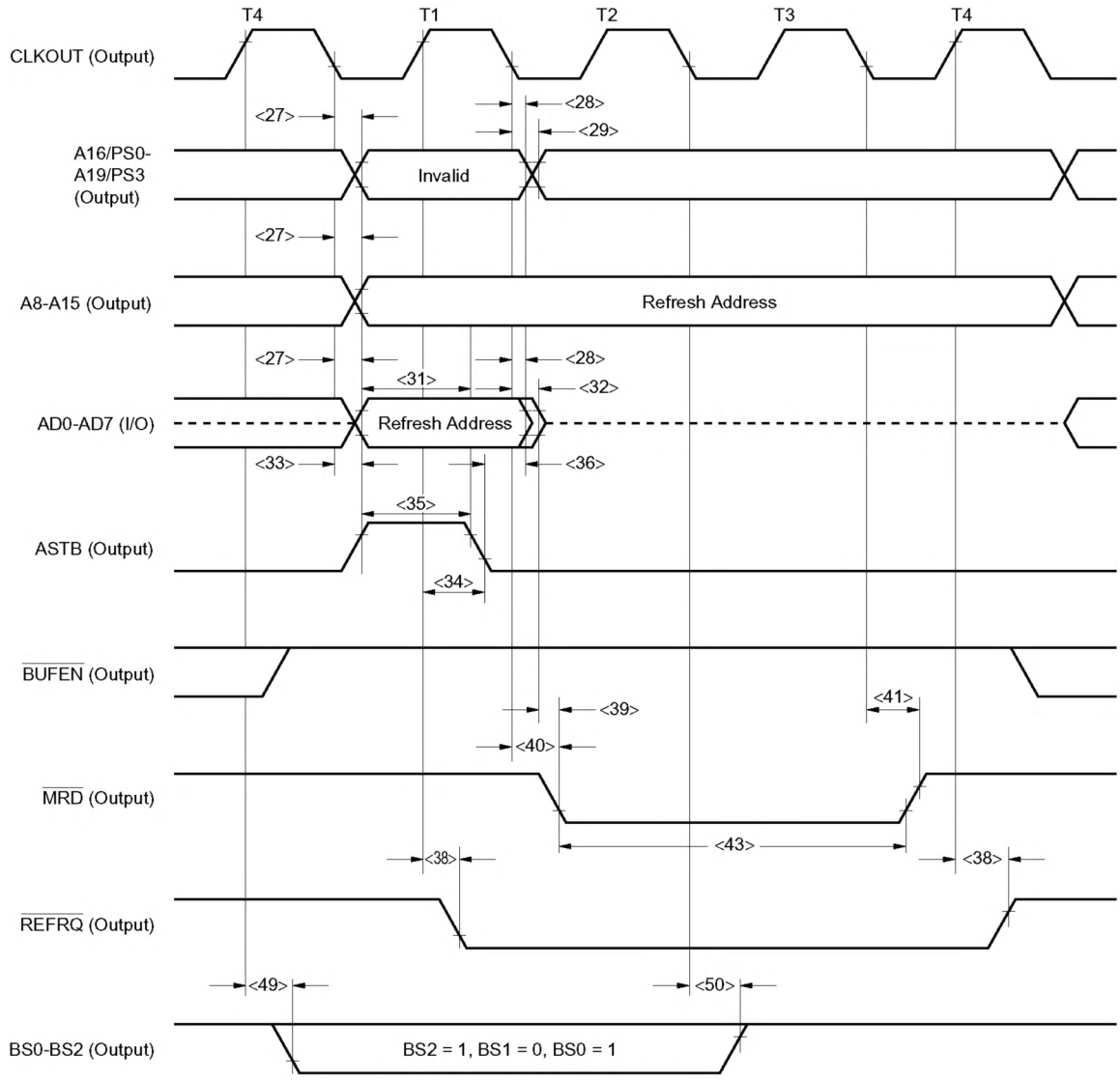
$\overline{\text{BUSLOCK}}$ Output Timing



Access Interval

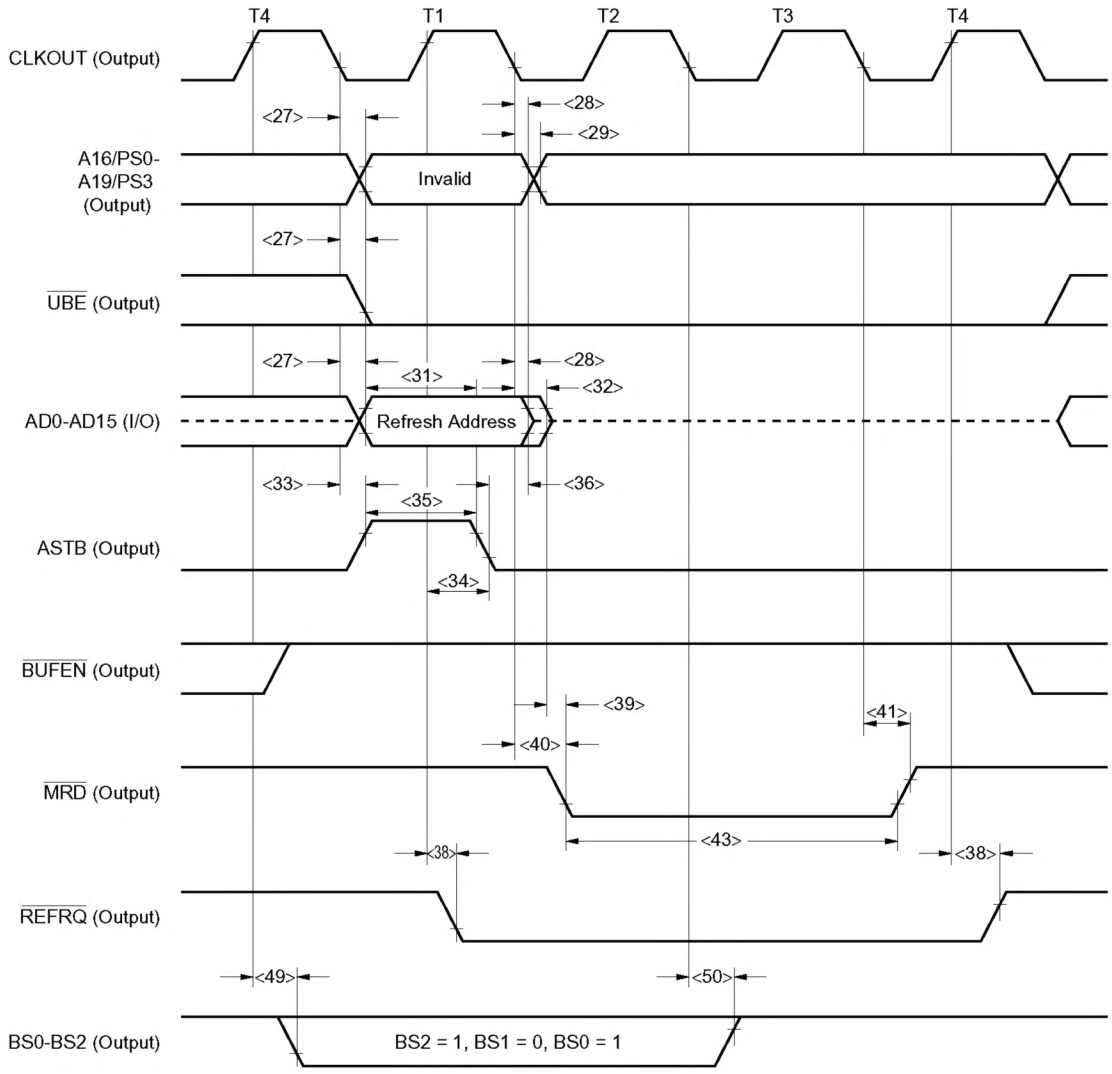


Refresh Timing (V40HL)



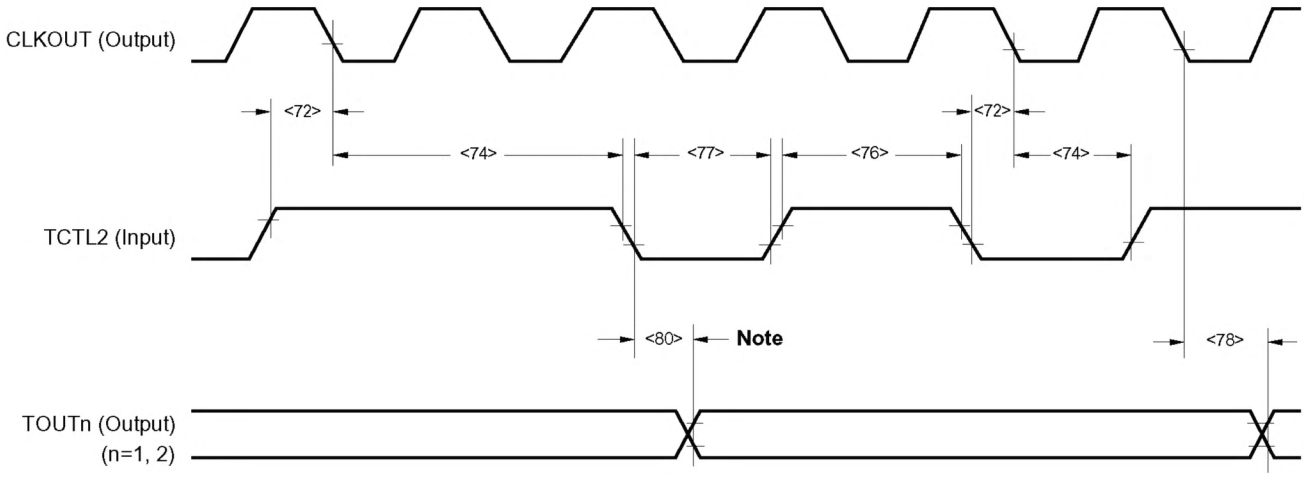
Remark A dashed line indicates high impedance.

Refresh Timing (V50HL)



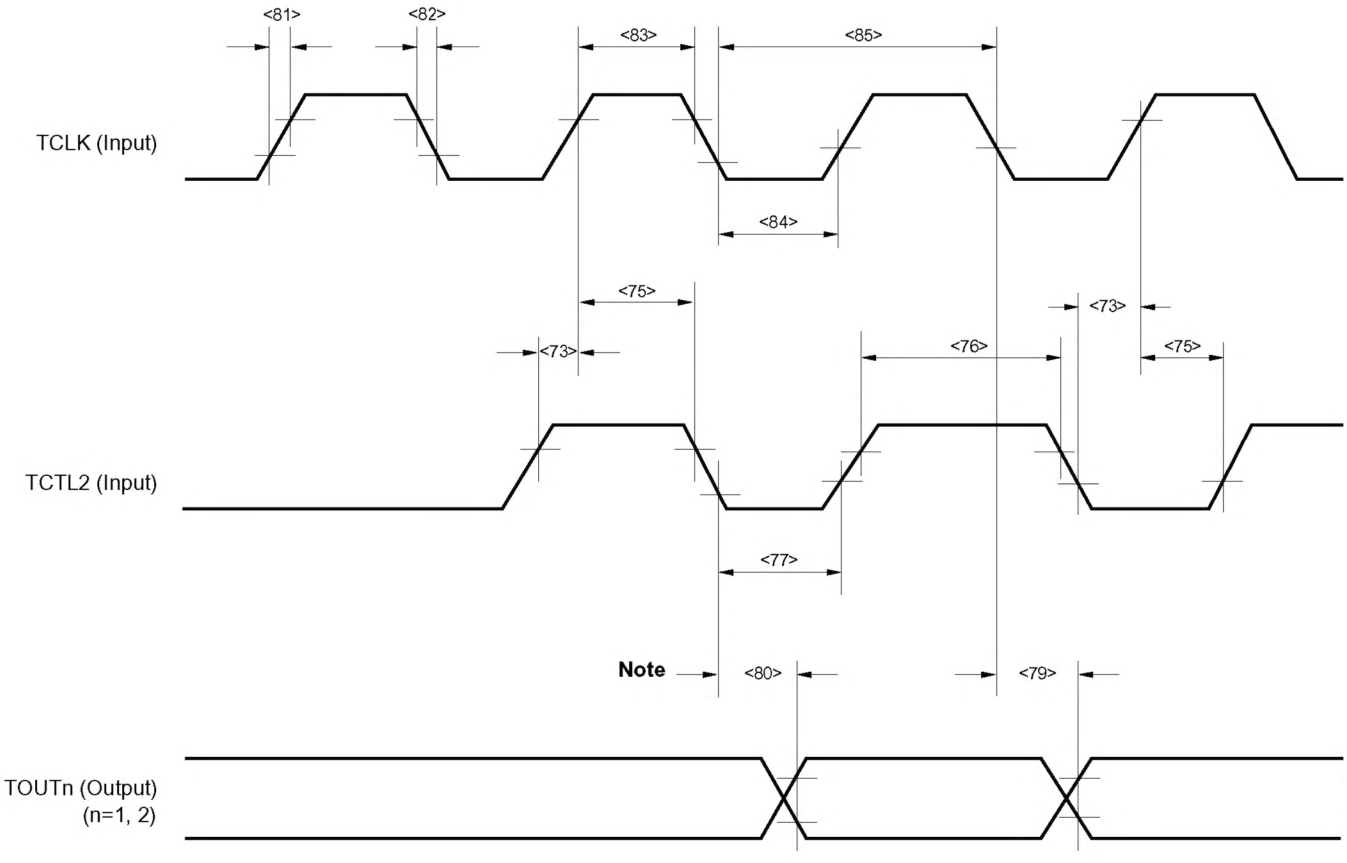
Remark A dashed line indicates high impedance.

TCU Timing (1)



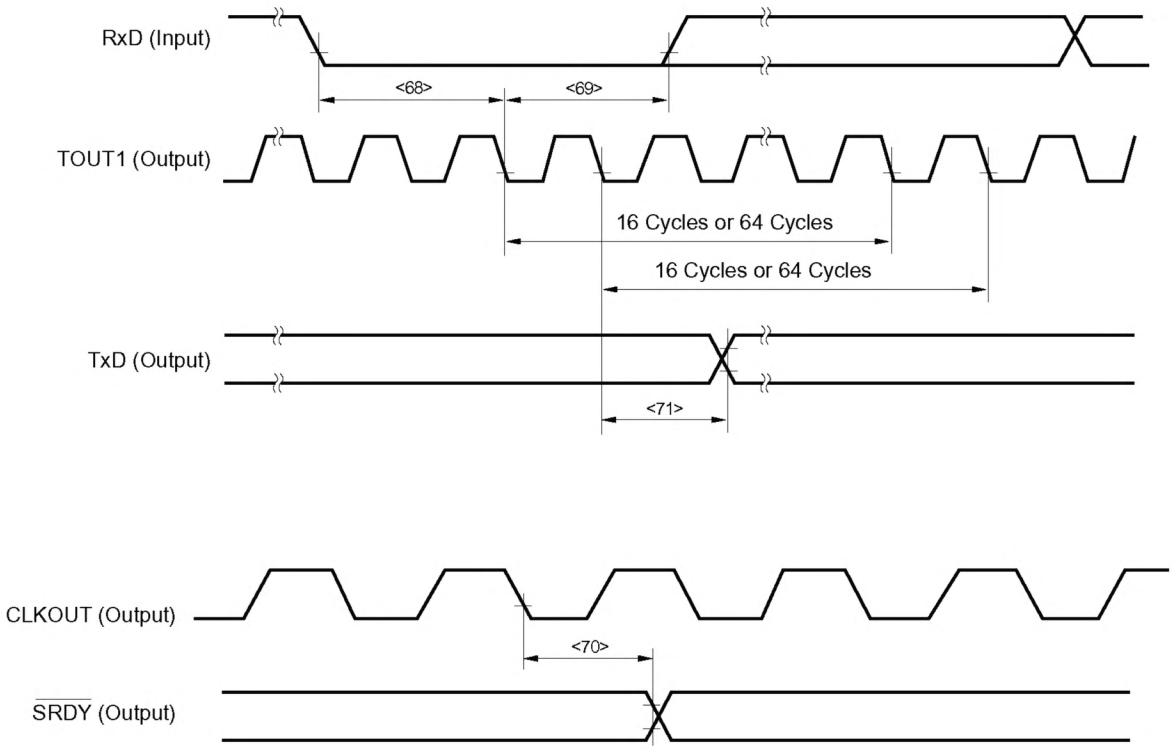
Note Applies to TOUT2 output.

TCU Timing (2)

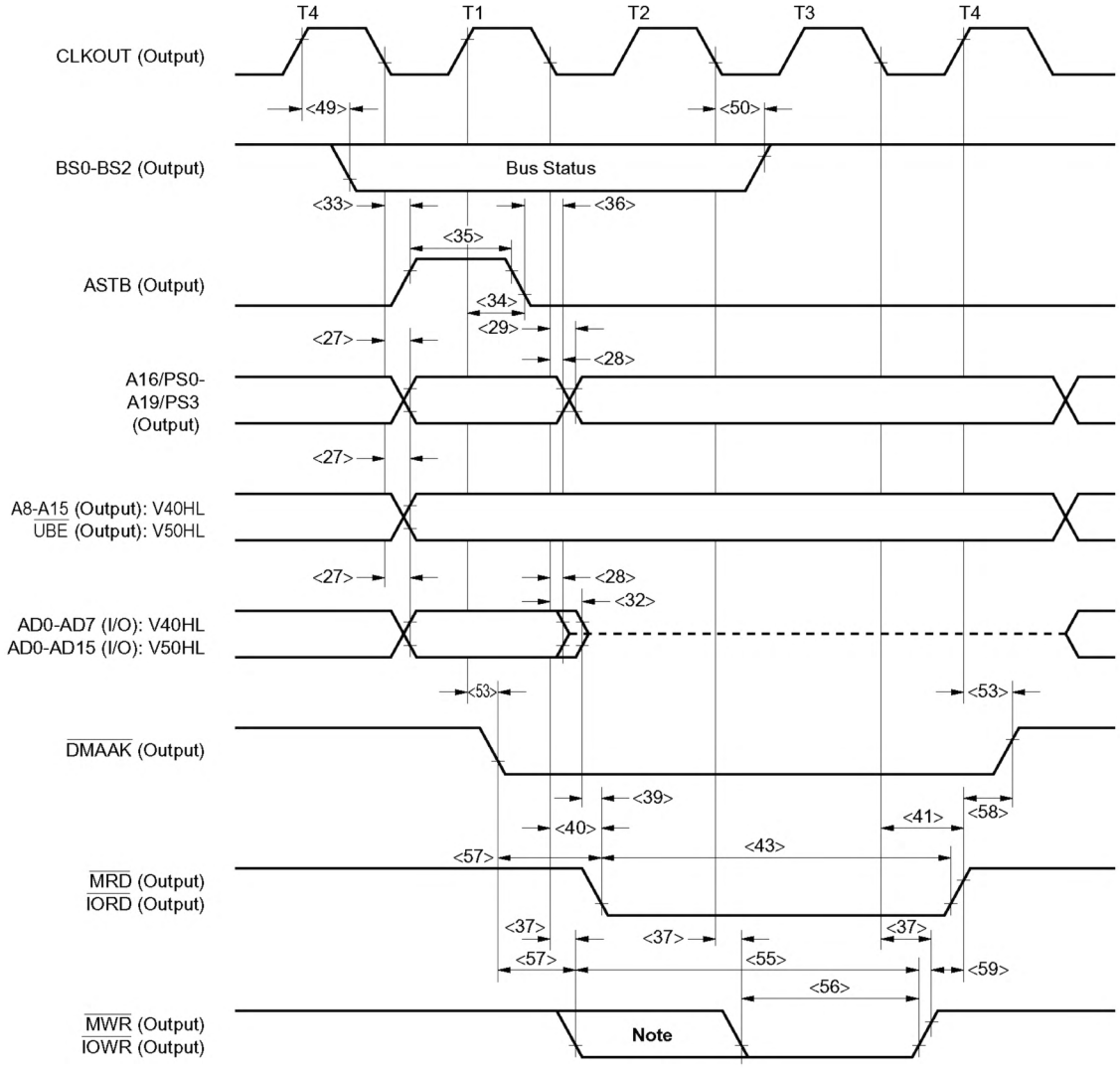


Note Applies to TOUT2 output.

SCU Timing


RxD (Input)
<68>
<69>
TOUT1 (Output)
16 Cycles or 64 Cycles
16 Cycles or 64 Cycles
TxD (Output)
<71>
CLKOUT (Output)
<70>
SRDY (Output)

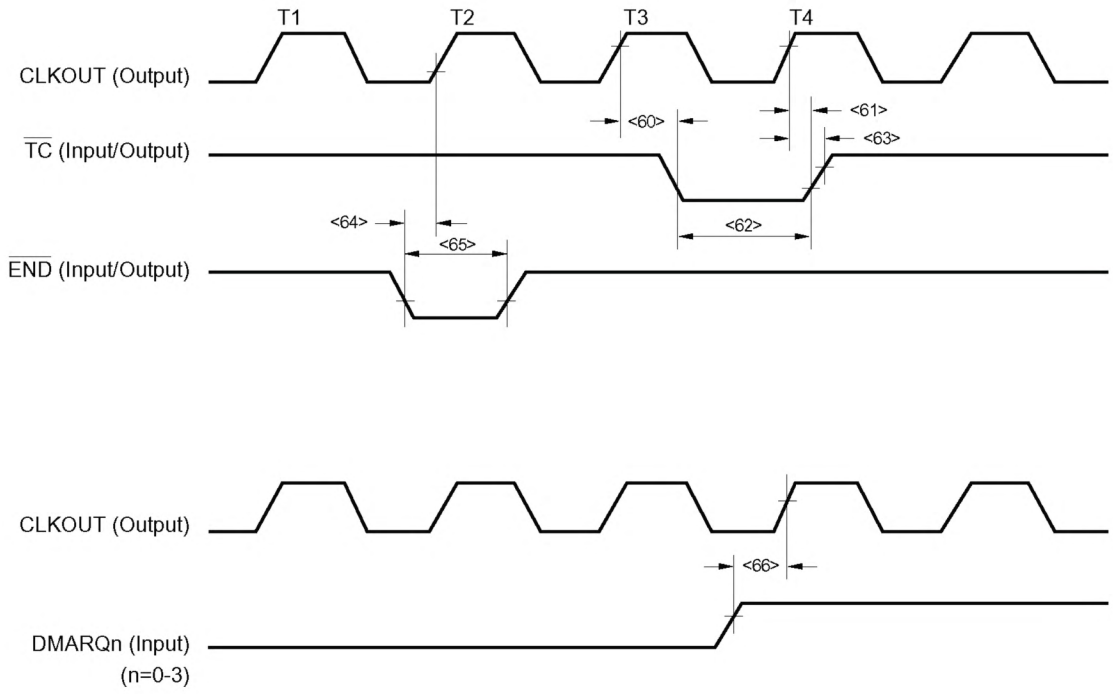
DMAU Timing (1)



Note Low-level signal is output in extended write mode.

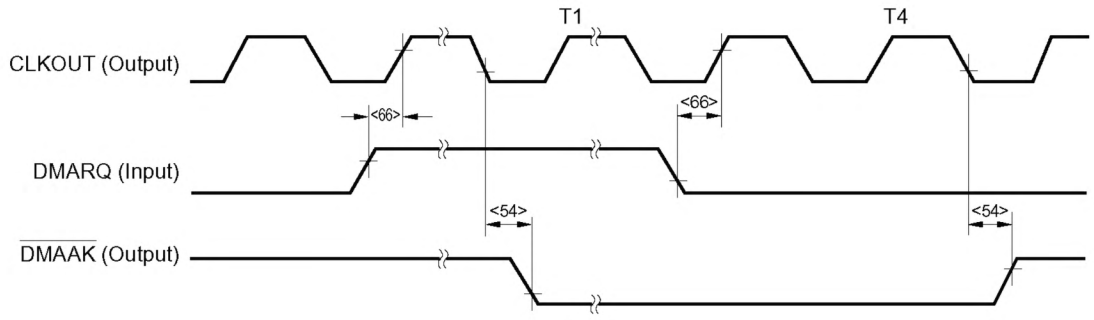
Remark A dashed line indicates high impedance.

DMAU Timing (2)

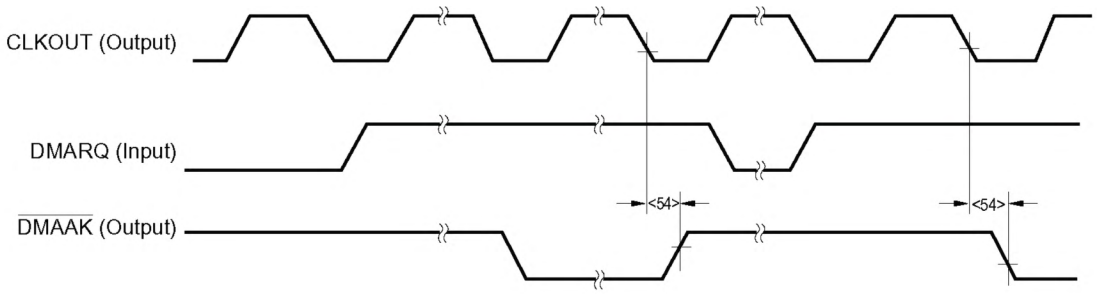


DMAU Timing (3) (Cascade Mode)

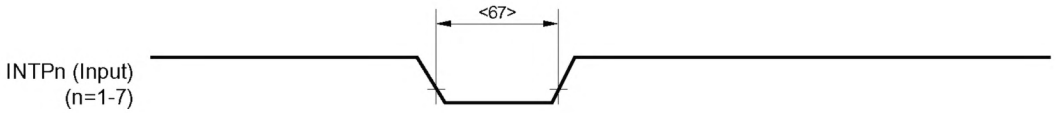
In Normal Operation:



When Refresh Cycle is Inserted:

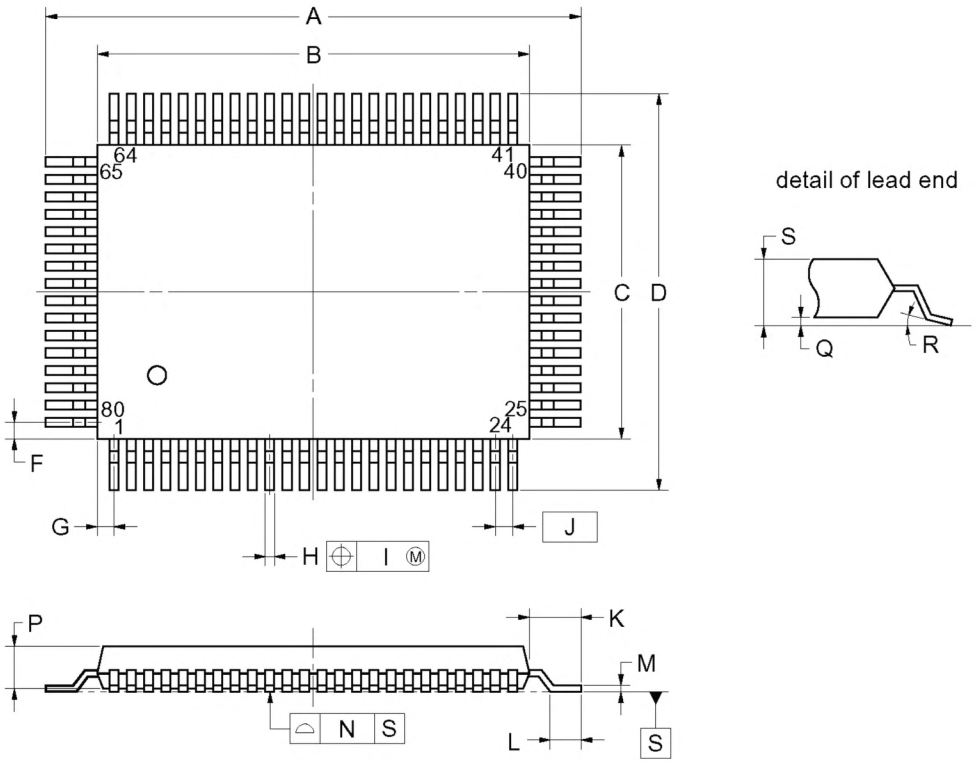


ICU Timing



17. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14x20)



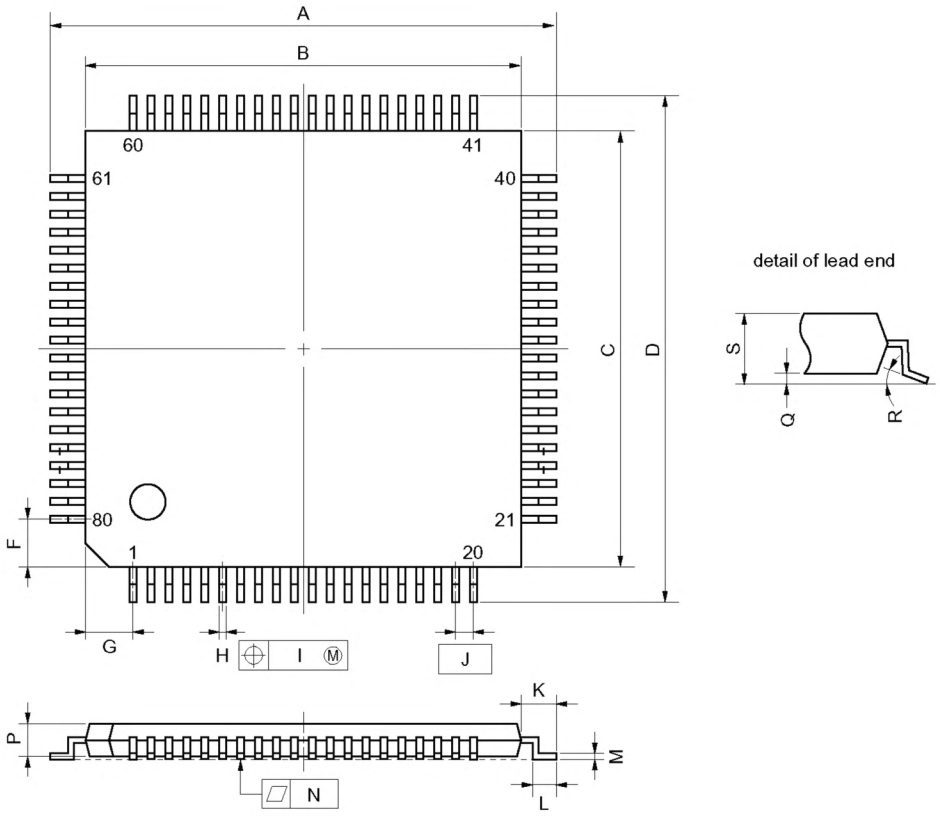
NOTE

1. Controlling dimension —— millimeter.
2. Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	0.8	0.031
H	$0.37^{+0.08}_{-0.07}$	$0.015^{+0.003}_{-0.004}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.08}_{-0.07}$	$0.007^{+0.003}_{-0.004}$
N	0.10	0.004
P	2.7±0.1	$0.106^{+0.005}_{-0.004}$
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P80GF-80-3B9-4

80 PIN PLASTIC TQFP (FINE PITCH) (□12)



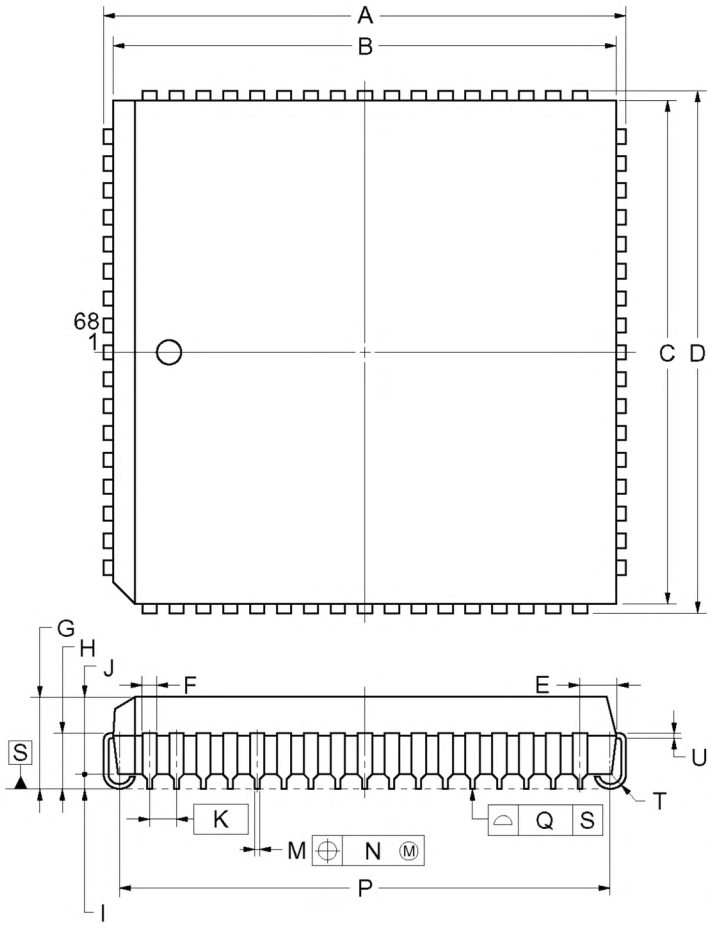
NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	0.551±0.008
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.0±0.2	0.551±0.008
F	1.25	0.049
G	1.25	0.049
H	0.22±0.05	$0.009^{+0.002}_{-0.003}$
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	0.145±0.05	$0.006^{+0.002}_{-0.003}$
N	0.10	0.004
P	1.0±0.05	$0.040^{+0.002}_{-0.003}$
Q	0.1±0.05	0.004±0.002
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.2 MAX.	0.048 MAX.

S80GK-50-9EU

68 PIN PLASTIC QFJ (950 x 950 mil)



ITEM	MILLIMETERS	INCHES
A	25.2±0.2	0.992±0.008
B	24.20±0.1	$0.953^{+0.004}_{-0.005}$
C	24.20±0.1	$0.953^{+0.004}_{-0.005}$
D	25.2±0.2	0.992±0.008
E	1.94±0.15	$0.076^{+0.007}_{-0.006}$
F	0.6	0.024
G	4.4±0.2	$0.173^{+0.009}_{-0.008}$
H	2.8±0.2	$0.110^{+0.009}_{-0.008}$
I	0.9 MIN.	0.035 MIN.
J	3.4±0.1	$0.134^{+0.004}_{-0.005}$
K	1.27 (T.P.)	0.050 (T.P.)
M	0.42±0.08	$0.017^{+0.003}_{-0.004}$
N	0.12	0.005
P	23.12±0.2	$0.910^{+0.009}_{-0.008}$
Q	0.15	0.006
T	R 0.8	R 0.031
U	$0.22^{+0.08}_{-0.07}$	$0.009^{+0.003}_{-0.004}$

P68L-50A1-3

NOTES

1. Controlling dimension —— millimeter.

2. Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

18. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended in the table below.

For the details of recommended soldering conditions for the surface mounting type, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact our salesman.

Table 18-1. Soldering Conditions

(1) μPD70208HGF-×-3B9 : 80-pin plastic QFP (14 × 20 mm)
μPD70216HGF-×-3B9 : 80-pin plastic QFP (14 × 20 mm)

(a) K, E, X masks

Soldering Method	Soldering Conditions	Recommended Conditions Symbol
Infrared reflow	Package peak temperature : 230 °C, Time: 30 sec. max. (210 °C min.), Number of times: 1, Number of days[Note]: 7 days (after this, prebaking is necessary at 125 °C for 10 hours)	IR30-107-1
VPS	Package peak temperature: 215 °C, Time: 40 sec. max. (200 °C min.), Number of times: 1, Number of days[Note]: 7 days (after this, prebaking is necessary at 125 °C for 10 hours)	VP15-107-1
Wave soldering	Solder bath temperature: 260 °C max. Time: 10 sec. max., Number of times: 1, Preheating temperature: 120 °C max. (Package surface temperature), Number of days[Note]: 7 days (after this, prebaking is necessary at 125 °C for 10 hours).	WS60-107-1
Partial pin heating	Pin temperature: 300 °C max., Time: 3 sec. max. (per device side)	—

(b) P, M masks

Soldering Method	Soldering Conditions	Recommended Conditions Symbol
Infrared reflow	Package peak temperature: 235 °C, Time: 30 sec. max. (210 °C min.), Number of times: 2 max., Number of days[Note]: 7 days (after this, prebaking is necessary at 125 °C for 20 hours).	IR35-207-2
VPS	Package peak temperature: 215 °C, Time: 40 sec. (200 °C min.) Number of times: 2 max., Number of days[Note]: 7 days (after this prebaking is necessary at 125 °C for 20 hours).	VP15-207-2
Wave soldering	Solder bath temperature: 260 °C max., Time: 10 sec. max., Number of times: 1, Preheating temperature: 120 °C max. (Package surface temperature). Number of days[Note]: 7 days (after this, prebaking is necessary at 125 °C for 20 hours).	WS60-207-1
Partial pin heating	Pin temperature: 300 °C max., Time: 3 sec. max. (per device side)	—

Note This means the number of days after unpacking the dry pack. Storage conditions are 25 °C and 65% RH max.

(c) L, F masks

Soldering Method	Soldering Conditions	Recommended Conditions Symbol
Infrared reflow	Package peak temperature: 235 °C, Time: 30 sec. max. (210 °C min.), Number of times: 3 max.	IR35-00-3
VPS	Package peak temperature: 215 °C, Time: 40 sec. (200 °C min.) Number of times: 3 max.	VP15-00-3
Wave soldering	Solder bath temperature: 260 °C max., Time: 10 sec. max., Number of times: 1, Preheating temperature: 120 °C max. (Package surface temperature)	WS60-00-1
Partial pin heating	Pin temperature: 300 °C max., Time: 3 sec. max. (per device side)	—

Caution Do not use one soldering method in combination with another. (however, partial pin heating can be performed with other soldering methods).

(2) μPD70208HGK-×-9EU : 80-pin plastic TQFP (fine pitch) (12 × 12 mm)
μPD70216HGK-×-9EU : 80-pin plastic TQFP (fine pitch) (12 × 12 mm)

(a) K, E, X masks

Soldering Method	Soldering Conditions	Recommended Conditions Symbol
Infrared reflow	Package peak temperature : 230 °C, Time: 30 sec. max. (210 °C min.), Number of timers: 1, Number of days[Note]: 1 day (after this, prebaking is necessary at 125 °C for 10 hours)	IR30-101-1
VPS	Package peak temperature: 215 °C, Time: 40 sec. max. (200 °C min.), Number of times: 1, Number of days[Note]: 1 day (after this, prebaking is necessary at 125 °C for 10 hours)	VP15-101-1
Partial pin heating	Pin temperature: 300 °C max., Time: 3 sec. max. (per device side)	—

(b) P, M, L, F masks

Soldering Method	Soldering Conditions	Recommended Conditions Symbol
Infrared reflow	Package peak temperature: 235 °C, Time: 30 sec. max. (210 °C min.), Number of times: 2 max., Number of days[Note]: 7 days (after this, prebaking is necessary at 125 °C for 10 hours).	IR35-107-2
VPS	Package peak temperature: 215 °C, Time: 40 sec. (200 °C min.), Number of times: 2 max., Number of days[Note]: 7 days (after this prebaking is necessary at 125 °C for 10 hours).	VP15-107-2
Partial heating	Pin temperature: 300 °C max., Time: 3 sec. max. (per device side)	—

Note This means the number of days after unpacking the dry pack. Storage conditions are 25 °C and 65% RH max.

Caution Do not use one soldering method in combination with another. (however, partial pin heating can be performed with other soldering methods).

(3) μPD70208HLP-× : 68-pin plastic QFJ (950 × 950 mil)
μPD70216HLP-× : 68-pin plastic QFJ (950 × 950 mil)

(a) K, E, X masks

Soldering Method	Soldering Conditions	Recommended Conditions Symbol
Infrared reflow	Package peak temperature : 230 °C, Time: 30 sec. max. (210 °C min.), Number of timers: 1, Number of days[Note]: 7 days (after this, prebaking is necessary at 125 °C for 36 hours)	IR30-367-1
VPS	Package peak temperature: 215 °C, Time: 40 sec. max. (200 °C min.), Number of times: 1, Number of days[Note]: 7 days (after this, prebaking is necessary at 125 °C for 36 hours)	VP15-367-1
Partial pin heating	Pin temperature: 300 °C max., Time: 3 sec. max. (per device side)	—

(b) P, M, L, F masks

Soldering Method	Soldering Conditions	Recommended Conditions Symbol
Infrared reflow	Package peak temperature: 235 °C, Time: 30 sec. max. (210 °C min.), Number of times: 3 max., Number of days[Note]: 7 days (after this, prebaking is necessary at 125 °C for 36 hours).	IR35-367-3
VPS	Package peak temperature: 215 °C, Time: 40 sec. (200 °C min.), Number of times: 3 max., Number of days[Note]: 7 days (after this prebaking is necessary at 125 °C for 36 hours).	VP15-367-3
Partial pin heating	Pin temperature: 300 °C max., Time: 3 sec. max. (per device side)	—

Note This means the number of days after unpacking the dry pack. Storage conditions are 25 °C and 65% RH max.

Caution Do not use one soldering method in combination with another. (however, partial pin heating can be performed with other soldering methods).