Cat. No. 25-1513

Tandy 1000 HX

Technical Reference Manual

TANDY®

TANDY 1000 HX
TECHNICAL REFERENCE MANUAL
Cat. No. 25-1513

Tandy 1000 HX
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Contents

Sections

Important Customer Note:

A gray stripe has been printed along the right edge of the title page of each of the sections to facilitate your finding the beginning of the section. Also, a tabbed divider for each section has been provided for insertion at this point.

1000 HX Main Logic Board

1000 HX Main Logic Board
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INTRODUCTION TO THE TANDY 1000 HX COMPUTER

The Tandy 1000 HX Computer is modular in design to allow maximum flexibility in system configuration. The computer consists of a Main Unit, and a monitor. The Main Unit is supplied with one 3 1/2" internal disk drive. A second internal 3 1/2" disk drive is optional. Each disk drive has a capacity of 720K bytes formatted. The standard types of monitors used with the Tandy 1000 HX are the monochrome composite and the color RGB monitor.

The Tandy 1000 HX has a standard 256K of system RAM. An optional DMA/RAM board allows the Tandy 1000 HX to be expanded by 128K or 384K of RAM. This board will fit onto the expansion slot. With a fully populated RAM board installed, the Tandy 1000 HX will have 640K bytes of RAM allowed by the system memory map.

Other features include a parallel printer port, two built-in joystick interfaces, and a headphone connection for private listening.

The Main Unit is the heart of the Tandy 1000 HX. It houses the Main Logic Assembly, system power supply, internal 3 1/2" disk drive, and keyboard.

The Main Logic Assembly is a large board mounted to the bottom of the Main Unit and interconnected to the keyboard, power supply, and disk drive by a series of cables. Figure 1 shows the Tandy 1000 HX.

The Power Supply is a 28W switching regulator type, designed to provide adequate power capacity for a fully configured system.

The Internal 3 1/2" Disk Drive uses double-sided, double-density diskettes to read, write, or store data. These are soft sector diskettes. The Disk Drive assembly is installed in the standard unit. All system programs, with the exception of the system startup sequence, are stored on disk.

Either a monochrome or a color display may be used with the Tandy 1000 HX. The monochrome monitor is a high-resolution green phosphor display which provides excellent visual quality. It features a 12" screen with an anti-glare surface. Each display is capable of 25 lines of 80 characters. The character matrix is 8 wide x 9 high.

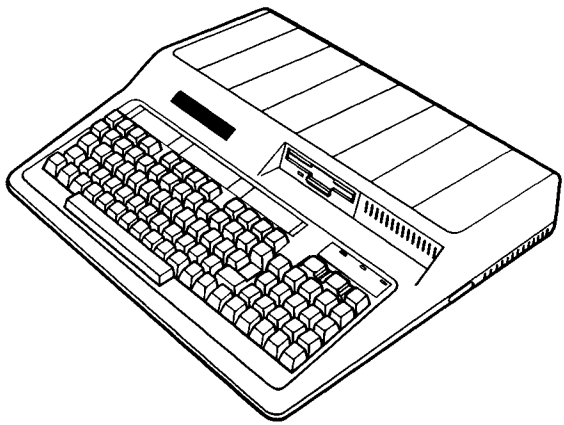


Figure 1. TANDY 1000 HX

SPECIFICATIONS

Processor: Intel 8088-2

Dimensions: 3 1/4 x 17 x 14 1/2 (HWD)

Weight: 11 lbs

Power Requirements: 120 VAC, 60 Hz

With 3 1/2" Disk Drives, Memory Cards, and RS-232:
AC Current: 0.7 - 0.8 Amps with Floppy doing R/W tests.
Leakage Current: 0.5 mA
Power Supply Output:
+5 VDC 3.0 Amps max., 1.9 Amps Typ.
+12 VDC 2.0 Amps max. 1.2 Amps continuous
-12 VDC .1 Amp max.

Environment:
Air Temperature
System ON: 55 to 85 degrees F (13 to 30 degrees C)
System OFF: -40 to 150 degrees F (-40 to 69 degrees C)
Humidity: System ON-OFF: 8% to 80%

Disk Drive Specifications
Power:

Supply		
Voltage	+5 VDC Input	+12 VDC Input
Ripple		
0 to 50 kHz	0.1 Vpp	0.1 Vpp
Tolerance		
Including Ripple	+/-5%	+/-5%
Standby Current		
Nominal	50 mA	0.3 mA
Average Current		130 mA
(Read)		
Peak Current		500 mA
(Motor Start)		
Peak Current		450 mA
(Stepping during Motor On)		
Operating Current		
Nominal	240 mA	

Connector Pin Assignments

J1 -- Speaker Interface
(2-Pin Vertical Header)

1 -- Sound	2 -- Ground

J2 -- PWR, NUM, CAP

1 -- Power Indicator	2 -- Gnd
3 -- Num Indicator	4 -- NUMLOCK Control
5 -- CAPS Indicator	6 -- CAPS Control

J3 -- Keyboard Interface

1 -- X1	7 -- X0
2 -- X5	8 -- X7
3 -- X4	9 -- X3
4 -- X3	10 -- X1
5 -- X2	11 -- X5
6 -- X6	12 -- X4

J4 -- Fan

1 -- +12V	2 -- GND

J5 -- DC POWER
(6-Pin Vertical Header)

1 -- +5 VDC	2 -- +5 VDC
3 -- GND	4 -- Ground
5 -- +12V	6 -- -12V

J6 -- Keyboard Interface

1 -- Y0	8 -- Y6
2 -- Y1	9 -- Y7
3 -- Y11	10 -- Y8
4 -- Y2	11 -- Y9
5 -- Y3	12 -- Y10
6 -- Y4	13 -- Y11
7 -- Y5	

J7 -- Audio Jack

1 -- GND	2 -- AUDIOOUT

J8 -- Right Joystick
(6-Pin Rt. Angle Circular Din)

1 -- Y Axis	2 -- X Axis
3 -- Ground	4 -- Switch 1
5 -- +5 VDC	6 -- Switch 2

J9 -- Left Joystick
(6-Pin Rt. Angle Circular Din)

1 -- Y Axis	2 -- X Axis
3 -- Ground	4 -- Switch 1
5 -- +5 VDC	6 -- Switch 2

J10 -- 3 1/2" Disk Interface Internal
(Dual 17-Pin Vertical Header)

1 -- NC	2 -- NC
3 -- +5 V.	4 -- NC
5 -- +5 V.	6 -- NC
7 -- +5 V.	8 -- INDEX*
9 -- +5 V.	10 -- DS0
11 -- +5 V.	12 -- DS2
13 -- Ground	14 -- NC
15 -- Ground	16 -- MTRON*
17 -- Ground	18 -- DIR*
19 -- Ground	20 -- STEP*
21 -- Ground	22 -- WRDATA*
23 -- Ground	24 -- WEN*
25 -- Ground	26 -- TRK0*
27 -- Ground	28 -- WRPRT*
29 -- +12 V.	30 -- RDDATA*
31 -- +12 V.	32 -- SIDESELECT*
33 -- +12 V.	34 -- NC

J11 -- Expansion Interface Connectors
(Dual 31-Pin Header)

A01 -- NMI	B01 -- Ground
A02 -- D7	B02 -- RESET
A03 -- D6	B03 -- +5 VDC
A04 -- D5	B04 -- IR2
A05 -- D4	B05 -- NC
A06 -- D3	B06 -- FDCDMRQ*
A07 -- D2	B07 -- -12 VDC
A08 -- D1	B08 -- NC
A09 -- D0	B09 -- +12 VDC
A10 -- RDYIN	B10 -- Ground
A11 -- AEN	B11 -- MEMW*
A12 -- A19	B12 -- MEMR*
A13 -- A18	B13 -- IOW*
A14 -- A17	B14 -- IOR*
A15 -- A16	B15 -- NC
A16 -- A15	B16 -- NC
A17 -- A14	B17 -- NC
A18 -- A13	B18 -- NC
A19 -- A12	B19 -- REFRESH*
A20 -- A11	B20 -- CLK
A21 -- A10	B21 -- RFSH
A22 -- A09	B22 -- BREQ*
A23 -- A08	B23 -- NC
A24 -- A07	B24 -- IR4
A25 -- A06	B25 -- IR3
A26 -- A05	B26 -- FDCDACK*
A27 -- A04	B27 -- DMATC
A28 -- A03	B28 -- ALE
A29 -- A02	B29 -- +5 VDC
A30 -- A01	B30 -- OSC
A31 -- A00	B31 -- Ground

J12 -- Parallel Interface
(34-Edge Card)

1 -- PPSTROBE*	2 -- Ground
3 -- PPDATA0	4 -- Ground
5 -- PPDATA1	6 -- Ground
7 -- PPDATA2	8 -- Ground
9 -- PPDATA3	10 -- Ground
11 -- PPDATA4	12 -- Ground
13 -- PPDATA5	14 -- NC
15 -- PPDATA6	16 -- Ground
17 -- PPDATA7	18 -- Ground
19 -- PPACK*	20 -- Ground
21 -- PPBUSY	22 -- Ground
23 -- PPE	24 -- Ground
25 -- PPSEL*	26 -- NC
27 -- PPAUTOF*	28 -- PPFAULT
29 -- NC	30 -- PPINIT*
31 -- Ground	32 -- NC
33 -- Ground	34 -- +5 V

J13 -- Floppy Disk Interface External

1 -- +12V	2 -- +5V
3 -- +12V	4 -- +5V
5 -- GND	6 -- +5V
7 -- GND	8 -- +5V
9 -- GND	10 -- INDEX*
11 -- GND	12 -- TK0*
13 -- GND	14 -- STEP*
15 -- SIDESELECT*	16 -- MTRON*
17 -- DIR*	18 -- GND
19 -- WRPRT*	20 -- GND
21 -- RDDATA*	22 -- GND
23 -- WRDATA*	24 -- GND
25 -- WEN*	26 -- GND
27 -- NC	28 -- +12V
29 -- DSEXT*	30 -- +12V

J14 -- Composite Output
(Rt. Angle RCA-Type Phone Jack)

1 -- Compvid	2 -- Ground

J15 -- RGBI Video
(9-Pin Socket Rt. Angle D-Subminiature)

1 -- Ground	2 -- Ground
3 -- Red	4 -- Green
5 -- Blue	6 -- Intensity
7 -- Green (Monochrome Video)	8 -- HSYNC
9 -- VSYNC	

REVISION			
LTR	DESCRIPTION	DATE	APPD

SPECIFICATION - OPTION CARD

REFERENCE DRAWINGS
B1720019
D1720020
C1720011

MAT'L		DRAFT	DATE 1/23/86	TITLE	
		CHECK	DATE		
		DESIGN	DATE	SPECIFICATION OPTION CARD	
FINISH		APPD	DATE		
		APPD	DATE		
		USED ON	TANDY	DWG. NO. A-3080083	
				SCALE	SHEET OF

NOTES (UNLESS OTHERWISE SPECIFIED):

DIM. ARE IN INCHES AND APPLY AFTER PLATING	TOLERANCE xx ± .010 xxx ± .005
DO NOT SCALE DWG.	ANGLES ± 1°

Option Card Description

PINOUT:

IBM Bus Signal	Signal	PIN	PIN	SIGNAL	IBM Bus Signal
GND	GND	B01	A01	NMI	I/OCHCK*
RESETDRV	BRESET	B02	A02	D7	D7
+5V	+5V	B03	A03	D6	D6
IRQ2	IR2	B04	A04	D5	D5
-5VDC	NC	B05	A05	D4	D4
DRQ2	FDCDMARQ0*	B06	A06	D3	D3
-12V	-12V	B07	A07	D2	D2
Reserved	NC	B08	A08	D1	D1
+12V	+12V	B09	A09	D0	D0
GND	GND	B10	A10	READY	I/OCHRDY
MEMW*	MEMW*	B11	A11	AEN	AEN
MEMR*	MEMR*	B12	A12	A19	A19
IOW*	IOW*	B13	A13	A18	A18
IOR*	IOR*	B14	A14	A17	A17
DACK3*	NC	B15	A15	A16	A16
DRQ3	NC	B16	A16	A15	A15
DACK1*	NC	B17	A17	A14	A14
DRQ1	NC	B18	A18	A13	A13
DACK0*	REFRESH*	B19	A19	A12	A12
CLOCK	CLK	B20	A20	A11	A11
IRQ7	RFSH*	B21	A21	A10	A10
IRQ6	BREQ*	B22	A22	A09	A09
IRQ5	NC	B23	A23	A08	A08
IRQ4	IR4	B24	A24	A07	A07
IRQ3	IR3	B25	A25	A06	A06
DACK2*	FDCDMACK*	B26	A26	A05	A05
T/C	TC	B27	A27	A04	A04
ALE	ALE	B28	A28	A03	A03
+5V	+5V	B29	A29	A02	A02
OSC	OSC	B30	A30	A01	A01
GND	GND	B31	A31	A00	A00

OSC	O	Oscillator: 14.31818 Mhz High-speed clock with a 50% duty cycle
CLK	O	System clock: It can be 4.77 Mhz with a 33% duty cycle or 7.16 Mhz with a 50% duty cycle.
BRESET	O	Buffered Reset: This line is used to reset or initialize system logic upon power-up or during a lowline voltage outage. This signal is synchronized to the falling edge of clock and is active high.
A0-A19	O	Address bits 0 to 19: These lines are used to address memory and I/O devices within the system. The 20address lines allow

		access of upto 1 megabyte of memory. A0 is the least significant (LSB) and A19 is the most significant (MSB). These lines are generated by either the processor or DMA controller. They are active high.
D0-D7	I/O	Data Bits 0 to 7: These lines provide data bus bits 0 to 7 for the processor, memory, and I/O devices. D0 is the least significant bit (LSB) and D7 is the most significant bit (MSB). These lines are active high.
ALE	O	Address Latch Enable: This line is provided by the Bus Controller and is used on the system board to latch valid addresses from the processor. It is available to the I/O channel as an indicator of a valid processor address (when used with AEN). Processor addresses are latched with the falling edge of ALE.
NMI	I	-Nonmaskable Interrupt: This line provides the processor with parity (error) information on memory or devices in the I/O channel. When this signal is active low, a parity error is indicated.
RDYIN	I	Ready In: This line, normally high (ready), is pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. It allows slower devices to attach to the I/O channel with a minimum of difficulty. Any slow device using this line should drive it low immediately upon detecting a valid address and a read or write command. This line should never be held low longer than 10 clock cycles. Machine cycles (I/O or memory) are extended by an integral number of CLK cycles (210ns or 140ns, depending upon CPU speed).
IR2-IR4 BREQ, RFSH*	I	Interrupt Request: These lines are used to signal the processor that an I/O device requires attention. They are prioritized with IRQ2 as the highest priority and RFSH* as the lowest. An Interrupt Request is generated by raising an IRQ line (low to high) and holding it high until it is acknowledged by the processor (interrupt service routine).
IOR*	O	-I/O Read command: This command line instructs an I/O device to drive its data

		onto the data bus. It may be driven by the processor or the DMA controller. This signal is active low.
IOW*	O	-I/O Write command: This command line instructs an I/O device to read the data on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.
MEMR*	O	Memory Read command: This command line instructs the memory to drive its data onto the data bus. It may be driven by the processor or the DMA controller. This signal is active low.
MEMW*	0	Memory Write command: This command line instructs the memory to store the data present on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.
FDCDMRQ*	O	FDC DMA Request: This line is an asynchronous channel request used by a floppy disk to gain DMA service. A request is generated by bringing the line to an active level (high). The line must be held high until the FDCDACK* line goes active.
REFRESH* FDCDACK*	I	-DMA Acknowledge: These lines are used to acknowledge FDC DMA requests and to refresh system dynamic memory. They are active low.
AEN	O	Address Enable: This line is used to de-gate the processor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active (high), the DMA controller has control of the address bus, data bus, read commnad lines (memory and I/O), and the write command lines (memory and I/O).
DMATC	I	Terminal Count: This line provides a pulse when the terminal count for any DMA channel is reached. This signal is active high.
Voltages: +5Vdc+/-5%, 1.4A,		located on 2 connector pins (.45A per option board).

+12Vdc+/-5%, 0.1A,	located on 1 connector pin (0.03A per option board).
-12Vdc+/-10%, 0.1A,	located on 1 connector pin (0.03A per option board).
GND (Ground),	located on 3 connector pins

BUS INTERFACE SPECIFICATIONS

This specification is for the primary bus on the Tandy 1000 HX main logic board, which also is available to the option board connectors. The specification describes the signals in the following manner. See Figures 2 and 3.

- The following signal nomenclature is used in the schematic and literature. Signals designated with the suffix "*" are logically "true low" (normal inactive state is high); if they are not so designated, the signal is logically "true high."
- Direction -- input or output -- is referenced to the CPU.
- Brief functional description of the signal.
- Description of the "drive" or "load" characteristics of the signal. This includes the specific source by IC type and reference designator, drive capability for "output" signals, and actual load for "input" signals. The drive/load is defined in "unit loads" and specified as "high/low." This specification is for the main logic board only. Some signals have an alternate source, an external bus master such as the DMA.
- 1 Unit Load (UL) is defined as: Ioh = .04mA @ 2.4V, Iol = 1.6mA @ 0.5V

Signal Listing

A00 - A19	O	ADDRESS	SOURCE: U23,U32,U36 Drive - 65/15 UL Latch Strobe - ALE Output Enable - AEN Alternate external source
D0-D7	I/O	DATA	SOURCE: U40 Drive - 37/15 UL Direction Control - RD* (CPU read signal) Enable - DEN*
ALE	O	ADDRESS LATCH STROBE	SOURCE: U6
IOW*	O	I/O WRITE STROBE	Drive - 50/7.5 UL
IOR*	O	I/O READ STROBE	Output Enable - AEN
MEMW*	O	MEMORY WRITE STROBE	Pull-Up - 4.7K ohms

MEMR*	O	MEMORY READ STROBE	Alternate external source
CLK	O	CPU CLOCK	7.16MHz, 50% duty cycle or 4.77MHz, 33% duty cycle SOURCE: U23 Drive - 75/7.5 UL
OSC	O	OSCILLATOR	14.32MHz, 50% duty cycle SOURCE: U23 Drive - 75/7.5 UL
NMI	I	NON-MASKABLE INTERRUPT	To System NMI Load: 1/1 UL, U16
RDYIN	I	SYSTEM WAIT	SOURCE: OPEN-COLLECTOR OR 3-STATE BUFFERS Load: 1 UL and 1.0K ohm pull-up. 10/0.9 UL Set LOW by Peripherals (I/O or Memory) to extend READ or WRITE cycles.
RESET	O	SYSTEM RESET	Power On or Manual SOURCE: U23 Drive: 75/7.5 UL
BREQ*	I	BUS REQUEST	From external masters Load: 1 UL and 10K ohm pull-up. 10/0.9 UL
AEN	O	BUS GRANT	To external masters SOURCE: U23 Drive - 75/7.5 UL
IR2	I	INTERRUPT REQUEST#2	To system interrupt controller
IR3	I	INTERRUPT REQUEST#3	Load: 1 UL and 2.2K pull-down
IR4	I	INTERRUPT REQUEST#4	

The following are not sourced by the CPU but are to be SOURCED (O) Output or Loaded (I) Input by an external DMA source:

RFSH	I	REQUEST DMA CHANNEL#0	Dedicated input requests to DMA
DRQ1	I	REQUEST DMA CHANNEL#1	
FDCDMRQ	I	REQUEST DMA CHANNEL#2	1 MOS load 40/160 UL
DRQ3	I	REQUEST DMA CHANNEL#3	
REFRESH*	O	ACKNOWLEDGE DRQ0*	Dedicated output acknowledges from DMA.
DACK1*	O	ACKNOWLEDGE DRQ1*	
FDCDACK*	O	ACKNOWLEDGE DRQ2*	
DACK3*	O	ACKNOWLEDGE DRQ3*	
DMATC	O	TERMINAL COUNT	Used by DMA Controller to indicate Terminal Count reached. Drive: 2/2 UL

+5VDC	+5VDC	4% 1.0 Amps available on the bus.
+12VDC	+12VDC	5% .3 Amps available on the bus.
-12VDC	-12VDC	+8.3% - 25% 0.06 Amps available on the bus.
GROUND	Power Return for +5, +12, -12 VDC.	

SYSTEM TIMING DIAGRAMS

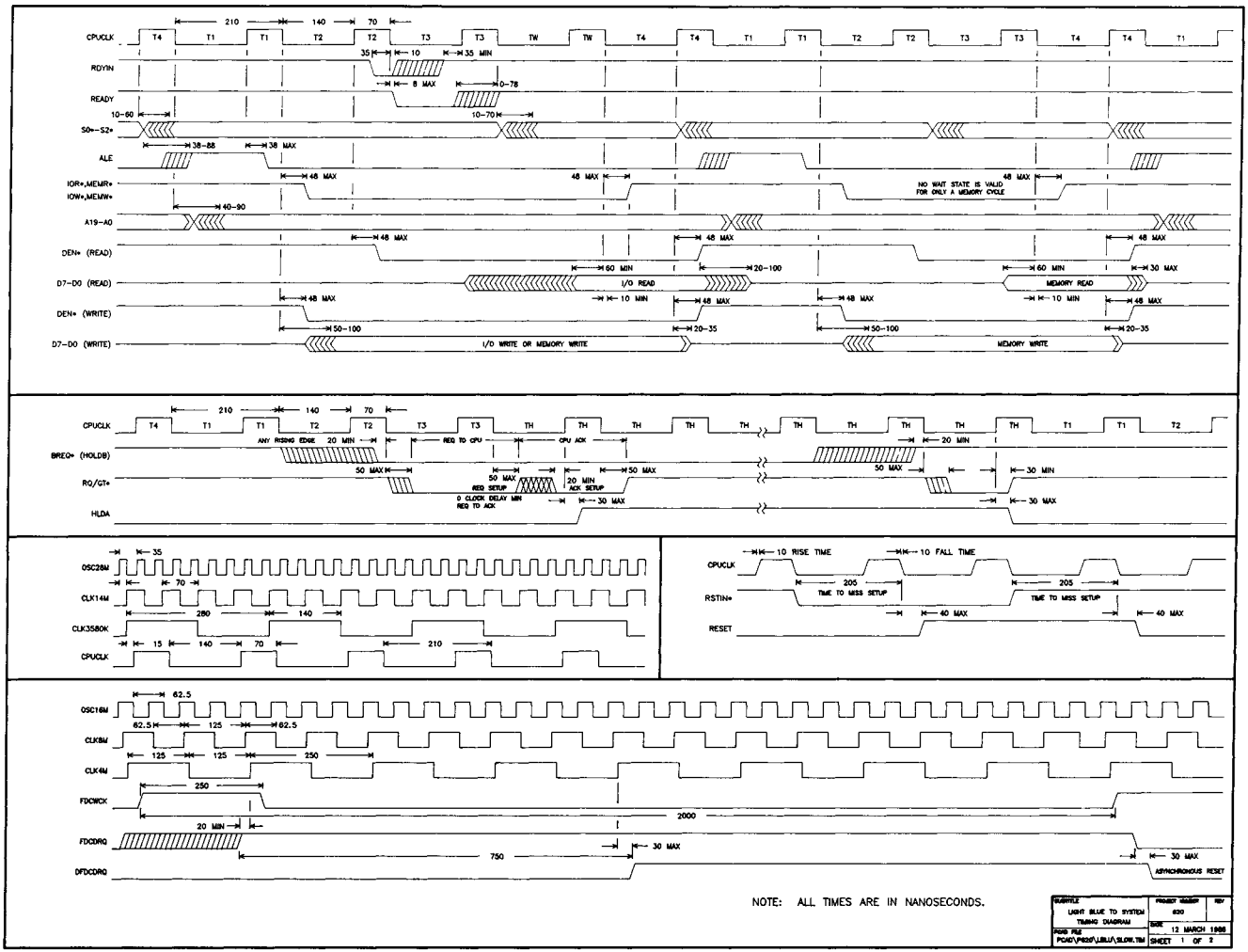


Figure 2. Light Blue to System Timing (1 of 2)

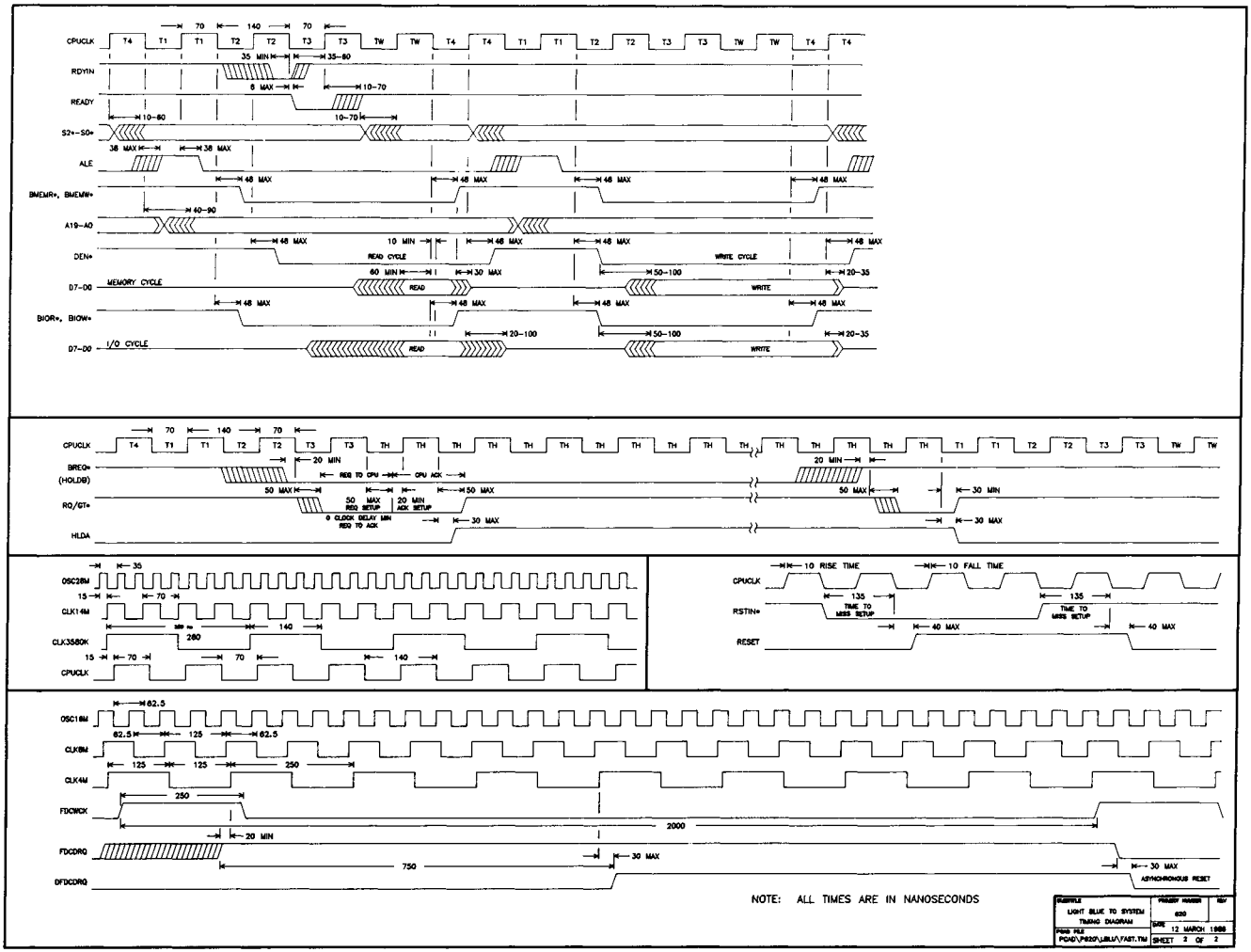


Figure 2 (Cont.) Light Blue to System Timing (2 of 2)

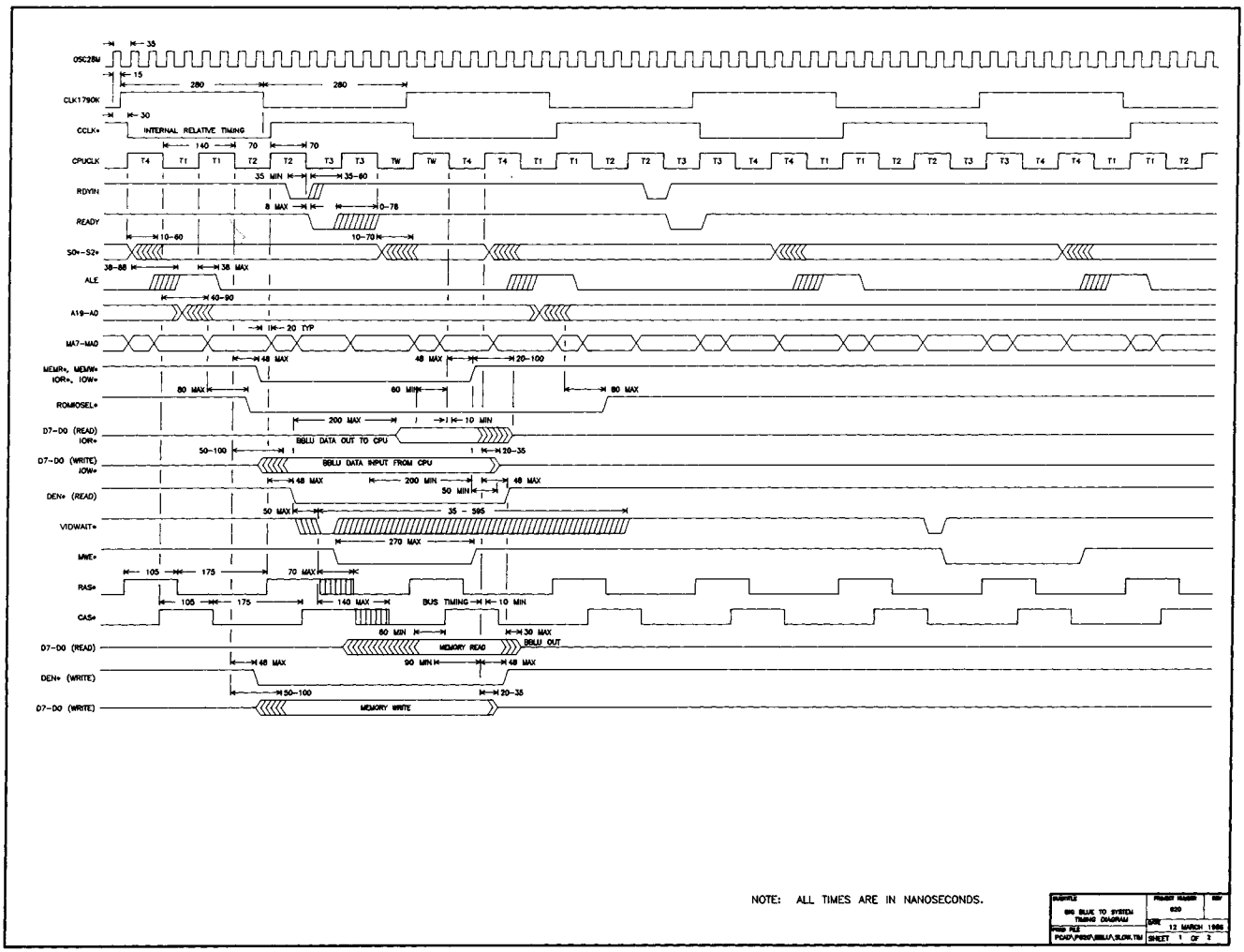


Figure 3. Big Blue to System Timing (1 of 2)

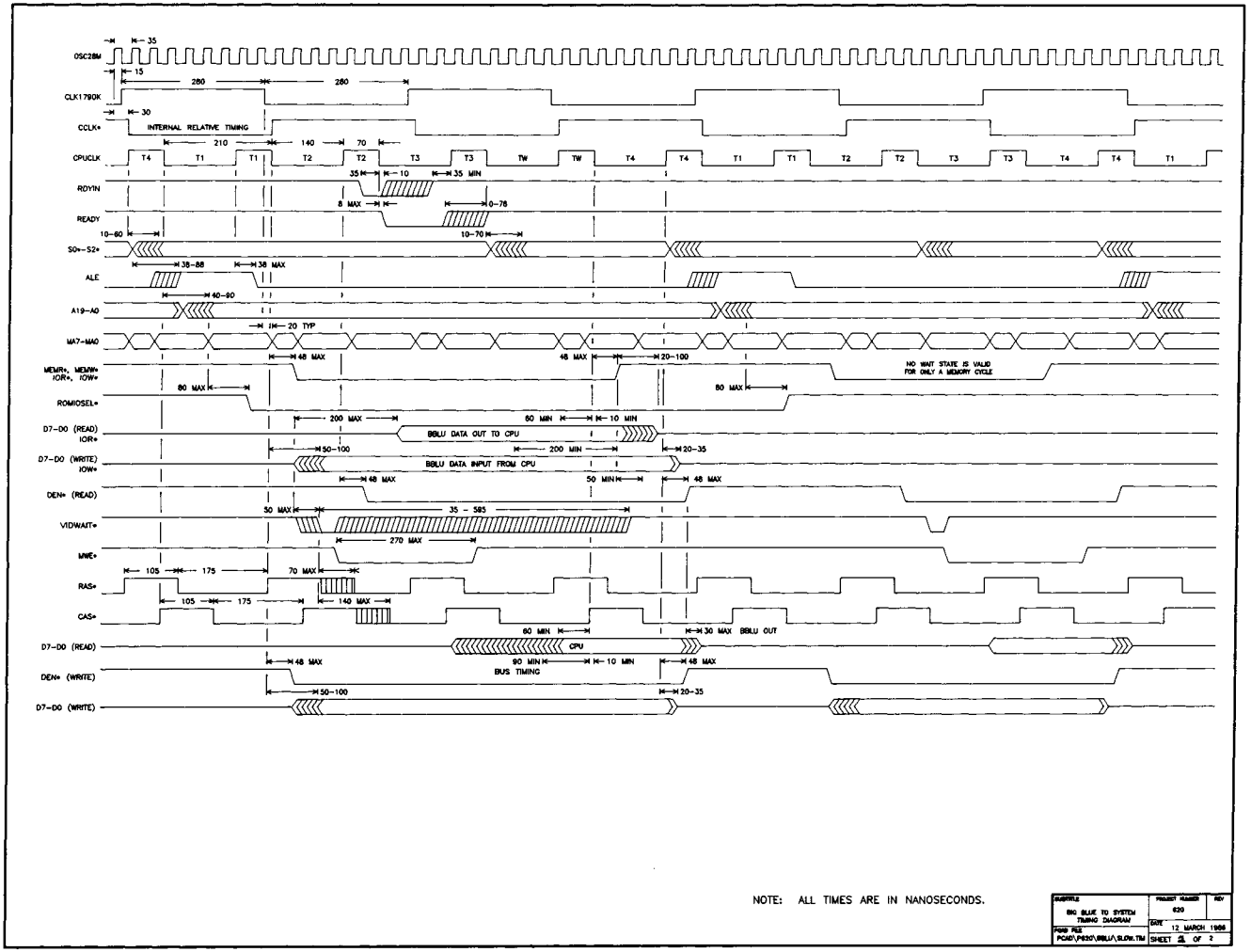


Figure 3 (Cont.) Big Blue to System Timing (2 of 2)

THEORY OF OPERATION

Main Logic Board

The Block Diagram of the main logic board (Figure 4) shows the basic functional divisions.

CPU Function

The CPU function consists of the CPU (Intel 8088-2) U-28, the address interface, data interface, the CPU control signal generator, the bus control signal generator and the interrupt controller (Intel 8259A) U-37.

Non-CPU Function, Main Logic Board

The non-CPU functions can be divided into two main parts: memory and I/O. Memory consists of RAM and ROM. RAM or Video/System Memory (Figure 5) serves as storage for both the video data and program data. ROM memory contains the BIOS and diagnostics. I/O consists of all the peripheral functions: keyboard, floppy disk controller, printer, joystick and sound.

Processor Address/Data Interface

The 8088 has three groups of Address/Data lines; AD0 - AD7, A8 - A15 and A16 - A19. AD0 - AD7 are multiplexed address and data lines. To separate and save the address that comes out first, the signals are applied to U36 (74HCT373) and latched by ALE. Additionally, the signals are applied to data transceiver U40 (74HCT245). U40 is enabled only during the data portion of the CPU cycle. (The exception is during an Interrupt Acknowledge cycle.) Direction of transmission is controlled by the RD* (READ) signal from the Timing Control Generator. Address lines A8 - A15 are present during the entire CPU cycle and need only to be buffered. Address lines A16 - A19 are multiplexed with status signals S4 - S7 and need to be latched. The results are: A8 - A11, A16 - A19 are latched into U31 (74HCT373) by ALE and A12 - A15 are buffered by half of U23 (74HCT244). The outputs from these latches/buffers/transceivers are the BUS Signals A0 - A19, D0 - D7.

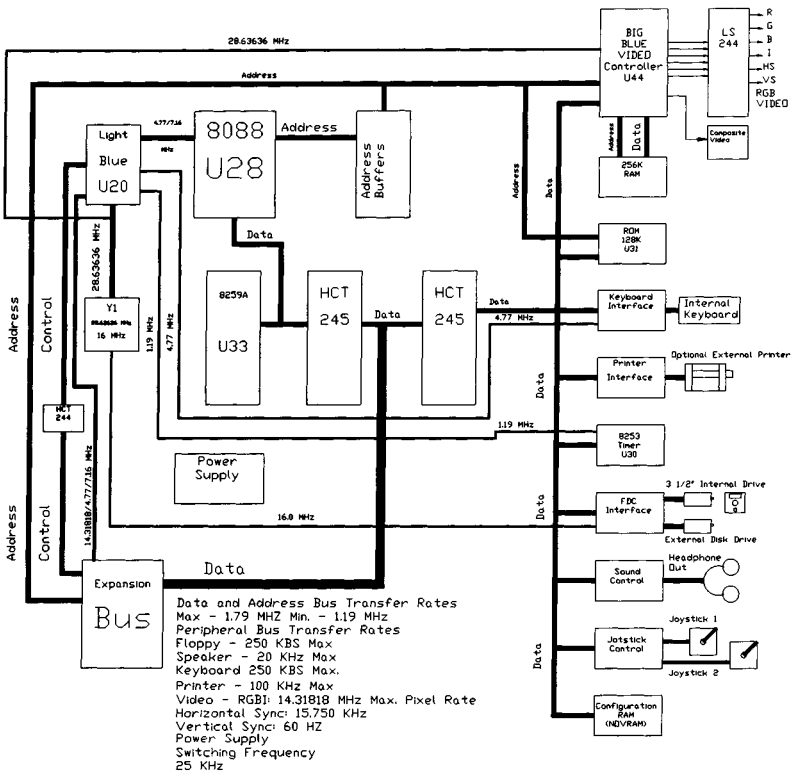


Figure 4. Main Logic Block Diagram

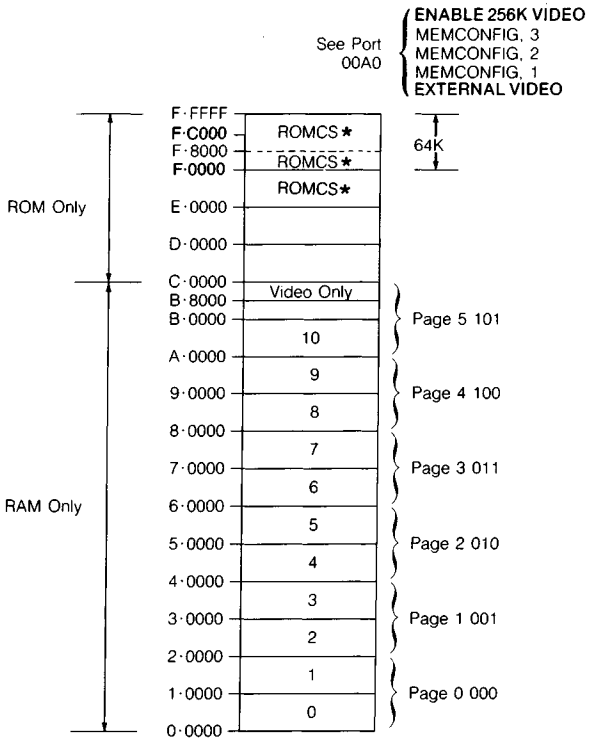


Figure 5. Memory Map

CPU Control Signal Generation

The 8088 CPU uses a 4.77 (7.16) MHz clock with a special duty cycle (4.77 → 33% high, 67% low, - 7.16 → 50% high, 50% low). This clock is produced by the Timing Control Generator. The Timing Control Generator receives a 28.63636 MHz input clock and divides it by 6 to produce 4.77 MHz CPUCLK or by 4 to produce 7.16 MHz CPUCLK, and by 24 to produce D4CLK (1.193 MHz). In addition to being used by the control signal logic, the clocks are buffered by U20 (74HCT244) for the bus signals OSCY (14 MHz), CLKY (CPU clock: 4.77/7.16 MHz). (See the Bus Interface Specification).

The RESET signals (RESET and BRESET) originate at U20 (Timing Control Generator) which synchronizes the input RSTIN*. RSTIN* originates from C132 which is discharged to 0 volts by diode CR2 when the power is off.

The READY circuit synchronizes the system "ready" signals with the CPU clock and generates the CPU input READY. If a function needs one or more "wait" states added to its access, it must set the RDYIN line low. From the main logic board, RDYIN is set low by the sound IC for 32 extra "wait states" and the video/system memory sets RDYIN low for typically one or two "wait" cycles. The READY circuit of the Timing Control Generator (U20) is operated in the non-asynchronous mode; i.e. two sequential edges of clock (a rising edge first) are required to set the READY signal true. RDYIN is pulled-up by R20.

IFL Equations

U16 Buffer Control **Checksum: FF6C**

Inputs		Outputs
PIN 1 = !mio	PIN 7 = !fdcack	PIN 15 = !disnmi
PIN 2 = !memr	PIN 8 = !ior	Pin 16 = !romcs
PIN 3 = a19	PIN 9 = !refresh	PIN 17 = !bufenb
PIN 4 = a18	PIN 11 = nmien	PIN 18 = !bufdir
PIN 5 = a17	PIN 13 = nmi	
PIN 6 = !memios	PIN 14 = !romdis	

Equations:

```
/**  Logic Equations **/

disnmi = !nmien  #  !nmi;

romcs  = memr & !refresh & a19 & a18 & a17 & !romdis;

bufenb = !memios & romcs
       # memios & fdcack;

bufdir = memr & !mio & !fdcack
       # memr & !mio & memios
       # memr & !mio & ior
       # mio & ior
       # ior & fdcack & !memios & !memr;
```

System Control Signal Generation

The Timing Control Generator (U20) provides the timing strobes required by the system. These include LIOW*, LIOR*, LMEMW*, LMEMR*, LALE, LDEN* and LIO/M*. They are buffered by U6 and become IOW*, IOR*, MEMW*, MEMR*, ALE, DEN* and IO/M*. All external devices, except the 8259A Interrupt Controller, are buffered by a HCT244 (U6) that is controlled by the DEN* signal. Since the 8259A is not buffered, the DEN* signal must remain inactive during access to the 8259A. The signals LIOW*, LIOR*, LMEMW*, LMEMR*, LALE, LDEN* and LIO/M* are synthesized 8088 status signals S0*, S1*, S2* and INTCS* (8259A chip select). See Figure 6.

Bus Specification

Specifications for the bus will include the expansion connector pin/signal assignments and the signal characteristics. Refer to the Expansion I/F Connector diagram. See Figure 7.

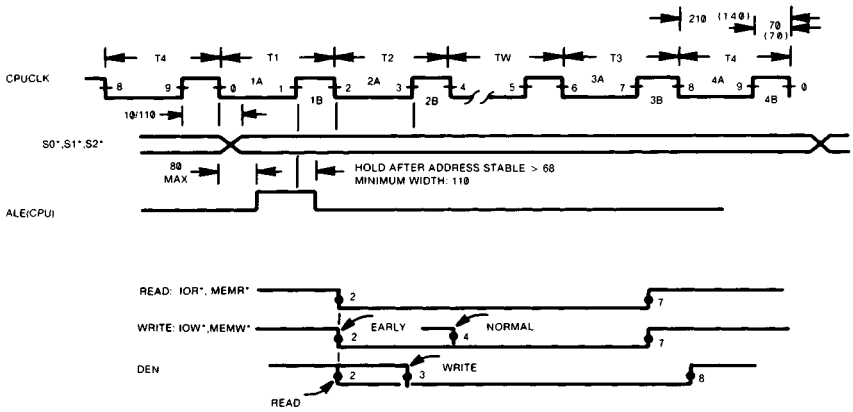


Figure 6. System Control Timing

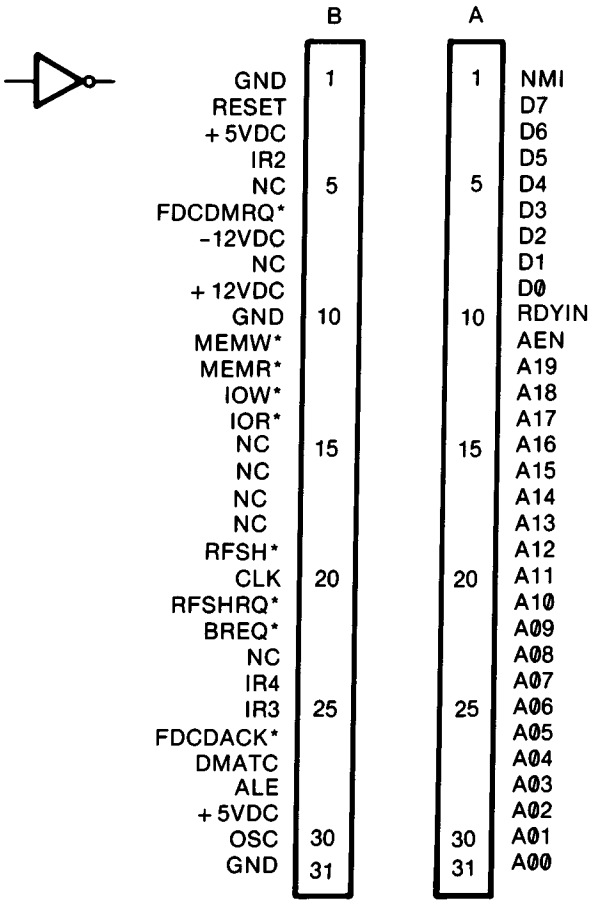


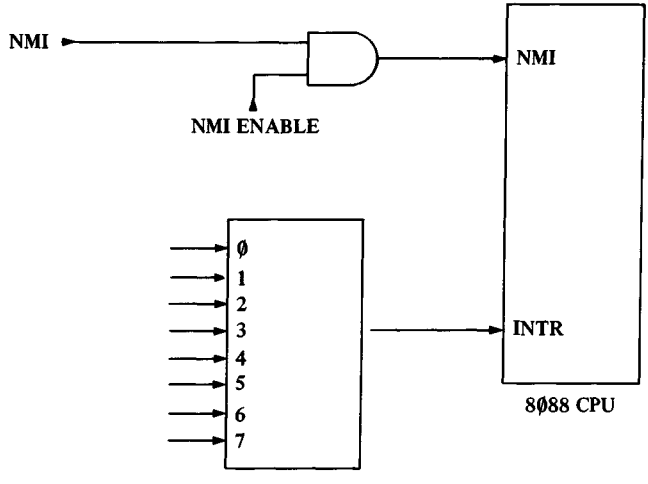
Figure 7. Expansion I/F Connector

Interrupt Function

The 8088 supports two types of interrupts: maskable (by the CPU, INT) and non-maskable (NMI). See Figure 8. The 8259A Interrupt Controller is the source of the INT for the 8088. The 8259A has eight interrupt inputs controlled through software commands. It can mask (disable) and prioritize (arrange priority) to the inputs which can generate INT. These eight interrupts are:

#0	Timer Channel 0	Software Timer
#1	Keyboard	Keyboard Code Received
#2	Hard Disk Controller	Optional Function, Interrupt on Bus
#3	Comm 2	Optional Function, Interrupt on Bus
#4	Comm 1	Optional Function, Interrupt on Bus
#5	Vertical Sync	Software Timer for Video
#6	Disk Controller, Floppy	Ready to Receive/Transmit Data
#7	Printer	Data Transmission Complete

The NMI interrupt is not maskable by the CPU but it can be enabled/disabled by hardware. The enable is at Port 00A0 Bit 7. The enable is cleared by RESET. There is no specific function assigned to NMI and it is available on the bus.



8259A INTERRUPT CONTROLLER

INTERRUPT	FUNCTION
NMI	AVAILABLE ON BUS
Ø	8253 TIMER CH Ø (REFRESH)
1	KEYBOARD
2	HARD DISK
3	SECONDARY COMM.
4	PRIMARY COMM.
5	VERTICAL SYNC.
6	FLOPPY DISK CONTROLLER
7	PARALLEL PORT

Figure 8. Interrupt Structure

Bus Interface

The interface to the main bus is divided into three parts: address/control strobes, memory data and I/O data. The address/control strobe part (A0 - A19, MEMR*, MEMW*, IOR*, IOW*) is shared by both the I/O and the memory sections. The address buffers are U23, U32 and U36. One function of the address bus is the select logic for each of the functions. U27 decodes all the I/O chip selects except those for the Video/System Memory I/O ports which are decoded by U31. The memory selects are decoded by U31 except the ROMCS*, which is decoded by U16. The I/O data transceiver is U44 with its output enable and direction control decoded by U16.

Keyboard / Timer / Sound Circuits

The Keyboard Interface consists of an 8048 CPU (U9) and a Keyboard Controller (U13), which is a Custom Gate Array. Included in U13 is an 8255 programmable peripheral interface equivalent design. It has three 8 bit parallel ports, A, B and C. Port A is configured as an input port and is used for keyboard data. Port B is configured as an output port and is used for control signals for the sound, keyboard and timer functions. Port C is split into 4 inputs, including the timer channel and #2 monitor and 4 outputs including the keyboard/multifunction interface signals.

The 8048 generates strobes to the keyboard. Data from the keyboard is received by the 8048, translated to an 8 bit asynchronous serial format, and transmitted to the Keyboard Controller. The Keyboard Controller translates this serial data into a parallel format and makes it available to the data bus. The serial data from the 8048 consists of a clock signal and a data signal. The clock consists of 8 consecutive positive pulses (signal normal state is logic low). The rising edge of each pulse is centered in the middle of each data period. The data signals consists of 8 data periods and an "end-of-character" bit. Normal state of the data signal is logic high which represents a logic 1. Thus, the data signal will change only if the data bit is a 0. The ninth and last data bit is always a 0. In the absence of a ninth clock, it will set the interrupt and busy signals. See Figure 9 for the Keyboard Timing Chart.

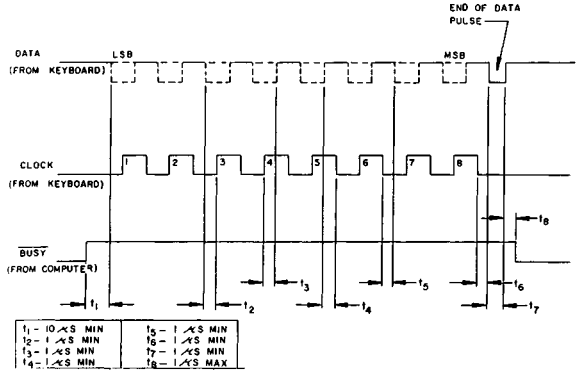


Figure 9. Keyboard Timing Chart

Timer Function

The Timer is an 8253 Timer/Counter consisting of three independent counters. The clock for all three counters is 1.1925 MHz. The gates for counters #0 and #1 are permanently "on". The gate for counter #2 is controlled by a bit of the keyboard interface (8255 Port B). The output of counter #0 is dedicated to system interrupt #0 (8259 IR0) for software timing functions. The output of counter #1 is dedicated to the REFRESH function. When the optional DMA/Memory board is installed, DMA channel #0 is used for refreshing the RAM memory. Counter #1 sets RFSHRQ* (DRQ0) every 15 micro-seconds to initiate a single "dummy" memory read. The output of counter #2 is routed to the sound circuit and into the 8255 Port C for monitoring by the CPU. See Figure 10.

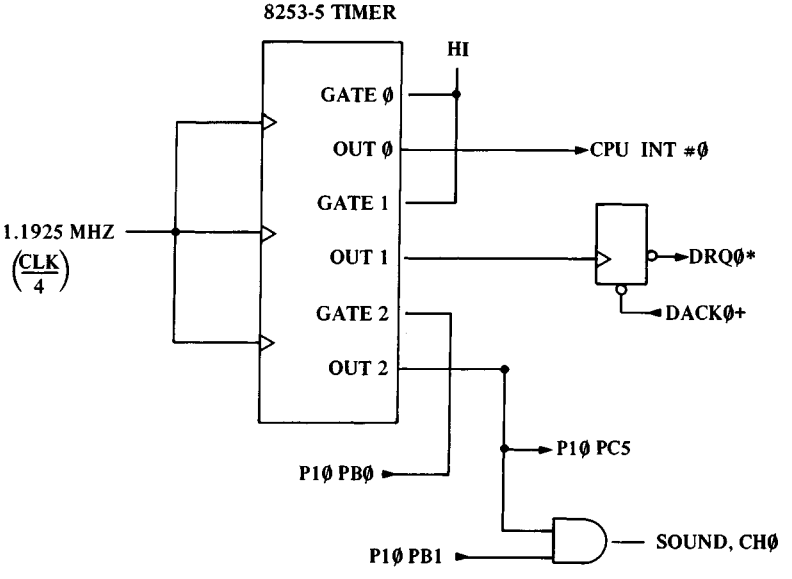
Sound Function

The sound function consists of an internal and an external sound circuit. These are directly connected to the Headphone Output via U5. The source of the sound frequencies is U19, a Complex Sound Generator. Internally, U19 has three programmable tone generators and a noise generator. The frequency and output level of each is controlled by software. The four internal generators are summed with an external input into a single output. The external source is from the 8253 counter #2 (programmable frequency and fixed amplitude). It is one of two selectable sources for the external audio out signal. This signal is intended as an input into an external earplug. The two sound frequency sources are:

1. Complex sound generator U19.

2. The 8253 counter at channel 2.

The output driver for Audio Out is U5. See Figure 11.



CHANNEL Ø: MODE Ø, INTERRUPT ON T/C
1: MODE Ø, NEGATIVE PULSE ON T/C
2: MODE 3, SQUARE WAVE OUTPUT

Figure 10. System Timer 8253-5

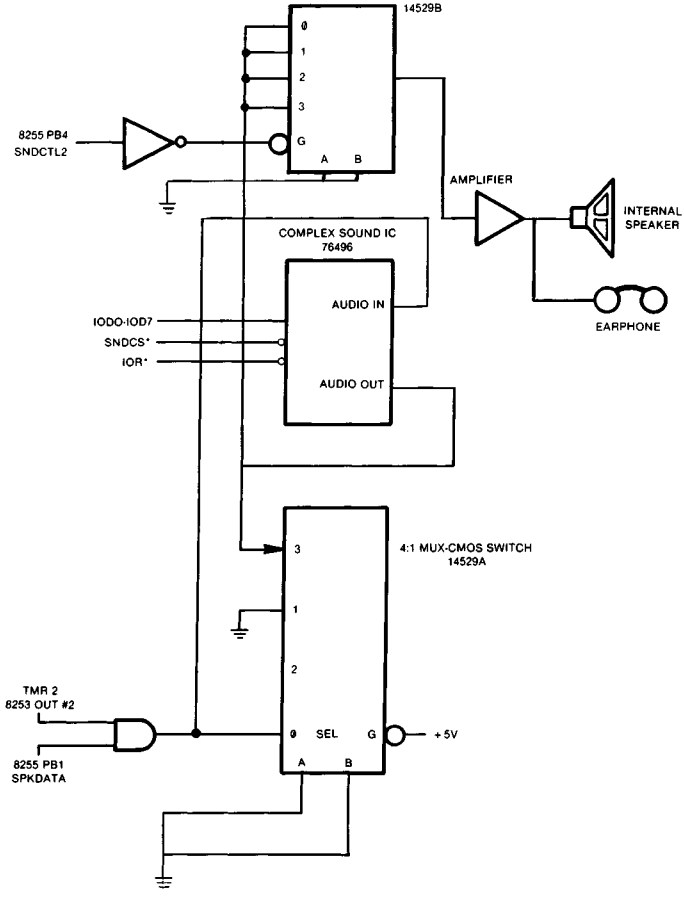


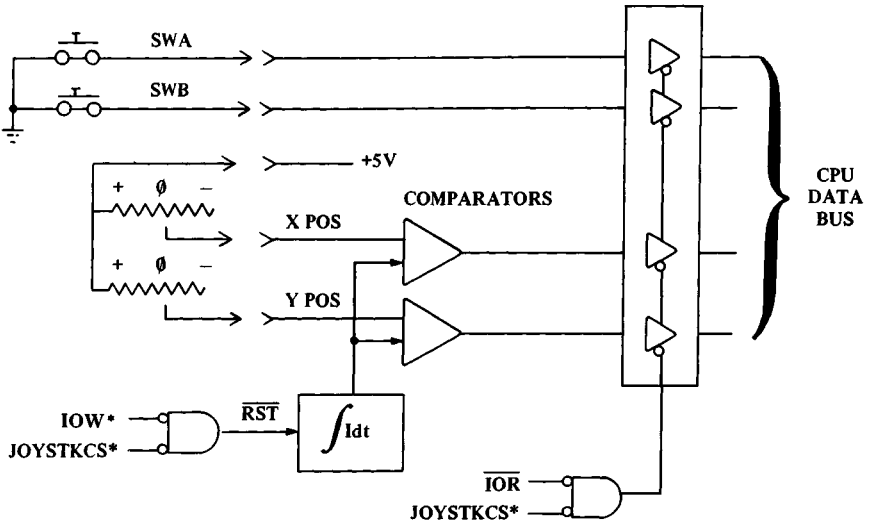
Figure 11. Sound Functional Block Diagram

Joystick Interface

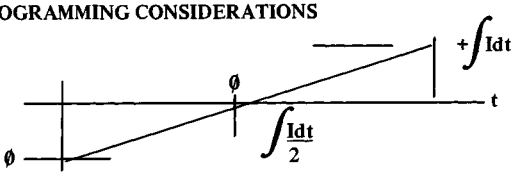
The joystick interface converts positional information from hand-held joysticks (1 or 2) into CPU data. Each joystick provides 1 or 2 push-buttons and X, Y position for a total of 4 bits each. Two joysticks can be used. The joystick handle is connected to two potentiometers mounted perpendicular to each other; one for X position, one for Y position. Through the cable, the main logic board applies +5 VDC to one side and ground to the other of the pots. The pot wiper is the position signal: a voltage between 0 and +5 VDC. This signal is applied to one input of a comparator U24. The other comparator input is the reference signal (a ramp between 0.0 to +5.0 volts.) When the position signal is equal to or greater than the reference signal, the comparator output goes true. This comparator output is the X or Y position data bit. The ramp is reset to 0.0 VDC whenever a "write" is made at Port 200/201 Hex. The IOW* signal turns on Q2, which discharges C129 to 0.0 volts. When Q2 is turned off, Q1, R22, R28, R35, and CR3 create a constant-current source that linearly charges C129 to +5.0 VDC in 1.12 milliseconds. The joystick information is "read" by the CPU at Port 200/201 Hex through U26. See Figure 12.

Printer Interface

The printer interface is totally contained in a custom Gate Array U37 and is shown in Figure 13. Functionally, the printer interface consists of an output data latch (write port 378) and accompanying input data buffer. The data written to the output port latch may be read at port 37A. The input data from the printer connector may be read back at port 378. The input buffer is for reading printer input signals (read port 379), I/O address decoding, data transceiver, and interrupt logic. The interrupt is logically connected to ACKNOWLEDGE* if interrupts are enabled (37A Bit 4).



PROGRAMMING CONSIDERATIONS



IOR's
@ REGULAR INTERVALS

ONCE TRIGGERED BY SOFTWARE THE INTERGRATOR CIRCUIT PRODUCES A PULSE THE DURATION OF WHICH IS DEPENDENT ON JOYSK POSITION.

Figure 12. Joystick I/F

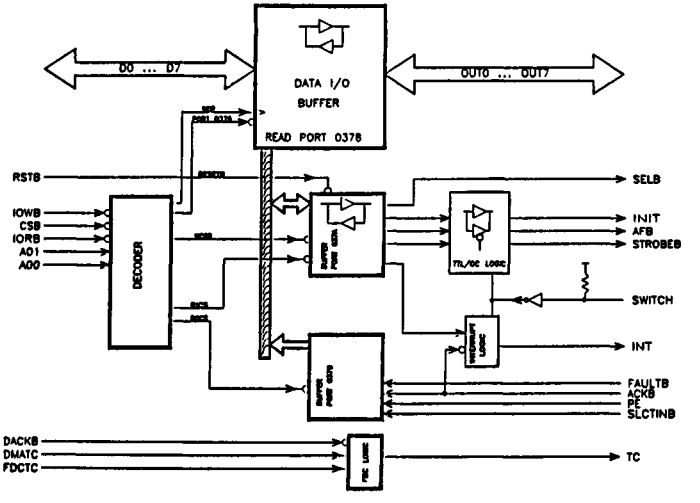


Figure 13. Printer Block Diagram

Pin Definitions of the FDSL:

Pin	Name	Type	Description
1.	CLK16M	Input	Raw Clock 16 MHz
2.	WCK	Output	Write Clock
3.	FDCCLK	Output	FDC Clock
4.	RDDATA*	Input	Serial Data From FDD
5.	RDD	Output	Serial Data From FDC
6.	RDW	Output	Read Data Window
7.	FRES/S	Input	Step Pulses to Move the Head
8.	RW*/SEEK	Input	Specifies Seek Mode When High
9.	TRK0*	Input	From FDD Indicating Head @ Track 0
10.	F/TRK0	Output	To FDC Indicating Head @ Track 0
11.	STEP*	Output	Moves Head Of FDD
13.	WRDATA*	Output	Serial Data To FDD
14.	WRE	Input	Write Enable
15.	WRD	Input	Write Data From FDC
16.	PS1	Input	Write Precompensation Status
17.	PS0	Input	Write Precompensation Status
18.	FDCDMRQ*	Output	DRQ Delayed By 1 µsec.
19.	FDCINT	Output	Interrupt Request
20.	DRQ	Input	FDC DMA Request
21.	DMA/INTE	Input	DMA Request & FDC Interrupt Enable
22.	INT+	Input	Interrupt Request Generated By FDC
23	SWITCH	Input	0 = Low Density Drive 1 = High Density Drive

Table 1.

Floppy Disk Controller Interface

The FDC interface consists of the NEC uPD765A controller and Custom FDC Support Chip (FDSL). The clocks are generated by the FDSL. The FDSL receives a raw clock of 16 MHz. The clock outputs to the FDC Controller consist of Write Clock (WCK) at 250 nsec every 2 usec, and FDC Clock (FDCCLK) at 4.00 MHz which is applied to the FDC Controller for its internal processor clock (CLK pin 19).

The FDSL receives the step signal (FRES/S) from the FDC Controller and generates the step pulses (STEP*) to the FDD to move the heads. The FDSL receives the Track 0 signal from the FDD (TRK0*) and relays it to the FDC Controller with the F/TRK0 signal.

The FDSL also handles DMA Request and Interrupt Enable (DMA/INTE) as well as Interrupt Request (INT+) generated by the FDC Controller. The FDSL receives DMA Request (DRQ) from the FDC Controller and generates a 1 usec delayed DMA Request (FDCDMRQ*) to the Expansion Bus.

The FDSL converts Serial Read Data (RDDATA*) from the FDD into Serial Read Data (RDD) and Read Data Window (RDW) and sends it on to the FDC Controller.

The FDC Controller supplies Write Enable (WRE), Serial Data (WRD) and Write Pre-compensation (PS0, PS1) to the FDSL to produce Serial Output Data (WRDATA*) to the FDD. The FDC Controller also generates the (RW*/SEEK) signal to the FDSL to put the FDC in Seek Mode. (High signal to indicate Seek Mode).

Pin Definitions for the FDSL are found in Table 1. Pin definitions for the uPD765A may be found in the Device Specifications Section.

Video System Logic

A major block of the Tandy 1000 HX is the video interface circuitry. A block diagram of the video controller circuit is shown in Figure 14. This custom part contains all of the logic necessary to generate an IBM compatible color video display. The video interface logic consists of the 84 pin custom video circuit, 8 - 64K X 4 RAMs, a 74LS244 buffer, and associated circuitry for generation of composite video.

The Tandy 1000 HX video interface circuitry controls 256K of memory. See Video System Memory Map, Figure 15. This RAM is shared by the CPU and the video. Normally, the video only requires 16K or 32K for the video screen and the remainder of the 256K is available for system memory uses.

The Tandy 1000 HX video interface custom circuit is composed of a 6845 equivalent design, dynamic RAM address generation/ timing (see Figure 16.), and video attribute controller logic.

Normal functioning of the video interface custom circuit is as follows: After the 6845 is programmed with a correct set of operating values (see Table 2), the address inputs to the dynamic RAMs are generated by a 4:1 multiplexer. This MUX switches between video (6845) addresses and CPU addresses as well as between row and column addresses. In addition, the video interface chip provides the RAM timing signals and generates a wait signal to CPU for proper synchronization with the video RAM access cycles.

The outputs from the RAM chips are only connected to the video interface custom circuit, so all CPU read/write operations are buffered by this part. During a normal display cycle, video data from the RAM chips is first latched in the Video Attribute latch and the Video Character latch. The video interface requires a memory organization of 64K X 16 and will latch 16 bits of memory during each access to RAM. From the output of the two latches, the data is supplied to the character ROM for the Alpha modes or to the shift registers for graphics modes. A final 2:1 MUX is used to switch between foreground or background in the alpha mode.

From the 2:1 MUX, the RGBI data is combined with the PC color select data and latched in the Pre-Palette latch. This latch synchronizes the RGBI data before it is used to address the palette.

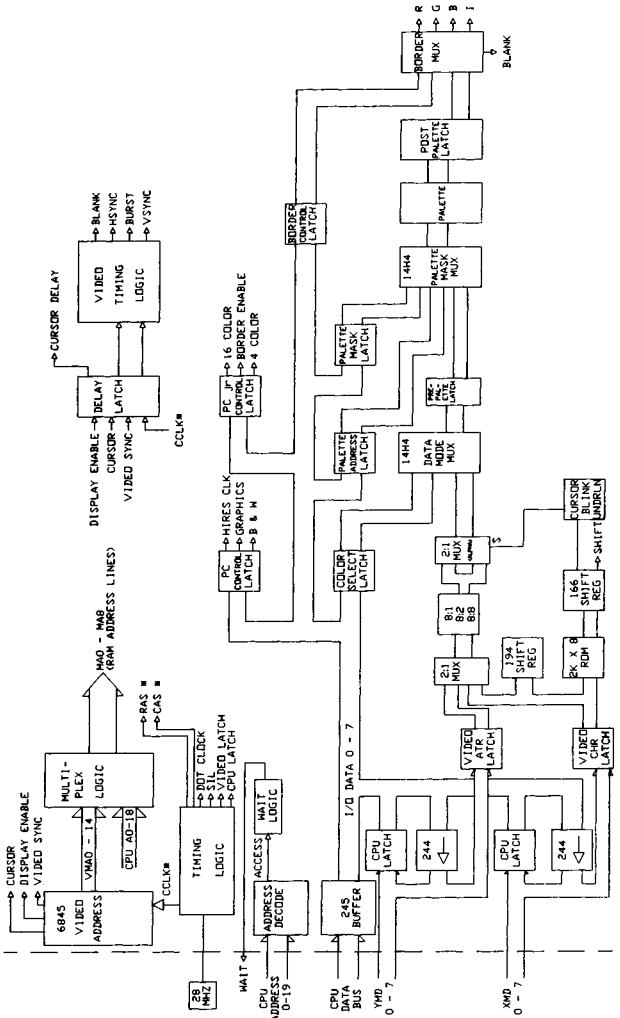


Figure 14. Video Controller Block Diagram

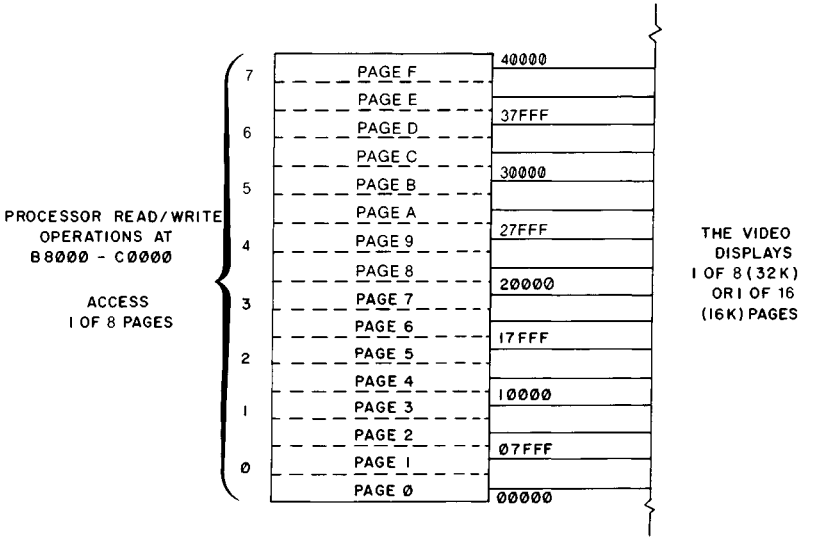


Figure 15. Video System Memory Map

Main System Board Ram Timing Specification

AC Operating Conditions and Characteristics

Parameter	Symbol	Min.	Max.	Units
Random Read or Write Cycle Time	tRC	279	--	ns
Read Write Cycle Time	tRWC	279	--	ns
Access Time from Row Address Strobe	tRAC	--	200	ns
Access Time from Column Address	tCAC	--	100	ns
Output Buffer and Turn-Off Delay	tOFF	0	30	ns
Row Address Strobe Precharge Time	tRP	100	--	ns
Row Address Strobe Pulse Width	tRASl	170	--	ns
Column Address Strobe Pulse Width	tCAS	130	--	ns
Row Address Setup Time	tASR	0	--	ns
Row Address Hold Time	tRAH	20	--	ns
Column Address Setup Time	tASC	0	--	ns
Column Address Hold Time	tCAH	35	--	ns
Transition Time (Rise and Fall)	tT	--	50	ns
Read Command Setup Time	tRCS	0	--	ns
Read Command Hold Time	tRCH	0	--	ns
Read Command Hold Time Referenced to RAS	tRRH	0	--	ns
Write Command Hold Time	tWCH	35	--	ns
Write Command Hold Time Referenced to RAS	tWCR	95	--	ns
Write Command Pulse Width	tWP	35	--	ns
Write Command to Row Strobe Lead Time	tRWL	45	--	ns
Write Command to Column Strobe Lead Time	tCWL	45	--	ns
Data in Setup Time	tDS	0		ns
Data in Hold Time	tDH	35	--	ns
Data in Hold Time Referenced to RAS	tDHR	95	--	ns
Column to Row Strobe Precharge Time	tCRP	0	--	ns
RAS Hold Time	tRSH	85	--	ns
Refresh Period	tRFSH	--	2.0	ns
WRITE Command Setup Time	tWCS	0	--	ns
CAS to WRITE Delay	tCWD	45	--	ns
RAS to WRITE Delay	tRWD	120	--	ns
CAS Hold Time	tCSH	200	--	ns

Figure 16. Main System Board RAM Timing Specification

PROGRAMMING TABLE FOR THE 6845 All Values in Hex (Decimal)

Register Address	40 x 25 Alpha	80 x 25 Alpha	Low Res. Graphics	High Res. Graphics	40 x 25 Alpha	80 x 25 Alpha	Low Res Graphics	High Res Graphics
	Monitor Mode				TV Mode			
00 Horizontal Total	38 (56)	71 (113)	38 (56)	71 (113)	38 (56)	71 (113)	38 (56)	71 (113)
01 Horizontal Displayed	28 (40)	50 (80)	28 (40)	50 (80)	28 (40)	50 (80)	28 (40)	50 (80)
02 Horizontal Sync Position	2D (45)	59 (89)	2D (45)	59 (89)	2D (45)	59 (89)	2D (45)	59 (89)
03 Horizontal Sync Width	08 (8)	10 (16)	08 (8)	10 (16)	08 (8)	10 (16)	08 (8)	10 (16)
04 Vertical Total	1C (28)	1C (28)	7F (127)	3F (63)	1F (31)	1F (31)	7F (127)	3F (63)
05 Vertical Total Adjust	01 (1)	01 (1)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)
06 Vertical Displayed	19 (25)	19 (25)	64 (100)	32 (50)	19 (25)	19 (25)	64 (100)	32 (50)
07 Vertical Sync Position	1A (26)	1A (26)	70 (112)	38 (56)	1C (28)	1C (28)	70 (112)	38 (56)
08 Interlace Mode	02 (2)	02 (2)	02 (2)	02 (2)	02 (2)	02 (2)	02 (2)	02 (2)
09 Max Scan Line Address	08 (8)	08 (8)	01 (1)	03 (3)	07 (7)	07 (7)	01 (1)	03 (3)
10 Cursor Start	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)
11 Cursor End	07 (7)	07 (7)	07 (7)	07 (7)	07 (7)	07 (7)	07 (7)	07 (7)
12 Start Address (High)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)
13 Start Address (Low)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)

Table 2

The palette mask MUX is used to switch between incoming RGBI data and the palette address register. During a CPU write to the palette, this address register selects one of the 16 palette locations. Also, the palette mask MUX allows any of the input RGBI bits to be set to zero.

The palette allows the 16 colors to be remapped in any desired organization. Normally the pallete is set for a 1:1 mapping (red = red, blue = blue, etc.) for PC compatibility. However, instantly changing the on-screen colors is a very powerful tool for animation or graphics programs.

After the palette, the RGBI data is resynchronized in the Post Palette register. The final logic before the RGBI data is buffered off the chip is the Border MUX. This MUX allows the Border to be replaced with any color selected by the border color latch. This latch is normally disabled in PC modes, but it is used in all PCjr modes.

I/O MAP SUMMARY

Block	Usage	Function
0000-001F	0000-000F	Optional DMA Function
0020-003F	0020-0021	Interrupt Controller
0040-005F	0040-0043	Timer
0060-007F	0060-0063	PIO Function
0080-009F	0080-0083	Optional DMA Page Register
00A0-00BF	00A0	NMI Mask Register
00C0-00DF	00C0-00C1	Sound Generator
00E0-01FF		Reserved
0200-020F	0200-0201	Joystick Interface
0210-031F		Reserved
0320-032F		Reserved Hard Disk
0330-036F		Not Assigned
0370-037F	0378-037B	Printer
0380-03CF		Not Used
03D0-03DF	All	System Video
03E0-03EF		Reserved
03F0-03FF	03F1,03F2,F4,F5 03F8-03FF	Floppy Disk Controller Optional COM Port
0400-FFFF		Not Usable

Address	Description
0000	DMA Controller IOW* = 0: Channel 0 Base and Current Address Internal Flip/Flop = 0: Write A0-A7 Internal Flip/Flop = 1: Write A8-A15 IOR* = 0: Channel 0 Current Address Internal Flip/Flop = 0: Read A0-A7 Internal Flip/Flop = 1: Read A8-A15
0001	DMA Controller IOW* = 0: Channel 0 Base and Current Word Count Internal Flip/Flop = 0: Write W0-W7 Internal Flip/Flop = 1: Write W8-W15 IOR* = 0: Channel 0 Current Word Count Internal Flip/Flop = 0: Read W0-W7 Internal Flip/Flop = 1: Read W8-W15
0002	DMA Controller IOW* = 0: Channel 1 Base and Current Address Internal Flip/Flop = 0: Write A0-A7 Internal Flip/Flop = 1: Write A8-A15 IOR* = 0: Channel 1 Current Address Internal Flip/Flop = 0: Read A0-A7 Internal Flip/Flop = 1: Read A8-A15

Address	Description
0003	DMA Controller IOW* = 0: Channel 1 Base and Current Word Count Internal Flip/Flop = 0: Write W0-W7 Internal Flip/Flop = 1: Write A8-A15 IOR* = 0: Channel 1 Current Word Count Internal Flip/Flop = 0: Read W0-W7 Internal Flip/Flop = 1: Read W8-W15
0004	DMA Controller IOW* = 0: Channel 2 Base and Current Address Internal Flip/Flop = 0: Write A0-A7 Internal Flip/Flop = 1: Write A8-A15 IOR* = 0: Channel 2 Current Address Internal Flip/Flop = 0: Read A0-A7 Internal Flip/Flop = 1: Read A8-A15
0005	DMA Controller IOW* = 0: Channel 2 Base and Current Word Count Internal Flip/Flop = 0: Write W0-W7 Internal Flip/Flop = 1: Write W8-W15 IOR* = 0: Channel 2 Current Word Count Internal Flip/Flop = 0: Read W0-W7 Internal Flip/Flop = 1: Read W8-W15
0006	DMA Controller IOW* = 0: Channel 3 Base and Current Address Internal Flip/Flop = 0: Write A0-A7 Internal Flip/Flop = 1: Write A8-A15 IOR* = 0: Channel 3 Current Address Internal Flip/Flop = 0: Read A0-A7 Internal Flip/Flop = 1: Read A8-A15
0007	DMA Controller IOW* = 0: Channel 3 Base and Current Word Count Internal Flip/Flop = 0: Write W0-W7 Internal Flip/Flop = 1: Write W8-W15 IOR* = 0: Channel 3 Current Word Count Internal Flip/Flop = 0: Read W0-W7 Internal Flip/Flop = 1: Read W8-W15

0008	DMA Controller IOW* = 0, Write Command Register
Bit	**Description**
0	0 = Memory to Memory Disable 1 = Memory to Memory Enable
1	0 = Channel 0 Address Hold Disable 1 = Channel 0 Address Hold Enable X If bit 0 = 0
2	0 = Controller enable 1 = Controller disable
3	0 = Normal timing 1 = Compressed timing X If bit 0 = 1
4	0 = Fixed priority 1 = Rotating priority
5	0 = Late write selection 1 = Extended write selection X = If bit 3 = 1
6	0 = DREQ sense active high 1 = DREQ sense active low
7	0 = DACK sense active low 1 = DACK sense active high
	IOR* = 0, Read Status Register
Bit	**Description**
0	1 = Channel 0 has reached TC
1	1 = Channel 1 has reached TC
2	1 = Channel 2 has reached TC
3	1 = Channel 3 has reached TC
4	1 = Channel 0 Request
5	1 = Channel 1 Request
6	1 = Channel 2 Request
7	1 = Channel 3 Request
0009	DMA Controller IOW* = 0, Write Request Register
Bit	**Description**
0-1	Bit1 Bit0 0 0 Select channel 0 0 1 Select channel 1 1 0 Select channel 2 1 1 Select channel 3
2	0 Reset request bit 1 Set request bit
3-7	Don't Care IOR* = 0, Illegal

000A	DMA Controller IOW* = 0, Write Single Mask Register		
Bit	**Description**		
0-1	Bit1	Bit0	
	0	0	Select channel 0 mask bit
	0	1	Select channel 1 mask bit
	1	0	Select channel 2 mask bit
	1	1	Select channel 3 mask bit
2	0	Clear mask bit (Disable Channel)	
	1	Set mask bit (Disable Channel)	
3-7	Don't care IOR* = 0, Illegal		
000B	DMA Controller IOW* = 0, Write Mode Register		
Bit	**Description**		
0-1	Bit1	Bit0	
	0	0	Channel 0 select
	0	1	Channel 1 select
	1	0	Channel 2 select
	1	1	Channel 3 select
2-3	Bit3	Bit2	
	0	0	Verify transfer
	0	1	Write transfer to memory
	1	0	Read transfer to memory
	1	1	Illegal
	X	If bits 6 and 7 = 11	
4	0	Autoinitialization disable	
	1	Autoinitialization enable	
5	0	Address increment select	
	1	Address decrement select	
6-7	Bit7	Bit6	
	0	0	Demand mode select
	0	1	Single mode select
	1	0	Block mode select
	1	1	Cascade mode select
	IOR* = 0, Illegal		
000C	DMA Controller IOW* = 0, Clear Byte Pointer Flip/Flop IOR* = 0, Illegal		

000D	DMA Controller IOW* = 0, Master Clear IOR* = 0, Read Temporary Register
000E	DMA Controller IOW* = 0, Clear Mask Register IOR* = 0, Illegal
000F	DMA Controller IOW* = 0, Write all Mask Register Bits

Bit	Description
0	0 = Clear channel 0 mask bit (Enable) 1 = Set channel 0 mask bit (Disable)
1	0 = Clear channel 1 mask bit (Enable) 1 = Set channel 1 mask bit (Disable)
2	0 = Clear channel 2 mask bit (Enable) 1 = Set channel 2 mask bit (Disable)
3	0 = Clear channel 3 mask bit (Enable) 1 = Set channel 3 mask bit (Disable)
4-7	Don't care IOR* = Illegal

0010 - 001F	Not Used

Address	Description
0020	8259A Interrupt Controller

Note: Initialization Words are setup by the operating system and are generally not to be changed. Writing an initialization word may cancel pending interrupts.

Bit4 = 1: INITIALIZATION COMMAND WORD 1

Bit0 = 0: ICW4 needed
= 1: ICW4 not needed
Bit1 = 0: Cascade Mode
= 1: Single
Bit2 = Not used
Bit3 = 0: Edge Triggered Mode
= 1: Level Triggered Mode
when the SL bit is active
Bit5 - 7: Not Used

```
Bit4 = 0 &          OPERATION CONTROL WORD 2
Bit3 = 0            Bit0 - 2:  Determine the interrupt level acted on
                               when the SL bit is active

                               Interrupt Level = 0 1 2 3 4 5 6 7
                                    Bit0 (L0):   0 1 0 1 0 1 0 1
                                    Bit1 (L1):   0 0 1 1 0 0 1 1
                                    Bit2 (L2):   0 0 0 0 1 1 1 1

                    Bit5 - 7   Control Rotate and End of Interrupt
                                modes

B7 B6 B5
 0  0  1   Non-specific EOI command                    End of Interrupt
 0  1  1   Specific EOI command                        End of Interest
 1  0  1   Rotate on non-specific EOI command         Automatic Rotation
 1  0  0   Rotate in Automatic EOI Mode (set)        Automatic Rotation
 0  0  0   Rotate in Automatic EOI Mode (clear)      Automatic Rotation
 1  1  1   *Rotate on Specific EOI command          Specific Rotation
 1  1  0   *Set priority command                     Specific Rotation
 0  1  0   No operation

  *L0 - L2 are used

Bit4 = 0 &          OPERATION CONTROL WORD 3
Bit3 = 1            Bit0 - 1:
                    Bit1 Bit0- Read Register Command
                      0    0 - No Action
                      0    1 - No Action
                      1    0 - Read IR Register on next IOR* Pulse
                      1    1 - Read IS Register on next IOR* Pulse

                    Bit2 = 0:  No Poll Command
                         = 1:  Poll Command

                    Bit5 - 6:

                    Bit6 Bit5- Special Mask Mode
                      0    0 - No Action
                      0    1 - No Action
                      1    0 - Reset Special Mask
                      1    1 - Set Special Mask

                    Bit7 = 0
```

0021 8259A Interrupt Controller

INITIALIZATION CONTROL WORD 2
Bit0 - 7: Not Used
Bit3 - 7: T3 - T7 of Interrupt Vector Address
(8086/8088 Mode)

INITIALIZATION CONTROL WORD 3 (Master Device)
Bit0 - 7: =1 Indicated IR input has a slave
=0 Indicated IR input does not have a slave

INITIALIZATION CONTROL WORD 3 (Slave Device)
Bit0 - 2 = IDO - 2

Bit0	Bit1	Bit2	-	Slave ID #
0	0	0	-	0
0	0	1	-	1
0	1	0	-	2
0	1	1	-	3
1	0	0	-	4
1	0	1	-	5
1	1	0	-	6
1	1	1	-	7

Bit3 - 7 = 0 (Not Used)

INITIALIZATION CONTROL WORD 4
Bit0: Type of Processor
=0 MCS-80/85 Mode
=1 8086/8088 Mode
Bit1: Type of End Of Interrupt
=0 Normal EOI
=1 Auto EOI
Bit2 - 3: Buffering Mode

Bit3	Bit2	
0	X	Non-buffered Mode
1	0	Buffered Mode/Slave
1	1	Buffered Mode/Master

Bit4: Nesting Mode
=0 Not Special Fully Nested Mode
=1 Special Fully Nested Mode
Bit5 - 7: =0 (Not Used)

OPERATION CONTROL WORD 1 (IOR*/IOW*)
Bit0 - 7: Interrupt Mask for IRQ0 - IRQ7
=0 Mask Reset (Enable)
=1 Mask Set (Disable)

NOTE: Peripherals Requesting an interrupt service must generate a low to high edge and then remain at a logic high until service is acknowledged. Failure to do so will result in a Default Service for IRQ7.

```
0022-003F          Not Used

Address            Description
0040/0044          8253-5 Timer
                   IOW* = 0:  Load Counter No. 0
                   IOR* = 0:  Read Counter No. 0
0041/0045          8253-5 Timer
                   IOW* = 0:  Load Counter No. 1
                   IOR* = 0:  Read Counter No. 1
Address            Description
0040/0044          8253-5 Timer
                   IOW* = 0:  Load Counter No. 0
                   IOR* = 0:  Read Counter No. 0
0041/0045          8253-5 Timer
                   IOW* = 0:  Load Counter No. 1
                   IOR* = 0:  Read Counter No. 1
0042/0046          8253-5 Timer
                   IOW* = 0:  Load Counter No. 2
                   IOR* = 0:  Read Counter No. 2
0043/0047          8253-5 Timer
                   IOW* = 0:  Write Mode Word
                        Control Word Format
                        Bit0:  BCD
                          = 0:  BCD Counter (4 Decades)
                          = 1:  Binary Counter 16 bits
                        BIT1 - 3:  Mode Selection
                         Bit3 Bit2 Bit1
                          0     0    0     Mode 0
                          0     0    0     Mode 1
                          X     1    0     Mode 2
                          X     1    1     Mode 3
                          1     0    0     Mode 4
                          1     0    1     Mode 5
                        BIT4 - 5:    Read/Load
                         Bit5 Bit4
                          0    0     Counter Latching Operation
                          0    1     Read/Load LSB only
                          1    0     Read/Load MSB only
                          1    1     Read/Load LSB first, then MSB
                        BIT6 - 7:  Select Counter
                         Bit7 Bit6
                          0    0     Select Counter 0
                          0    1     Select Counter 1
                          1    0     Select Counter 2
                          1    1     Illegal
                   IOR* = 0:  No-Operation 3-State
0048-005F          Not Used
```

0060 PORT A / KEYBOARD INTERFACE CONTROL PORTS (READ ONLY)

BIT	Description
0	Keyboard Bit 0-LSB
1	Keyboard Bit 1
2	Keyboard Bit 2
3	Keyboard Bit 3
4	Keyboard Bit 4
5	Keyboard Bit 5
6	Keyboard Bit 6
7	Keyboard Bit 7-MSB

0061 PORT B - READ or WRITE

BIT	Description
0	1 = 8253 Gate #2 Enable
1	1 = Speaker Data Out Enable
2	Not Used
3	Not Used
4	1 = Disable Internal Speaker (Sound Control 2)
5	0 = Not Used
6	0 = Not Used
7	1 = Keyboard Clear

0062 PORT C - READ/WRITE: Bits 0-3; READ ONLY: BITS 4-7

BIT	Description
0	(Output) Not Used
1	(Output) Not Used
2	(Output) Not Used
3	(Output) CPU Clock Rate 0 = 4.77 MHz (PC Compatible Rate) 1 = 7.16 MHz (Default by Boot ROM)
4	EEPROM Serial Data Read
5	8253 Out #2
6	Monochrome Mode 0 = Color Monitor 1 = (Not Supported)
7	0 = Reserved

0063-007F Not Used

Address	Description
0080	DMA Page Reg. (Not Used)

0081	WRITE ONLY
Address	**Description**
Bit 0	DMA Ch 2 Address A16
Bit 1	DMA Ch 2 Address A17
Bit 2	DMA Ch 2 Address A18
Bit 3	DMA Ch 2 Address A19
Bit 4	Not Used
Bit 5	Not Used
Bit 6	Not Used
Bit 7	Not Used

0082	WRITE ONLY
Address	**Description**
Bit 0	DMA Ch 3 Address A16
Bit 1	DMA Ch 3 Address A17
Bit 2	DMA Ch 3 Address A18
Bit 3	DMA Ch 3 Address A19
Bit 4	Not Used
Bit 5	Not Used
Bit 6	Not Used
Bit 7	Not Used

0083	WRITE ONLY
Address	**Description**
Bit 0	DMA Ch 0 - 1 Address A16
Bit 1	DMA Ch 0 - 1 Address A17
Bit 2	DMA Ch 0 - 1 Address A18
Bit 3	DMA Ch 0 - 1 Address A19
Bit 4	Not Used
Bit 5	Not Used
Bit 6	Not Used
Bit 7	Not Used

0084-008F	Not Used

00A0-00A7	NMI Mask Register, Write only
Bit	**Description**
0	External Video 0 = Normal Operation 1 = All Video Addresses and Ports are Disabled
1	MEMCONFIG 1 - A17 128K SW
2	MEMCONFIG 2 - A18 256K SW
3	MEMCONFIG 3 - A19 512K SW
4	"1" Enable 256K of Video RAM
5	Not Used
6	Not Used
7	1 = Enable NMI 0 = Disabled

BIT 4 256K Enable	BIT 3	BIT 2	BIT 1	MEMORY START	MEMORY LENGTH	MEMORY RANGE
0	0	0	0	0 0000	128K	0 0000-1 FFFF
0	0	0	1	2 0000	128K	2 0000-3 FFFF
0	0	1	0	4 0000	128K	4 0000-5 FFFF
0	0	1	1	6 0000	128K	6 0000-7 FFFF
0	1	0	0	8 0000	128K	8 0000-9 FFFF
1	0	0	1	0 0000	256K	0 0000-3 FFFF
1	0	1	0	2 0000	256K	2 0000-5 FFFF
1	0	1	0	4 0000	256K	4 0000-7 FFFF
1	1	0	0	6 0000	256K	6 0000-9 FFFF

NOTE: To turn off on-board video, be sure Port AOH, Data Bit 0 is a "1" AND Video Array Register 3 (Selected by writing 03 into 3DAH) Data Bit 0 (Write to Port 3DEH) must be = "0" to disable 3B8H and 3BAH.

00A8 - 00AF Not Used

Address	Description
00C0-00C7	Sound SN76496

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bitl	Bit0	
= 1	0	0	0	F6	F7	F8	F9	Update Tone Frequency 1
= 0	X	F0	F1	F2	F3	F4	F5	Additional Frequency Data
= 1	0	0	1	A0	Al	A2	A3	Update Tone Attenuation 1
= 1	0	1	0	F6	F7	F8	F9	Update Tone Frequency 2
= 0	X	F0	F1	F2	F3	F4	F5	Additional Frequency Data
= 1	0	1	1	A0	Al	A2	A3	Update Tone Attenuation 2
= 1	1	0	0	F6	F7	F8	F9	Update Tone Frequency 3
= 0	X	F0	F1	F2	F3	F4	F5	Additional Frequency Data
= 1	1	0	1	A0	Al	A2	A3	Update Tone Attenuation 3
= 1	1	1	0	X	FB	NFO	NFI	Update Noise Control
= 1	1	1	1	AO	Al	A2	A3	Update Noise Attenuation

00C8-00DF Not Used
00E0-01FF Reserved
WRITE (IOW*)
0200 - 0207 Joystick
Clear (Resets Integrator to Zero)
0208 - 020F Not Used

0201 READ — R = Right Joystick, L = Left Joystick

Bit	Description
0	R - X Horizontal Position
1	R - Y Vertical Position
2	L - X Horizontal Position
3	L - Y Vertical Position
4	R Button #1 (Logic 0 = Button Depressed)
5	R Button #2 (Logic 0 = Button Depressed)
6	L Button #1 (Logic 0 = Button Depressed)
7	L Button #2 (Logic 0 = Button Depressed)

Addresses

0370 - 0377 — Not Used

0378 — Printer - Data Latch

Bit	Description
0	Data Bit 0 - LSB
1	Data Bit 1 -
2	Data Bit 2 -
3	Data Bit 3 -
4	Data Bit 4 -
5	Data Bit 5 -
6	Data Bit 6 -
7	Data Bit 7 - MSB

0379 — Printer - Read Status

Bit	Description
0	Not Used
1	Not Used
2	Not Used
3	0 = Error
4	1 = Printer Select
5	0 = End of Form
6	0 = Acknowledge
7	0 = Busy

037A (037E) — Printer - Control Latch

Bit	Description
0	0 = Strobe
1	0 = Auto FD XT
2	0 = Initialize
3	0 = Select Printer
4	1 = Enable Interrupt
5	0 = Enable Output Data
6	Not Used
7	Not Used

```
037B            Not Used
037C            D0 - Serial Data Write
                D1 - EEPROM Chip Enable
                D2 - Serial Data Clock
037D - 03D3     Not Used

03D4            6845 Address Register
03D5            6845 Data Register
03D6            Not Used
03D7            Not Used

03D8            Mode Select Register
Bit 0           High Resolution Clock
                  =0:  Selects 40 by 25 Alphanumeric Mode
                  =1:  Selects 80 by 25 Alphanumeric Mode
Bit 1           Graphics Select
                  =0:  Selects Alphanumeric Mode
                  =1:  Selects 320 by 200 Graphics Mode
Bit 2           Black and White
                  =0:  Selects Color Mode
                  =1:  Selects Black and White Mode
Bit 3           Video Enable
                  =0:  Disables Video Signal
                  =1:  Enables Video Signal
Bit 4           640 Dot Graphics
                  =0:  Disables 640 by 200 B&W Graphics Mode
                  =1:  Enables 640 by 200 B&W Graphics Mode
Bit 5           Blink Enable
                  =0:  Disables Blinking
                  =1:  Enables Blinking

03D9            Color Select Register
Bit 0           Background Blue
Bit 1           Background Green
Bit 2           Background Red
Bit 3           Background Intensity
Bit 4           Foreground Intensity
Bit 5           Color Select

03DA, 03DE      Write Video Array Address & Read Status (3DA)
                Write Video Array Data (3DE)
```

READ (3DA)		WRITE (3DE)
00 Bit 0	Display Inactive	Not Used
00 Bit 1	Light Pen Set	Not Used
00 Bit 2	Light Switch Status	Not Used
00 Bit 3	Vertical Retrace	Not Used
00 Bit 4	Not Used	Not Used
01 Bit 0		Palette Mask 0
01 Bit 1		Palette Mask 1
01 Bit 2		Palette Mask 2
01 Bit 3		Palette Mask 3
02 Bit 0		Border Blue
02 Bit 1		Border Green
02 Bit 2		Border Red
02 Bit 3		Border Intensity
02 Bit 5		Reserved = 0
03 Bit 0		Mono Enable = "1"
03 Bit 1		Reserved = 0
03 Bit 2		Border Enable
03 Bit 3		4-Color High Resolution
03 Bit 4		16 Color Mode
03 Bit 5		Extra Video Mode
10-1F Bit 0		Palette Blue
10-1F Bit 1		Palette Green
10-1F Bit 2		Palette Red
10-1F Bit 3		Palette Intensity
Bits 4 - 7		Not Used

03DB	Clear Light Pen Latch (Not Used on Tandy 1000 HX)
03DC	Preset Light Pen Latch (Not Used on Tandy 1000 HX)

03DD Extended Ram Page Register - CPU Relative

Bit	Description
0	Extended Addressing Modes
1	Not Used
2	Not Used
3	CRT Video Page Address "17"
4	CRT Video Page Address "18"
5	CPU Page Address "17"
6	CPU Page Address "18"
7	Select 64K or 256K Ram

```
03DF                CRT Processor Page Register
                    - Video Mem Relative
 Bit 0              A14                 CRT Page 0
 Bit 1              A15                 CRT Page 1
 Bit 2              A16                 CRT Page 2
 Bit 3              A14                 Processor Page 0
 Bit 4              A15                 Processor Page 1
 Bit 5              A16                 Processor Page 2
 Bit 6                                  Video Address Mode 0
 Bit 7                                  Video Address Mode 1

03F1                D0 - Not Used
                    D1 - = 1 DSO = DSO
                         = 0 DSO = DS2
                    D2 - = 1 (3 Drive Selects)
03F2, 3F0, 3F3      DOR Register (Write Only)
                    Bit0 - 1:  Drive Select
                      Bit1 Bit0
                       0    0          Drive Select A*
                       0    1          Drive Select B*
                       1    0          Drive Select C*
                    Bit2:  0 = FDC Reset
                    Bit3:  1 = Enable DMA Req/Interrupt
                    Bit4:  1 = Drive A Motor On
                    Bit5:  1 = Drive B Motor On
                    Bit6:  1 = FDC Terminal Count
                    Bit7:  Not Used

03F4, 3F6           FDC - Status (Read Only)
                        - See FDC Specification
03F5, 3F7           FDC - Data (R/W) - See FDC Specification
03F8 - 03FF         COM 1 Port

For Ports 3F0 - 3F7, the following general conditions apply:
                    A1 = Don't Care
                    For DOR, A2 = 0
                    For FDC, A2 = 1
```

DATA	IBM PC 0062 -- PORT C -- READ ONLY	IBM PCjr 0062 -- PORT C -- READ ONLY	TANDY 1000 HX 0062 -- PORT C --
BIT 0	CONFIG SW16 OR (R/W)	1 = KEYBOARD LATCHED	(OUT) NOT USED
	CONFIG SW12 (R/W)		
	SEE PORT 0061, BIT 2 (R/W)		
BIT 1	CONFIG SW15 (R/W)	0 = INTERNAL MODEM INSTALLED	(OUT) NOT USED
BIT 2	CONFIG SW14 (R/W)	0 = DISKETTE DRIVE INSTALLED	(OUT) NOT USED
BIT 3	CONFIG SW13 (R/W)	0 = 64K RAM EXPANSION	FAST (0=STD OPERATION) read/write "0"=4.77MHz "1"=7.16MHz
		INSTALLED	read/write "0"=4.77MHz "1"=7.16MHz
BIT 4	CASSETTE DATA IN (R)	SAME VIDEO	EEPROM SERIAL DATA- READ ONLY
BIT 5	8253 OUT #2 (R)	SAME	(IN) SAME
BIT 6	1=I/O CHECK (PARITY ERROR) (R)	KEYBOARD DATA	MONOCHROME MODE 0=COLOR MONITOR 1=350 LINE MONITOR MONO
BIT 7	1=RAM PARITY ERROR (R)	KEYBOARD CABLE INSTALLED	RESERVED = 0
	HARDWARE LOGIC ATTACHED IS FOR INPUT ONLY.		IN TANDY 1000 THE HARDWARE LOGIC IS CONFIGURED SO THAT PORT C IS SPLIT WITH INPUT: PC4 -- PC7 OUTPUT: PC0 -- PC3

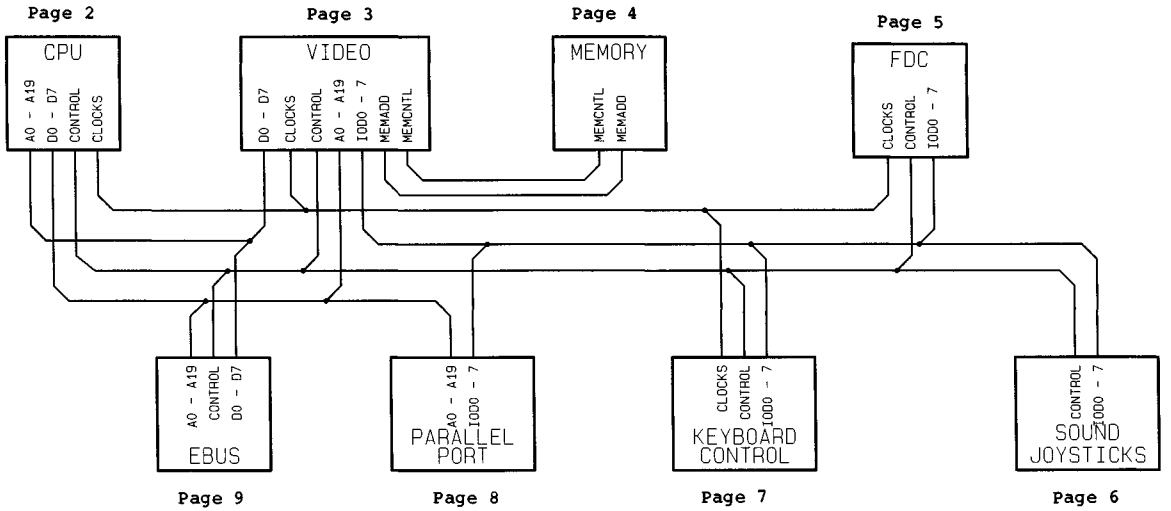
DATA	IBM PC 0061 -- PORT B -- READ OR WRITE	IBM PCjr 0061 -- PORT B -- READ OR WRITE	TANDY 1000 HX 0061 -- PORT B -- READ OR WRITE
BIT 0	1=8253 GATE #2 ENABLED	SAME	SAME
BIT 1	SPEAKER DATA OUT	SAME	SAME
BIT 2	1=ENABLE READING	1=ALPHA (GRAPHICS)	NO FUNCTION
	CONFIG SW13 THRU 16		
	(I/O CHAN ROM SIZE) OR		
	0=ENABLE READING		
V	CONFIG SW12 (@PC0 -- PC3)		
BIT 3	1=CASSETTE MOTOR OFF	SAME	NO FUNCTION
BIT 4	0=ENABLE RAM PARITY	1=DISABLE CASSETTE MTR RELAY, INTERNAL BEEPER	1=DISABLE INTERNAL SPEAKER (SOUNDCONT2)
BIT 5	0=ENABLE I/O CH PARITY	SPKR SW 0	
BIT 6	0=HOLD KEYBOARD CLK LOW	SPKR SW 1	
BIT 7	0=ENABLE KEYBOARD	1=KEYBOARD CLEAR	1=KEYBOARD CLEAR
	1=CLEAR KEYBOARD AND		
V	ENABLE CONFIG SW 1-8		

VIDEO / SYSTEM MEMORY ADDRESS MAP

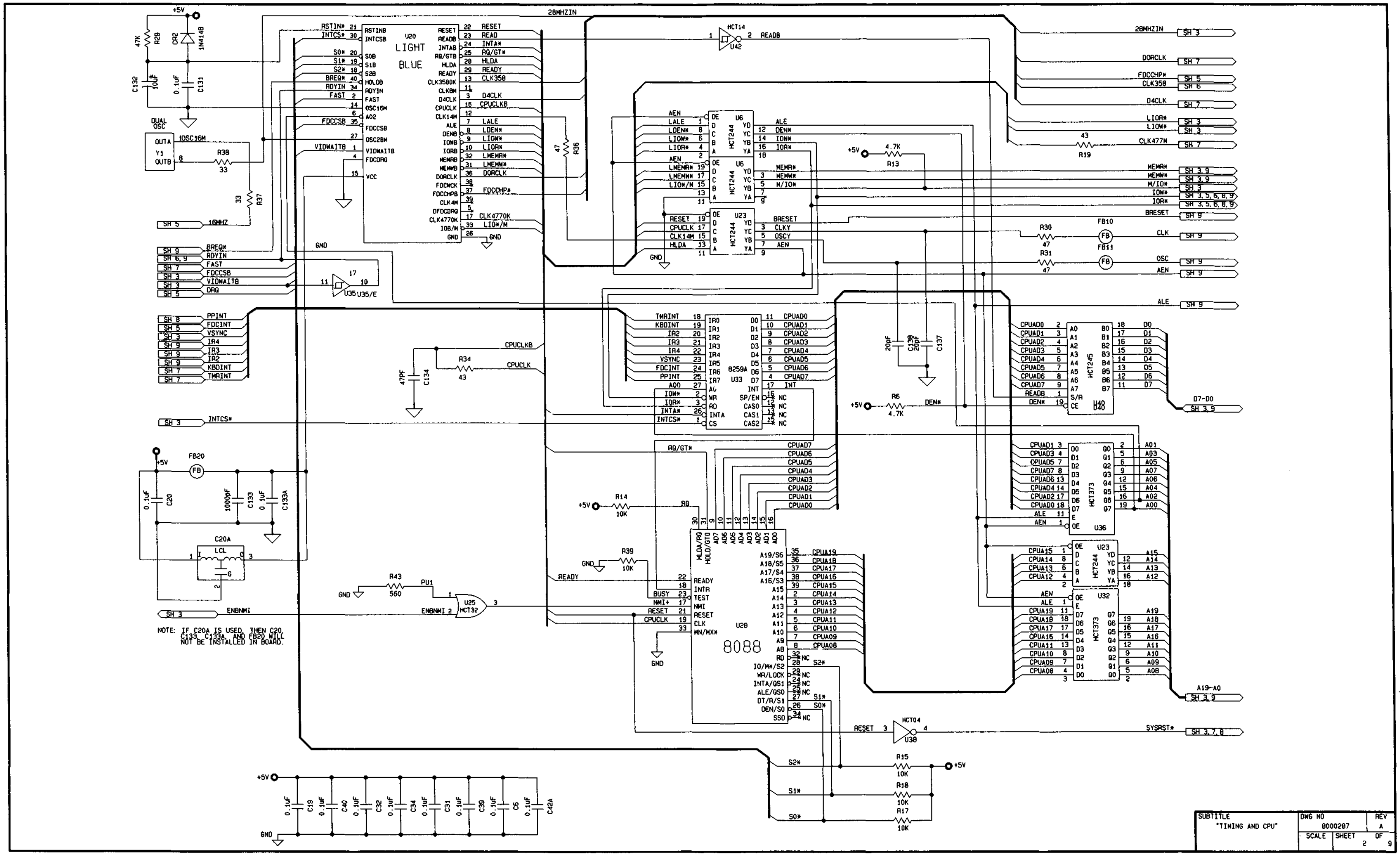
0A0 BIT 4	MC3 0A0 BIT 3 A19	MC2 0A0 BIT 2 A18	MC1 0A0 BIT 1 A17	VIDEO/SYSTEM MEMORY START ADDRESS	VIDEO/SYSTEM MEMORY LENGTH	VIDEO/SYSTEM MEMORY ADDRESS RANGE
0*	0	0	0	00000 (0)	128K	00000-1FFFF
0	0	0	1	20000 (128K)	128K	20000-3FFFF
0	0	1	0	40000 (256K)	128K	40000-5FFFF
0	0	1	1	60000 (324K)	128K	60000-7FFFF
0	1	0	0	80000 (512K)	128K	80000-9FFFF
1	0	0	1	00000 (0)	256K	00000-3FFFF
1	0	1	0	20000 (128K)	256K	20000-5FFFF
1	0	1	1	40000 (156K)	256K	40000-7FFFF
1	1	0	0	60000 (384K)	256K	60000-9FFFF

* ENDBIP 256K OF VIDEO ROM IF "1"

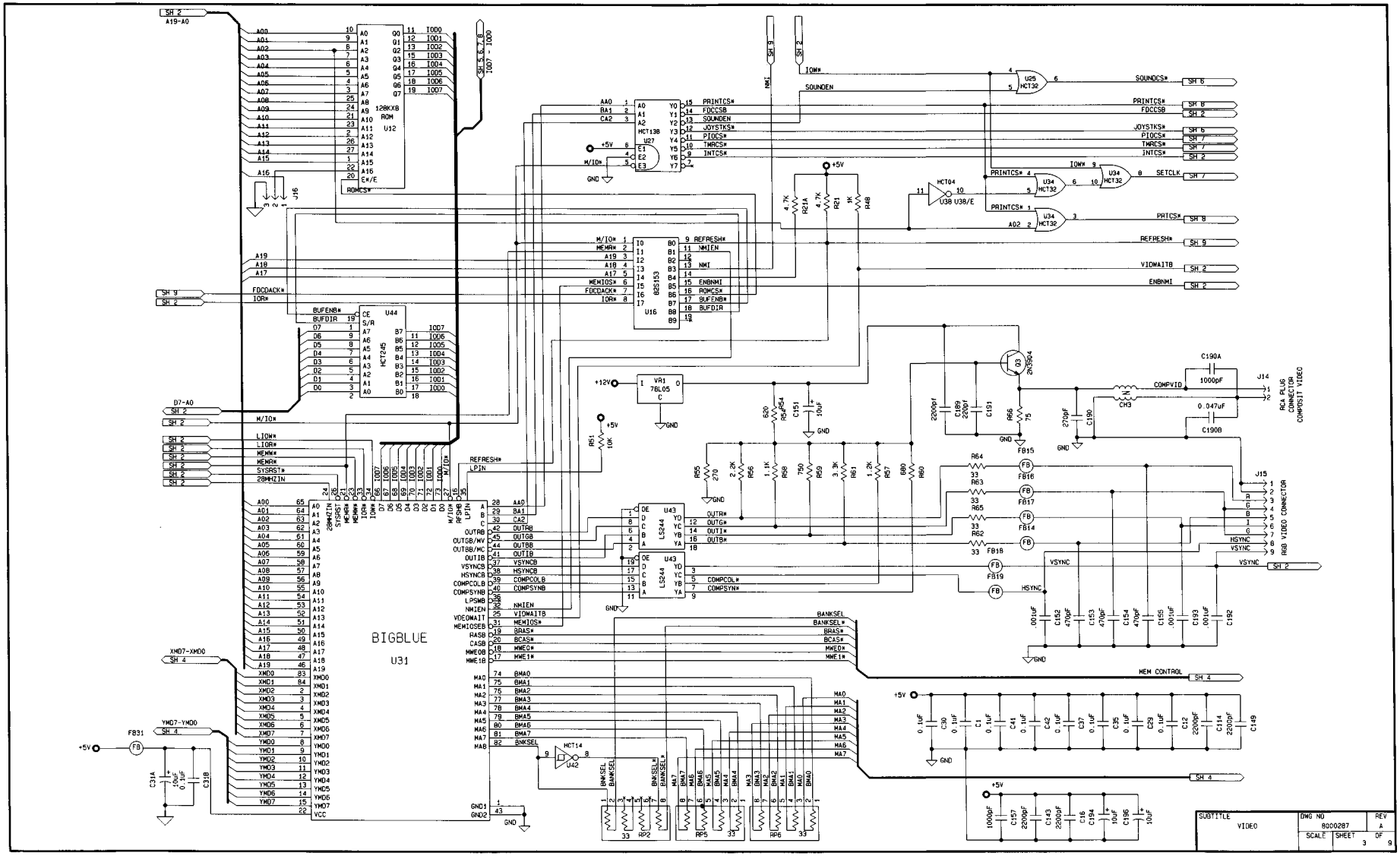
ZONE	LETTER	REVISION DESCRIPTION	DATE	APPROVED
	A	"RELEASED FOR PRODUCTION"	6/12/87	

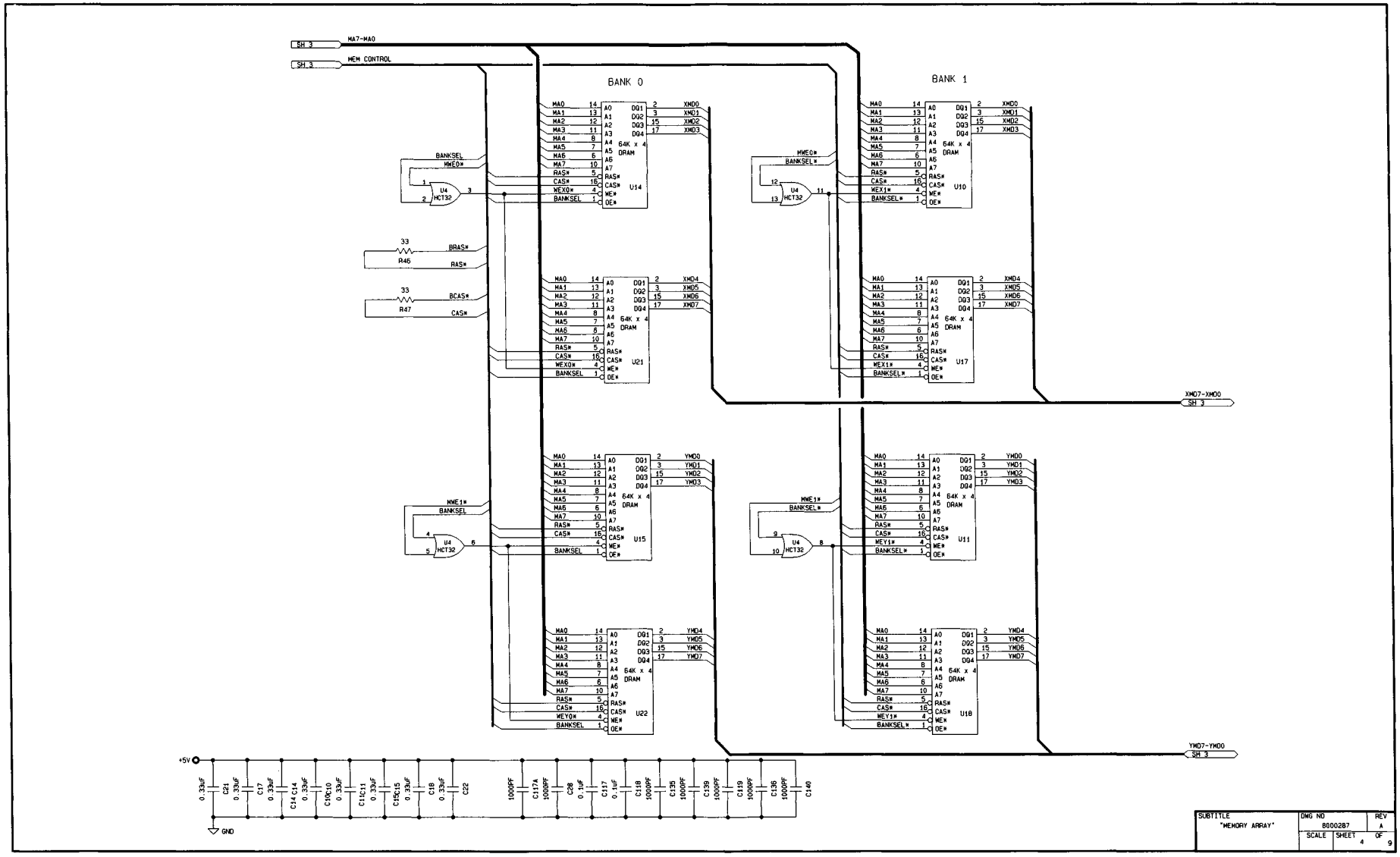


DRAFT	DATE	TITLE	T1000C "MAIN LOGIC BOARD"
CHECK	DATE		
DESIGN	DATE		
APPR	DATE 8/19/87		
APPR	DATE 9/1/87		
824 848 USED ON	TANDY	DWG NO D- 8000287	REV A
		SCALE	SHEET 1 OF 9

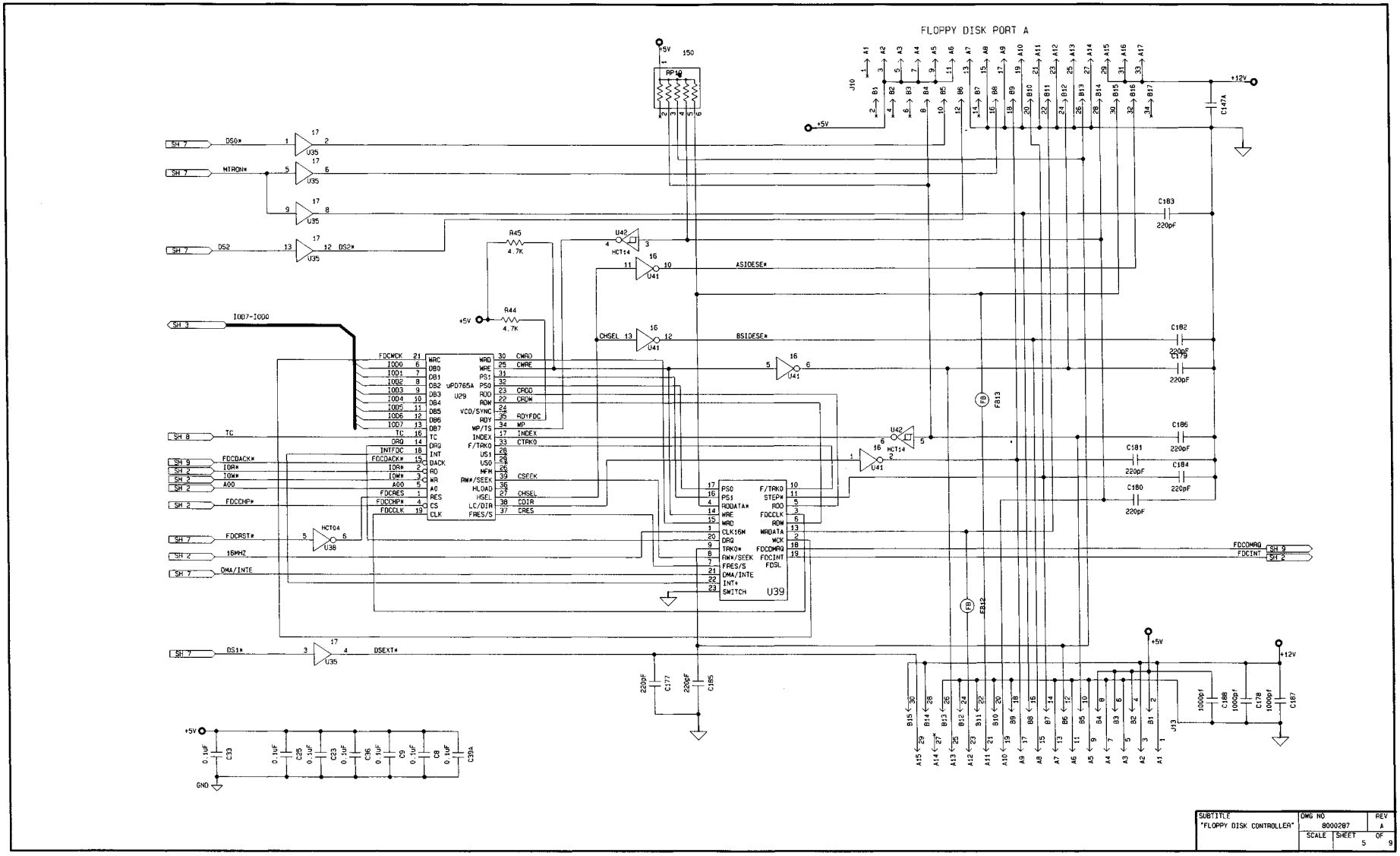


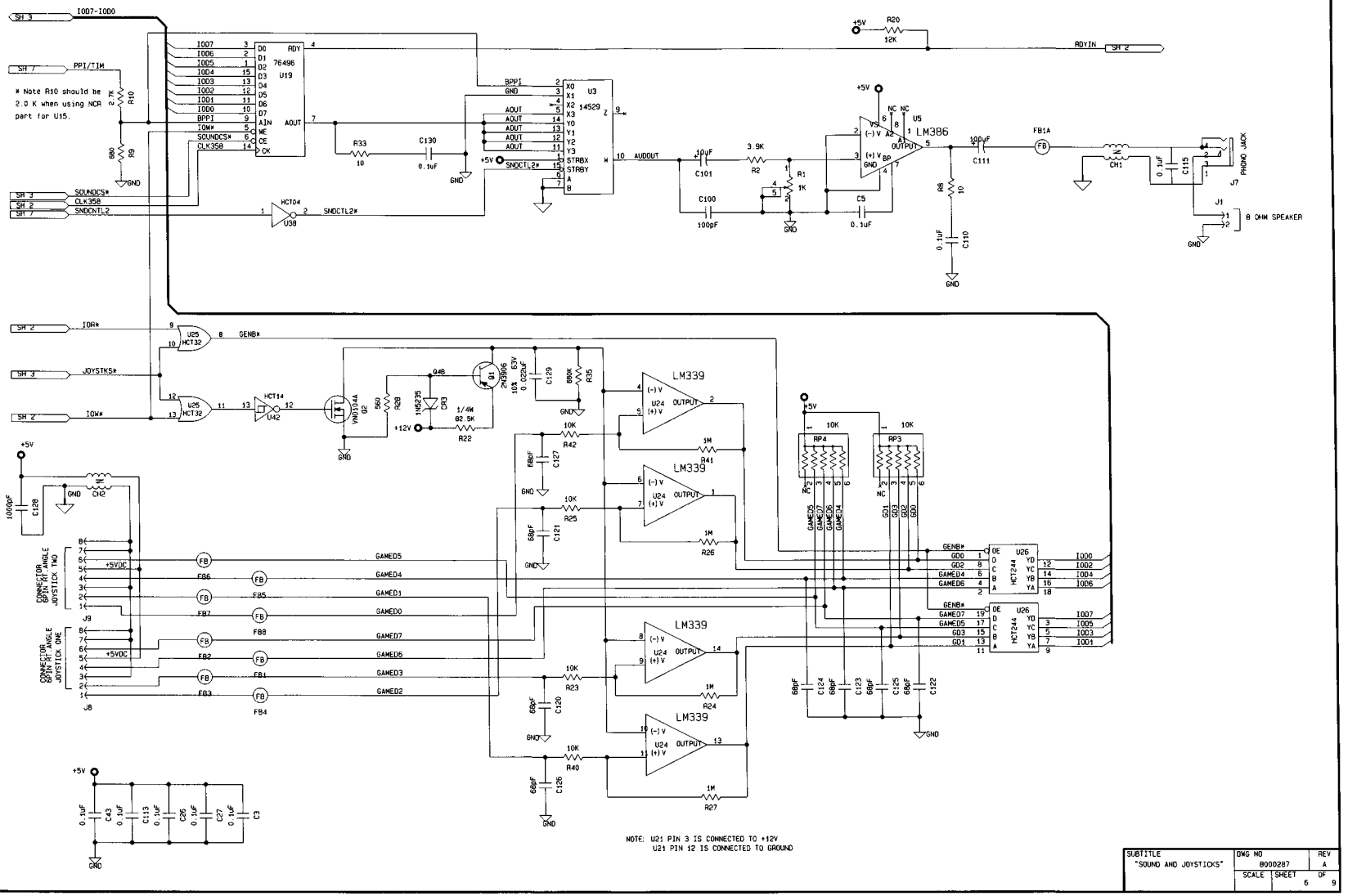
28MHZIN
U20
LIGHT BLUE
U28
8088
8259A
U33
HCT244
U6
U23
HCT245
U40
HCT373
U36
U32
HCT14
U42
HCT32
U25
HCT04
U38
U35
DUAL OSC
Y1
NOTE: IF C20A IS USED, THEN C20, C133, C133A, AND FB20 WILL NOT BE INSTALLED IN BOARD.
D7-D0
A19-A0
SYSRST*
SUBTITLE
"TIMING AND CPU"
DWG NO
8000287
REV
A
SCALE
SHEET
2
OF
9

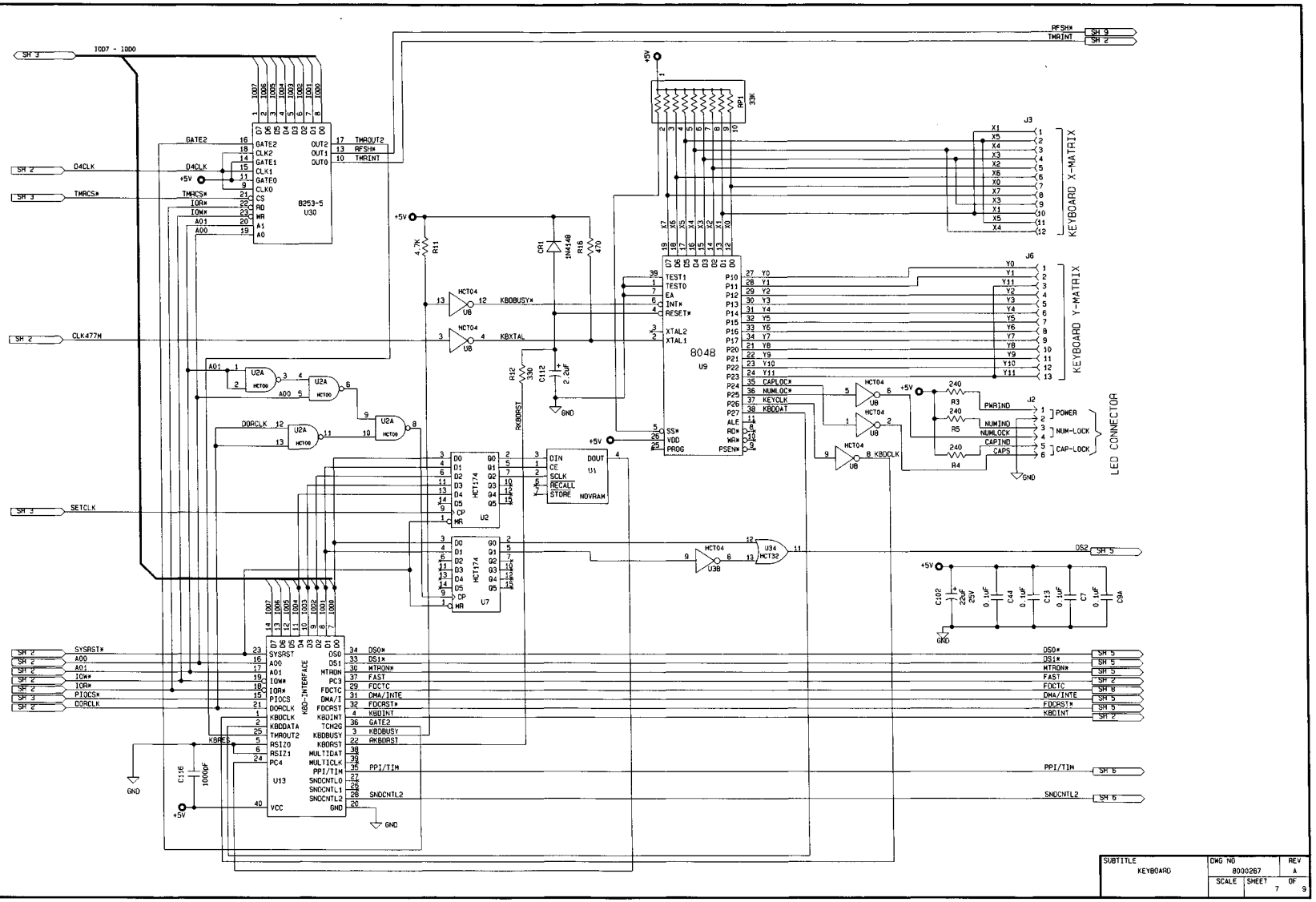

BIGBLUE
U31
SUBTITLE
VIDEO
DWG NO
8000287
REV
A
SCALE
SHEET
3
OF
9



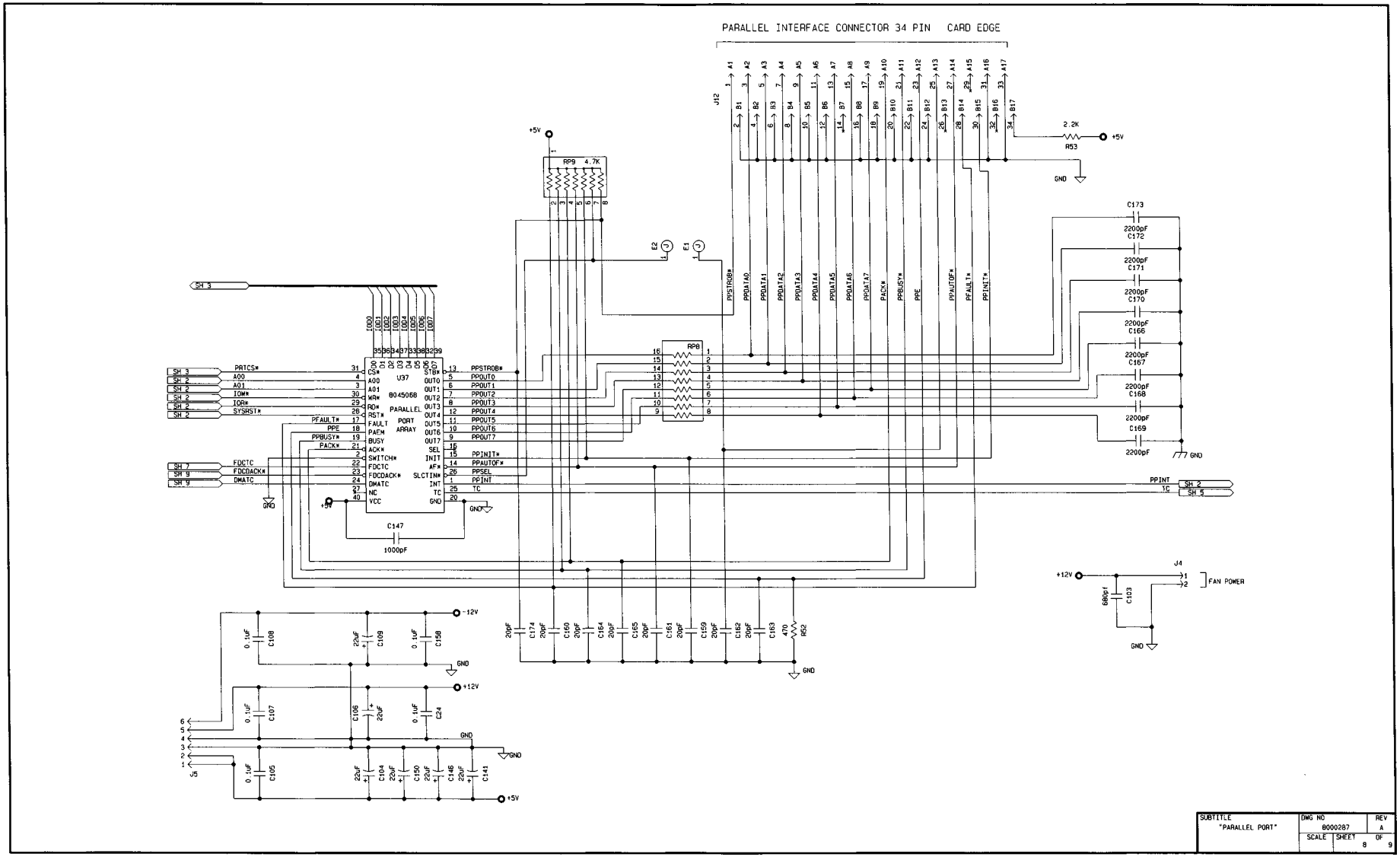
SUBTITLE	DWG NO	REV
"MEMORY ARRAY"	8000287	A
	SCALE	SHEET 4 OF 9


FLOPPY DISK PORT A
SUBTITLE
"FLOPPY DISK CONTROLLER"
DWG NO
8000287
REV
A
SCALE
SHEET
5
OF
9

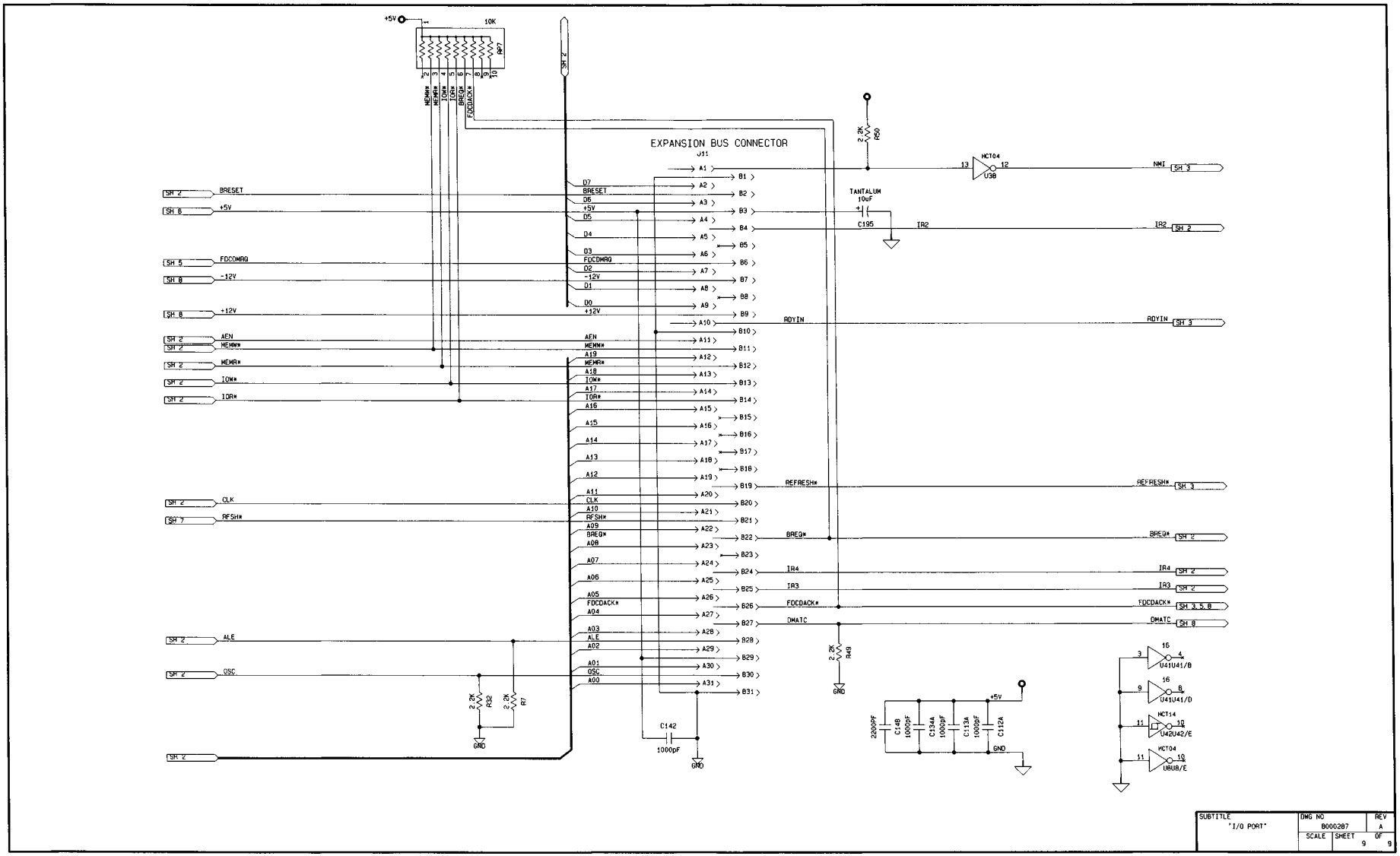

SH 3
IOD7-IOD0
SH 7
PPI/TIM
* Note R10 should be 2.0 K when using NCR part for U15.
R10 2.7K
R9 680
GND
IOD7
IOD6
IOD5
IOD4
IOD3
IOD2
IOD1
IOD0
BPPI
IOW#
SOUNDCS#
CLK358
76496
U19
RDY
AOUT
AIN
WE
CE
CK
R33 10
C130 0.1uF
+5V
R20 12K
RDYIN
SH 2
BPPI
GND
AOUT
ADUT
SNDCTL2#
U3
14529
X0
X1
X2
X3
Y0
Y1
Y2
Y3
STRBX
STRBY
A
B
C
AUDOUT
C101 10uF
3.9K
R2
C100 100pF
R1 1K
C5 0.1uF
LM386
NC NC
U5
(-) V
(+) V
GND
BP
OUTPUT
100uF
C111
FB1A
FB
CH1
0.1uF
C115
PHONO JACK
J7
J1
8 OHM SPEAKER
R8 10
0.1uF
C110
SH 3
SOUNDCS#
CLK358
SH 2
SNDCNTL2
SH 7
SNDCNTL2
HCT04
U38
SH 2
IOR#
SH 3
JOYSTKS#
SH 2
IOW#
U25
HCT32
GENB#
HCT14
U42
VN0104
Q2
360
R28
Q48
2N3906
1N5235
D43
+12V
1/4W
82.5K
R22
0.022uF
C129
680K
R35
LM339
U24
OUTPUT
10K
R42
R41 1M
R25
R26
R23
R24
R40
R27
68pF
C127
C121
C120
C126
GND
RP4
RP3
10K
NC
GAMED5
GAMED7
GAMED6
GAMED4
GD1
GD3
GD2
GD0
U26
HCT244
OE
YD
YC
YB
YA
IOD0
IOD2
IOD4
IOD6
IOD7
IOD5
IOD3
IOD1
C124
C123
C125
C122
+5VDC
CONNECTOR 8PIN RT. ANGLE JOYSTICK TWO
J9
CONNECTOR 8PIN RT. ANGLE JOYSTICK ONE
J8
FB6
FB5
FB7
FB8
FB2
FB1
FB3
FB4
GAMED5
GAMED4
GAMED1
GAMED0
GAMED7
GAMED6
GAMED3
GAMED2
CH2
10000pF
C128
C43 0.1uF
C113 0.1uF
C26 0.1uF
C27 0.1uF
C3 0.1uF
NOTE: U21 PIN 3 IS CONNECTED TO +12V
U21 PIN 12 IS CONNECTED TO GROUND
SUBTITLE
"SOUND AND JOYSTICKS"
DWG NO
8000287
REV
A
SCALE
SHEET
6 OF 9



SUBTITLE	DWG NO	REV
KEYBOARD	8000267	A
	SCALE	SHEET 7 OF 9



SUBTITLE "PARALLEL PORT"	DWG NO 8000287	REV A
	SCALE	SHEET 8 OF 9



SUBTITLE	DWG NO	REV
"I/O PORT"	B000287	A
	SCALE	SHEET 9 OF 9

ZONE	LETTER	REVISION DESCRIPTION	DATE	APPROVED
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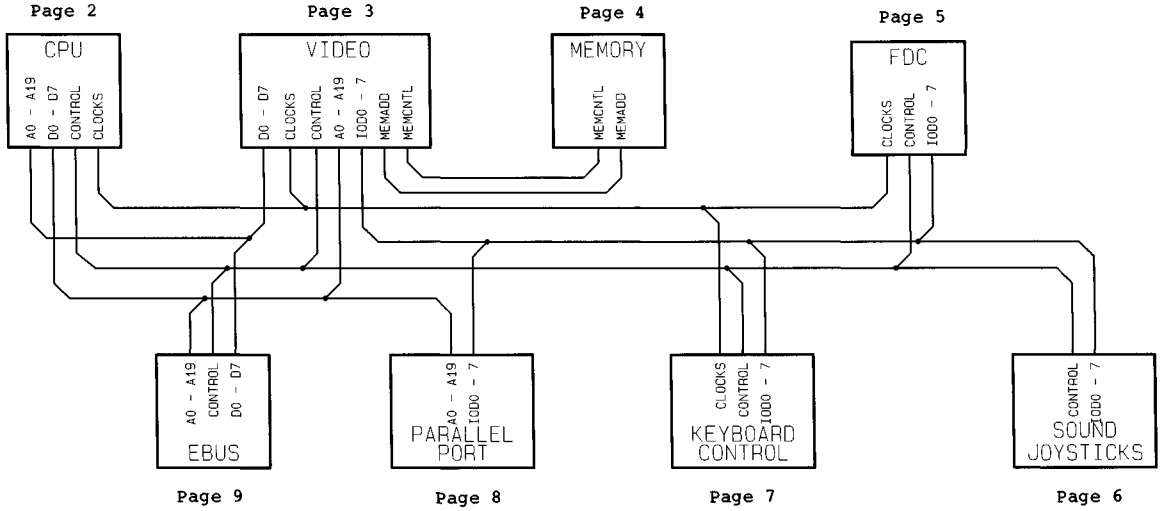
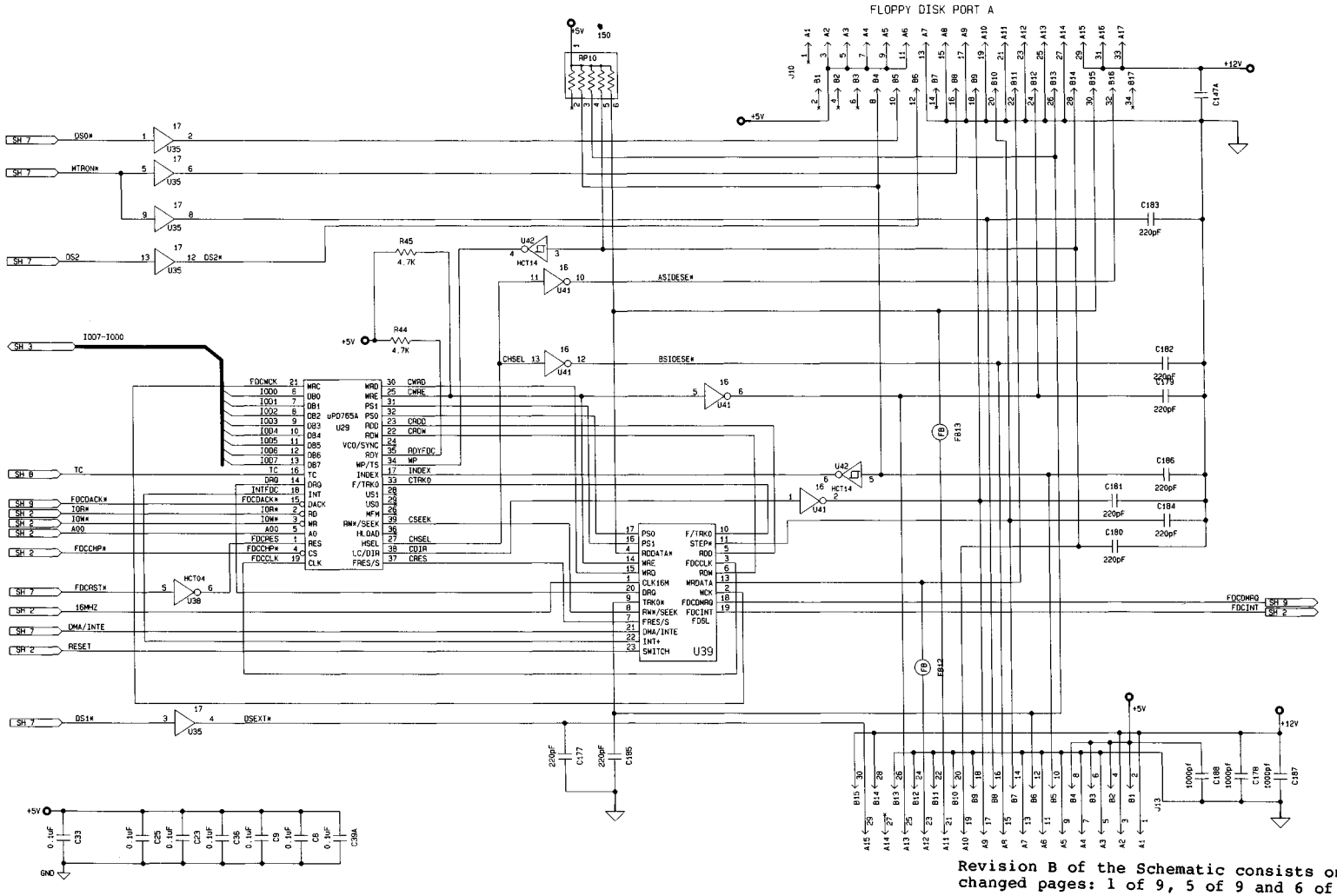
	B	PRODUCTION RELEASE TCO#13246, 13249		



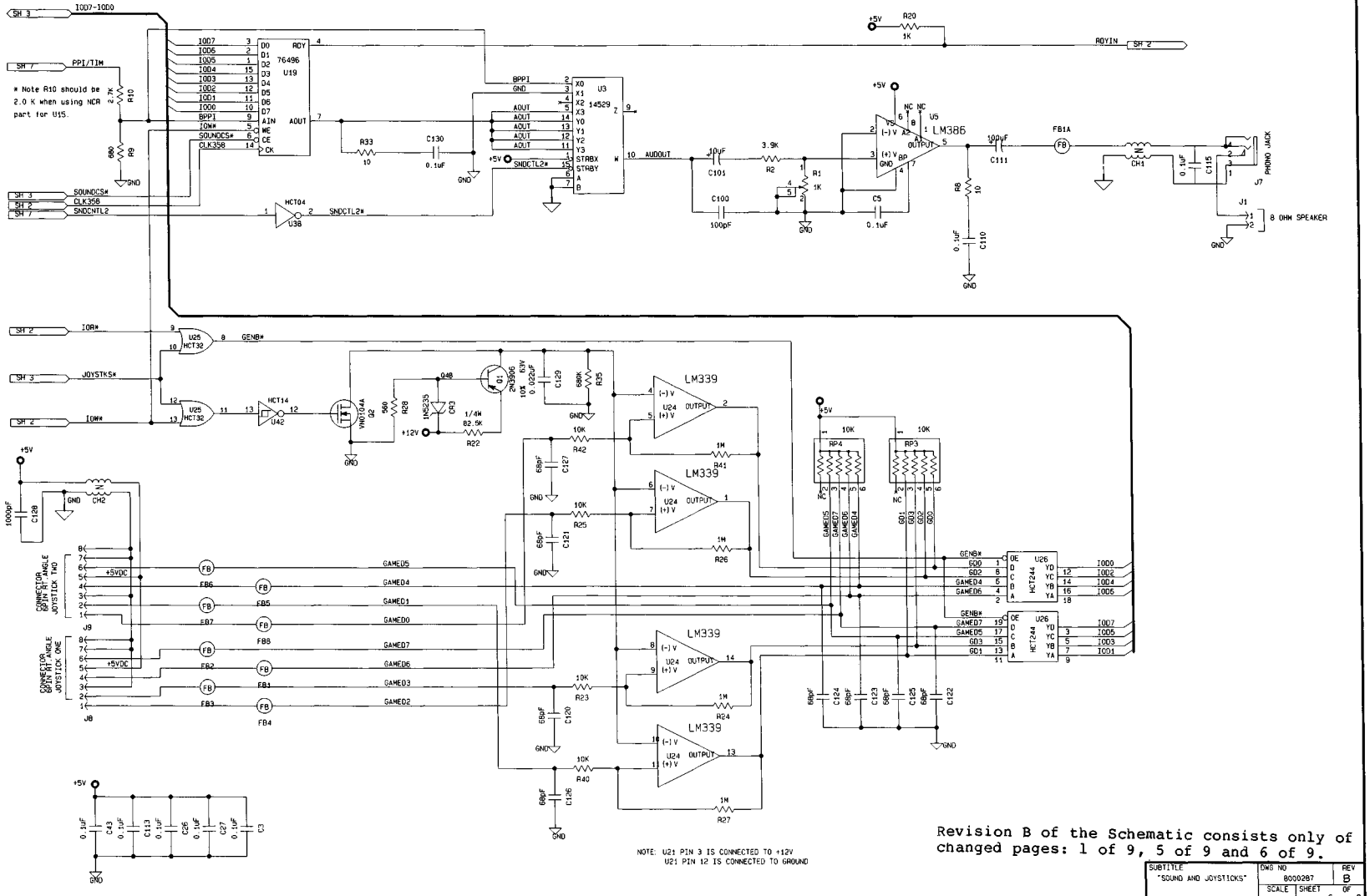
Revision B of the Schematic consists only of changed pages: 1 of 9, 5 of 9 and 6 of 9.

DRAFT	DATE	TITLE	T1000C "MAIN LOGIC BOARD"
CHECK	DATE		
DESIGN	DATE		
APPD	DATE 7/4/87		
APPD	DATE 7/1/87		
824 848 USED ON	TANDY	DWG NO D- B0002B7	REV B
		SCALE	SHEET 1 OF 9



Revision B of the Schematic consists only of changed pages: 1 of 9, 5 of 9 and 6 of 9.

SUBTITLE	DWG NO	REV
"FLOPPY DISK CONTROLLER"	8000287	B
	SCALE / SHEET	OF
	5	9



Revision B of the Schematic consists only of changed pages: 1 of 9, 5 of 9 and 6 of 9.

SUBTITLE	DWG NO	REV
"SOUND AND JOYSTICKS"	8000287	B
	SCALE / SHEET	6 OF 9

1000 HX Devices

1000 HX Devices
Contents

Device	Manufacturer
8088 (CPU)	intel
8253 Interval Timer	intel
8259A Interrupt Controller	intel
Floppy Disk Support	Motorola
Keyboard Interface	Motorola
8048	NEC
µPD765 (FDC)	NEC
Direct Memory Access (DMA)	Tandy
Printer Interface	Tandy
Timing Control Generator	Tandy
Video Controller	Tandy
8496 Sound Generator	NCR

8088
8-BIT HMOS MICROPROCESSOR
8088/8088-2

- 8-Bit Data Bus Interface
- 16-Bit Internal Architecture
- Direct Addressing Capability to 1 Mbyte of Memory
- Direct Software Compatibility with 8086 CPU
- 14-Word by 16-Bit Register Set with Symmetrical Operations
- 24 Operand Addressing Modes
- Byte, Word, and Block Operations
- 8-Bit and 16-Bit Signed and Unsigned Arithmetic in Binary or Decimal, Including Multiply and Divide
- Two Clock Rates:
  - 5 MHz for 8088
  - 8 MHz for 8088-2
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range

The Intel® 8088 is a high performance microprocessor implemented in N-channel, depletion load, silicon gate technology (HMOS), and packaged in a 40-pin CERDIP package. The processor has attributes of both 8- and 16-bit microprocessors. It is directly compatible with 8086 software and 8080/8085 hardware and peripherals.

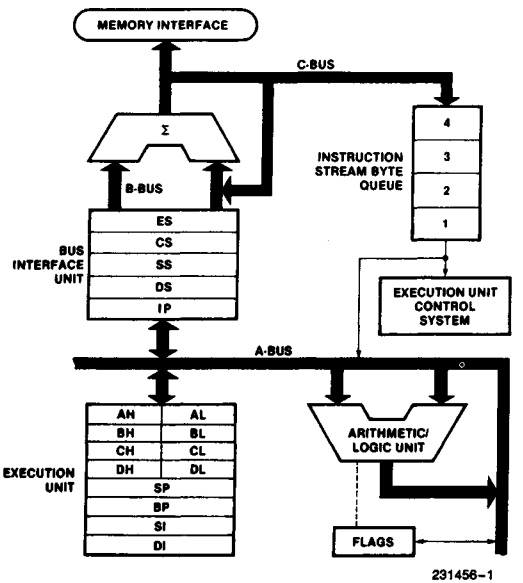


Figure 1. 8088 CPU Functional Block Diagram

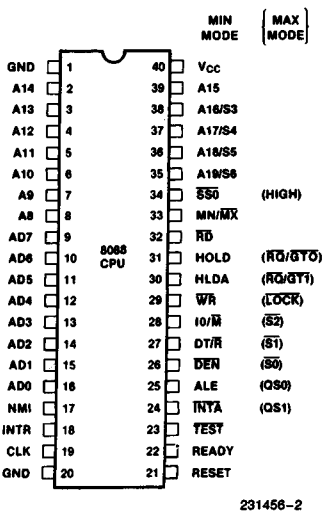


Figure 2. 8088 Pin Configuration

November 1988
Order Number: 231456-002

Table 1. Pin Description

The following pin function descriptions are for 8088 systems in either minimum or maximum mode. The "local bus" in these descriptions is the direct multiplexed bus interface connection to the 8088 (without regard to additional bus buffers).

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>AD7–AD0</td><td>9–16</td><td>I/O</td><td>ADDRESS DATA BUS: These lines constitute the time multiplexed memory/IO address (T1) and data (T2, T3, Tw, T4) bus. These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".</td></tr>
<tr><td>A15–A8</td><td>2–8, 39</td><td>O</td><td>ADDRESS BUS: These lines provide address bits 8 through 15 for the entire bus cycle (T1–T4). These lines do not have to be latched by ALE to remain valid. A15–A8 are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".</td></tr>
<tr><td>A19/S6, A18/S5, A17/S4, A16/S3</td><td>35–38</td><td>O</td><td>ADDRESS/STATUS: During T1, these are the four most significant address lines for memory operations. During I/O operations, these lines are LOW. During memory and I/O operations, status information is available on these lines during T2, T3, Tw, and T4. S6 is always low. The status of the interrupt enable flag bit (S5) is updated at the beginning of each clock cycle. S4 and S3 are encoded as shown.
This information indicates which segment register is presently being used for data accessing.
These lines float to 3-state OFF during local bus "hold acknowledge".
<table>
<tr><th>S4</th><th>S3</th><th>Characteristics</th></tr>
<tr><td>0 (LOW)</td><td>0</td><td>Alternate Data</td></tr>
<tr><td>0</td><td>1</td><td>Stack</td></tr>
<tr><td>1 (HIGH)</td><td>0</td><td>Code or None</td></tr>
<tr><td>1</td><td>1</td><td>Data</td></tr>
<tr><td>S6 is 0 (LOW)</td><td></td><td></td></tr>
</table></td></tr>
<tr><td>$\overline{RD}$</td><td>32</td><td>O</td><td>READ: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the IO/$\overline{M}$ pin or S2. This signal is used to read devices which reside on the 8088 local bus. $\overline{RD}$ is active LOW during T2, T3 and Tw of any read cycle, and is guaranteed to remain HIGH in T2 until the 8088 local bus has floated.
This signal floats to 3-state OFF in "hold acknowledge".</td></tr>
<tr><td>READY</td><td>22</td><td>I</td><td>READY: is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The RDY signal from memory or I/O is synchronized by the 8284 clock generator to form READY. This signal is active HIGH. The 8088 READY input is not synchronized. Correct operation is not guaranteed if the set up and hold times are not met.</td></tr>
<tr><td>INTR</td><td>18</td><td>I</td><td>INTERRUPT REQUEST: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.</td></tr>
<tr><td>$\overline{TEST}$</td><td>23</td><td>I</td><td>$\overline{TEST}$: input is examined by the "wait for test" instruction. If the $\overline{TEST}$ input is LOW, execution continues, otherwise the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.</td></tr>
</table>

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
NMI	17	I	**NON-MASKABLE INTERRUPT:** is an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	**RESET:** causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the instruction set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	**CLOCK:** provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
V_{CC}	40		**V_{CC}:** is the +5V ±10% power supply pin.
GND	1, 20		**GND:** are the ground pins.
MN/$\overline{MX}$	33	I	**MINIMUM/MAXIMUM:** indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

The following pin function descriptions are for the 8088 minimum mode (i.e., MN/$\overline{MX}$ = V_{CC}). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described above.

Symbol	Pin No.	Type	Name and Function
IO/$\overline{M}$	28	O	**STATUS LINE:** is an inverted maximum mode $\overline{S2}$. It is used to distinguish a memory access from an I/O access. IO/$\overline{M}$ becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (I/O = HIGH, M = LOW). IO/$\overline{M}$ floats to 3-state OFF in local bus "hold acknowledge".
$\overline{WR}$	29	O	**WRITE:** strobe indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the IO/$\overline{M}$ signal. WR is active for T2, T3, and Tw of any write cycle. It is active LOW, and floats to 3-state OFF in local bus "hold acknowledge".
$\overline{INTA}$	24	O	**INTA:** is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T2, T3, and Tw of each interrupt acknowledge cycle.
ALE	25	O	**ADDRESS LATCH ENABLE:** is provided by the processor to latch the address into an address latch. It is a HIGH pulse active during clock low of T1 of any bus cycle. Note that ALE is never floated.
DT/$\overline{R}$	27	O	**DATA TRANSMIT/RECEIVE:** is needed in a minimum system that desires to use a data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/$\overline{R}$ is equivalent to $\overline{ST}$ in the maximum mode, and its timing is the same as for IO/$\overline{M}$ (T = HIGH, R = LOW). This signal floats to 3-state OFF in local "hold acknowledge".
$\overline{DEN}$	26	O	**DATA ENABLE:** is provided as an output enable for the data bus transceiver in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access, and for $\overline{INTA}$ cycles. For a read or $\overline{INTA}$ cycle, it is active from the middle of T2 until the middle of T4, while for a write cycle, it is active from the beginning of T2 until the middle of T4. $\overline{DEN}$ floats to 3-state OFF during local bus "hold acknowledge".

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
HOLD, HLDA	31, 30	I, O	**HOLD:** indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement, in the middle of a T4 or T1 clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor lowers HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. Hold is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the set up time.
$\overline{SSO}$	34	O	**STATUS LINE:** is logically equivalent to $\overline{SO}$ in the maximum mode. The combination of $\overline{SSO}$, IO/$\overline{M}$ and DT/$\overline{R}$ allows the system to completely decode the current bus cycle status.

IO/$\overline{M}$	DT/$\overline{R}$	$\overline{SSO}$	Characteristics
1(HIGH)	0	0	Interrupt Acknowledge
1	0	1	Read I/O Port
1	1	0	Write I/O Port
1	1	1	Halt
0(LOW)	0	0	Code Access
0	0	1	Read Memory
0	1	0	Write Memory
0	1	1	Passive

The following pin function descriptions are for the 8088/8288 system in maximum mode (i.e., MN/$\overline{MX}$ = GND). Only the pin functions which are unique to maximum mode are described; all other pin functions are as described above.

Symbol	Pin No.	Type	Name and Function
$\overline{S2}$, $\overline{S1}$, $\overline{S0}$	26–28	O	**STATUS:** is active during clock high of T4, T1, and T2, and is returned to the passive state (1,1,1) during T3 or during Tw when READY is HIGH. This status is used by the 8288 bus controller to generate all memory and I/O access control signals. Any change by $\overline{S2}$, $\overline{S1}$, or $\overline{S0}$ during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 and Tw is used to indicate the end of a bus cycle. These signals float to 3-state OFF during "hold acknowledge". During the first clock cycle after RESET becomes active, these signals are active HIGH. After this first clock, they float to 3-state OFF.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Characteristics
0(LOW)	0	0	Interrupt Acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1(HIGH)	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{RQ}/\overline{GT0}$, $\overline{RQ}/\overline{GT1}$	30, 31	I/O	**REQUEST/GRANT:** pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GT0}$ having higher priority than $\overline{RQ}/\overline{GT1}$. $\overline{RQ}/\overline{GT}$ has an internal pull-up resistor, so may be left unconnected. The request/grant sequence is as follows (See Figure 8): 1. A pulse of one CLK wide from another local bus master indicates a local bus request ("hold") to the 8088 (pulse 1). 2. During a T4 or TI clock cycle, a pulse one clock wide from the 8088 to the requesting master (pulse 2), indicates that the 8088 has allowed the local bus to float and that it will enter the "hold acknowledge" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "hold acknowledge". The same rules as for HOLD/HOLDA apply as for when the bus is released. 3. A pulse one CLK wide from the requesting master indicates to the 8088 (pulse 3) that the "hold" request is about to end and that the 8088 can reclaim the local bus at the next CLK. The CPU then enters T4. Each master-master exchange of the local bus is a sequence of three pulses. There must be one idle CLK cycle after each bus exchange. Pulses are active LOW. If the request is made while the CPU is performing a memory cycle, it will release the local bus during T4 of the cycle when all the following conditions are met: 1. Request occurs on or before T2. 2. Current cycle is not the low bit of a word. 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. If the local bus is idle when the request is made the two possible events will follow: 1. Local bus will be released during the next clock. 2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.
$\overline{LOCK}$	29	O	**$\overline{LOCK}$:** indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active (LOW). The $\overline{LOCK}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to 3-state off in "hold acknowledge".
QS1, QS0	24, 25	O	**QUEUE STATUS:** provide status to allow external tracking of the internal 8088 instruction queue. The queue status is valid during the CLK cycle after which the queue operation is performed.

QS1	QS0	Characteristics
0(LOW)	0	No Operation
0	1	First Byte of Opcode from Queue
1(HIGH)	0	Empty the Queue
1	1	Subsequent Byte from Queue

—	34	O	Pin 34 is always high in the maximum mode.

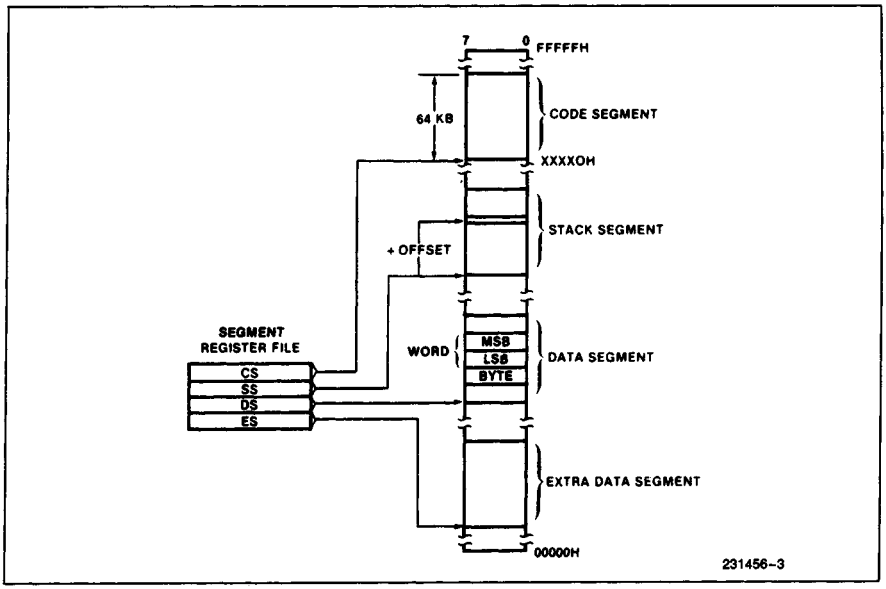


Figure 3. Memory Organization

FUNCTIONAL DESCRIPTION

Memory Organization

The processor provides a 20-bit address to memory which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra data, and stack segments of up to 64K bytes each, with each segment falling on 16-byte boundaries (See Figure 3).

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to the rules of the following table. All information in one segment type share the same logical attributes (e.g. code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster, and more structured.

Word (16-bit) operands can be located on even or odd address boundaries. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU will automatically execute two fetch or write cycles for 16-bit operands.

Memory Reference Used	Segment Register Used	Segment Selection Rule
Instructions	CODE (CS)	Automatic with all instruction prefetch.
Stack	STACK (SS)	All stack pushes and pops. Memory references relative to BP base register except data references.
Local Data	DATA (DS)	Data references when: relative to stack, destination of string operation, or explicity overridden.
External (Global) Data	EXTRA (ES)	Destination of string operations: Explicitly selected using a segment override.

Certain locations in memory are reserved for specific CPU operations (See Figure 4). Locations from addresses FFFF0H through FFFFFH are reserved for operations including a jump to the initial system initialization routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be located. Locations 00000H through 003FFH are reserved for interrupt operations. Four-byte pointers consisting of a 16-bit segment address and a 16-bit offset address direct program flow to one of the 256 possible interrupt service routines. The pointer elements are assumed to have been stored at their respective places in reserved memory prior to the occurrence of interrupts.

Minimum and Maximum Modes

The requirements for supporting minimum and maximum 8088 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the 8088 is equipped with a strap pin (MN/$\overline{MX}$) which defines the system configuration. The definition of a certain subset of the pins changes, dependent on the condition of the strap pin. When the MN/$\overline{MX}$ pin is strapped to GND, the 8088 defines pins 24 through 31 and 34 in maximum mode. When the MN/$\overline{MX}$ pin is strapped to V_{CC}, the 8088 generates bus control signals itself on pins 24 through 31 and 34.

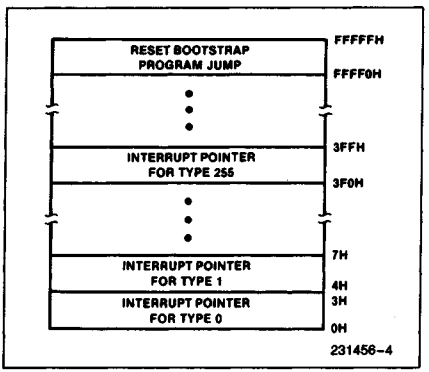


Figure 4. Reserved Memory Locations

The minimum mode 8088 can be used with either a multiplexed or demultiplexed bus. The multiplexed bus configuration is compatible with the MCS-85™ multiplexed bus peripherals. This configuration (See Figure 5) provides the user with a minimum chip count system. This architecture provides the 8088 processing power in a highly integrated form.

The demultiplexed mode requires one latch (for 64K addressability) or two latches (for a full megabyte of addressing). A third latch can be used for buffering if the address bus loading requires it. A transceiver can also be used if data bus buffering is required (See Figure 6). The 8088 provides $\overline{DEN}$ and DT/$\overline{R}$ to control the transceiver, and ALE to latch the addresses. This configuration of the minimum mode provides the standard demultiplexed bus structure with heavy bus buffering and relaxed bus timing requirements.

The maximum mode employs the 8288 bus controller (See Figure 7). The 8288 decodes status lines $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$, and provides the system with all bus control signals. Moving the bus control to the 8288 provides better source and sink current capability to the control lines, and frees the 8088 pins for extended large system features. Hardware lock, queue status, and two request/grant interfaces are provided by the 8088 in maximum mode. These features allow co-processors in local bus and remote bus configurations.

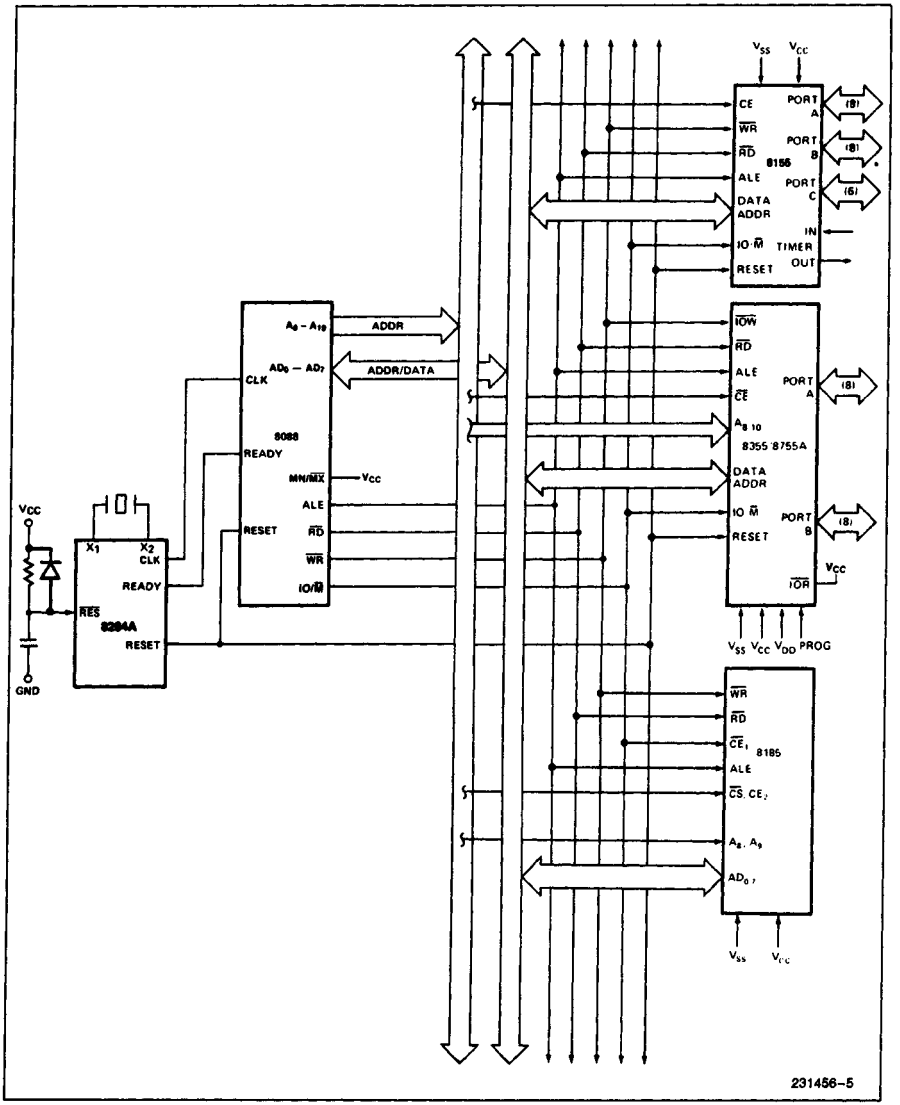


Figure 5. Multiplexed Bus Configuration

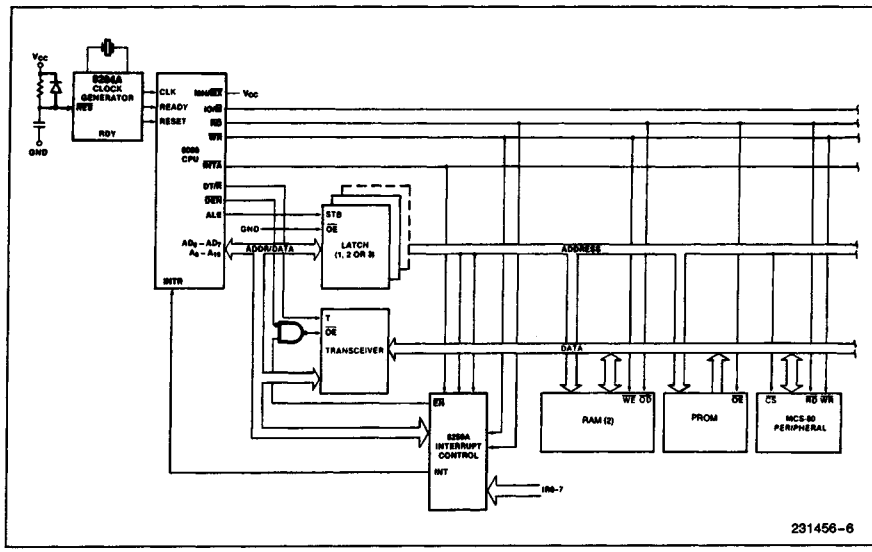


Figure 6. Demultiplexed Bus Configuration

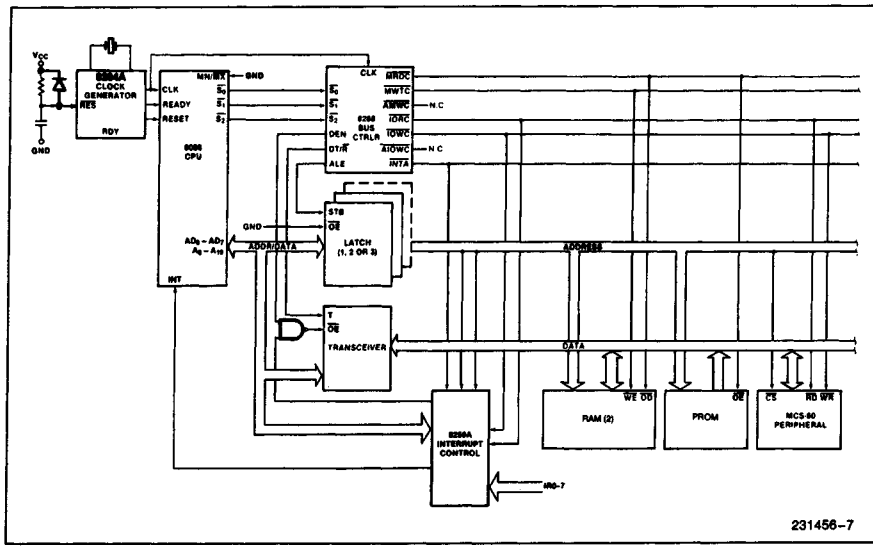


Figure 7. Fully Buffered System Using Bus Controller

Bus Operation

The 8088 address/data bus is broken into three parts—the lower eight address/data bits (AD0–AD7), the middle eight address bits (A8–A15), and the upper four address bits (A16–A19). The address/data bits and the highest four address bits are time multiplexed. This technique provides the most efficient use of pins on the processor, permitting the use of a standard 40 lead package. The middle eight address bits are not multiplexed, i.e. they remain valid throughout each bus cycle. In addition, the bus can be demultiplexed at the processor with a single address latch if a standard, non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T1, T2, T3, and T4 (See Figure 8). The address is emitted from the processor during T1 and data transfer occurs on the bus during T3 and T4. T2 is used primarily for chang-

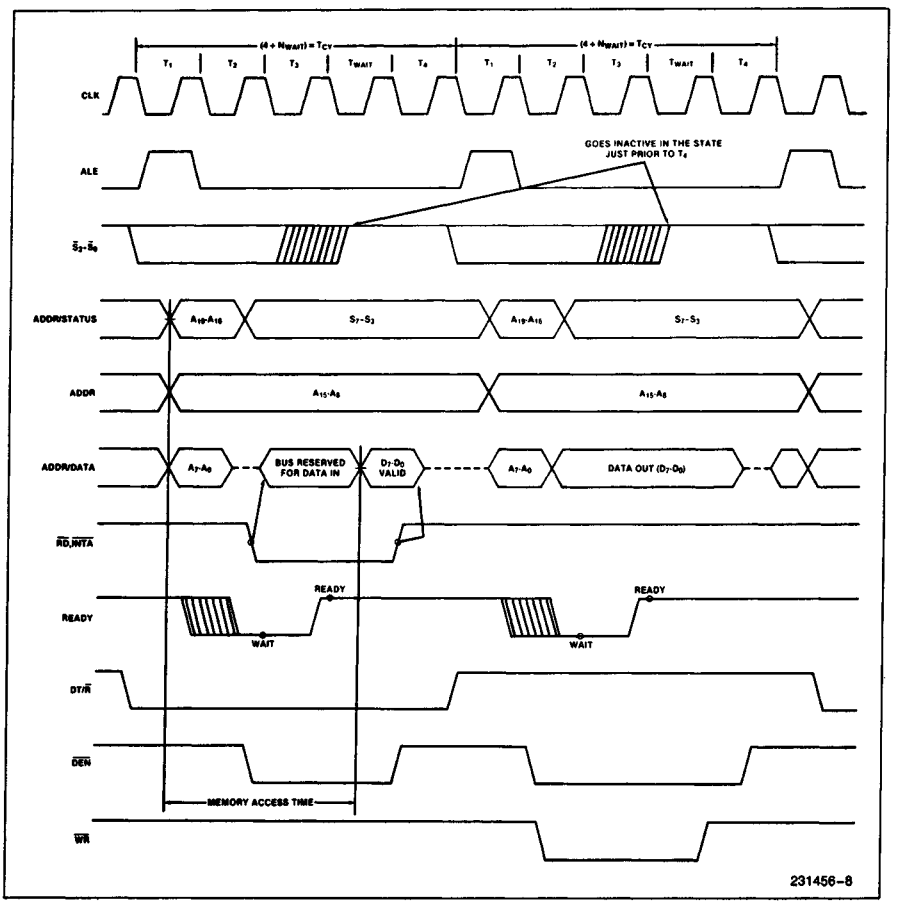


Figure 8. Basic System Timing

ing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "wait" states (Tw) are inserted between T3 and T4. Each inserted "wait" state is of the same duration as a CLK cycle. Periods can occur between 8088 driven bus cycles. These are referred to as "idle" states (Ti), or inactive CLK cycles. The processor uses these cycles for internal housekeeping.

During T1 of any bus cycle, the ALE (address latch enable) signal is emitted (by either the processor or the 8288 bus controller, depending on the MN/$\overline{MX}$ strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ are used by the bus controller, in maximum mode, to identify the type of bus transaction according to the following table:

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Characteristics
0(LOW)	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1(HIGH)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (No Bus Cycle)

Status bits S3 through S6 are multiplexed with high order address bits and are therefore valid during T2 through T4. S3 and S4 indicate which segment register was used for this bus cycle in forming the address according to the following table:

S_4	S_3	Characteristics
0(LOW)	0	Alternate Data (Extra Segment)
0	1	Stack
1(HIGH)	0	Code or None
1	1	Data

S5 is a reflection of the PSW interrupt enable bit. S6 is always equal to 0.

I/O Addressing

In the 8088, I/O operations can address up to a maximum of 64K I/O registers. The I/O address appears in the same format as the memory address on bus lines A15–A0. The address lines A19–A16 are zero in I/O operations. The variable I/O instructions, which use register DX as a pointer, have full address capability, while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space. I/O ports are addressed in the same manner as memory locations.

Designers familiar with the 8085 or upgrading an 8085 design should note that the 8085 addresses I/O with an 8-bit address on both halves of the 16-bit address bus. The 8088 uses a full 16-bit address on its lower 16 address lines.

EXTERNAL INTERFACE

Processor Reset and Initialization

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The 8088 RESET is required to be HIGH for greater than four clock cycles. The 8088 will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 7 clock cycles. After this interval the 8088 operates normally, beginning with the instruction in absolute locations FFFF0H (See Figure 4). The RESET input is internally synchronized to the processor clock. At initialization, the HIGH to LOW transition of RESET must occur no sooner than 50 μs after power up, to allow complete initialization of the 8088.

NMI asserted prior to the 2nd clock after the end of RESET will not be honored. If NMI is asserted after that point and during the internal reset sequence, the processor may execute one instruction before responding to the interrupt. A hold request active immediately after RESET will be honored before the first instruction fetch.

All 3-state outputs float to 3-state OFF during RESET. Status is active in the idle state for the first clock after RESET becomes active and then floats to 3-state OFF. ALE and HLDA are driven low.

Interrupt Operations

Interrupt operations fall into two classes: software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the instruction set description in the iAPX 88 book or the iAPX 86,88 User's Manual. Hardware interrupts can be classified as nonmaskable or maskable.

Interrupts result in a transfer of control to a new program location. A 256 element table containing address pointers to the interrupt service program locations resides in absolute locations 0 through 3FFH (See Figure 4), which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt "type." An interrupting device supplies an 8-bit type number, during the interrupt acknowledge sequence, which is used to vector through the appropriate element to the new interrupt service program location.

Non-Maskable Interrupt (NMI)

The processor provides a single non-maskable interrupt (NMI) pin which has higher priority than the maskable interrupt request (INTR) pin. A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW to HIGH transition. The activation of this pin causes a type 2 interrupt.

NMI is required to have a duration in the HIGH state of greater than two clock cycles, but is not required to be synchronized to the clock. Any higher going transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves (2 bytes in the case of word moves) of a block type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during, or after the servicing of NMI. Another high-going edge triggers another response if it occurs after the start of the NMI procedure. The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

Maskable Interrupt (INTR)

The 8088 provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable (IF) flag bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK. To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block type instruction. During interrupt response sequence, further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt, or single step), although the FLAGS register which is automatically pushed onto the stack reflects the state of the processor prior to the interrupt. Until the old FLAGS register is restored, the enable bit will be zero unless specifically set by an instruction.

During the response sequence (See Figure 9), the processor executes two successive (back to back) interrupt acknowledge cycles. The 8088 emits the LOCK signal (maximum mode only) from T2 of the first bus cycle until T2 of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle, a byte is fetched from the external interrupt system (e.g., 8259A PIC) which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector lookup table. An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. The interrupt return instruction includes a flags pop which returns the status of the original interrupt enable bit when it restores the flags.

HALT

When a software HALT instruction is executed, the processor indicates that it is entering the HALT state in one of two ways, depending upon which mode is strapped. In minimum mode, the processor issues ALE, delayed by one clock cycle, to allow the system to latch the halt status. Halt status is available on IO/$\overline{M}$, DT/$\overline{R}$, and $\overline{SSO}$. In maximum mode, the processor issues appropriate HALT status on $\overline{S2}$, $\overline{S1}$, and $\overline{S0}$, and the 8288 bus controller issues one ALE. The 8088 will not leave the HALT state when a local bus hold is entered while in HALT. In this case, the processor reissues the HALT indicator at the end of the local bus hold. An interrupt request or RESET will force the 8088 out of the HALT state.

Read/Modify/Write (Semaphore) Operations via LOCK

The LOCK status information is provided by the processor when consecutive bus cycles are required during the execution of an instruction. This allows the processor to perform read/modify/write operations on memory (via the "exchange register with memory" instruction), without another system bus master receiving intervening memory cycles. This is useful in multiprocessor system configurations to accomplish "test and set lock" operations. The $\overline{LOCK}$ signal is activated (LOW) in the clock cycle following decoding of the LOCK prefix instruction. It is deactivated at the end of the last bus cycle of the instruction following the LOCK prefix. While $\overline{LOCK}$ is active, a request on a $\overline{RQ}$/$\overline{GT}$ pin will be recorded, and then honored at the end of the LOCK.

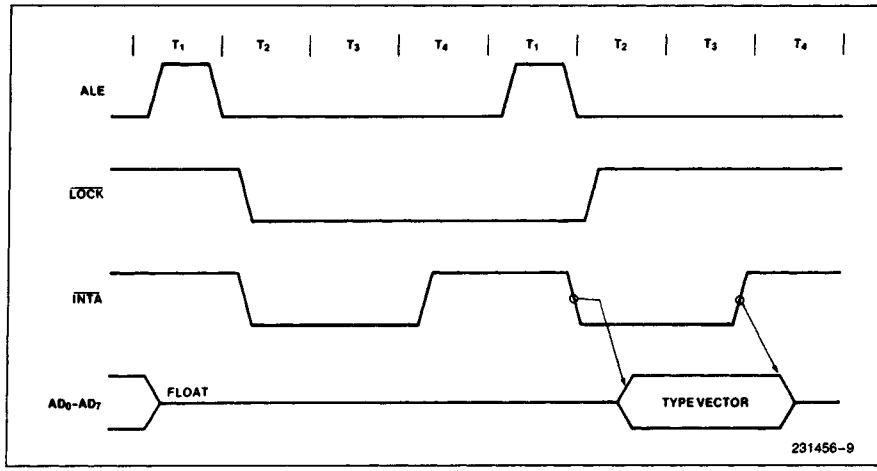


Figure 9. Interrupt Acknowledge Sequence

External Synchronization via $\overline{TEST}$

As an alternative to interrupts, the 8088 provides a single software-testable input pin ($\overline{TEST}$). This input is utilized by executing a WAIT instruction. The single WAIT instruction is repeatedly executed until the $\overline{TEST}$ input goes active (LOW). The execution of WAIT does not consume bus cycles once the queue is full.

If a local bus request occurs during WAIT execution, the 8088 3-states all output drivers. If interrupts are enabled, the 8088 will recognize interrupts and process them. The WAIT instruction is then refetched, and reexecuted.

Basic System Timing

In minimum mode, the MN/$\overline{MX}$ pin is strapped to V_{CC} and the processor emits bus control signals compatible with the 8085 bus structure. In maximum mode, the MN/$\overline{MX}$ pin is strapped to GND and the processor emits coded status information which the 8288 bus controller uses to generate MULTIBUS compatible bus control signals.

System Timing—Minimum System

(See Figure 8)

The read cycle begins in T1 with the assertion of the address latch enable (ALE) signal. The trailing (low going) edge of this signal is used to latch the address information, which is valid on the address/data bus (AD0–AD7) at this time, into the 8282/8283 latch. Address lines A8 through A15 do not need to be latched because they remain valid throughout the bus cycle. From T1 to T4 the IO/$\overline{M}$ signal indicates a memory or I/O operation. At T2 the address is removed from the address/data bus and the bus goes to a high impedance state. The read control signal is also asserted at T2. The read ($\overline{RD}$) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later, valid data will be available on the bus and the addressed device will drive the READY line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will again 3-state its bus drivers. If a transceiver is required to buffer the 8088 local bus, signals DT/$\overline{R}$ and $\overline{DEN}$ are provided by the 8088.

A write cycle also begins with the assertion of ALE and the emission of the address. The IO/$\overline{M}$ signal is again asserted to indicate a memory or I/O write operation. In T2, immediately following the address emission, the processor emits the data to be written into the addressed location. This data remains valid until at least the middle of T4. During T2, T3, and Tw, the processor asserts the write control signal. The write ($\overline{WR}$) signal becomes active at the beginning of T2, as opposed to the read, which is delayed somewhat into T2 to provide time for the bus to float.

The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge ($\overline{INTA}$) signal is asserted in place of the read ($\overline{RD}$) signal and the address bus is floated. (See Figure 9) In the second of two successive $\overline{INTA}$ cycles, a byte of information is read from the data bus, as supplied by the interrupt system logic (i.e. 8259A priority interrupt controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into the interrupt vector lookup table, as described earlier.

Bus Timing—Medium Complexity Systems

(See Figure 10)

For medium complexity systems, the MN/$\overline{MX}$ pin is connected to GND and the 8288 bus controller is added to the system, as well as a latch for latching the system address, and a transceiver to allow for bus loading greater than the 8088 is capable of handling. Signals ALE, $\overline{DEN}$, and DT/$\overline{R}$ are generated by the 8288 instead of the processor in this configuration, although their timing remains relatively the same. The 8088 status outputs ($\overline{S2}$, $\overline{S1}$, and $\overline{S0}$) provide type of cycle information and become 8288 inputs. This bus cycle information specifies read (code, data, or I/O), write (data or I/O), interrupt acknowledge, or software halt. The 8288 thus issues control signals specifying memory read or write, I/O read or write, or interrupt acknowledge. The 8288 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence, data is not valid at the leading edge of write. The transceiver receives the usual T and $\overline{OE}$ inputs from the 8288's DT/$\overline{R}$ and $\overline{DEN}$ outputs.

The pointer into the interrupt vector table, which is passed during the second $\overline{INTA}$ cycle, can derive from an 8259A located on either the local bus or the system bus. If the master 8289A priority interrupt controller is positioned on the local bus, a TTL gate is required to disable the transceiver when reading from the master 8259A during the interrupt acknowledge sequence and software "poll".

The 8088 Compared to the 8086

The 8088 CPU is an 8-bit processor designed around the 8086 internal structure. Most internal functions of the 8088 are identical to the equivalent 8086 functions. The 8088 handles the external bus the same way the 8086 does with the distinction of handling only 8 bits at a time. Sixteen-bit operands are fetched or written in two consecutive bus cycles. Both processors will appear identical to the software engineer, with the exception of execution time. The internal register structure is identical and all instructions have the same end result. The differences between the 8088 and 8086 are outlined below. The engineer who is unfamiliar with the 8086 is referred to the iAPX 86, 88 User's Manual, Chapters 2 and 4, for function description and instruction set information. Internally, there are three differences between the 8088 and the 8086. All changes are related to the 8-bit bus interface.

- The queue length is 4 bytes in the 8088, whereas the 8086 queue contains 6 bytes, or three words. The queue was shortened to prevent overuse of the bus by the BIU when prefetching instructions. This was required because of the additional time necessary to fetch instructions 8 bits at a time.
- To further optimize the queue, the prefetching algorithm was changed. The 8088 BIU will fetch a new instruction to load into the queue each time there is a 1 byte hole (space available) in the queue. The 8086 waits until a 2-byte space is available.
- The internal execution time of the instruction set is affected by the 8-bit interface. All 16-bit fetches and writes from/to memory take an additional four clock cycles. The CPU is also limited by the speed of instruction fetches. This latter problem only occurs when a series of simple operations occur. When the more sophisticated instructions of the 8088 are being used, the queue has time to fill and the execution proceeds as fast as the execution unit will allow.

The 8088 and 8086 are completely software compatible by virtue of their identical execution units. Software that is system dependent may not be completely transferable, but software that is not system dependent will operate equally as well on an 8088 and an 8086.

The hardware interface of the 8088 contains the major differences between the two CPUs. The pin assignments are nearly identical, however, with the following functional changes:

- A8–A15—These pins are only address outputs on the 8088. These address lines are latched internally and remain valid throughout a bus cycle in a manner similar to the 8085 upper address lines.
- $\overline{BHE}$ has no meaning on the 8088 and has been eliminated.

- $\overline{SSO}$ provides the $\overline{SO}$ status information in the minimum mode. This output occurs on pin 34 in minimum mode only. DT/$\overline{R}$, IO/$\overline{M}$, and $\overline{SSO}$ provide the complete bus status in minimum mode.
- IO/$\overline{M}$ has been inverted to be compatible with the MCS-85 bus structure.
- ALE is delayed by one clock cycle in the minimum mode when entering HALT, to allow the status to be latched with ALE.

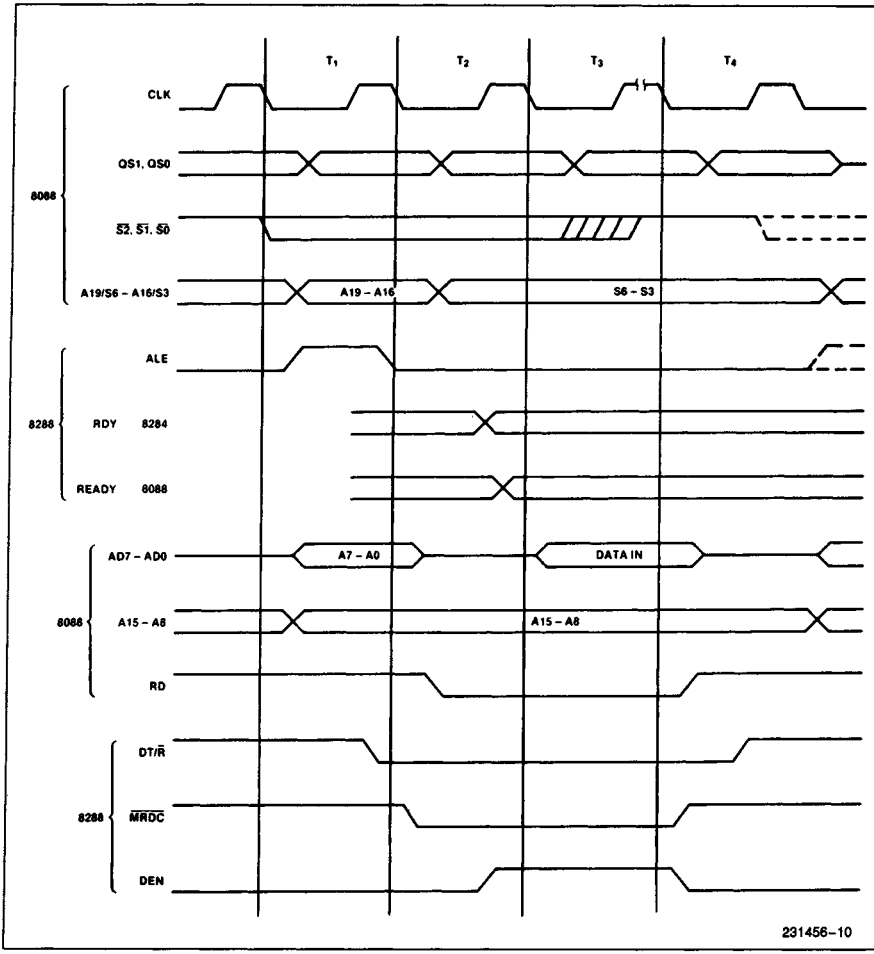


Figure 10. Medium Complexity System Timing

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ....0°C to +70°C
Case Temperature (Plastic) .....0°C to +95°C
Case Temperature (CERDIP) .....0°C to +75°C
Storage Temperature .....−65°C to +150°C
Voltage on Any Pin with Respect to Ground .....−1.0 to +7V
Power Dissipation .....2.5 Watt

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

(T_A = 0°C to 70°C, T_{CASE} (Plastic) = 0°C to 95°C, T_{CASE} (CERDIP) = 0°C to 75°C)*
(V_{CC} = 5V ±10% for 8088, V_{CC} = 5V ±5% for 8088-2)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	+0.8	V	(Note 1)
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	(Notes 1, 2)
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{CC}	8088 Power Supply Current: 8088-2 P8088		340 350 250	mA	T_A = 25°C
I_{LI}	Input Leakage Current		±10	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{LO}	Output and I/O Leakage Current		±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
V_{CL}	Clock Input Low Voltage	−0.5	+0.6	V	
V_{CH}	Clock Input High Voltage	3.9	V_{CC} + 1.0	V	
C_{IN}	Capacitance If Input Buffer (All Input Except AD_0–AD_7, RQ/GT)		15	pF	fc = 1 MHz
C_{IO}	Capacitance of I/O Buffer AD_0–AD_7, RQ/GT)		15	pF	fc = 1 MHz

NOTES:
*For Extended Temperature EXPRESS V_{CC} = 5V ±5%
1. V_{IL} tested with MN/$\overline{MX}$ Pin = 0V
   V_{IH} tested with MN/$\overline{MX}$ Pin = 5V
   MN/$\overline{MX}$ Pin is a strap Pin
2. Not applicable to $\overline{RQ}$/$\overline{GT0}$ and $\overline{RQ}$/$\overline{GT1}$ Pins (Pin 30 and 31)

A.C. CHARACTERISTICS

(T_A = 0°C to 70°C, T_{CASE} (Plastic) = 0°C to 95°C, T_{CASE} (CERDIP) = 0°C to 75°C)*
(V_{CC} = 5V ±10% for 8088, V_{CC} = 5V ±5% for 8088-2)

MINIMUM COMPLEXITY SYSTEM TIMING REQUIREMENTS

Symbol	Parameter	8088		8088-2		Units	Test Conditions
		Min	Max	Min	Max		
TCLCL	CLK Cycle Period	200	500	125	500	ns	
TCLCH	CLK Low Time	118		68		ns	
TCHCL	CLK High Time	69		44		ns	
TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
TCL2CL2	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		20		ns	
TCLDX	Data in Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into 8284 (Notes 1, 2)	35		35		ns	
TCLR1X	RDY Hold Time into 8284 (Notes 1, 2)	0		0		ns	
TRYHCH	READY Setup Time into 8088	118		68		ns	
TCHRYX	READY Hold Time into 8088	30		20		ns	
TRYLCL	READY Inactive to CLK (Note 3)	−8		−8		ns	
THVCH	HOLD Setup Time	35		20		ns	
TINVCH	INTR, NMI, $\overline{\text{TEST}}$ Setup Time (Note 2)	30		15		ns	
TILIH	Input Rise Time (Except CLK)		20		20	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		12	ns	From 2.0V to 0.8V

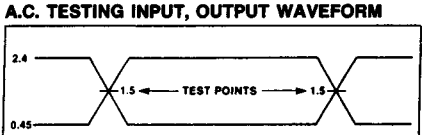
A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

Symbol	Parameter	8088		8088-2		Units	Test Conditions
		Min	Max	Min	Max		
TCLAV	Address Valid Delay	10	110	10	70	ns	
TCLAX	Address Hold Time	10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	ns	
TLHLL	ALE Width	TCLCH−20		TCLCH−10		ns	
TCLLH	ALE Active Delay		80		50	ns	
TCHLL	ALE Inactive Delay		85		55	ns	
TLLAX	Address Hold Time to ALE Inactive	TCHCL−10		TCHCL−10		ns	
TCLDV	Data Valid Delay	10	110	10	60	ns	
TCHDX	Data Hold Time	10		10		ns	
TWHDX	Data Hold Time after $\overline{WR}$	TCLCH−30		TCLCH−30		ns	
TCVCTV	Control Active Delay 1	10	110	10	70	ns	
TCHCTV	Control Active Delay 2	10	110	10	60	ns	
TCVCTX	Control Inactive Delay	10	110	10	70	ns	
TAZRL	Address Float to READ Active	0		0		ns	
TCLRL	$\overline{RD}$ Active Delay	10	165	10	100	ns	
TCLRH	$\overline{RD}$ Inactive Delay	10	150	10	80	ns	
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL−45		TCLCL−40		ns	
TCLHAV	HLDA Valid Delay	10	160	10	100	ns	
TRLRH	$\overline{RD}$ Width	2TCLCL−75		2TCLCL−50		ns	
TWLWH	$\overline{WR}$ Width	2TCLCL−60		2TCLCL−40		ns	
TAVAL	Address Valid to ALE Low	TCLCH−60		TCLCH−40		ns	
TOLOH	Output Rise Time		20		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		12		12	ns	From 2.0V to 0.8V

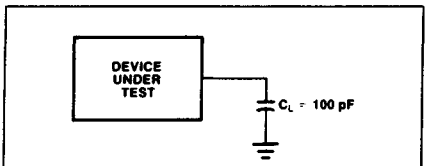
NOTES:
*For Extended Temperature EXPRESS V_{CC} = 5V ±5%
1. Signal at 8284A shown for reference only. See 8284A data sheet for the most recent specifications.
2. Set up requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state (8 ns into T3 state).

A.C. TESTING INPUT, OUTPUT WAVEFORM



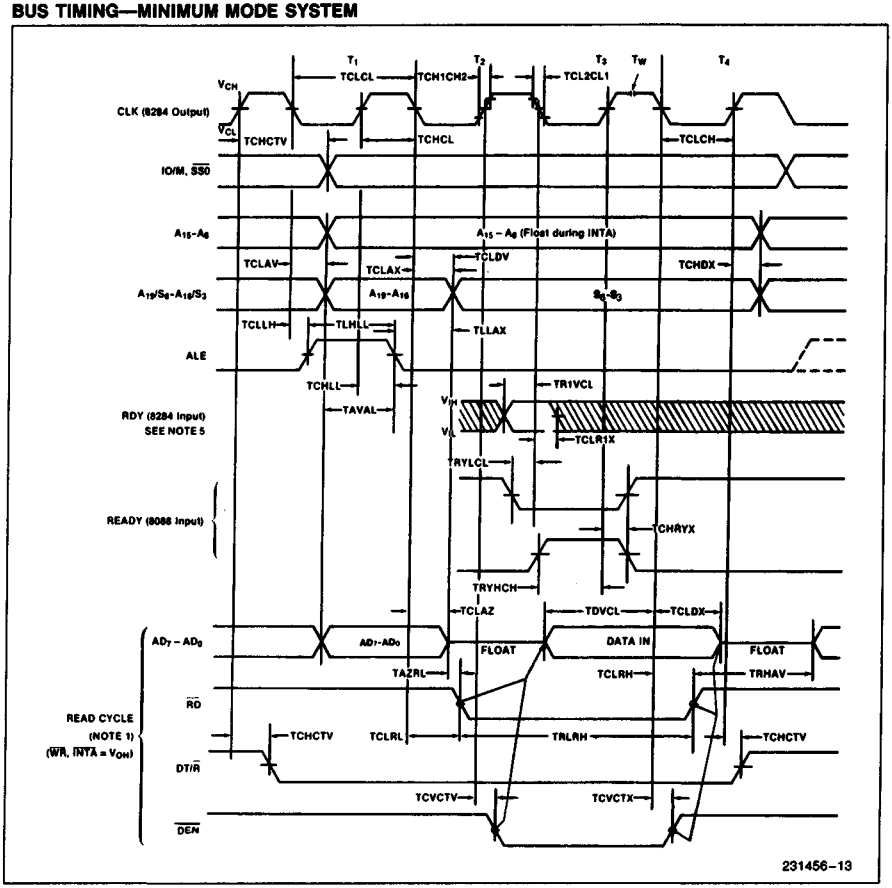
A.C. Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

A.C. TESTING LOAD CIRCUIT



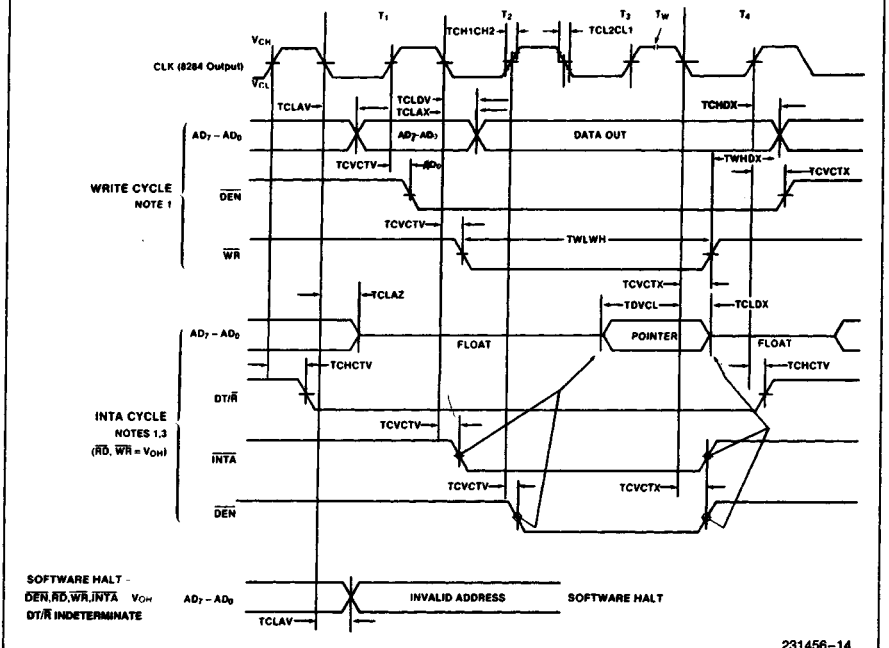
WAVEFORMS

BUS TIMING—MINIMUM MODE SYSTEM



WAVEFORMS (Continued)

BUS TIMING—MINIMUM MODE SYSTEM (Continued)



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NOTES:
1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, T_w to determine if T_w machines states are to be inserted.
3. Two INTA cycles run back-to-back. The 8088 local ADDR/DATA bus is floating during both INTA cycles. Control signals are shown for the second INTA cycle.
4. Signals at 8284 are shown for reference only.
5. All timing measurements are made at 1.5V unless otherwise noted.

A.C. CHARACTERISTICS

MAX MODE SYSTEM (USING 8288 BUS CONTROLLER)

TIMING REQUIREMENTS

Symbol	Parameter	8088		8088-2		Units	Test Conditions
		Min	Max	Min	Max		
TCLCL	CLK Cycle Period	200	500	125	500	ns	
TCLCH	CLK Low Time	118		68		ns	
TCHCL	CLK High Time	69		44		ns	
TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		20		ns	
TCLDX	Data in Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into 8284 (Notes 1, 2)	35		35		ns	
TCLR1X	RDY Hold Time into 8284 (Notes 1, 2)	0		0		ns	
TRYHCH	READY Setup Time into 8088	118		68		ns	
TCHRYX	READY Hold Time into 8088	30		20		ns	
TRYLCL	READY Inactive to CLK (Note 4)	−8		−8		ns	
TINVCH	Setup Time for Recognition (INTR, NMI, TEST) (Note 2)	30		15		ns	
TGVCH	RQ/GT Setup Time	30		15		ns	
TCHGX	RQ Hold Time into 8088	40		30		ns	
TILIH	Input Rise Time (Except CLK)		20		20	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		12	ns	From 2.0V to 0.8V

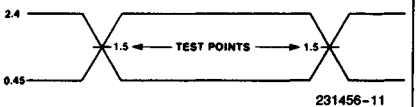
A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES

Symbol	Parameter	8088		8088-2		Units	Test Conditions
		Min	Max	Min	Max		
TCLML	Command Active Delay (Note 1)	10	35	10	35	ns	
TCLMH	Command Inactive Delay (Note 1)	10	35	10	35	ns	
TRYHSH	READY Active to Status Passive (Note 3)		110		65	ns	
TCHSV	Status Active Delay	10	110	10	60	ns	
TCLSH	Status Inactive Delay	10	130	10	70	ns	
TCLAV	Address Valid Delay	10	110	10	70	ns	
TCLAX	Address Hold Time	10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	ns	
TSVLH	Status Valid to ALE High (Note 1)		15		15	ns	
TSVMCH	Status Valid to MCE High (Note 1)		15		15	ns	
TCLLH	CLK Low to ALE Valid (Note 1)		15		15	ns	
TCLMCH	CLK Low to MCE (Note 1)		15		15	ns	
TCHLL	ALE Inactive Delay (Note 1)		15		15	ns	
TCLMCL	MCE Inactive Delay (Note 1)		15		15	ns	
TCLDV	Data Valid Delay	10	110	10	60	ns	
TCHDX	Data Hold Time	10		10		ns	
TCVNV	Control Active Delay (Note 1)	5	45	5	45	ns	C_L = 20–100 pF for All 8088 Outputs in Addition to Internal Loads
TCVNX	Control Inactive Delay (Note 1)	10	45	10	45	ns	
TAZRL	Address Float to Read Active	0		0		ns	
TCLRL	$\overline{RD}$ Active Delay	10	165	10	100	ns	
TCLRH	$\overline{RD}$ Inactive Delay	10	150	10	80	ns	
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL–45		TCLCL–40		ns	
TCHDTL	Direction Control Active Delay (Note 1)		50		50	ns	
TCHDTH	Direction Control Inactive Delay (Note 1)		30		30	ns	
TCLGL	GT Active Delay		85		50	ns	
TCLGH	GT Inactive Delay		85		50	ns	
TRLRH	$\overline{RD}$ Width	2TCLCL–75		2TCLCL–50		ns	
TOLOH	Output Rise Time		20		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		12		12	ns	From 2.0V to 0.8V

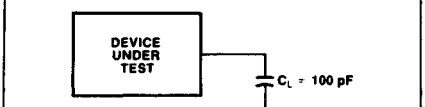
NOTES:
1. Signal at 8284 or 8288 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T3 and wait states.
4. Applies only to T2 state (8 ns into T3 state).

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. Testing; Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

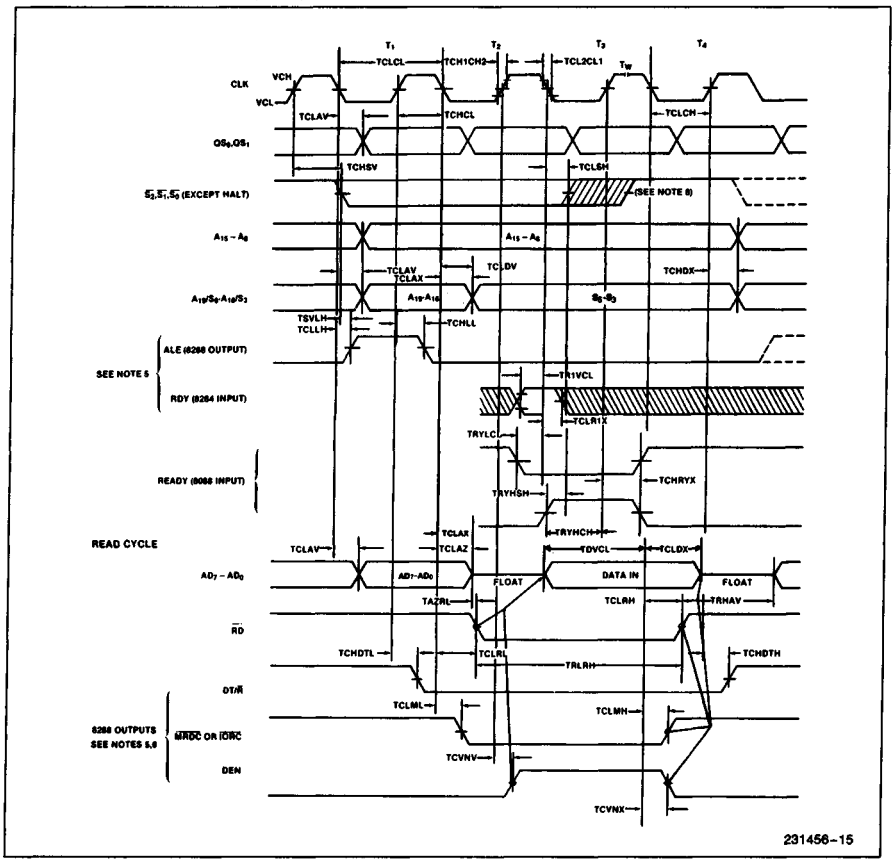
A.C. TESTING LOAD CIRCUIT



C_L Includes Jig Capacitance

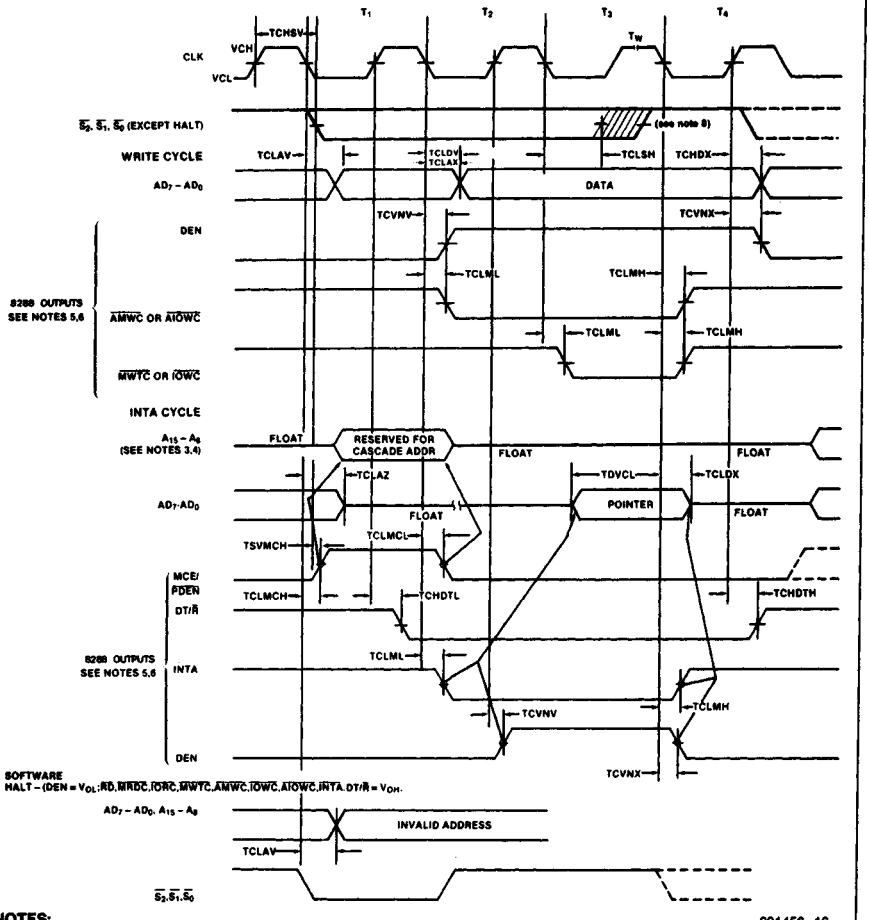
WAVEFORMS

BUS TIMING—MAXIMUM MODE SYSTEM



WAVEFORMS (Continued)

BUS TIMING—MAXIMUM MODE SYSTEM (USING 8288)



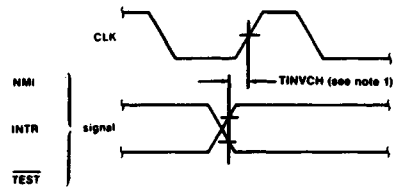
231456-16

NOTES:

1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, T_w to determine if T_w machines states are to be inserted.
3. Cascade address is valid between first and second INTA cycles.
4. Two INTA cycles run back-to-back. The 8088 local ADDR/DATA bus is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
5. Signals at 8284 or 8288 are shown for reference only.
6. The issuance of the 8288 command and control signals (MRDC, MWTC, AMWC, IORC, IOWC, AIOWC, INTA and DEN) lags the active high 8288 CEN.
7. All timing measurements are made at 1.5V unless otherwise noted.
8. Status inactive in state just prior to T_4.

WAVEFORMS (Continued)

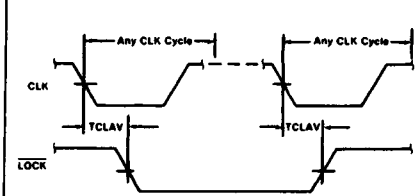
ASYNCHRONOUS SIGNAL RECOGNITION



231456-17

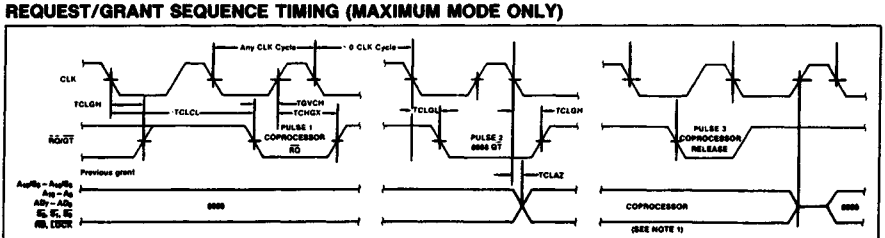
NOTE:
1. Setup requirements for asynchronous signals only to guarantee recognition at next CLK.

BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)



231456-18

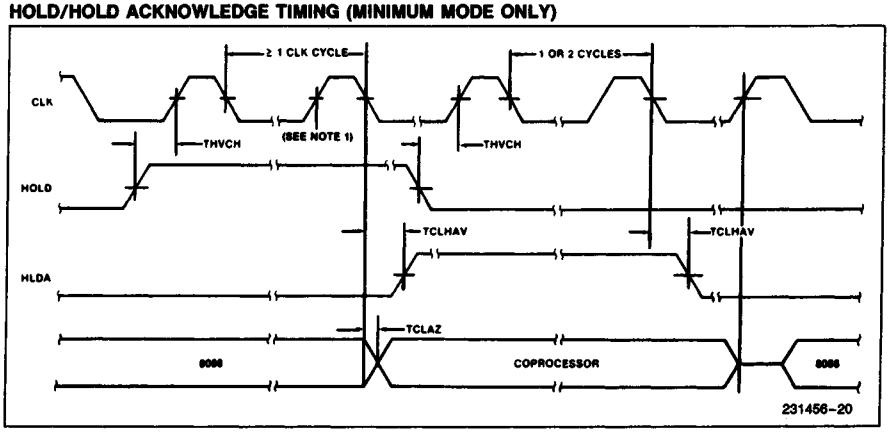
REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)



231456-19

NOTE:
1. The coprocessor may not drive the busses outside the region shown without risking contention.

HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)



231456-20

8086/8088 Instruction Set Summary

Mnemonic and Description	Instruction Code			
DATA TRANSFER				
MOV = Move:	76543210	76543210	76543210	76543210
Register/Memory to/from Register	100010dw	mod reg r/m		
Immediate to Register/Memory	1100011w	mod000r/m	data	data if w = 1
Immediate to Register	1011wreg	data	data if w = 1	
Memory to Accumulator	1010000w	addr-low	addr-high	
Accumulator to Memory	1010001w	addr-low	addr-high	
Register/Memory to Segment Register	10001110	mod0reg r/m		
Segment Register to Register/Memory	10001100	mod0reg r/m		
PUSH = Push:				
Register/Memory	11111111	mod110r/m		
Register	01010reg			
Segment Register	000reg110			
POP = Pop:				
Register/Memory	10001111	mod000r/m		
Register	01011reg			
Segment Register	000reg111			
XCHG = Exchange:				
Register/Memory with Register	1000011w	mod reg r/m		
Register with Accumulator	10010reg			
IN = Input from:				
Fixed Port	1110010w	port		
Variable Port	1110110w			
OUT = Output to:				
Fixed Port	1110011w	port		
Variable Port	1110111w			
XLAT = Translate Byte to AL	11010111			
LEA = Load EA to Register	10001101	mod reg r/m		
LDS = Load Pointer to DS	11000101	mod reg r/m		
LES = Load Pointer to ES	11000100	mod reg r/m		
LAHF = Load AH with Flags	10011111			
SAHF = Store AH into Flags	10011110			
PUSHF = Push Flags	10011100			
POPF = Pop Flags	10011101			

8086/8088 Instruction Set Summary (Continued)

Mnemonic and Description	Instruction Code			
ARITHMETIC	76543210	76543210	76543210	76543210
ADD = Add:				
Reg./Memory with Register to Either	000000dw	mod reg r/m		
Immediate to Register/Memory	100000sw	mod 000 r/m	data	data if s:w = 01
Immediate to Accumulator	0000010w	data	data if w = 1	
ADC = Add with Carry:				
Reg./Memory with Register to Either	000100dw	mod reg r/m		
Immediate to Register/Memory	100000sw	mod 010 r/m	data	data if s:w = 01
Immediate to Accumulator	0001010w	data	data if w = 1	
INC = Increment:				
Register/Memory	1111111w	mod 000 r/m		
Register	01000reg			
AAA = ASCII Adjust for Add	00110111			
BAA = Decimal Adjust for Add	00100111			
SUB = Subtract:				
Reg./Memory and Register to Either	001010dw	mod reg r/m		
Immediate from Register/Memory	100000sw	mod 101 r/m	data	data if s:w = 01
Immediate from Accumulator	0010110w	data	data if w = 1	
SSB = Subtract with Borrow				
Reg./Memory and Register to Either	000110dw	mod reg r/m		
Immediate from Register/Memory	100000sw	mod 011 r/m	data	data if s:w = 01
Immediate from Accumulator	000111w	data	data if w = 1	
DEC = Decrement:				
Register/memory	1111111w	mod 001 r/m		
Register	01001 reg			
NEG = Change sign	1111011w	mod 011 r/m		
CMP = Compare:				
Register/Memory and Register	001110dw	mod reg r/m		
Immediate with Register/Memory	100000sw	mod 111 r/m	data	data if s:w = 01
Immediate with Accumulator	0011110w	data	data if w = 1	
AAS = ASCII Adjust for Subtract	00111111			
DAS = Decimal Adjust for Subtract	00101111			
MUL = Multiply (Unsigned)	1111011w	mod 100 r/m		
IMUL = Integer Multiply (Signed)	1111011w	mod 101 r/m		
AAM = ASCII Adjust for Multiply	11010100	00001010		
DIV = Divide (Unsigned)	1111011w	mod 110 r/m		
IDIV = Integer Divide (Signed)	1111011w	mod 111 r/m		
AAD = ASCII Adjust for Divide	11010101	00001010		
CBW = Convert Byte to Word	10011000			
CWD = Convert Word to Double Word	10011001			

8086/8088 Instruction Set Summary (Continued)

Mnemonic and Description	Instruction Code			
LOGIC	76543210	76543210	76543210	76543210
NOT = Invert	1111011w	mod 010 r/m		
SHL/SAL = Shift Logical/Arithmetic Left	110100vw	mod 100 r/m		
SHR = Shift Logical Right	110100vw	mod 101 r/m		
SAR = Shift Arithmetic Right	110100vw	mod 111 r/m		
ROL = Rotate Left	110100vw	mod 000 r/m		
ROR = Rotate Right	110100vw	mod 001 r/m		
RCL = Rotate Through Carry Flag Left	110100vw	mod 010 r/m		
RCR = Rotate Through Carry Right	110100vw	mod 011 r/m		
AND = And:				
Reg./Memory and Register to Either	001000dw	mod reg r/m		
Immediate to Register/Memory	1000000w	mod 100 r/m	data	data if w = 1
Immediate to Accumulator	0010010w	data	data if w = 1	
TEST = And Function to Flags. No Result:				
Register/Memory and Register	1000010w	mod reg r/m		
Immediate Data and Register/Memory	1111011w	mod 000 r/m	data	data if w = 1
Immediate Data and Accumulator	1010100w	data	data if w = 1	
OR = Or:				
Reg./Memory and Register to Either	000010dw	mod reg r/m		
Immediate to Register/Memory	1000000w	mod 001 r/m	data	data if w = 1
Immediate to Accumulator	0000110w	data	data if w = 1	
XOR = Exclusive or:				
Reg./Memory and Register to Either	001100dw	mod reg r/m		
Immediate to Register/Memory	1000000w	mod 110 r/m	data	data if w = 1
Immediate to Accumulator	0011010w	data	data if w = 1	
STRING MANIPULATION				
REP = Repeat	1111001z			
MOVS = Move Byte/Word	1010010w			
CMPS = Compare Byte/Word	1010011w			
SCAS = Scan Byte/Word	1010111w			
LODS = Load Byte/Wd to AL/AX	1010110w			
STOS = Stor Byte/Wd from AL/A	1010101w			
CONTROL TRANSFER				
CALL = Call:				
Direct Within Segment	11101000	disp-low	disp-high	
Indirect Within Segment	11111111	mod 010 r/m		
Direct Intersegment	10011010	offset-low	offset-high	
		seg-low	seg-high	
Indirect Intersegment	11111111	mod 011 r/m		

8086/8088 Instruction Set Summary (Continued)

Mnemonic and Description	Instruction Code		
JMP = Unconditional Jump:	76543210	76543210	76543210
Direct Within Segment	11101001	disp-low	disp-high
Direct Within Segment-Short	11101011	disp	
Indirect Within Segment	11111111	mod 100 r/m	
Direct Intersegment	11101010	offset-low	offset-high
		seg-low	seg-high
Indirect Intersegment	11111111	mod 101 r/m	
RET = Return from CALL:			
Within Segment	11000011		
Within Seg Adding Immed to SP	11000010	data-low	data-high
Intersegment	11001011		
Intersegment Adding Immediate to SP	11001010	data-low	data-high
JE/JZ = Jump on Equal/Zero	01110100	disp	
JL/JNGE = Jump on Less/Not Greater or Equal	01111100	disp	
JLE/JNG = Jump on Less or Equal/ Not Greater	01111110	disp	
JB/JNAE = Jump on Below/Not Above or Equal	01110010	disp	
JBE/JNA = Jump on Below or Equal/ Not Above	01110110	disp	
JP/JPE = Jump on Parity/Parity Even	01111010	disp	
JO = Jump on Overflow	01110000	disp	
JS = Jump on Sign	01111000	disp	
JNE/JNZ = Jump on Not Equal/Not Zero	01110101	disp	
JNL/JGE = Jump on Not Less/Greater or Equal	01111101	disp	
JNLE/JG = Jump on Not Less or Equal/ Greater	01111111	disp	
JNB/JAE = Jump on Not Below/Above or Equal	01110011	disp	
JNBE/JA = Jump on Not Below or Equal/Above	01110111	disp	
JNP/JPO = Jump on Not Par/Par Odd	01111011	disp	
JNO = Jump on Not Overflow	01110001	disp	
JNS = Jump on Not Sign	01111001	disp	
LOOP = Loop CX Times	11100010	disp	
LOOPZ/LOOPE = Loop While Zero/Equal	11100001	disp	
LOOPNZ/LOOPNE = Loop While Not Zero/Equal	11100000	disp	
JCXZ = Jump on CX Zero	11100011	disp	
INT = Interrupt			
Type Specified	11001101	type	
Type 3	11001100		
INTO = Interrupt on Overflow	11001110		
IRET = Interrupt Return	11001111		

8086/8088 Instruction Set Summary (Continued)

Mnemonic and Description	Instruction Code	
	76543210	76543210
PROCESSOR CONTROL		
CLC = Clear Carry	11111000	
CMC = Complement Carry	11110101	
STC = Set Carry	11111001	
CLD = Clear Direction	11111100	
STD = Set Direction	11111101	
CLI = Clear Interrupt	11111010	
STI = Set Interrupt	11111011	
HLT = Halt	11110100	
WAIT = Wait	10011011	
ESC = Escape (to External Device)	11011xxx	mod x x x r/m
LOCK = Bus Lock Prefix	11110000	

NOTES:
AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value
Greater = more positive:
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction; if w = 0 then byte instruction
if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16 bits, disp-high is absent
if mod = 10 then DISP = disp-high; disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)
*except if mod = 00 and r/m = then EA = disp-high: disp-low.
if s:w = 01 then 16 bits of immediate data form the operand
if s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand
if v = 0 then "count" = 1; if v = 1 then "count" in (CL) register
x = don't care
z is used for string primitives for comparison with ZF FLAG
SEGMENT OVERRIDE PREFIX

001 reg 110

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:
FLAGS =
X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

8253/8253-5
PROGRAMMABLE INTERVAL TIMER

- **MCS-85™ Compatible 8253-5**
- **3 Independent 16-Bit Counters**
- **DC to 2.6 MHz**
- **Programmable Counter Modes**
- **Count Binary or BCD**
- **Single +5V Supply**
- **Available in EXPRESS**
  - **— Standard Temperature Range**
  - **— Extended Temperature Range**

The Intel® 8253 is a programmable counter/timer device designed for use as an Intel microcomputer peripheral. It uses NMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP.

It is organized as 3 independent 16-bit counters, each with a count rate of up to 2.6 MHz. All modes of operation are software programmable.

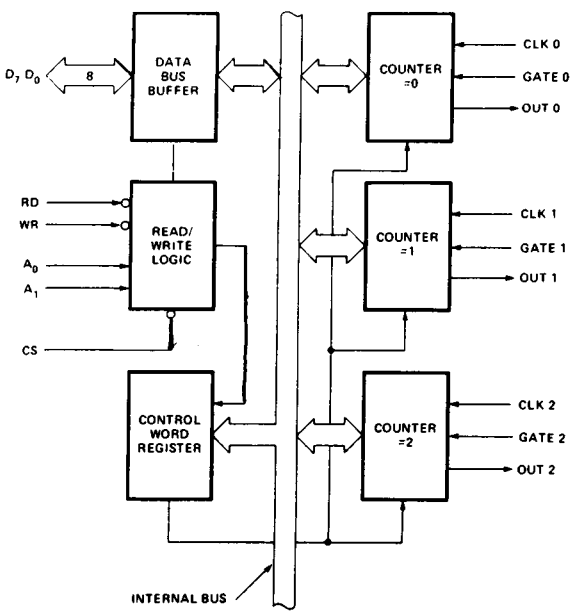


Figure 1. Block Diagram

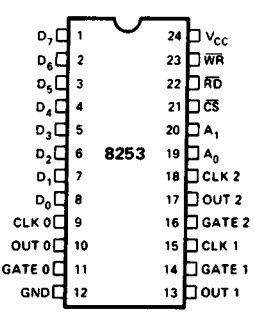


Figure 2. Pin Configuration

November 1986
Order Number: 231306-001

FUNCTIONAL DESCRIPTION

General

The 8253 is programmable interval timer/counter specifically designed for use with the Intel™ Microcomputer systems. Its function is that of a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 8253 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in systems software, the programmer configures the 8253 to match his requirements, initializes one of the counters of the 8253 with the desired quantity, then upon command the 8253 will count out the delay and interrupt the CPU when it has completed its tasks. It is easy to see that the software overhead is minimal and that multiple delays can easily be maintained by assignment of priority levels.

Other counter/timer functions that are non-delay in nature but also common to most microcomputers can be implemented with the 8253.

- Programmable Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real Time Clock
- Digital One-Shot
- Complex Motor Controller

Data Bus Buffer

The 3-state, bi-directional, 8-bit buffer is used to interface the 8253 to the system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput CPU instructions. The Data Bus Buffer has three basic functions.

1. Programming the MODES of the 8253.
2. Loading the count registers.
3. Reading the count values.

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and in turn generates control signals for overall device operation. It is enabled or disabled by CS so that no operation can occur to change the function unless the device has been selected by the system logic.

$\overline{RD}$ (Read)

A "low" on this input informs the 8253 that the CPU is inputting data in the form of a counters value.

$\overline{WR}$ (Write)

A "low" on this input informs the 8253 that the CPU is outputting data in the form of mode information or loading counters.

A0, A1

These inputs are normally connected to the address bus. Their function is to select one of the three counters to be operated on and to address the control word register for mode selection.

$\overline{CS}$ (Chip Select)

A "low" on this input enables the 8253. No reading or writing will occur unless the device is selected. The $\overline{CS}$ input has no effect upon the actual operation of the counters.

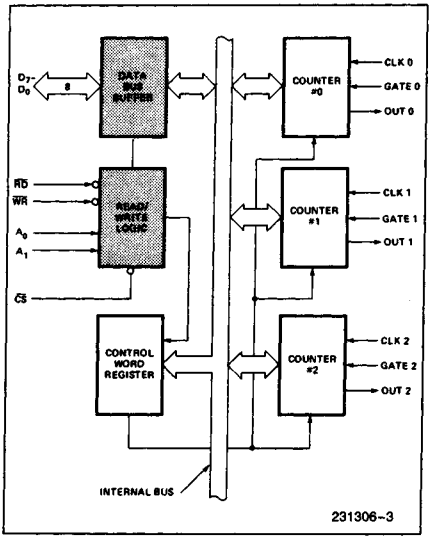


Figure 3. Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation 3-State
1	X	X	X	X	Disable 3-State
0	1	1	X	X	No-Operation 3-State

Control Word Register

The Control Word Register is selected when A0, A1 are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operation MODE of each counter, selection of binary or BCD counting and the loading of each count register.

The Control Word Register can only be written into; no read operation of its contents is available.

Counter #0, Counter #1, Counter #2

These three functional blocks are identical in operation so only a single counter will be described. Each Counter consists of a single, 16-bit, pre-settable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of MODES stored in the Control Word Register.

The counters are fully independent and each can have separate MODE configuration and counting operation, binary or BCD. Also, there are special features in the control word that handle the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications and special commands and logic are included in the 8253 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

8253 SYSTEM INTERFACE

The 8253 is a component of the Intel™ Microcomputer systems and interfaces in the same manner as all other peripherals of the family. It is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an Intel 8205 for larger systems.

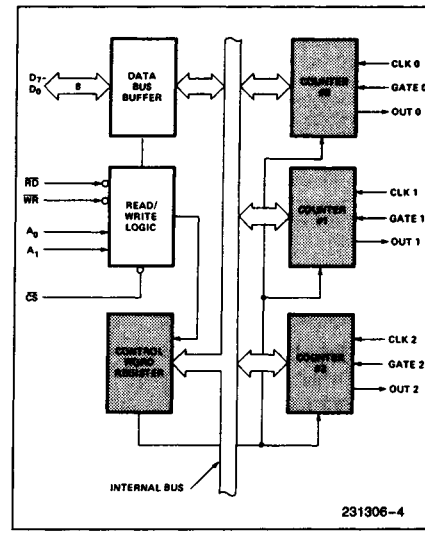


Figure 4. Block Diagram Showing Control Word Register and Counter Functions

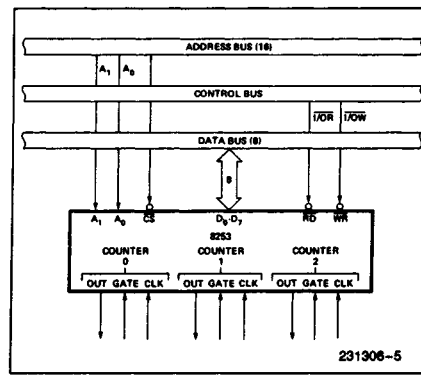


Figure 5. 8253 System Interface

OPERATIONAL DESCRIPTION

General

The complete functional definition of the 8253 is programmed by the systems software. A set of control words *must* be sent out by the CPU to initialize each counter of the 8253 with the desired MODE and quantity information. Prior to initialization, the MODE, count, and output of all counters is undefined. These control words program the MODE, Loading sequence and selection of binary or BCD counting.

Once programmed, the 8253 is ready to perform whatever timing tasks it is assigned to accomplish.

The actual counting operation of each counter is completely independent and additional logic is provided on-chip so that the usual problems associated with efficient monitoring and management of external, asynchronous events or rates to the microcomputer system have been eliminated.

Programming the 8253

All of the MODES for each counter are programmed by the systems software by simple I/O operations.

Each counter of the 8253 is individually programmed by writing a control word into the Control Word Register. (A0, A1 = 11)

Control Word Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Definition Of Control

SC—SELECT COUNTER:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

RL—READ/LOAD:

RL1	RL0	
0	0	Counter Latching operation (see READ/WRITE Procedure Section).
1	0	Read/Load most significant byte only.
0	1	Read/Load least significant byte only.
1	1	Read/Load least significant byte first, then most significant byte.

M—MODE:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD:

0	Binary Counter 16-Bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

Counter Loading

The count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits), followed by a rising edge and a falling edge of the clock. Any read of the counter prior to that falling clock edge may yield invalid data.

MODE DEFINITION

MODE 0: Interrupt on Terminal Count. The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached, the output will go high and remain high until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count has been reached.

Rewriting a counter register during counting results in the following:

(1) Write 1st byte stops the current counting.
(2) Write 2nd byte starts the new count.

MODE 1: Programmable One-Shot. The output will go low on the count following the rising edge of the gate input.

The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

MODE 2: Rate Generator. Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Thus, the gate input can be used to synchronize the counter.

When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

MODE 3: Square Wave Rate Generator. Similar to MODE 2 except that the output will remain high until one half the count has been completed (or even numbers) and go low for the other half of the count. This is accomplished by decrementing the counter by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the clock by 2. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by 2 until timeout. Then the whole process is repeated. In this way, if the count is odd, the output will be high for (N + 1)/2 counts and low for (N − 1)/2 counts.

In Modes 2 and 3, if a CLK source other than the system clock is used, GATE should be pulsed immediately following $\overline{WR}$ of a new count value.

MODE 4: Software Triggered Strobe. After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

If the count register is reloaded during counting, the new count will be loaded on the next CLK pulse. The count will be inhibited while the GATE input is low.

MODE 5: Hardware Triggered Strobe. The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

Signal Status Modes	Low Or Going Low	Rising	High
0	Disables counting	—	Enables counting
1	—	1) Initiates counting 2) Resets output after next clock	—
2	1) Disables counting 2) Sets output immediately high	1) Reloads counter 2) Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	1) Reloads counter 2) Initiates counting	Enables counting
4	Disables counting	—	Enables counting
5	—	Initiates counting	—

Figure 6. Gate Pin Operations Summary

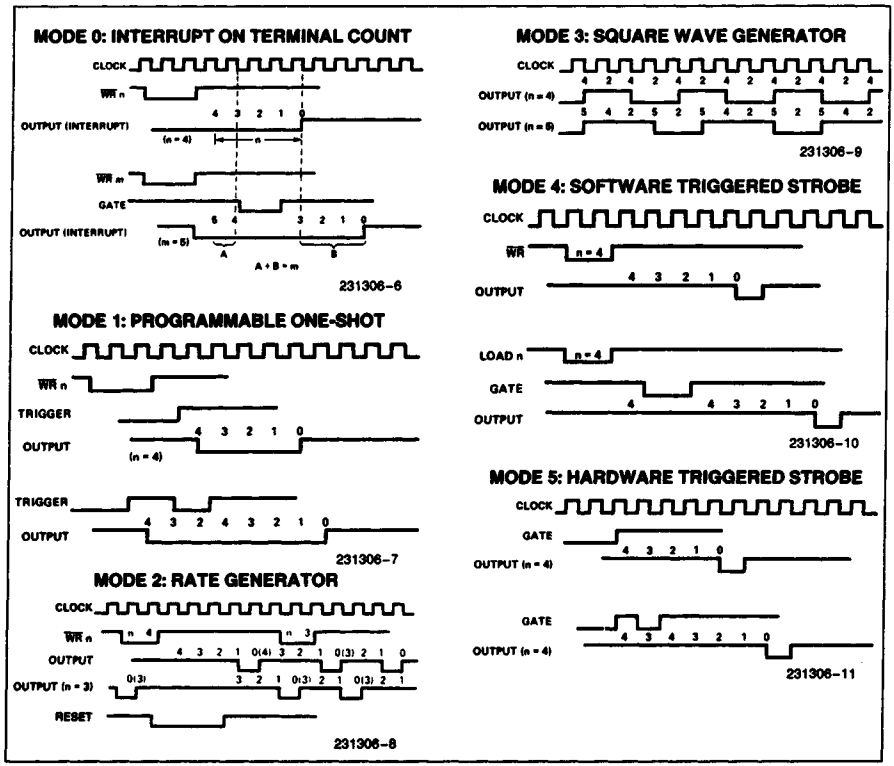


Figure 7. 8253 Timing Diagrams

8253 READ/WRITE PROCEDURE

Write Operations

The systems software must program each counter of the 8253 with the mode and quantity desired. The programmer must write out to the 8253 a MODE control word and the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

The actual order of the programming is quite flexible. Writing out of the MODE control word can be in any sequence of counter selection, e.g., counter #0 does not have to be first or counter #2 last. Each counter's MODE control word register has a separate address so that its loading is completely sequence independent. (SC0, SC1).

The loading of the Count Register with the actual count value, however, must be done in exactly the sequence programmed in the MODE control word (RL0, RL1). This loading of the counter's count register is still sequence independent like the MODE control word loading, but when a selected count register is to be loaded it *must* be loaded with the number of bytes programmed in the MODE control word (RL0, RL1). The one or two bytes to be loaded in the count register do not have to follow the associated MODE control word. They can be programmed at any time following the MODE control word loading as long as the correct number of bytes is loaded in order.

All counters are down counters. Thus, the value loaded into the count register will actually be decremented. Loading all zeros into a count register will result in the maximum count (2^{16} for Binary or 10^4 for BCD). In MODE 0 the new count will not restart until the load has been completed. It will accept one of two bytes depending on how the MODE control words (RL0, RL1) are programmed. Then proceed with the restart operation.

	MODE Control Word Counter n
LSB	Counter Register byte Counter n
MSB	Counter Register byte Counter n

NOTE:
Format shown is a simple example of loading the 8253 and does not imply that it is the only format that can be used.

Figure 8. Programming Format

			A1	A0
No. 1		MODE Control Word Counter 0	1	1
No. 2		MODE Control Word Counter 1	1	1
No. 3		MODE Control Word Counter 2	1	1
No. 4	LSB	Count Register Byte Counter 1	0	1
No. 5	MSB	Count Register Byte Counter 1	0	1
No. 6	LSB	Count Register Byte Counter 2	1	0
No. 7	MSB	Count Register Byte Counter 2	1	0
No. 8	LSB	Count Register Byte Counter 0	0	0
No. 9	MSB	Count Register Byte Counter 0	0	0

NOTE:
The exclusive addresses of each counter's count register make the task of programming the 8253 a very simple matter, and maximum effective use of the device will result if this feature is fully initilized.

Figure 9. Alternate Programming Formats

Read Operations

In most counter applications it becomes necessary to read the value of the count in progress and make a computational decision based on this quantity. Event counters are probably the most common application that uses this function. The 8253 contains logic that will allow the programmer to easily read the contents of any of the three counters without disturbing the actual count in progress.

There are two methods that the programmer can use to read the value of the counters. The first method involves the use of simple I/O read operations of the selected counter. By controlling the A0, A1 inputs to the 8253 the programmer can select the counter to be read (remember that no read operation of the mode register is allowed A0, A1-11). The only requirement with this method is that in order to assure a stable count reading the actual operation of the selected counter *must be inhibited* either by controlling the Gate input or by external logic that inhibits the clock input. The contents of the counter selected will be available as follows:

First I/O Read contains the least significant byte (LSB).

Second I/O Read contains the most significant byte (MSB).

Due to the internal logic of the 8253 it is absolutely necessary to complete the entire reading procedure. If two bytes are programmed to be read, then two bytes *must* be read before any loading WR command can be sent to the same counter.

Read Operation Chart

A1	A0	RD	
0	0	0	Read Counter No. 0
0	1	0	Read Counter No. 1
1	0	0	Read Counter No. 2
1	1	0	Illegal

Reading While Counting

In order for the programmer to read the contents of any counter without effecting or disturbing the counting operation the 8253 has special internal logic that can be accessed using simple $\overline{WR}$ commands to the MODE register. Basically, when the programmer wishes to read the contents of a selected counter "on the fly" he loads the MODE register with a special code which latches the present count value into a storage register so that its contents contain an accurate, stable quantity. The programmer then issues a normal read command to the selected counter and the contents of the latched register is available.

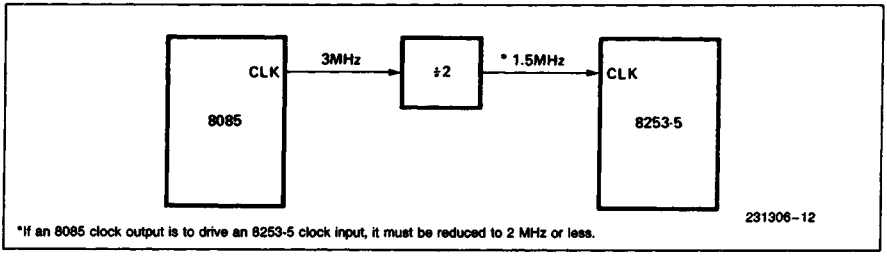
MODE Register for Latching Count

A0, A1 = 11

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

SC1, SC0— specify counter to be latched.
D5, D4 — 00 designates counter latching operation.
X — don't care.

The same limitation applies to this mode of reading the counter as the previous method. That is, it is mandatory to complete the entire read operation as programmed. This command has no effect on the counter's mode.



*If an 8085 clock output is to drive an 8253-5 clock input, it must be reduced to 2 MHz or less.

Figure 10. MCS-85™ Clock Interface*

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .....0°C to 70°C
Storage Temperature .....−65°C to +150°C
Voltage On Any Pin
with Respect to Ground.....−0.5V to 7V
Power Dissipation .....1 Watt

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10%*

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.2	V_{CC} + .5V	V	
V_{OL}	Output Low Voltage		0.45	V	(Note 1)
V_{OH}	Output High Voltage	2.4		V	(Note 2)
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0.45V
I_{CC}	V_{CC} Supply Current		140	mA	

CAPACITANCE T_A = 25°C, V_{CC} = GND = 0V

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5.0V ±10%, GND = 0V*

Bus Parameters(3)

READ CYCLE

Symbol	Parameter	8253		8253-5		Unit
		Min	Max	Min	Max	
t_{AR}	Address Stable before $\overline{READ}$	50		30		ns
t_{RA}	Address Hold Time for $\overline{READ}$	5		5		ns
t_{RR}	$\overline{READ}$ Pulse Width	400		300		ns
t_{RD}	Data Delay from $\overline{READ}$(4)		300		200	ns
t_{DF}	$\overline{READ}$ to Data Floating	25	125	25	100	ns
t_{RV}	Recovery Time between $\overline{READ}$ and Any Other Control Signal	1		1		μs

A.C. CHARACTERISTICS (Continued)

WRITE CYCLE

Symbol	Parameter	8253		8253-5		Unit
		Min	Max	Min	Max	
t_{AW}	Address Stable before $\overline{WRITE}$	50		30		ns
t_{WA}	Address Hold Time for $\overline{WRITE}$	30		30		ns
t_{WW}	$\overline{WRITE}$ Pulse Width	400		300		ns
t_{DW}	Data Set Up Time for $\overline{WRITE}$	300		250		ns
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		30		ns
t_{RV}	Recovery Time between $\overline{WRITE}$ and Any Other Control Signal	1		1		μs

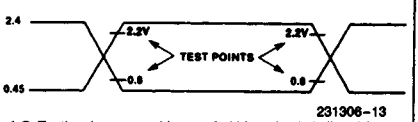
CLOCK AND GATE TIMING

Symbol	Parameter	8253		8253-5		Unit
		Min	Max	Min	Max	
t_{CLK}	Clock Period	380	dc	380	dc	ns
t_{PWH}	High Pulse Width	230		230		ns
t_{PWL}	Low Pulse Width	150		150		ns
t_{GW}	Gate Width High	150		150		ns
t_{GL}	Gate Width Low	100		100		ns
t_{GS}	Gate Set Up Time to CLK ↑	100		100		ns
t_{GH}	Gate Hold Time after CLK ↑	50		50		ns
t_{OD}	Output Delay from CLK ↓ (4)		400		400	ns
t_{ODG}	Output Delay from Gate ↓ (4)		300		300	ns

NOTES:
1. I_{OL} = 2.2 mA.
2. I_{OH} = −400 μA.
3. AC timings measured at V_{OH} 2.2, V_{OL} = 0.8.
4. C_L = 150 pF.

*For Extended Temperature EXPRESS, use M8253 electrical parameters.

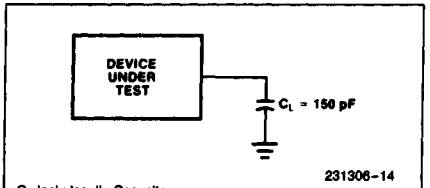
A.C. TESTING INPUT, OUTPUT WAVEFORM



231306-13

A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.2V for a Logic "1" and 0.8V for a Logic "0".

A.C. TESTING LOAD CIRCUIT

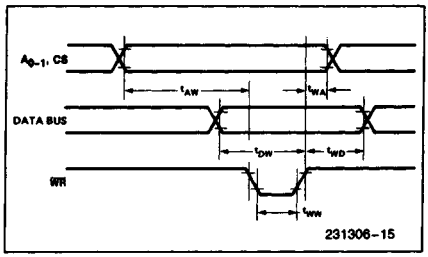


231306-14

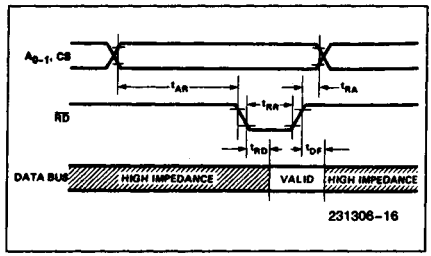
C_L Includes Jig Capacitance

WAVEFORMS

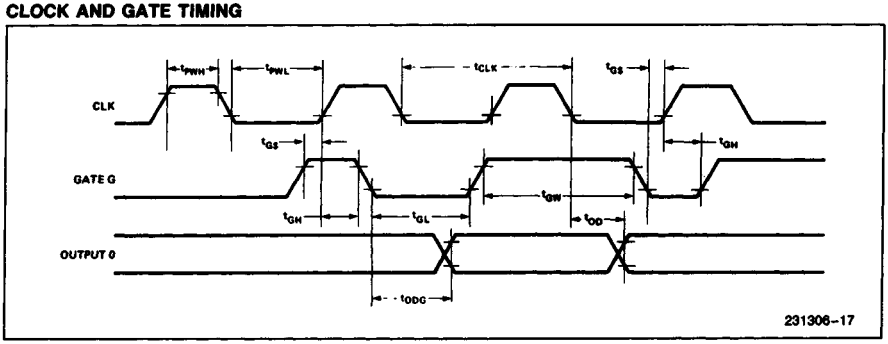
WRITE TIMING



READ TIMING



CLOCK AND GATE TIMING



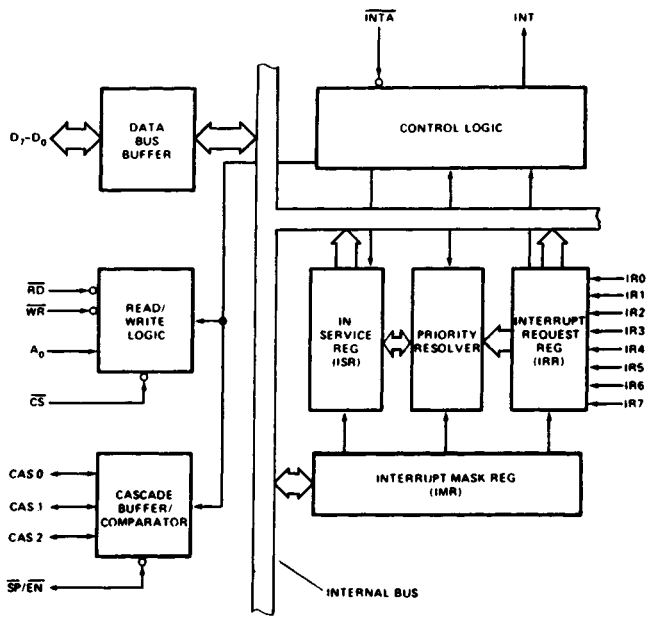
8259A
PROGRAMMABLE INTERRUPT CONTROLLER
8259A/8259A-2/8259A-8

- **8086, 8088 Compatible**
- **MCS-80®, MCS-85® Compatible**
- **Eight-Level Priority Controller**
- **Expandable to 64 Levels**
- **Programmable Interrupt Modes**
- **Individual Request Mask Capability**
- **Single +5V Supply (No Clocks)**
- **28-Pin Dual-In-Line Package**
- **Available in EXPRESS**
  - **— Standard Temperature Range**
  - **— Extended Temperature Range**

The Intel 8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.

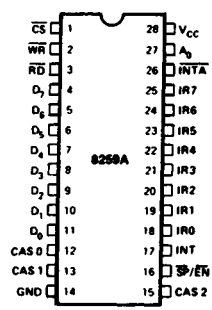
The 8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

The 8259A is fully upward compatible with the Intel 8259. Software originally written for the 8259 will operate the 8259A in all 8259 equivalent modes (MCS-80/85, Non-Buffered, Edge Triggered).



231468-1

Figure 1. Block Diagram



231468-2

Figure 2. Pin Configuration

October 1986
Order Number: 231468-001

Table 1. Pin Description

Symbol	Pin No.	Type	Name and Function
V_{CC}	28	I	**SUPPLY:** +5V Supply.
GND	14	I	**GROUND**
$\overline{CS}$	1	I	**CHIP SELECT:** A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the 8259A. INTA functions are independent of CS.
$\overline{WR}$	2	I	**WRITE:** A low on this pin when CS is low enables the 8259A to accept command words from the CPU.
$\overline{RD}$	3	I	**READ:** A low on this pin when CS is low enables the 8259A to release status onto the data bus for the CPU.
D_7-D_0	4-11	I/O	**BIDIRECTIONAL DATA BUS:** Control, status and interrupt-vector information is transferred via this bus.
CAS_0-CAS_2	12, 13, 15	I/O	**CASCADE LINES:** The CAS lines form a private 8259A bus to control a multiple 8259A structure. These pins are outputs for a master 8259A and inputs for a slave 8259A.
$\overline{SP}/\overline{EN}$	16	I/O	**SLAVE PROGRAM/ENABLE BUFFER:** This is a dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers (EN). When not in the buffered mode it is used as an input to designate a master (SP = 1) or slave (SP = 0).
INT	17	O	**INTERRUPT:** This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IR_0-IR_7	18-25	I	**INTERRUPT REQUESTS:** Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).
$\overline{INTA}$	26	I	**INTERRUPT ACKNOWLEDGE:** This pin is used to enable 8259A interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
A_0	27	I	**A0 ADDRESS LINE:** This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the 8259A to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for 8086, 8088).

FUNCTIONAL DESCRIPTION

Interrupts in Microcomputer Systems

Microcomputer system design requires that I.O devices such as keyboards, displays, sensors and other components receive servicing in a an efficient manner so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

The most common method of servicing such devices is the *Polled* approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuous polling cycle and that such a method would have a serious detrimental effect on system throughput, thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desirable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete, however, the processor would resume exactly where it left off.

This method is called *Interrupt*. It is easy to see that system throughput would drastically increase, and thus more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt to the CPU based on this determination.

Each peripheral device or structure usually has a special program or "routine" that is associated with its specific functional or operational requirements; this is referred to as a "service routine". The PIC, after issuing an Interrupt to the CPU, must somehow input information into the CPU that can "point" the Program Counter to the service routine associated with the requesting device. This "pointer" is an address in a vectoring table and will often be referred to, in this document, as vectoring data.

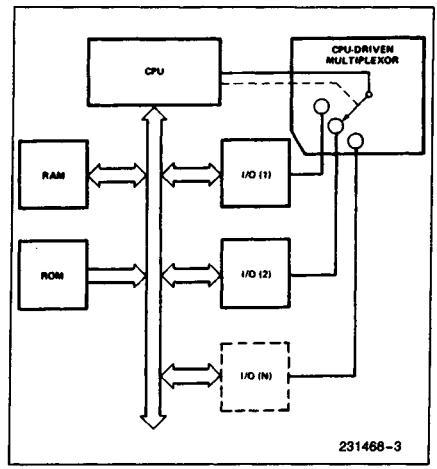


Figure 3a. Polled Method

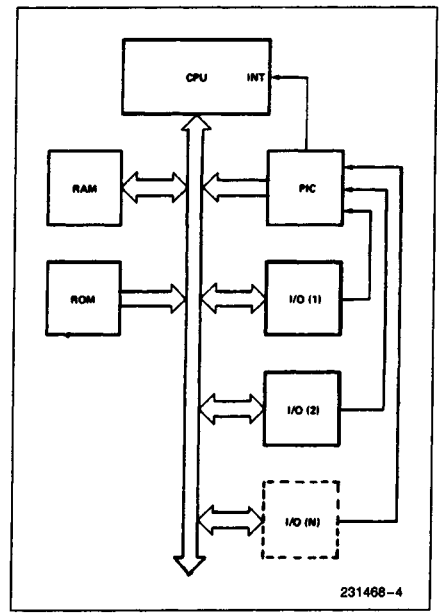


Figure 3b. Interrupt Method

The 8259A is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight levels or requests and has built-in features for expandability to other 8259A's (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the 8259A can be configured to match his system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

INTERRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service (ISR). The IRR is used to store all the interrupt levels which are requesting service; and the ISR is used to store all the interrupt levels which are being serviced.

PRIORITY RESOLVER

This logic block determines the priorites of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during $\overline{INTA}$ pulse.

INTERRUPT MASK REGISTER (IMR)

The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower quality.

INT (INTERRUPT)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with the 8080A, 8085A and 8086 input levels.

$\overline{INTA}$ (INTERRUPT ACKNOWLEDGE)

$\overline{INTA}$ pulses will cause the 8259A to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the 8259A.

DATA BUS BUFFER

This 3-state, bidirectional 8-bit buffer is used to interface the 8259A to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

READ/WRITE CONTROL LOGIC

The function of this block is to accept OUTput commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the 8259A to be transferred onto the Data Bus.

$\overline{CS}$ (CHIP SELECT)

A LOW on this input enables the 8259A. No reading or writing of the chip will occur unless the device is selected.

$\overline{WR}$ (WRITE)

A LOW on this input enables the CPU to write control words (ICWs and OCWs) to the 8259A.

$\overline{RD}$ (READ)

A LOW on this input enables the 8259A to send the status of the Interrupt Request Register (IRR), In Service Register (ISR), the Interrupt Mask Register (IMR), or the Interrupt level onto the Data Bus.

A_0

This input signal is used in conjunction with $\overline{WR}$ and $\overline{RD}$ signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

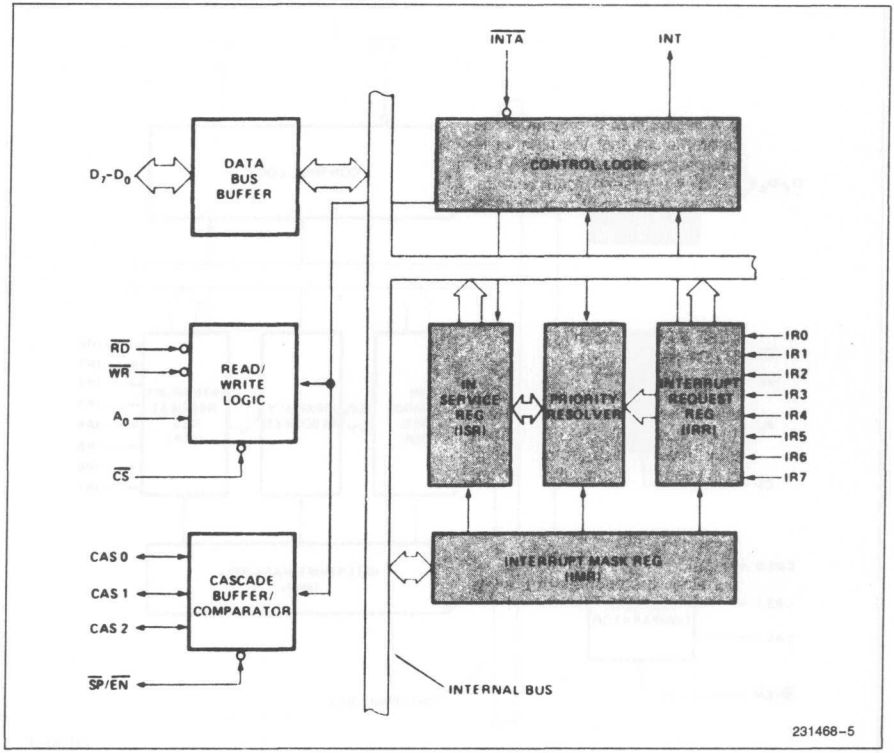


Figure 4a. 8259A Block Diagram

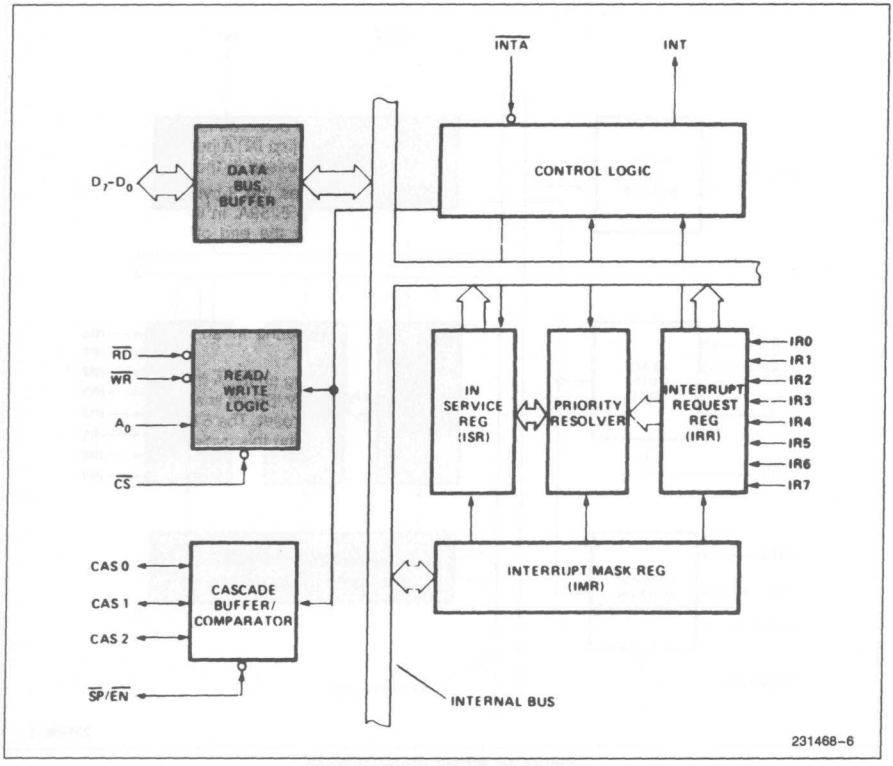


Figure 4b. 8259A Block Diagram

THE CASCADE BUFFER/COMPARATOR

This function block stores and compares the IDs of all 8259A's used in the system. The associated three I/O pins (CAS0-2) are outputs when the 8259A is used as a master and are inputs when the 8259A is used as a slave. As a master, the 8259A sends the ID of the interrupting slave device onto the CAS0–2 lines. The slave thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive $\overline{INTA}$ pulses. (See section "Cascading the 8259A".)

INTERRUPT SEQUENCE

The powerful features of the 8259A in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specific interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

The events occur as follows in an MCS-80/85 system:

1. One or more of the INTERRUPT REQUEST lines (IR7–0) are raised high, setting the corresponding IRR bit(s).
2. The 8259A evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{INTA}$ pulse.
4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The 8259A will also release a CALL instruction code (11001101) onto the 8-bit Data Bus through its D7–0 pins.
5. This CALL instruction will initiate two more $\overline{INTA}$ pulses to be sent to the 8259A from the CPU group.
6. These two $\overline{INTA}$ pulses allow the 8259A to release its preprogrammed subroutine address onto the Data Bus. The lower 8-bit address is released at the first $\overline{INTA}$ pulse and the higher 8-bit address is released at the second $\overline{INTA}$ pulse.
7. This completes the 3-byte CALL instruction released by the 8259A. In the AEOI mode the ISR bit is reset at the end of the third $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occuring in an 8086 system are the same until step 4.

4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The 8259A does not drive the Data Bus during this cycle.
5. The 8086 will initiate a second $\overline{INTA}$ pulse. During this pulse, the 8259A releases an 8-bit pointer onto the Data Bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode the ISR bit is reset at the end of the second $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e., the request was too short in duration) the 8259A will issue an interrupt level 7. Both the vectoring bytes and the CAS lines will look like an interrupt level 7 was requested.

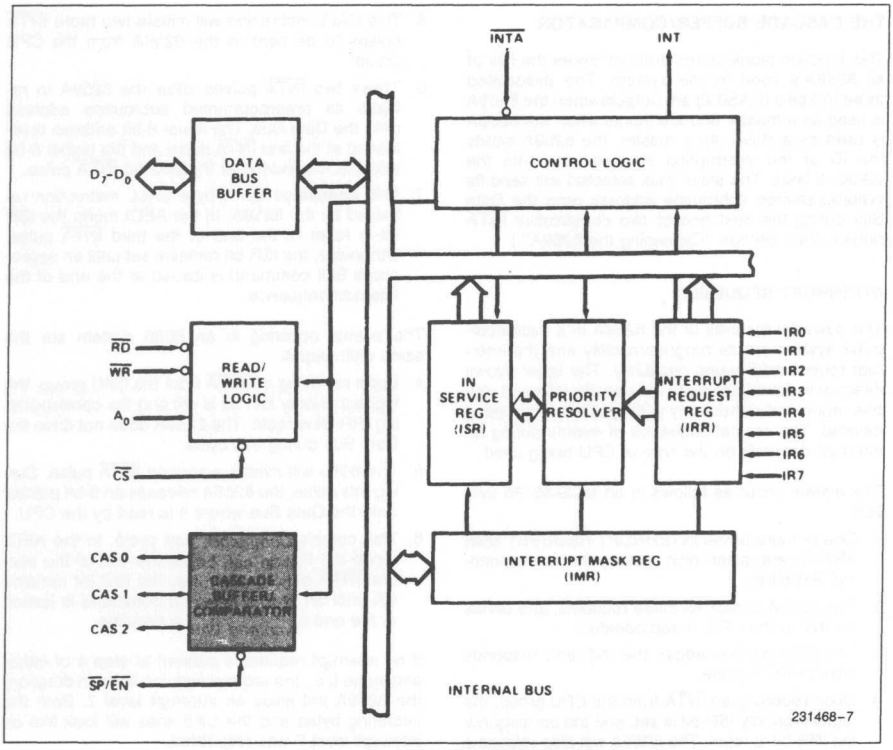


Figure 4c. 8259A Block Diagram

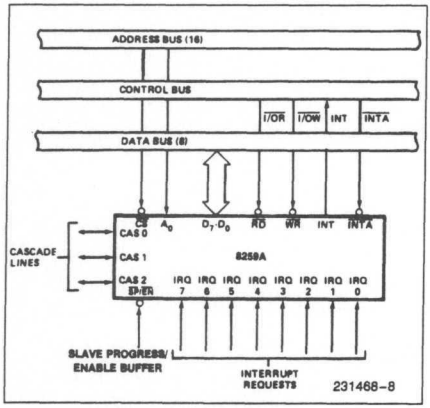


Figure 5. 8259A Interface to Standard System Bus

INTERRUPT SEQUENCE OUTPUTS

MCS-80®, MCS-85®

This sequence is timed by three $\overline{INTA}$ pulses. During the first $\overline{INTA}$ pulse the CALL opcode is enabled onto the data bus.

Content of First Interrupt Vector Byte

	D7	D6	D5	D4	D3	D2	D1	D0
CALL CODE	1	1	0	0	1	1	0	1

During the second $\overline{INTA}$ pulse the lower address of the appropriate service routine is enabled onto the data bus. When Interval = 4 bits A_5–A_7 are programmed, while A_0–A_4 are automatically inserted by the 8259A. When Interval = 8 only A_6 and A_7 are programmed, while A_0–A_5 are automatically inserted.

Content of Second Interrupt Vector Byte

IR	Interval = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR	Interval = 8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

During the third INTA pulse the higher address of the appropriate service routine, which was programmed as byte 2 of the initialization sequence (A_8–A_{15}), is enabled onto the bus.

Content of Third Interrupt Vector Byte

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

8086, 8088

8086 mode is similar to MCS-80 mode except that only two Interrupt Acknowledge cycles are issued by the processor and no CALL opcode is sent to the processor. The first interrupt acknowledge cycle is similar to that of MCS-80, 85 systems in that the 8259A uses it to internally freeze the state of the interrupts for priority resolution and as a master it issues the interrupt code on the cascade lines at the end of the INTA pulse. On this first cycle it does not issue any data to the processor and leaves its data bus buffers disabled. On the second interrupt acknowledge cycle in 8086 mode the master (or slave if so programmed) will send a byte of data to the processor with the acknowledged interrupt code composed as follows (note the state of the ADI mode control is ignored and A_5–A_{11} are unused in 8086 mode):

Content of Interrupt Vector Byte for 8086 System Mode

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

PROGRAMMING THE 8259A

The 8259A accepts two types of command words generated by the CPU:

1. *Initialization Command Words (ICWs):* Before normal operation can begin, each 8259A in the system must be brought to a starting point—by a sequence of 2 to 4 bytes timed by $\overline{WR}$ pulses.
2. *Operation Command Words (OCWs):* These are the command words which command the 8259A to operate in various interrupt modes. These modes are:
   a. Fully nested mode
   b. Rotating priority mode
   c. Special mask mode
   d. Polled mode

The OCWs can be written into the 8259A anytime after initialization.

INITIALIZATION COMMAND WORDS (ICWS)

General

Whenever a command is issued with A0 = 0 and D4 = 1, this is interpreted as Initialization Command Word 1 (ICW1). ICW1 starts the intiialization sequence during which the following automatically occur.

a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low-to-high transistion to generate an interrupt.

b. The Interrupt Mask Register is cleared.

c. IR7 input is assigned priority 7.

d. The slave mode address is set to 7.

e. Special Mask Mode is cleared and Status Read is set to IRR.

f. If IC4 = 0, then all functions selected in ICW4 are set to zero. (Non-Buffered mode*, no Auto-EOI, MCS-80, 85 system).

***NOTE:**
Master/Slave in ICW4 is only used in the buffered mode.

Initialization Command Words 1 and 2 (ICW1, ICW2)

A_5–A_{15}: *Page starting address of service routines.* In an MCS 80/85 system, the 8 request levels will generate CALLs to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus the 8 routines will occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A_0–A_{15}). When the routine interval is 4, A_0–A_4 are automatically inserted by the 8259A, while A_5–A_{15} are programmed externally. When the routine interval is 8, A_0–A_5 are automatically inserted by the 8259A, while A_6–A_{15} are programmed externally.

The 8-byte interval will maintain compatibility with current software, while the 4-byte interval is best for a compact jump table.

In an 8086 system A_{15}–A_{11} are inserted in the five most significant bits of the vectoring byte and the 8259A sets the three least significant bits according to the interrupt level. A_{10}–A_5 are ignored and ADI (Address interval) has no effect.

LTIM: If LTIM = 1, then the 8259A will operate in the level interrupt mode. Edge detect logic on the interrupt inputs will be disabled.

ADI: CALL address interval. ADI = 1 then interval = 4; ADI = 0 then interval = 8.

SNGL: Single. Means that this is the only 8259A in the system. If SNGL = 1 no ICW3 will be issued.

IC4: If this bit is set—ICW4 has to be read. If ICW4 is not needed, set IC4 = 0.

Initialization Command Word 3 (ICW3)

This word is read only when there is more than one 8259A in the system and cascading is used, in which case SNGL = 0. It will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when SP = 1, or in buffered mode when M/S = 1 in ICW4) a "1" is set for each slave in the system. The master then will release byte 1 of the call sequence (for MCS-80/85 system) and will enable the corresponding slave to release bytes 2 and 3 (for 8086 only byte 2) through the cascade lines.

b. In the slave mode (either when $\overline{SP}$ = 0, or if BUF = 1 and M/S = 0 in ICW4) bits 2–0 identify the slave. The slave compares its cascade input with these bits and, if they are equal, bytes 2 and 3 of the call sequence (or just byte 2 for 8086) are released by it on the Data Bus.

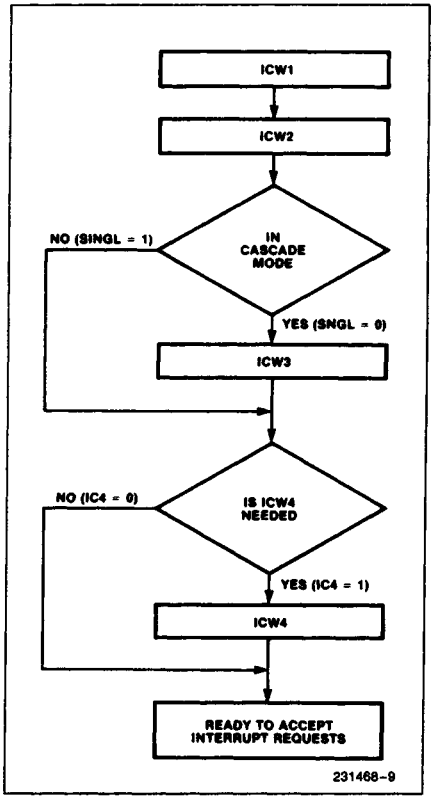


Figure 6. Initialization Sequence

Initialization Command Word 4 (ICW4)

SFNM: If SFNM = 1 the special fully nested mode is programmed.

BUF: If BUF = 1 the buffered mode is programmed. In buffered mode $\overline{SP}/\overline{EN}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S = 1 means the 8259A is programmed to be a master, M/S = 0 means the 8259A is programmed to be a slave. If BUF = 0, M/S has no function.

AEOI: If AEOI = 1 the automatic end of interrupt mode is programmed.

μPM: Microprocessor mode: μPM = 0 sets the 8259A for MCS-80, 85 system operation, μPM = 1 sets the 8259A for 8086 system operation.

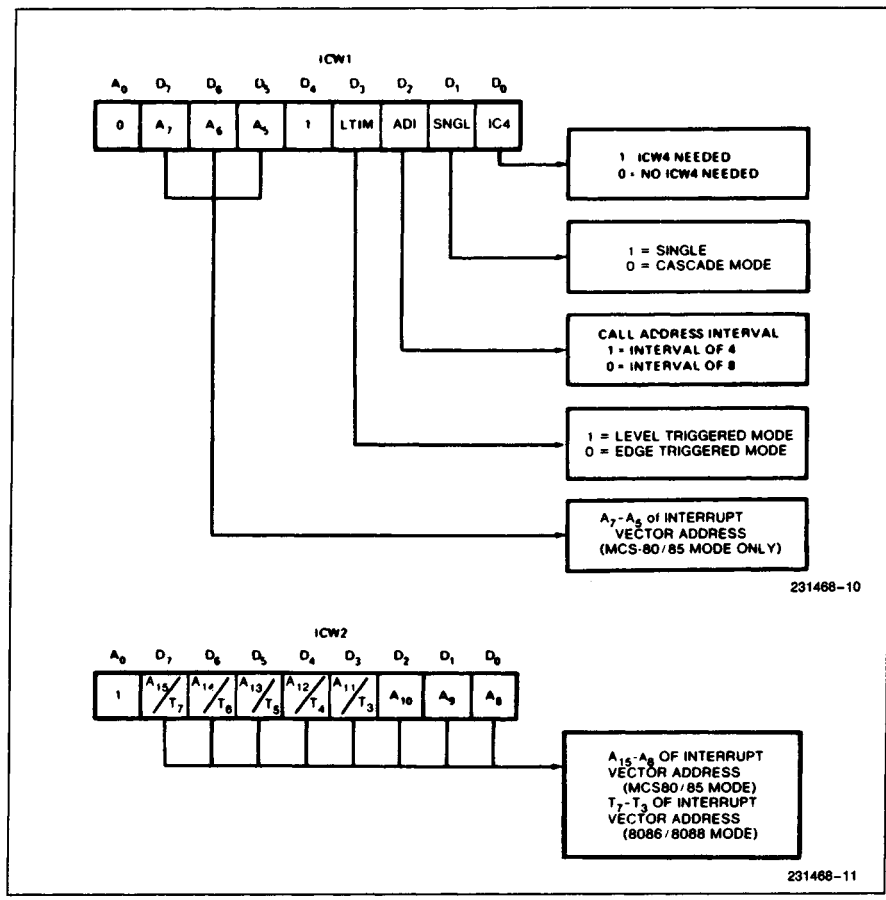
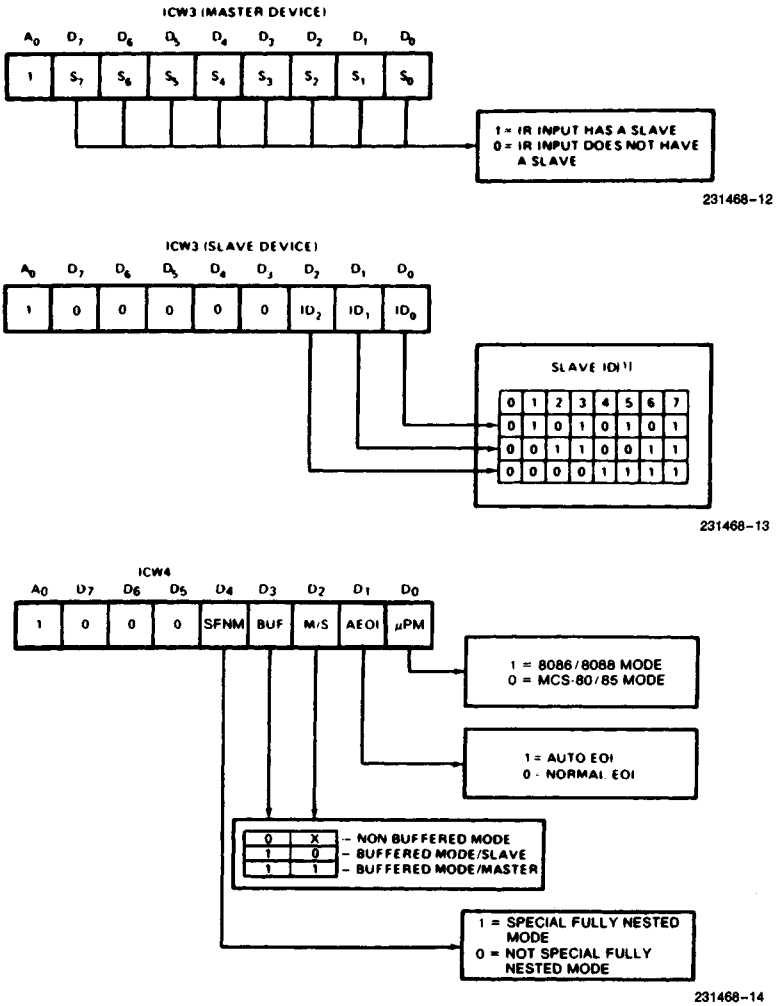


Figure 7. Initialization Command Word Format



NOTE:
Slave ID is equal to the corresponding master IR input.

Figure 7. Initialization Command Word Format (Continued)

OPERATION COMMAND WORDS (OCWS)

After the Initialization Command Words (ICWs) are programmed into the 8259A, the chip is ready to accept interrupt requests at its input lines. However, during the 8259A operation, a selection of algorithms can command the 8259A to operate in various modes through the Operation Command Words (OCWs).

Operation Control Words (OCWs)

OCW1

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	M7	M6	M5	M4	M3	M2	M1	M0

OCW2

0	R	SL	EOI	0	0	L2	L1	L0

OCW3

0	0	ESMM	SMM	0	1	P	RR	RIS

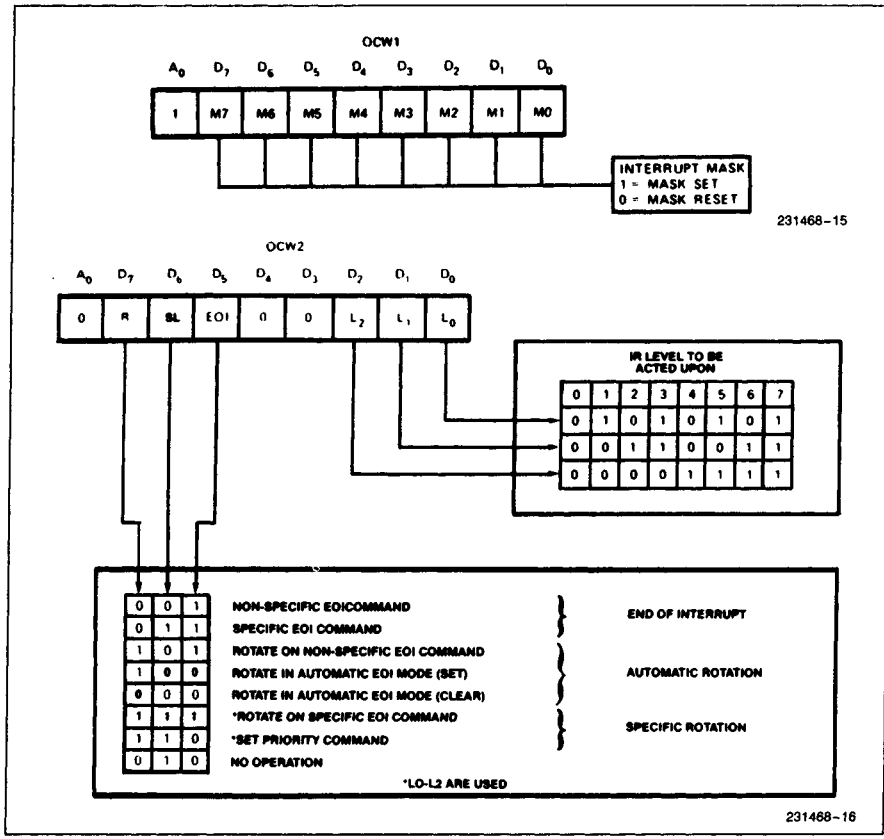


Figure 8. Operation Command Word Format

Operation Control Word 1 (OCW1)

OCW1 sets and clears the mask bits in the interrupt Mask Register (IMR). M_7–M_0 represent the eight mask bits. M = 1 indicates the channel is masked (inhibited), M = 0 indicates the channel is enabled.

Operation Control Word 2 (OCW2)

R, SL, EOI—These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations can be found on the Operation Command Word Format.

L_2, L_1, L_0—These bits determine the interrupt level acted upon when the SL bit is active.

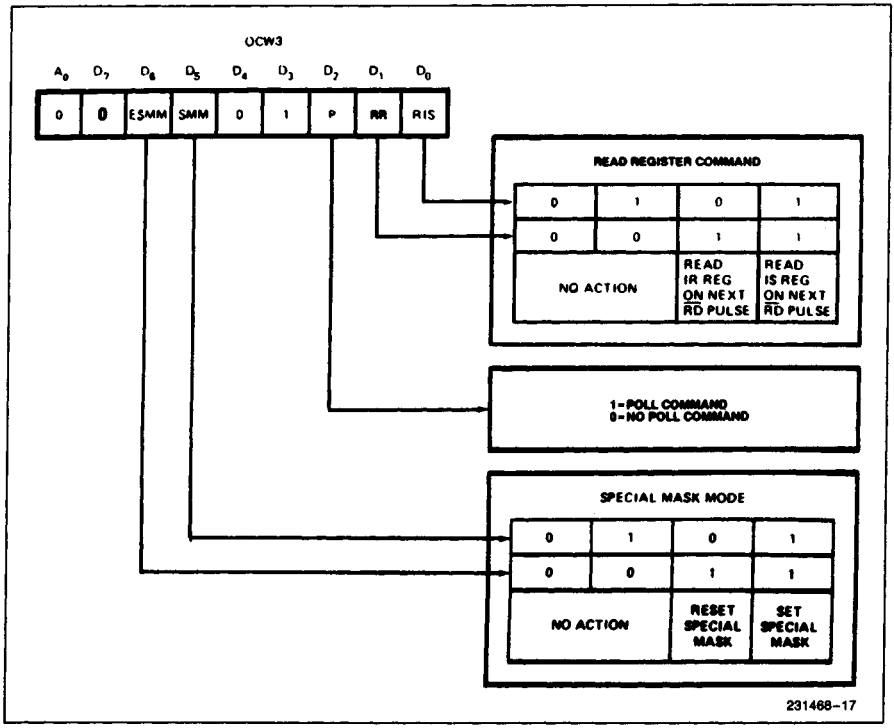


Figure 8. Operation Command Word Format (Continued)

Operation Control Word 3 (OCW3)

ESMM—Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESMM = 0 the SMM bit becomes a "don't care".

SMM—Special Mask Mode. If ESMM = 1 and SMM = 1 the 8259A will enter Special Mask Mode. If ESMM = 1 and SMM = 0 the 8259A will revert to normal mask mode. When ESMM = 0, SMM has no effect.

Fully Nested Mode

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority from 0 through 7 (0 highest). When an interrupt is acknowledged the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the Interrupt Service register (ISO-7) is set. This bit remains set until the microprocessor issues an End of Interrupt (EOI) command immediately before returning from the service routine, or if AEOI (Automatic End of Interrupt) bit is set, until the trailing edge of the last INTA. While the IS bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate an interrupt (which will be acknowledged only if the microprocessor internal Interupt enable flip-flop has been re-enabled through software).

After the initialization sequence, IR0 has the highest priority and IR7 the lowest. Priorities can be changed, as will be explained, in the rotating priority mode.

End of Interrupt (EOI)

The In Service (IS) bit can be reset either automatically following the trailing edge of the last in sequence $\overline{\text{INTA}}$ pulse (when AEOI bit in ICW1 is set) or by a command word that must be issued to the 8259A before returning from a service routine (EOI command). An EOI command must be issued twice if in the Cascade mode, once for the master and once for the corresponding slave.

There are two forms of EOI command: Specific and Non-Specific. When the 8259A is operated in modes which perserve the fully nested structure, it can determine which IS bit to reset on EOI. When a Non-Specific EOI command is issued the 8259A will automatically reset the highest IS bit of those that are set, since in the fully nested mode the highest IS level was necessarily the last level acknowledged and serviced. A non-specific EOI can be issued with OCW2 (EOI = 1, SL = 0, R = 0).

When a mode is used which may disturb the fully nested structure, the 8259A may no longer be able to determine the last level acknowledged. In this case a Specific End of Interrupt must be issued which includes as part of the command the IS level to be reset. A specific EOI can be issued with OCW2 (EOI = 1, SL = 1, R = 0, and L0–L2 is the binary level of the IS bit to be reset).

It should be noted that an IS bit that is masked by an IMR bit will not be cleared by a non-specific EOI if the 8259A is in the Special Mask Mode.

Automatic End of Interrupt (AEOI) Mode

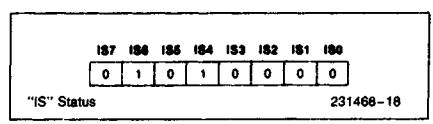
If AEOI = 1 in ICW4, then the 8259A will operate in AEOI mode continuously until reprogrammed by ICW4. in this mode the 8259A will automatically perform a non-specific EOI operation at the trailing edge of the last interrupt acknowledge pulse (third pulse in MCS-80/85, second in 8086). Note that from a system standpoint, this mode should be used only when a nested multilevel interrupt structure is not required within a single 8259A.

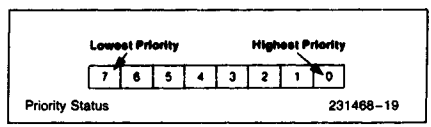
The AEOI mode can only be used in a master 8259A and not a slave.

Automatic Rotation (Equal Priority Devices)

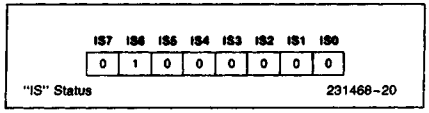
In some applications there are a number of interrupting devices of equal priority. In this mode a device, after being serviced, receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case until each of 7 other devices are serviced at most *once*. For example, if the priority and "in service" status is:

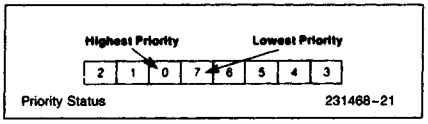
Before Rotate (IR4 the highest prioirity requiring service)





After Rotate (IR4 was serviced, all other priorities rotated correspondingly)





There are two ways to accomplish Automatic Rotation using OCW2, the Rotation on Non-Specific EOI Command (R = 1, SL = 0, EOI = 1) and the Rotate in Automatic EOI Mode which is set by (R = 1, SL = 0, EOI = 0) and cleared by (R = 0, SL = 0, EOI = 0).

Specific Rotation (Specific Priority)

The programmer can change priorities by programming the bottom priority and thus fixing all other priorities; i.e., if IR5 is programmed as the bottom priority device, then IR6 will have the highest one.

The Set Priority command is issued in OCW2 where: R = 1, SL = 1, L0-L2 is the binary priority level code of the bottom priority device.

Observe that in this mode internal status is updated by software control during OCW2. However, it is independent of the End of Interrupt (EOI) command (also executed by OCW2). Priority changes can be executed during an EOI command by using the Rotate on Specific EOI command in OCW2 (R = 1, SL = 1, EOI = 1 and L0-L2 = IR level to receive bottom priority).

Interrupt Masks

Each Interrupt Request input can bem masked individually by the Interrupt Mask Register (IMR) programmed through OCW1. Each bit in the IMR masks one interrupt channel if it is set (1). Bit 0 masks IR0, Bit 1 masks IR1 and so forth. Masking an IR channel does not affect the other channels operation.

Special Mask Mode

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty here is that if an Interrupt Request is acknowledged and an End of Interrupt command did not reset its IS bit (i.e., while executing a service routine), the 8259A would have inhibited all lower priority requests with no easy way for the routine to enable them.

That is where the Special Mask Mode comes in. In the special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level *and enables* interrupts from *all other* levels (lower as well as higher) that are not masked.

Thus, any interrupts may be selectively enabled by loading the mask register.

The special Mask Mode is set by OWC3 where: SSMM = 1, SMM = 1, and cleared where SSMM = 1, SMM = 0.

Poll Command

In this mode the INT output is not used or the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting P = '1" in OCW3. The 8259A treats the next $\overline{RD}$ pulse to the 8259A (i.e., $\overline{RD}$ = 0, $\overline{CS}$ = 0) as an interrupt acknowledge, sets the appropriate IS bit if there is a request, and reads the priority level. Interrupt is frozen from $\overline{WR}$ to $\overline{RD}$.

The word enabled onto the data bus during $\overline{RD}$ is:

D7	D6	D5	D4	D3	D2	D1	D0
I	—	—	—	—	W2	W1	W0

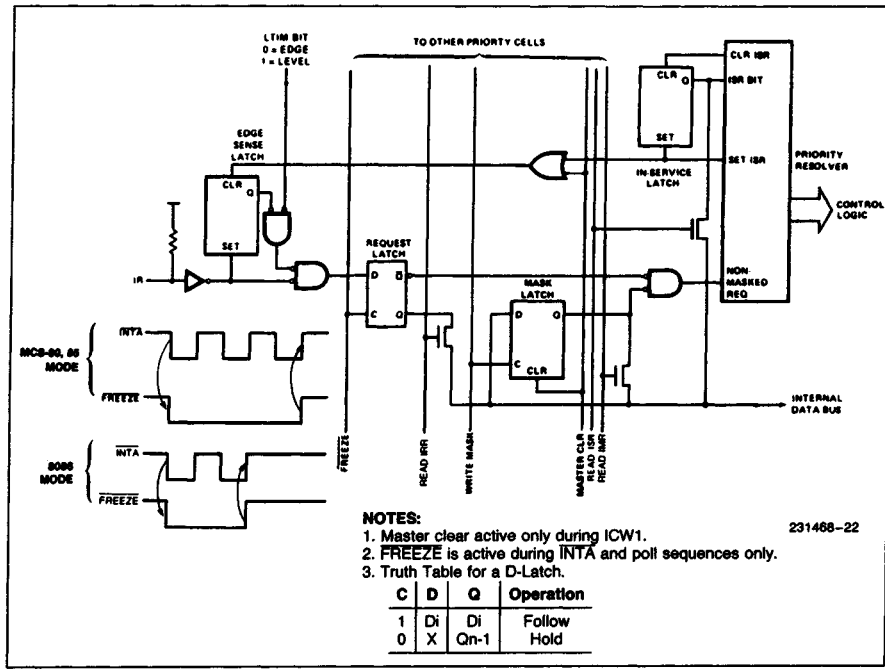
W0-W2: Binary code of the highest priority level requesting service.

I: Equal to "1" if there is an interrupt.

This mode is useful if there is a routine command common to several levels so that the $\overline{INTA}$ sequence is not needed (saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.

Reading the 8259A Status

The input status of several internal registers can be read to update the user information on the system.



231468-22

NOTES:
1. Master clear active only during ICW1.
2. $\overline{\text{FREEZE}}$ is active during $\overline{\text{INTA}}$ and poll sequences only.
3. Truth Table for a D-Latch.

C	D	Q	Operation
1	Di	Di	Follow
0	X	Qn-1	Hold

Figure 9. Priority Cell—Simplified Logic Diagram

The following registers can be read via OCW3 (IRR and ISR or OCW1 [IMR]).

Interrupt Request Register (IRR): 8-bit register which contains the levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged. (Not affected by IMR.)

In-Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt Command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 0.)

The ISR can be read, when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 1).

There is no need to write an OCW3 before every status read operation, as long as the status read corresponds with the previous one; i.e., the 8259A "remembers" whether the IRR or ISR has been previously selected by the OCW3. This is not true when poll is used.

After initialization the 8259A is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever $\overline{\text{RD}}$ is active and A0 = 1 (OCW1).

Polling overrides status read when P = 1, RR = 1 in OCW3.

Edge and Level Triggered Modes

This mode is programmed using bit 3 in ICW1.

If LTIM = '0', an interrupt request will be recognized by a low to high transition on an IR input. The IR input can remain high without generating another interrupt.

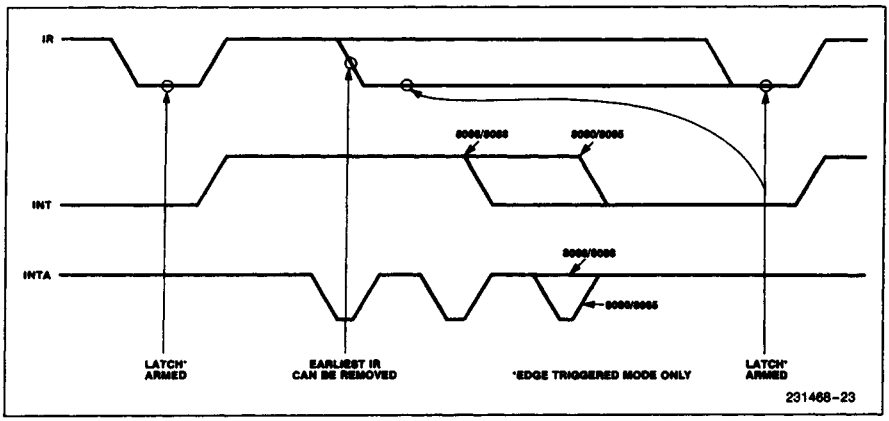


Figure 10. IR Triggering Timing Requirements

If LTIM = '1', an interrupt request will be recognized by a 'high' level on IR input, and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued or the CPU interrupts is enabled to prevent a second interrupt from occurring.

The priority cell diagram shows a conceptual circuit of the level sensitive and edge sensitive input circuitry of the 8259A. Be sure to note that the request latch is a transparent D type latch.

In both the edge and level triggered modes the IR inputs must remain high until after the falling edge of the first INTA. If the IR input goes low before this time a DEFAULT IR7 will occur when the CPU acknowledges the interrupt. This can be a useful safeguard for detecting interrupts caused by spurious noise glitches on the IR inputs. To implement this feature the IR7 routine is used for "clean up" simply executing a return instruction, thus ignoring the interrupt. If IR7 is needed for other purposes a default IR7 can still be detected by reading the ISR. A normal IR7 interrupt will set the corresponding ISR bit, a default IR7 won't. If a default IR7 routine occurs during a normal IR7 routine, however, the ISR will remain set. In this case it is necessary to keep track of whether or not the IR7 routine was previously entered. If another IR7 occurs it is a default.

The Special Fully Nest Mode

This mode will be used in the case of a big system where cascading is used, and the priority has to be conserved within each slave. In this case the fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

a. When an interrupt request from a certain slave is in service this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IR's within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nested mode a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.)

b. When exiting the Interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a non-specific End of Interrupt (EOI) command to the slave and then reading its In-Service register and checking for zero. If it is empty, a non-specific EOI can be sent to the master too. If not, no EOI should be sent.

Buffered Mode

When the 8259A is used in a large system where bus driving buffers are required on the data bus and the cascading mode is used, there exists the problem of enabling buffers.

The buffered mode will structure the 8259A to send an enable signal on $\overline{SP}/\overline{EN}$ to enable the buffers. In this mode, whenever the 8259A's data bus outputs are enabled, the $\overline{SP}/\overline{EN}$ output becomes active.

This modification forces the use of software programming to determine whether the 8259A is a master or a slave. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW4 determines whether it is a master or a slave.

CASCADE MODE

The 8259A can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

The master controls the slaves through the 3 line cascade bus. The cascade bus acts like chip selects to the slaves during the $\overline{INTA}$ sequence.

In a cascade configuration, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of INTA. (Byte 2 only for 8086/8088).

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first INTA pulse to the trailing edge of the third pulse. Each 8259A in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. An address decoder is required to activate the Chip Select (CS) input of each 8259A.

The cascade lines of the Master 8259A are activated only for slave inputs, non-slave inputs leave the cascade line inactive (low).

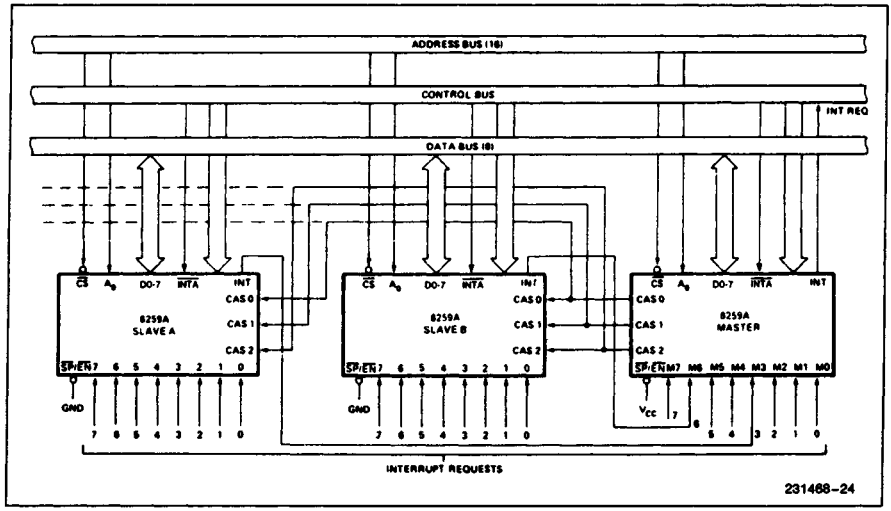


Figure 11. Cascading the 8259A

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .....0°C to 70°C
Storage Temperature .....−65°C to +150°C
Voltage on Any Pin
with Respect to Ground.....−0.5V to +7V
Power Dissipation 1W

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D. C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ±5% (8259A-8), V_{CC} = 5V ± 10% (8259A, 8259A-2))

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0*	V_{CC} + 0.5V	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
$V_{OH(INT)}$	Interrupt Output High Voltage	3.5		V	I_{OH} = −100 μA
		2.4		V	I_{OH} = −400 μA
I_{LI}	Input Load Current	−10	+10	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{LOL}	Output Leakage Current	−10	+10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
I_{CC}	V_{CC} Supply Current		85	mA	
I_{LIR}	IR Input Load Current		−300	μA	V_{IN} = 0
			10	μA	V_{IN} = V_{CC}

***NOTE:**
For Extended Temperature EXPRESS V_{IH} = 2.3V.

CAPACITANCE T_A = 25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured Pins Returned to V_{SS}

A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5% (8259 A-8), V_{CC} = 5V ±10% (8259A, 8259A-2)

TIMING REQUIREMENTS

Symbol	Parameter	8259A-8		8259A		8259A-2		Units	Test Conditions
		Min	Max	Min	Max	Min	Max		
TAHRL	AO/$\overline{CS}$ Setup to $\overline{RD}$/$\overline{INTA}$ ↓	50		0		0		ns	
TRHAX	AO/$\overline{CS}$ Hold after $\overline{RD}$/$\overline{INTA}$ ↑	5		0		0		ns	
TRLRH	$\overline{RD}$ Pulse Width	420		235		160		ns	
TAHWL	AO/$\overline{CS}$ Setup to $\overline{WR}$ ↓	50		0		0		ns	
TWHAX	AO/$\overline{CS}$ Hold after $\overline{WR}$ ↑	20		0		0		ns	
TWLWH	$\overline{WR}$ Pulse Width	400		290		190		ns	
TDVWH	Data Setup to $\overline{WR}$ ↑	300		240		160		ns	
TWHDX	Data Hold after $\overline{WR}$ ↑	40		0		0		ns	
TJLJH	Interrupt Request Width (Low)	100		100		100		ns	See Note 1
TCVIAL	Cascade Setup to Second or Third $\overline{INTA}$ ↓ (Slave Only)	55		55		40		ns	
TRHRL	End of $\overline{RD}$ to Next $\overline{RD}$ End of $\overline{INTA}$ to Next $\overline{INTA}$ within an $\overline{INTA}$ Sequence Only	160		160		160		ns	
TWHWL	End of $\overline{WR}$ to Next $\overline{WR}$	190		190		190		ns	
*TCHCL	End of Command to Next Command (Not Same Command Type)	500		500		500		ns	
	End of $\overline{INTA}$ Sequence to Next $\overline{INTA}$ Sequence.								

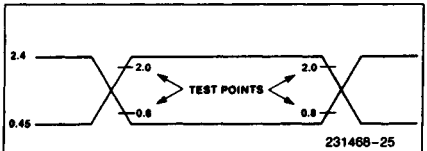
*Worst case timing for TCHCL in an actual microprocessor system is typically much greater than 500 ns (i.e. 8085A = 1.6 μs, 8085A-2 = 1 μs, 8086 = 1 μs, 8086-2 = 625 ns)

NOTE:
This is the low time required to clear the input latch in the edge triggered mode.

TIMING RESPONSES

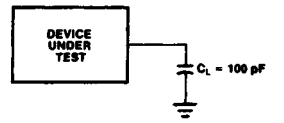
Symbol	Parameter	8259A-8		8259A		8259A-2		Units	Test Conditions
		Min	Max	Min	Max	Min	Max		
TRLDV	Data Valid from $\overline{RD}$/$\overline{INTA}$ ↓		300		200		120	ns	C of Data Bus = 100 pF
TRHDZ	Data Float after $\overline{RD}$/$\overline{INTA}$ ↑	10	200	10	100	10	85	ns	C of Data Bus Max Test C = 100 pF Min Test C = 15 pF
TJHIH	Interrupt Output Delay		400		350		.300	ns	
TIALCV	Cascade Valid from First $\overline{INTA}$ ↓ (Master Only)		565		565		360	ns	C_{INT} = 100 pF
TRLEL	Enable Active from $\overline{RD}$ ↓ or $\overline{INTA}$ ↓		160		125		100	ns	$C_{CASCADE}$ = 100 pF
TRHEH	Enable Inactive from $\overline{RD}$ ↑ or $\overline{INTA}$ ↑		325		150		150	ns	
TAHDV	Data Valid from Stable Address		350		200		200	ns	
TCVDV	Cascade Valid to Valid Data		300		300		200	ns	

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

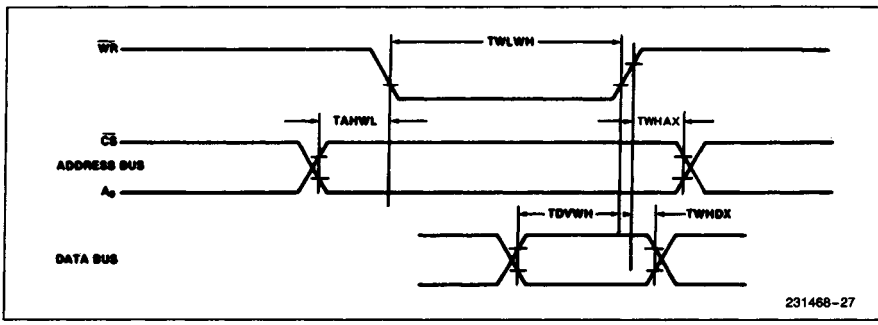
A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

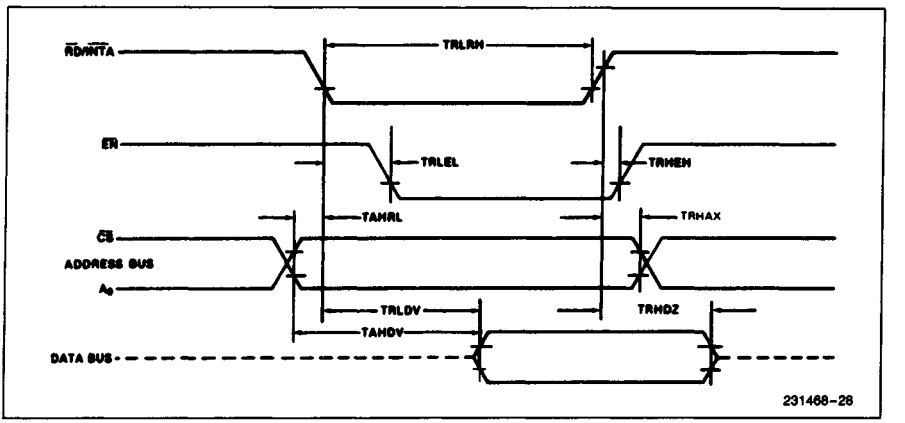
WAVEFORMS

WRITE

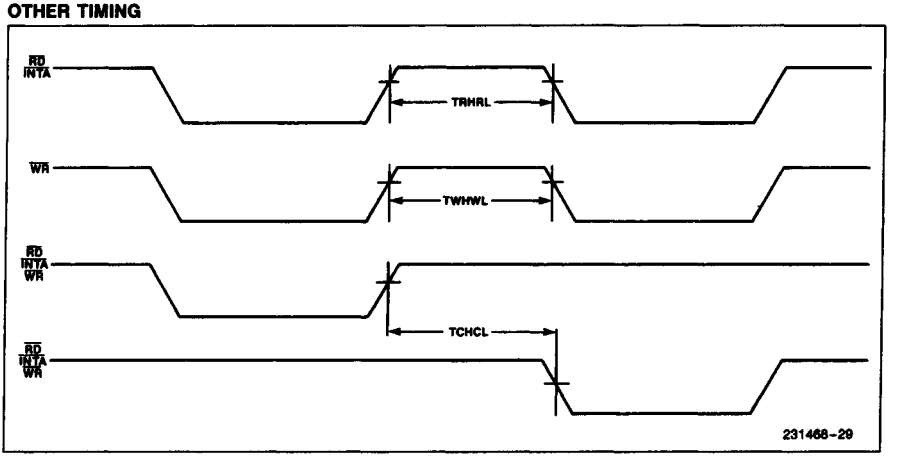


WAVEFORMS (Continued)

READ/INTA

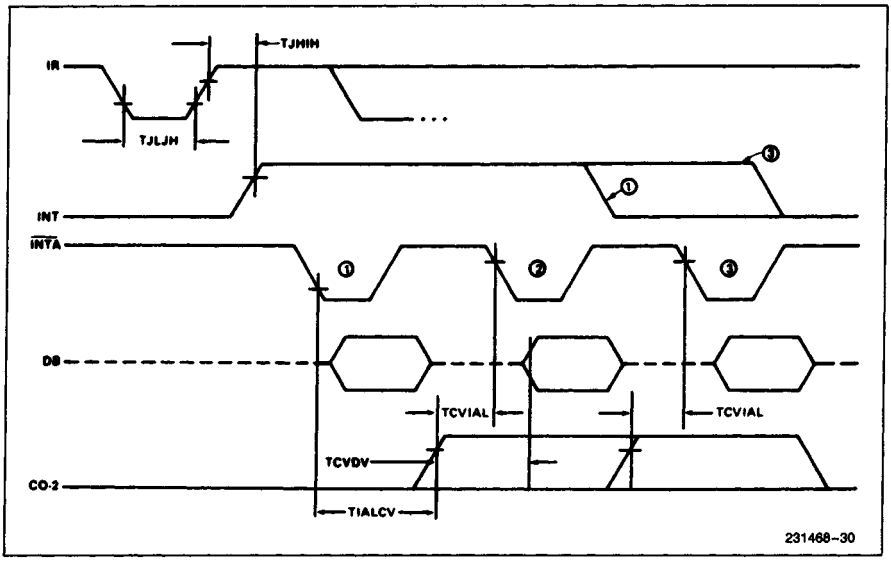


OTHER TIMING



WAVEFORMS (Continued)

$\overline{INTA}$ SEQUENCE



NOTES:
Interrupt output must remain HIGH at least until leading edge of first INTA.
1. Cycle 1 in 8086, 8088 systems, the Data Bus is not active.

Floppy Disk Support Chip Specification

Floppy Disk Support Chip Specification
Contents

Floppy Disk Support Logic
Tandy Part # 8xxxxxx
Jan 29, 1987
Preliminary

1.0 GENERAL DESECRIPTION

1.1 The Tandy Part # 8xxxxxx - Floppy Disk Support logic:

- Generates the clock to the 765 Floppy Disk Controller.
- Generates the write clock to the Floppy Disk Controller.
- Generaters step pulses, track 0 indicator, DMA request, and FDC interrupt signals.
- Generates the Read Data and Read Data Window signals.
- Generates the Write Data to the Floppy Disk.

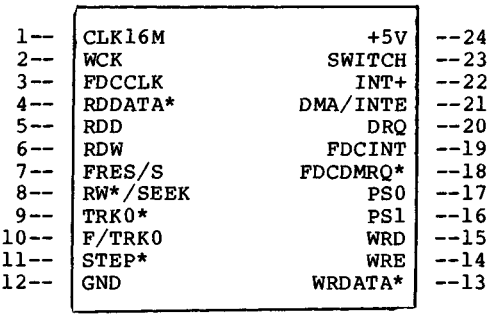
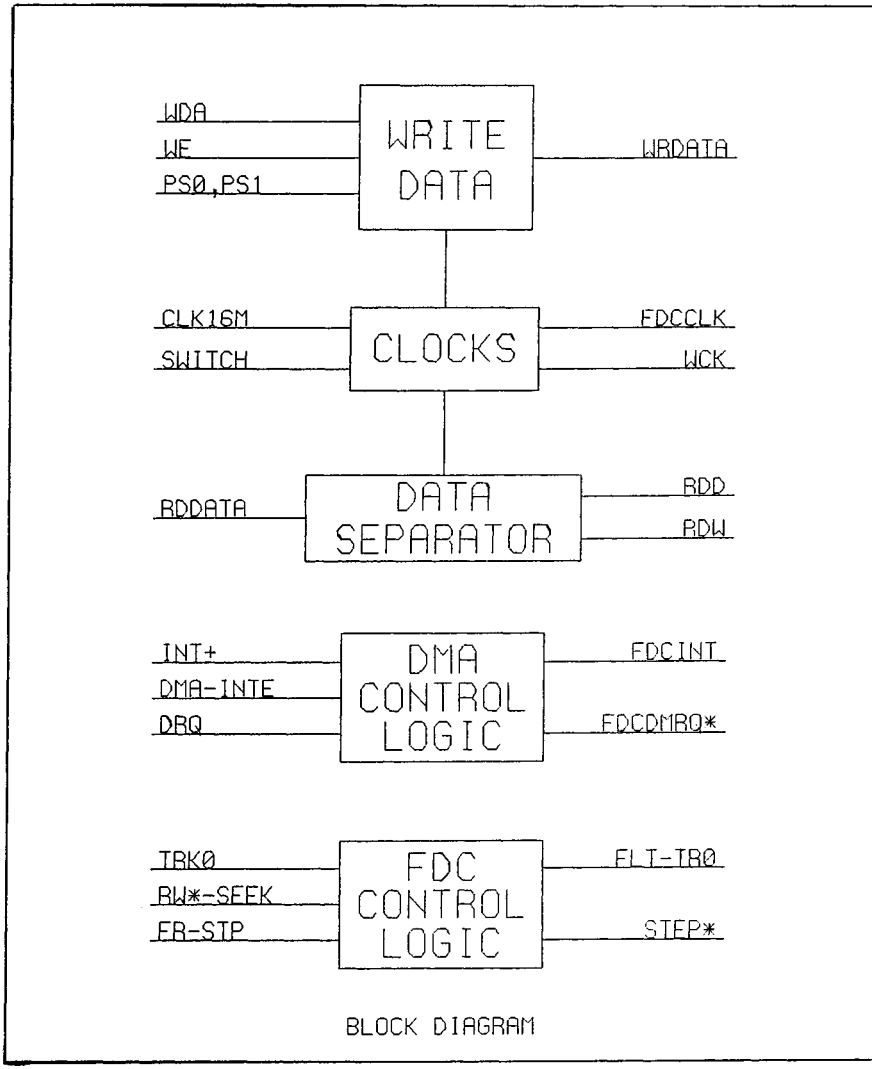


FIGURE 1. Pin Assignment

1.2 DESCRIPTION OF PINS:

PIN #	PIN NAME	TYPE	DESCRIPTION
1	CLK16M	INPUT	Frequency = 16.0000 Tolerance = 100pmm
2	WCK	OUTPUT	If SWITCH = 0, period = 2 us, 250 ns pulse If SWITCH = 1, period = 1 us, 250 ns pulse
3	FDCCLK	OUTPUT	If SWITCH = 0, then CLK16M/4 If SWITCH = 1, then CLK16M/2
4	RDDATA	INPUT	Serial data from FDD
5	RDD	OUTPUT	Serial data from FDC
6	RDW	OUTPUT	Read Data Window
7	FRES/S	INPUT	Step pulses to move head to another cylinder
8	RW*/SEEK	INPUT	Specifies seek mode when high
9	TRK0*	INPUT	From FDD, indicating head is on track 0
10	F/TRK0	OUTPUT	To FDC, indicating head is on track 0
11	STEP*	OUTPUT	Moves head of FDD
12	GND		Ground
13	WRDATA*	OUTPUT	Serial Data to FDD
14	WRE	INPUT	Write Enable
15	WRD	INPUT	Serial Data from FDC
16	PS1	INPUT	Write precompensation status
17	PS0	INPUT	Write precompensation status
18	FDCDMRQ*	OUTPUT	DRQ delayed by 1.0 usec.
19	FDCINT	OUTPUT	Interrupt request
20	DRQ	INPUT	FDC DMA Request
21	DMA/INTE	INPUT	DMA request and FDC interrupt enable
22	INT+	INPUT	Interrupt request generated by FDC
23	SWITCH	INPUT	0 = low density drive 1 = high density drive
24	+5V		+5 Volts



BLOCK DIAGRAM

2.0 ENVIROMENTAL SPECIFICATIONS

2.1 Storage temperature: -65°C min., +150°C max.
2.2 Operating temperature: 0°C min., +25°C typ, +70°C max.

3.0 DC ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Rating:
Voltage on any pin
w.r.t. Ground: -0.5 min., 7.0 max. volts

3.2 Operating Electrical Specifications:

	Min.	Typ.	Max.	Units
3.2.1 Operating Ambient:				
Air Temperatue Range	0	25	70	°C
3.2.2 Power Supplies:				
VCC	4.5	5.0	5.5	volts
VSS	0	0	0	volts
ICC				milli-amps
Total Power				milli-watts
3.2.3 Leakage Current, All Inputs:				
Vin = 0.0 v			-10	micro-amps
Vin = 5.0 v			+10	micro-amps
3.2.4 Input voltages:				
3.2.4.1 Except RDDATA*, TRK*				
Logic "0"			.8	volts
Logic "1"	2.0			volts
3.2.4.2 RDDATA*, TRK*				
Positive going threshold		1.8		volts
Negative going threshold		1.2		volts
Hysteresis voltage	220			milli-volts
3.2.5 Output Voltages:				
3.2.5.1 Except WRDATA*, STEP*				
Logic "0" @ 4.0 mA load			.4	volts
Logic "1" @ 4.0 mA load	2.4			volts
3.2.5.2 WRDATA*, STEP*				
Logic "0" @ 48 mA			.5	volts
3.2.6 Input Capacitance (0.0 < Vin < 5.0)				
All inputs			10	pf
3.2.7 Output Capacitance				
All loads			50	pf

4.0 AC CHARACTERISTICS

4.1 FDCCLK Timing

Parameter	Min.	Typ.	Max.	Units
t_H	90	120	130	nSec
t_R, t_F		5	10	nSec
t_L	100	120	160	nSec
t_{CY}	245	250	255	nSec

4.2 WCK Timing

t_H	100	250	250	nSec
t_R, t_F		5	10	nSec
t_L		$t_{CY}-(t_H+t_R+t_F)$		
t_{CY}		2.0		µSec

4.3 WRDATA* Timing

WCK_H-WE_H	20			nSec
WCK_L-WE_L	20			nSec
PSD	20		100	nSec
WDD	20		100	nSec
WDA_W		WCK_H-50		nSec
WRD_W	115	125	135	nSec
WDD_H-WRD_L early	150		250	nSec
WDD_H-WRD_L nominal	275		375	nSec
WDD_H-WRD_L late	400		500	nSec

4.4 DMA/INTERRUPT Timing

I_H-FI_H			30	nSec
I_L-FI_L			30	nSec
DI_L-FI_L			30	nSec
WCK_H-DRQ_H	0			nSec
WCK_L-DRQ_H		-20		nSec
DRQ_H-$FDRQ_H$	750		1050	nSec
DRQ_L-$FDRQ_L$			30	nSec
DI_L-$FDRQ_L$			30	nSec
FCK_H-$FDRQ_H$			30	nSec

4.5 CONTROL Timing

Parameter	Min.	Typ.	Max.	Units
T_L-FT_H			30	nSec
T_H-FT_L			30	nSec
RS_L-FT_L			30	nSec
F_H-S_L			30	nSec
F_L-S_H			30	nSec
RS_L-S_H			30	nSec

4.6 DATA SEPARATOR Timing

RDA_W	200	350	550	nSec
RDA_L-RDD_H	188		313	nSec
RDD_W	240	250	260	nSec
RDD_H-RDW_C	850	875	900	nSec
$RDW(ND)_W$		2.0		µSec
"A"				
RDA_S	3062			nSec
RDW_C-RDD_H	15			nSec
"B"				
RDA_S	4812			nSec
RDW_C-RDD_H			1938	nSec
"C"				
RDA_S	5062			nSec
RDW_C-RDD_H	15			nSec

FDSL AC TIMING

FIG. 1 FDCCLK

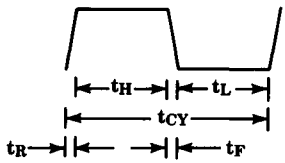
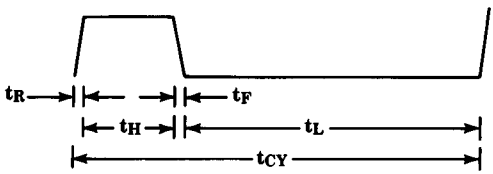


FIG. 2 WCK



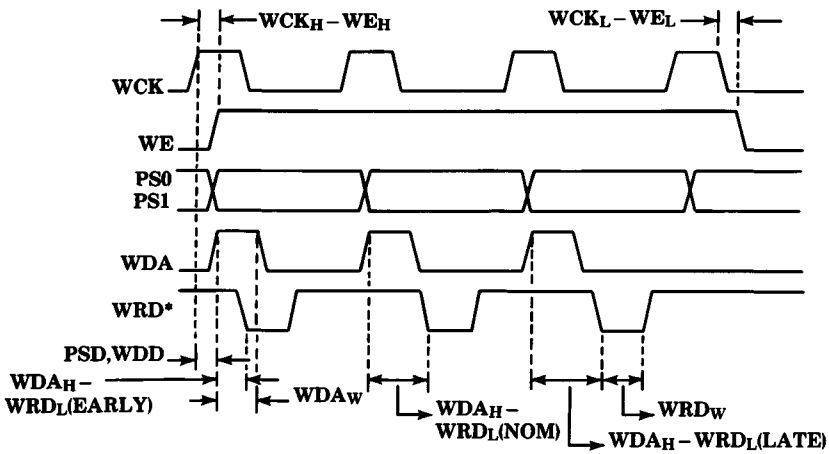


FIG. 3 WRITE DATA TIMING.

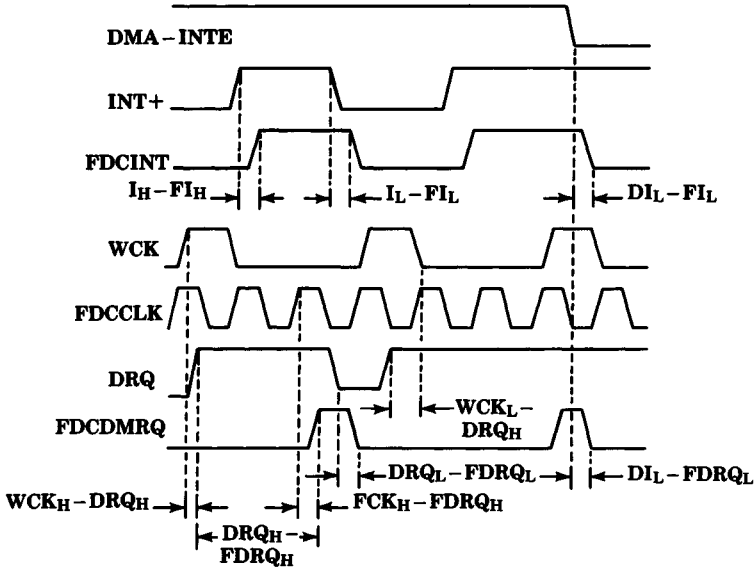


FIG. 4 DMA/INTERRUPT TIMING.

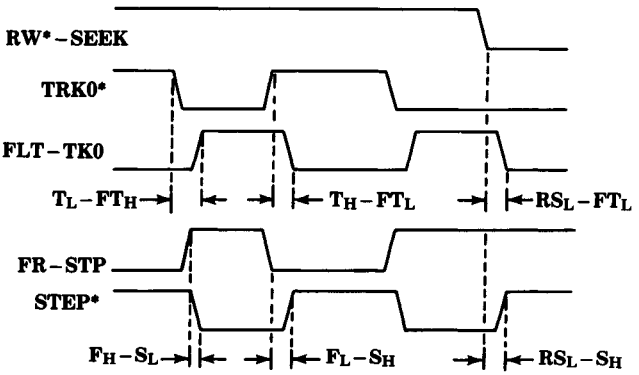


FIG. 5 CONTROL LOGIC TIMING.

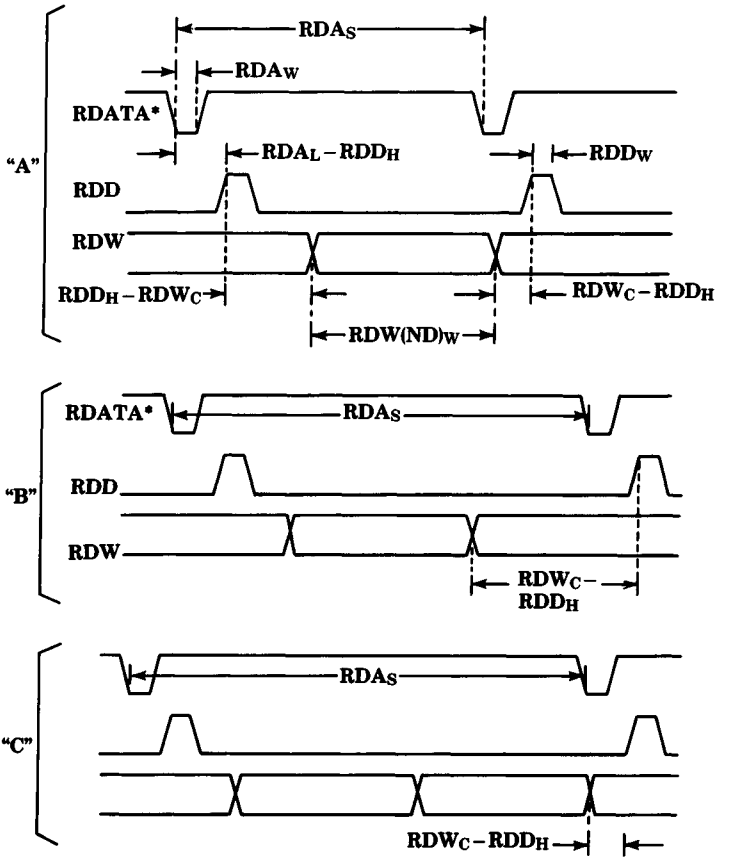


FIG. 6 DATA SEPARATOR TIMING.

Keyboard Interface Chip Specification

Keyboard Interface Chip Specification
Contents

KEYBOARD INTERFACE SPECIFICATION
TANDY PART # 8075069
MAY 05, 1986

1. GENERAL DESCRIPTION

1.1 The Tandy part# 8075069 - Keyboard Interface I.C provides two functions:

a. Interface between the system I/O bus and keyboard.

b. FDC support logic that generates DRIVE SELECT SIGNAL, MOTOR ON SIGNAL, FDC TERMINAL COUNT, FDC RESET and DMA/I.

Figure 1. shows block diagram of Keyboard Interface chip
Figure 2. shows pin configuration of Keyboard Interface chip.

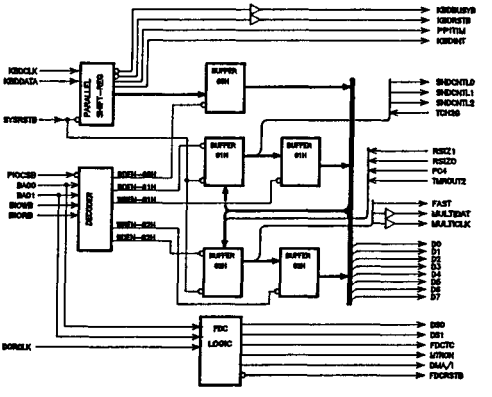


Figure 1.

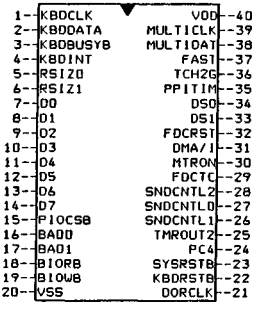


Figure 2.

1.2 DESCRIPTION OF EACH PINS:

Pin#	Pin Name	Type	Description
1	KBDCLK	input	Keyboard clock
2	KBDDATA	input	Keyboard data
3	KBDBUSYB	output	Keyboard busy signal
4	KBDINT	output	Keyboard interrupt signal
5	RSIZ0	input	Monochrome/color monitor mode
6	RSIZ1	input	Reserved
7	D0	input/output	Data I/O line
8	D1	input/output	Data I/O line
9	D2	input/output	Data I/O line
10	D3	input/output	Data I/O line
11	D4	input/output	Data I/O line
12	D5	input/output	Data I/O line
13	D6	input/output	Data I/O line
14	D7	input/output	Data I/O line
15	PIOCSB	input	Chip select strobe
16	BA00	input	CPU address line
17	BA01	input	CPU address line
18	BIORB	input	CPU I/O read strobe
19	BIOWB	input	CPU I/O write strobe
20	VSS	ground	Ground
21	DORCLK	input	Decode latch clock
22	KBDRSTB	output	Keyboard reset signal
23	SYSRSTB	input	System reset signal
24	PC4	input	Video memory size mode
25	TMROUT2	input	Timer counter from 8253 out2
26	SNDCNTL1	output	Sound control 1
27	SNDCNTL0	output	Sound control 0
28	SNDCNTL2	output	Sound control 2
29	FDCTC	output	FDC terminal count
30	MTRON	output	Motor ON signal to disk drive
31	DMA/I	output	DMA Request & FDC Interrupt enable
32	FDCRSTB	output	FDC reset signal
33	DS1	output	Drive select 1 signal
34	DS0	output	Drive select 0 signal
35	PPITIM	output	Timer Video signal
36	TCH2G	output	Timer channel 2 gate
37	FAST	input	4.77Mhz or 7.16Mhz mode select
38	MULTIDAT	output	Multi-data
39	MULTICLK	output	Multi-clock
40	VDD	power	+5 Volt Power Supply

2. ENVIRONMENTAL SPECIFICATIONS

2.1 Storage Temperature -65 C to 150 C
2.2 Operating Temperature 0 C to 70 C

3. ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Rating

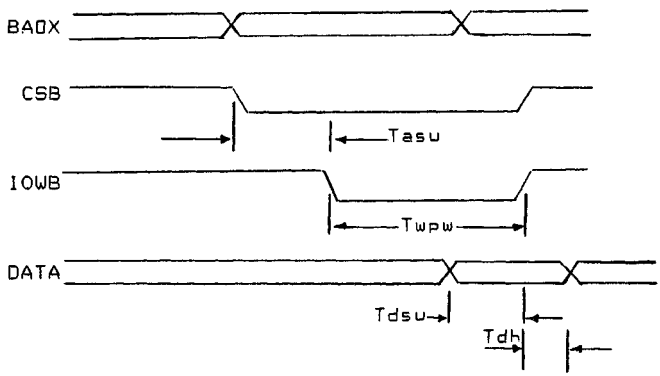
Parameter	Min.	Typ.	Max.	Units	Cond.
Voltage, any pin	-1.0		7.0	Volts	W.R.T ground
Power Dissipation			0.5	Watts	

3.2 D.C. Electrical Characteristics

Symb.	Parameter	Min.	Typ.	Max.	Units	Cond.
VDD	Supply Voltage	4.5	5.0	5.5	Volts	
Icc(q)	Quiescent current			50	uA	
Icc(o)	Operating Current			40	mA	
Vil	Input Low Voltage			0.8	Volts	TTL inputs
Vih	Input High Voltage	2.0			Volts	TTL inputs
Iin	Input Leakage	-10		10	uA	
Cin	Input Capacitance			7	pF	
Vol	Output Low Voltage			0.4	Volts	@4 mA
Voh	Output High Voltage	2.4			Volts	@-2 mA
Ioz	High Impedance Leak	-10		10	uA	

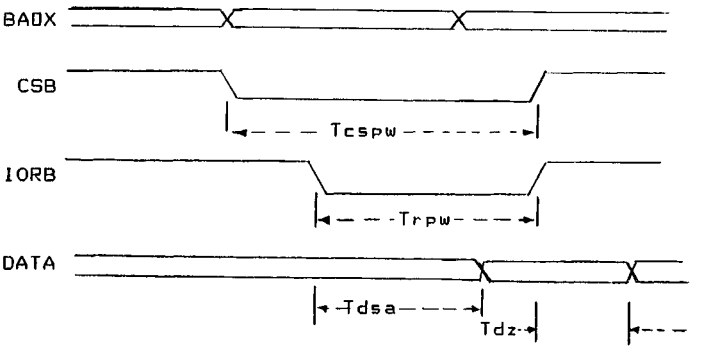
3.3 A.C Electrical Characteristics

3.3.1 Write Cycle



Symb.	Parameter	Min.	Typ.	Max.	Units	Cond.
Tasu	Address Setup	15			nS	
Twpw	Write Pulse Width	69			nS	
Tdsu	Data Setup	29			nS	
Tdh	Data Hold	6			nS	

3.3.2 Read Cycle



Symb.	Parameter	Min.	Typ.	Max.	Units	Cond.
Tcspw	Chip Select Width	69			nS	
Trpw	Read Pulse Width	69			nS	
Tda	Data Access			69	nS	
Tdz	Bus Hold/release	6		25	ns	

NEC
NEC Electronics Inc.

μPD8035HL/48H
HIGH-SPEED, 8-BIT, SINGLE-CHIP HMOS MICROCOMPUTERS

Description

The μPD8035HL and the μPD8048H make up the μPD8048H family of single-chip 8-bit microcomputers. The processors in this family differ only in their internal program memory options: the μPD8048H with 1K×8 bytes of mask ROM and the μPD8035HL with external memory.

The NEC μPD8035HL and μPD8048H are single component, 8-bit, parallel microprocessors using n-channel silicon gate MOS technology. The μPD8048H family of components functions efficiently in control as well as in arithmetic applications. Standard logic function implementation is facilitated by the large variety of branch and table look-up instructions.

The μPD8035HL/48H instruction set comprises 1 and 2 byte instructions with over 70% of them single-byte. Execution requires only 1 or 2 cycles per instruction and over 50% are single-cycle instructions.

The functions of the μPD8048H series of microprocessors can easily be expanded using standard 8080A/8085A peripherals and memories.

The μPD8048H contains the following functions usually found in external peripheral devices: 1024×8 bits of ROM program memory; 64×8 bits of RAM data memory; 27 I/O lines; an 8-bit interval timer/event counter; oscillator and clock circuitry.

The μPD8035HL is intended for applications using external program memory only. It contains all the features of the μPD8048H except the 1024×8-bit internal ROM. The external program memory can be implemented using standard 8080A/8085A memory products.

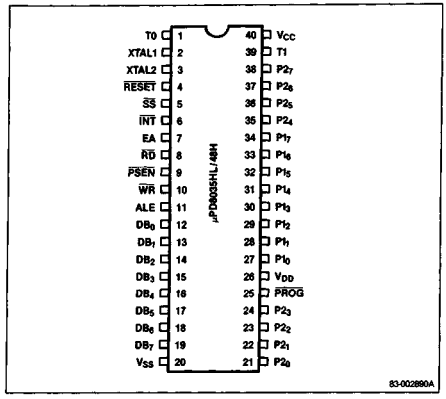
Features

- ☐ Fully compatible with industry standard 8048/8748/8035
- ☐ 2.5 μs cycle time: all instructions 1 or 2 bytes
- ☐ Interval timer/event counter
- ☐ 64×8-byte RAM data memory
- ☐ External and timer interrupts
- ☐ 96 instructions: 70% single byte
- ☐ 27 I/O lines
- ☐ Internal clock generator
- ☐ 8 level stack
- ☐ Compatible with 8080A/8085A peripherals
- ☐ HMOS silicon gate technology
- ☐ Single +5 V power supply

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD8035HLC	40-pin plastic DIP	6 MHz
μPD8048HC	40-pin plastic DIP	6 MHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1	T0	Test 0 input / output
2	XTAL1	Crystal 1 input
3	XTAL2	Crystal 2 input
4	$\overline{RESET}$	Reset input
5	$\overline{SS}$	Single step input
6	$\overline{INT}$	Interrupt input
7	EA	External access input
8	$\overline{RD}$	Read output
9	$\overline{PSEN}$	Program store enable output
10	$\overline{WR}$	Write output
11	ALE	Address latch enable output
12-19	DB_0-DB_7	Bidirectional data bus
20	V_{SS}	Ground
21-24, 35-38	$P2_0$-$P2_7$	Quasi-bidirectional Port 2
25	$\overline{PROG}$	Program output

Pin Identification (cont)

No.	Symbol	Function
26	V_{DD}	RAM power supply
27-34	$P1_0$-$P1_7$	Quasi-bidirectional Port 1
39	T1	Test 1 input
40	V_{CC}	Primary power supply

Pin Functions

XTAL 1 (Crystal 1)

XTAL1 is one side of the crystal, LC, or external frequency source (non-TTL-compatible V_{IH}).

XTAL 2 (Crystal 2)

XTAL2 is the other side of the crystal or frequency source.

T0 (Test 0)

T0 is the testable input using conditional transfer functions JT0 and JNT0. The internal state clock (CLK) is available to T0 using the ENT0 CLK instruction. T0 can also be used during programming as a testable flag.

T1 (Test 1)

T1 is the testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.

$\overline{\text{RESET}}$ (Reset)

An active low on $\overline{\text{RESET}}$ initializes the processor. $\overline{\text{RESET}}$ is also used for PROM programming verification and power-down (non-TTL compatible V_{IH}).

$\overline{\text{SS}}$ (Single Step)

An active low on $\overline{\text{SS}}$, together with ALE, causes the processor to execute the program one step at a time.

$\overline{\text{INT}}$ (Interrupt)

An active low on $\overline{\text{INT}}$ starts an interrupt if interrupts are enabled. A reset disables an interrupt. $\overline{\text{INT}}$ can be tested with the JNI instruction and, depending on the results, a jump to the specified address can occur.

EA (External Access)

An active high on EA disables internal program memory and fetches and accesses external program memory. EA is used for system testing and debugging.

$\overline{\text{RD}}$ (Read)

$\overline{\text{RD}}$ will pulse low when the processor performs a bus read. An active low on $\overline{\text{RD}}$ enables data onto the processor bus from a peripheral device and functions as a read strobe for external data memory.

$\overline{\text{WR}}$ (Write)

$\overline{\text{WR}}$ will pulse low when the processor performs a bus write. $\overline{\text{WR}}$ can also function as a write strobe for external data memory.

$\overline{\text{PSEN}}$ (Program Store Enable)

$\overline{\text{PSEN}}$ becomes active only during an external memory fetch. (Active low).

ALE (Address Latch Enable)

ALE occurs at each cycle. ALE can also be used as a clock output. The falling edge of ALE addresses external data memory or external program memory.

DB_0-DB_7 (Data Bus)

DB_0-DB_7 is a bidirectional port. Synchronous reads and writes can be performed on this port using $\overline{\text{RD}}$ and $\overline{\text{WR}}$ strobes. The contents of the DB_0-DB_7 bus can be latched in a static mode.

During an external memory fetch, DB_0-DB_7 output the low-order eight bits of the memory address. $\overline{\text{PSEN}}$ fetches the instruction. DB_0-DB_7 also output the address of an external data memory fetch. The addressed data is controlled by ALE, $\overline{\text{RD}}$, and $\overline{\text{WR}}$.

$P1_0$-$P1_7$ (Port 1)

$P1_0$-$P1_7$ is an 8-bit quasi-bidirectional port.

$P2_0$-$P2_7$ (Port 2)

$P2_0$-$P2_7$ is an 8-bit quasi-bidirectional port. $P2_0$-$P2_3$ output the high-order four bits of the address during an external program memory fetch. $P2_0$-$P2_3$ also function as a 4-bit I/O bus for the μPD82C43 I/O port expander.

$\overline{\text{PROG}}$ (Program Pulse)

$\overline{\text{PROG}}$ is used as an output pulse during a fetch when interfacing with the μPD82C43 I/O port expander.

V_{CC} (Primary Power Supply)

V_{CC} is the primary power supply. V_{CC} is +5V during normal operation.

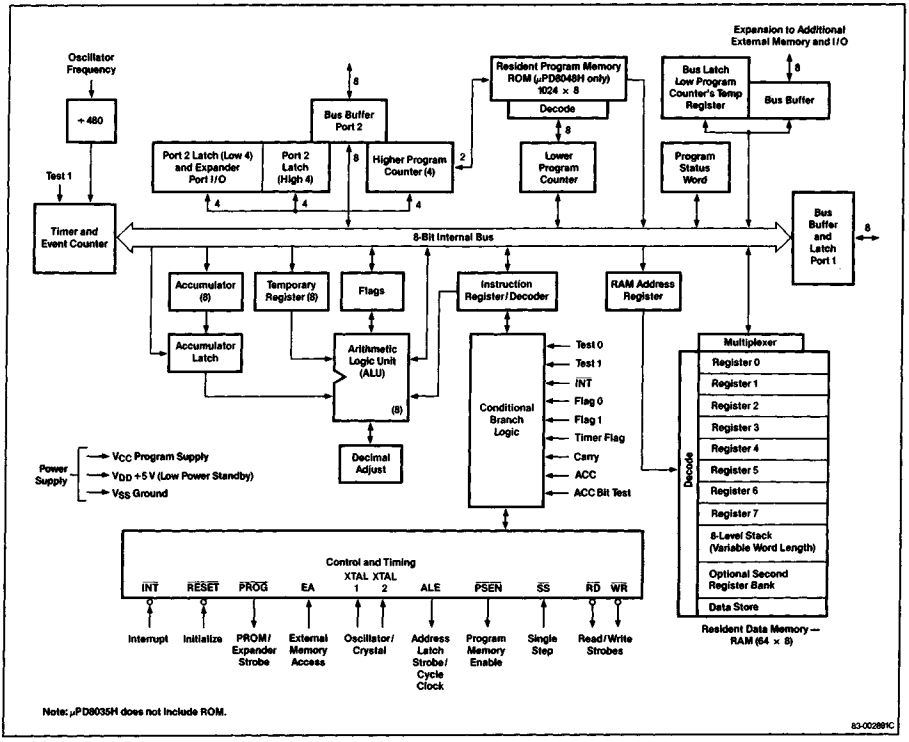
V_{DD} (RAM Power Supply)

V_{DD} must be set to +5 V for normal operation. V_{DD} supplies power to the internal RAM during standby mode.

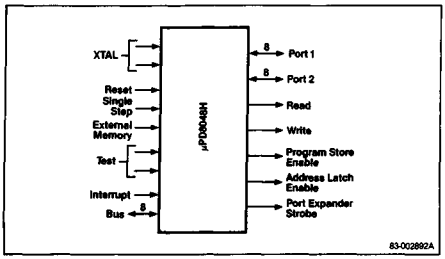
V_{SS} (Ground)

V_{SS} is ground potential.

Block Diagram



Logic Symbol



Absolute Maximum Ratings

$T_A = 25°C$

Operating temperature, T_{OPT}	0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C
Voltage on any pin, $V_{I/O}$	−0.5 V to +7 V (Note 1)
Power dissipation, P_D	1.5 W

Note:
(1) With respect to ground.

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input low voltage (All except XTAL1, XTAL2)	V_{IL}	−0.5		0.8	V	
Input low voltage ($\overline{RESET}$, X1, X2)	V_{IL1}	−0.5		0.8	V	
Input high voltage (All except XTAL1, XTAL2, $\overline{RESET}$)	V_{IH}	2.0		V_{CC}	V	
Input high voltage (XTAL1, XTAL2, $\overline{RESET}$)	V_{IH1}	3.8		V_{CC}	V	
Output low voltage (bus)	V_{OL}			0.45	V	$I_{OL} = 2.0$ mA
Output low voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL1}			0.45	V	$I_{OL} = 2.0$ mA
Output low voltage ($\overline{PROG}$)	V_{OL2}			0.45	V	$I_{OL} = 2.0$ mA

DC Characteristics (cont)

$T_A = 0°C$ to $+70°C$, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output low voltage (all other outputs)	V_{OL3}			0.45	V	$I_{OL} = 2.0$ mA
Output high voltage (bus)	V_{OH}	2.4			V	$I_{OH} = -400\,\mu A$
Output high voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OH1}	2.4			V	$I_{OH} = -400\,\mu A$
Output high voltage (all other outputs)	V_{OH2}	2.4			V	$I_{OH} = -40\,\mu A$
Input leakage current (T1, $\overline{INT}$)	I_{IL}			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Input leakage current ($P1_0$–$P1_7$, $P2_0$–$P2_7$, EA, $\overline{SS}$)	I_{IL1}			−500	μA	$V_{CC} \geq V_{IN} \geq V_{SS} + 0.45$ V
Output leakage current (bus, T0, high impedance state)	I_{OL}			±10	μA	$V_{CC} \geq V_{IN} \geq V_{SS} + 0.45$ V
Power down supply current	I_{DD}		4	8	mA	$T_A = 25°C$
Total supply current	$I_{DD} + I_{CC}$		50	80	mA	$T_A = 25°C$
RAM standby voltage	V_{DD}	2.2		5.5	V	Standby mode. Reset ≤ 0.6 V

AC Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
ALE pulse width	t_{LL}	410			ns	(Note 1)
Address setup to ALE	t_{AL}	220			ns	(Note 1)
Address hold from ALE	t_{LA}	120			ns	(Note 1)
Control pulse width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}	1050			ns	(Note 1)
Control pulse width ($\overline{PSEN}$)	t_{CC2}	800			ns	(Note 1)
Data setup $\overline{WR}$	t_{DW}	880			ns	(Note 1)
Data hold after $\overline{WR}$	t_{WD}	110			ns	(Note 2)
Data hold ($\overline{RD}$, $\overline{PSEN}$)	t_{DR}	0		220	ns	(Note 1)
$\overline{RD}$ to data in	t_{RD1}			800	ns	(Note 1)
$\overline{PSEN}$ to data in	t_{RD2}			550	ns	(Note 1)

AC Characteristics (cont)

$T_A = 0°C$ to $+70°C$, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address setup to $\overline{WR}$	t_{AW}	680			ns	(Note 1)
Address setup to data ($\overline{RD}$)	t_{AD1}			1570	ns	(Note 1)
Address setup to data ($\overline{PSEN}$)	t_{AD2}			1090	ns	(Note 1)
Address float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}	290			ns	(Note 1)
Address float to $\overline{PSEN}$	t_{AFC2}	40			ns	(Note 1)
ALE to control ($\overline{RD}$, $\overline{WR}$)	t_{LAFC1}	420			ns	(Note 1)
ALE to control ($\overline{PSEN}$)	t_{LAFC2}	170			ns	(Note 1)
Control to ALE ($\overline{RD}$, $\overline{WR}$, $\overline{PROG}$)	t_{CA1}	120			ns	(Note 1)
Control to ALE ($\overline{PSEN}$)	t_{CA2}	620			ns	(Note 1)
Port control setup to $\overline{PROG}$	t_{CP}	210			ns	(Note 1)
Port control hold to $\overline{PROG}$	t_{PC}	460			ns	(Note 1)
$\overline{PROG}$ to P2 input valid	t_{PR}			1300	ns	(Note 1)
Input data hold from $\overline{PROG}$	t_{PF}			250	ns	(Note 1)
Output data setup	t_{DP}	850			ns	(Note 1)
Output data hold	t_{PD}	200			ns	(Note 1)
$\overline{PROG}$ pulse width	t_{PP}	1500			ns	(Note 1)
Port 2 I/O data setup to ALE	t_{PL}	460			ns	(Note 1)
Port 2 I/O data hold to ALE	t_{LP}	150			ns	(Note 1)
Port output from ALE	t_{PV}			850	ns	(Note 1)
Cycle time	t_{CY}	2.5		15	μs	(Note 1)
TO rep rate	t_{OPRR}	500			ns	(Note 1)

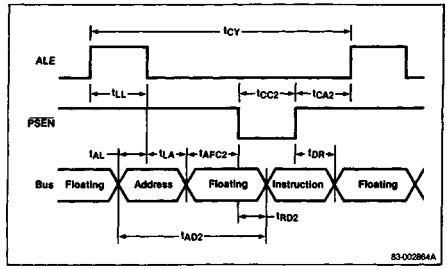
Note:

(1) Control outputs: $C_L = 80$ pF, bus outputs: $C_L = 150$ pF

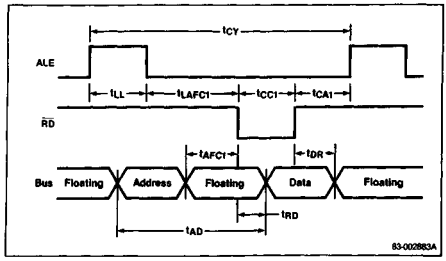
(2) Bus high impedance, load = 20 pF

Timing Waveforms

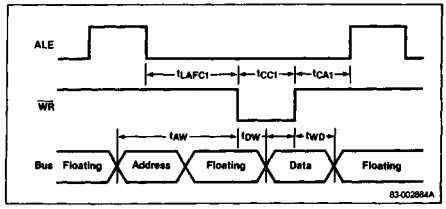
Instruction Fetch from External Memory



Read from External Data Memory

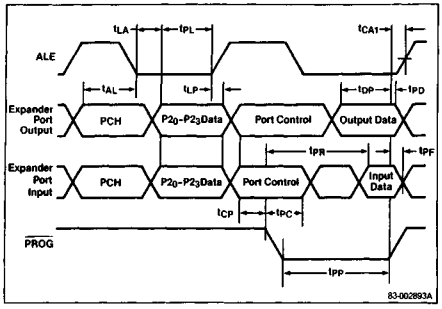


Write to External Memory



Timing Waveforms (cont)

Port 2 Timing



Bus Timing Requirements

Symbol	Timing Formula	Min/Max	Unit
t_{LL}	(7/30) t_{CY} – 170	Min	ns
t_{AL}	(2/15) t_{CY} – 110	Min	ns
t_{LA}	(1/15) t_{CY} – 40	Min	ns
t_{CC1}	(1/2) t_{CY} – 200	Min	ns
t_{CC2}	(2/5) t_{CY} – 200	Min	ns
t_{DW}	(13/30) t_{CY} – 200	Min	ns
t_{WD}	(1/15) t_{CY} – 50	Min	ns
t_{DR}	(1/10) t_{CY} – 30	Max	ns
t_{RD1}	(2/5) t_{CY} – 200	Max	ns
t_{RD2}	(3/10) t_{CY} – 200	Max	ns
t_{AW}	(1/3) t_{CY} – 150	Min	ns
t_{AD1}	(11/15) t_{CY} – 250	Max	ns
t_{AD2}	(8/15) t_{CY} – 250	Max	ns
t_{AFC1}	(2/15) t_{CY} – 40	Min	ns
t_{AFC2}	(1/30) t_{CY} – 40	Min	ns
t_{LAFC1}	(1/5) t_{CY} – 75	Min	ns
t_{LAFC2}	(1/10) t_{CY} – 75	Min	ns
t_{CA1}	(1/15) t_{CY} – 40	Min	ns
t_{CA2}	(4/15) t_{CY} – 40	Min	ns
t_{CP}	(1/10) t_{CY} – 40	Min	ns
t_{PC}	(4/15) t_{CY} – 200	Min	ns
t_{PR}	(17/30) t_{CY} – 120	Max	ns
t_{PF}	(1/10) t_{CY}	Max	ns
t_{DP}	(2/5) t_{CY} – 150	Min	ns
t_{PD}	(1/10) t_{CY} – 50	Min	ns
t_{PP}	(7/10) t_{CY} – 250	Min	ns
t_{PL}	(4/15) t_{CY} – 200	Min	ns
t_{LP}	(1/10) t_{CY} – 100	Min	ns
t_{PV}	(3/10) t_{CY} – 100	Max	ns
t_{OPRR}	(3/15) t_{CY}	Min	ns
t_{CY}	6 MHz		μs

Instruction Set

Mnemonic	Function	Description	Operation Code								Cycles	Bytes	Flags			
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			C	AC	F0	F1
Accumulator																
ADD A, # data	(A) ← (A) + data	Add immediate the specified data to the accumulator.	0	0	0	0	0	0	1	1	2	2	•			
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ADD A, Rr	(A) ← (A) + (Rr) r = 0–7	Add contents of designated register to the accumulator.	0	1	1	0	1	r	r	r	1	1	•			
ADD A, @ Rr	(A) ← (A) + ((Rr)) r = 0–1	Add indirect the contents of the data memory location to the accumulator.	0	1	1	0	0	0	0	r	1	1	•			
ADDC A, # data	(A) ← (A) + (C) + data	Add immediate with carry the specified data to the accumulator.	0	0	0	1	0	0	1	1	2	2	•			
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0–7	Add with carry the contents of the designated register to the accumulator.	0	1	1	1	1	r	r	r	1	1	•			
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0–1	Add indirect with carry the contents of data memory location to the accumulator.	0	1	1	1	0	0	0	r	1	1	•			
ANL A, # data	(A) ← (A) AND data	Logical AND specified immediate data with accumulator.	0	1	0	1	0	0	1	1	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ANL A, Rr	(A) ← (A) AND (Rr) r = 0–7	Logical AND contents of designated register with accumulator.	0	1	0	1	1	r	r	r	1	1				
ANL A, @ Rr	(A) ← (A) AND ((Rr)) r = 0–1	Logical AND indirect the contents of data memory with accumulator.	0	1	0	1	0	0	0	r	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the accumulator.	0	0	1	1	0	1	1	1	1	1				
CLR A	(A) ← 0	Clear the contents of the accumulator.	0	0	1	0	0	1	1	1	1	1				
DA A		Decimal adjust the contents of the accumulator.	0	1	0	1	0	1	1	1	1	1	•			
DEC A	(A) ← (A) – 1	Decrement by 1 the accumulator's contents.	0	0	0	0	0	1	1	1	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	0	0	0	1	0	1	1	1	1	1				
ORL A, # data	(A) ← (A) OR data	Logical OR specified immediate data with accumulator.	0	1	0	0	0	0	1	1	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0–7	Logical OR contents of designated register with accumulator.	0	1	0	0	1	r	r	r	1	1				
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0–1	Logical OR indirect the contents of data memory location with accumulator.	0	1	0	0	0	0	0	r	1	1				
RL A	(AN + 1) ← (AN); N = 0–6 (A_0) ← (A_7)	Rotate accumulator left by 1 bit without carry.	1	1	1	0	0	1	1	1	1	1				
RLC A	(AN + 1) ← (AN); N = 0–6 (A_0) ← (C) (C) ← (A_7)	Rotate accumulator left by 1 bit through carry.	1	1	1	1	0	1	1	1	1	1	•			
RR A	(AN) ← (AN + 1); N = 0–6 (A_7) ← (A_0)	Rotate accumulator right by 1 bit without carry.	0	1	1	1	0	1	1	1	1	1				

Instruction Set (cont)

Mnemonic	Function	Description	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Accumulator (cont)																
RRC A	(AN) ← (AN + 1); N = 0–6 (A_7) ← (C) (C) ← (A_0)	Rotate accumulator right by 1 bit through carry.	0	1	1	0	0	1	1	1	1	1	•			
SWAP A	(A_4–A_7) ← (A_0–A_3)	Swap the two 4-bit nibbles in the accumulator.	0	1	0	0	0	1	1	1	1	1				
XRL A, # data	(A) ← (A) XOR data	Logical XOR specified immediate data with accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0–7	Logical XOR contents of designated register with accumulator.	1	1	0	1	1	r	r	r	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0–1	Logical XOR indirect the contents of data memory location with accumulator.	1	1	0	1	0	0	0	r	1	1				
Branch																
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0–7 If (Rr) = 0; (PC_0–PC_7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2				
JBb addr	(PC_0–PC_7) ← addr if B_b = 1 (PC) ← (PC) + 2 if B_b = 0	Jump to specified address if accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2				
JC addr	(PC_0–PC_7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF0 addr	(PC_0–PC_7) ← addr if F0 = 1 (PC) ← (PC) + 2 if F0 = 0	Jump to specified address if flag F0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF1 addr	(PC_0–PC_7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if flag F1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JMP addr	(PC_8–PC_{10}) ← ($addr_8$–$addr_{10}$) (PC_0–PC_7) ← ($addr_0$–$addr_7$) (PC_{11}) ← DBF	Direct jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
JMPP @ A	(PC_0–PC_7) ← ((A))	Jump indirect to specified address with address page.	1	0	1	1	0	0	1	1	2	1				
JNC addr	(PC_0–PC_7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNI addr	(PC_0–PC_7) ← addr if I = 0 (PC) ← (PC) + 2 if I = 1	Jump to specified address if interrupt is low.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT0 addr	(PC_0–PC_7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT1 addr	(PC_0–PC_7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNZ addr	(PC_0–PC_7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 1	Jump to specified address if accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JTF addr	(PC_0–PC_7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if timer flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				

Instruction Set (cont)

Mnemonic	Function	Description	Operation Code								Cycles	Bytes	Flags			
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			C	AC	F0	F1
Branch (cont)																
JT0 addr	(PC_0–PC_7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT1 addr	(PC_0–PC_7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JZ addr	(PC_0–PC_7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 1	Jump to specified address if accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
Control																
EN I		Enable the external interrupt input.	0	0	0	0	0	1	0	1	1	1				
DIS I		Disable the external interrupt input.	0	0	0	1	0	1	0	1	1	1				
ENT0 CLK		Enable the clock output pin T0.	0	1	1	1	0	1	0	1	1	1				
SEL MB0	(DBF) ← 0	Select bank 0 (locations 0–2047) of program memory.	1	1	1	0	0	1	0	1	1	1				
SEL MB1	(DBF) ← 1	Select bank 1 (locations 2048–4095) of program memory.	1	1	1	1	0	1	0	1	1	1				
SEL RB0	(BS) ← 0	Select bank 0 (locations 0–7) of data memory.	1	1	0	0	0	1	0	1	1	1				
SEL RB1	(BS) ← 1	Select bank 1 (locations 24–31) of data memory.	1	1	0	1	0	1	0	1	1	1				
Data Moves																
MOV A, # data	(A) ← data	Move immediate the specified data into the accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
MOV A, Rr	(A) ← (Rr); r = 0–7	Move the contents of the designated registers into the accumulator.	1	1	1	1	1	r	r	r	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0–1	Move indirect the contents of data memory location into the accumulator.	1	1	1	1	0	0	0	r	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the program status word into the accumulator.	1	1	0	0	0	1	1	1	1	1				
MOV Rr, # data	(Rr) ← data; r = 0–7	Move immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2				
MOV Rr, A	(Rr) ← (A); r = 0–7	Move accumulator contents into the designated register.	1	0	1	0	1	r	r	r	1	1				
MOV @ Rr, A	((Rr)) ← (A); r = 0–1	Move indirect accumulator contents into data memory location.	1	0	1	0	0	0	0	r	1	1				
MOV @ Rr, # data	((Rr)) ← data; r = 0–1	Move immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	1 d_0	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1				
MOVP A, @ A	(PC_0–PC_7) ← (A) (A) ← ((PC))	Move data in the current page into the accumulator.	1	0	1	0	0	0	1	1	2	1				
MOVP3 A, @ A	(PC_0–PC_7) ← (A) (PC_8–PC_{10}) ← 011 (A) ← ((PC))	Move program data in page 3 into the accumulator.	1	1	1	0	0	0	1	1	2	1				

Instruction Set (cont)

Mnemonic	Function	Description	Operation Code								Cycles	Bytes	Flags			
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			C	AC	F0	F1
Data Moves (cont)																
MOVX A, @ R	(A) ← ((Rr)); r = 0–1	Move indirect the contents of external data memory into the accumulator.	1	0	0	0	0	0	0	r	2	1				
MOVX @ R, A	((Rr)) ← (A); r = 0–1	Move indirect the contents of the accumulator into external data memory.	1	0	0	1	0	0	0	r	2	1				
XCH A, Rr	(A) ↔ (Rr); r = 0–7	Exchange the accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1				
XCH A, @ Rr	(A) ↔ ((Rr)); r = 0–1	Exchange indirect contents of accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1				
XCHD A, @ Rr	$(A_0–A_3)$ ↔ $((Rr))_0–((Rr))_3$; r = 0–1	Exchange indirect 4-bit contents of accumulator and data memory.	0	0	1	1	0	0	0	r	1	1				
Flags																
CPL C	(C) ← NOT (C)	Complement contents of carry bit.	1	0	1	0	0	1	1	1	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement contents of flag F0.	1	0	0	1	0	1	0	1	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement contents of flag F1.	1	0	1	1	0	1	0	1	1	1				•
CLR C	(C) ← 0	Clear contents of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•			
CLR F0	(F0) ← 0	Clear contents of flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•	
CLR F1	(F1) ← 0	Clear contents of flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•
Input / Output																
ANL BUS, # data	(bus) ← (bus) AND data	Logical AND immediate specified data with contents of bus.	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ANL Pp, # data	(Pp) ← (Pp) AND data p = 1–2	Logical AND immediate specified data with designated port (1 or 2).	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
ANLD Pp, A	(Pp) ← (Pp) AND $(A_0–A_3)$; p = 4–7	Logical AND contents of accumulator with designated port (4–7).	1	0	0	1	1	1	p	p	2	1				
IN A, Pp	(A) ← (Pp); p = 1–2	Input data from designated port (1–2) into accumulator.	0	0	0	0	1	0	p	p	2	1				
INS A, BUS	(A) ← (bus)	Input strobed bus data into accumulator.	0	0	0	0	1	0	0	0	2	1				
MOVD A, Pp	$(A_0–A_3)$ ← (Pp); p = 4–7 $(A_4–A_7)$ ← 0	Move contents of designated port (4–7) into accumulator.	0	0	0	0	1	1	p	p	2	1				
MOVD Pp, A	(Pp) ← $(A_0–A_3)$; p = 4–7	Move contents of accumulator to designated port (4–7).	0	0	1	1	1	1	p	p	2	1				
ORL BUS, # data	(bus) ← (bus) OR data	Logical OR immediate specified data with contents of bus.	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ORLD Pp, A	(Pp) ← (Pp) OR $(A_0–A_3)$; p = 4–7	Logical OR contents of accumulator with designated port (4–7).	1	0	0	0	1	1	p	p	2	1				
ORL Pp, # data	(Pp) ← (Pp) OR data p = 1–2	Logical OR immediate specified data with designated port (1–2).	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
OUTL BUS, A	(bus) ← (A)	Output contents of accumulator onto bus.	0	0	0	0	0	0	1	0	2	1				
OUTL Pp,A	(Pp) ← (A); p = 1–2	Output contents of accumulator to designated port (1–2).	0	0	1	1	1	0	p	p	2	1				

NEC

Instruction Set (cont)

Mnemonic	Function	Description	Operation Code								Cycles	Bytes	Flags			
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			C	AC	F0	F1
Subroutine																
Registers																
DEC Rr (Rr)	(Rr) ← (Rr) − 1; r = 0–7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1				
INC Rr	(Rr) ← (Rr) + 1; r = 0–7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1				
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0–1	Increment indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1				
CALL addr	((SP)) ← (PC), (PSW_4–PSW_7), (SP) ← (SP) + 1 (PC_8–PC_{10}) ← ($addr_8$–$addr_{10}$) (PC_0–PC_7) ← ($addr_0$–$addr_7$) (PC_{11}) ← DBF	Call designated subroutine.	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
RET	(SP) ← (SP) − 1 (PC) ← ((SP))	Return from subroutine without restoring program status word.	1	0	0	0	0	0	1	1	2	1				
RETR	(SP) ← (SP) − 1 (PC) ← ((SP)) (PSW_4–PSW_7) ← ((SP))	Return from subroutine restoring program status word.	1	0	0	1	0	0	1	1	2	1				
Timer / Counter																
EN TCNTI		Enable internal interrupt flag for timer / counter output.	0	0	1	0	0	1	0	1	1	1				
DIS TCNTI		Disable internal interrupt flag for timer / counter output.	0	0	1	1	0	1	0	1	1	1				
MOV A, T	(A) ← (T)	Move contents of timer / counter into accumulator.	0	1	0	0	0	0	1	0	1	1				
MOV T, A	(T) ← (A)	Move contents of accumulator into timer / counter.	0	1	1	0	0	0	1	0	1	1				
STOP TCNT		Stop count for event counter.	0	1	1	0	0	1	0	1	1	1				
STRT CNT		Start count for event counter.	0	1	0	0	0	1	0	1	1	1				
STRT T		Start count for timer.	0	1	0	1	0	1	0	1	1	1				
Miscellaneous																
NOP		No operation performed.	0	0	0	0	0	0	0	0	1	1				

Note:

(1) Operation code designations *r* and *p* form the binary representation of the registers and ports involved.

(2) The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.

(3) References to the address and data are specified in bytes 2 and/or 1 of the instruction.

(4) Numerical subscripts appearing in the function column reference the specific bits affected.

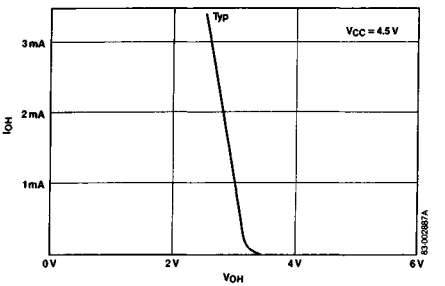
(5) When the bus is written to, with an OUTL instruction, the bus remains an output port until either device is reset or a MOVX instruction is excecuted.

Instruction Set Symbol Definitions

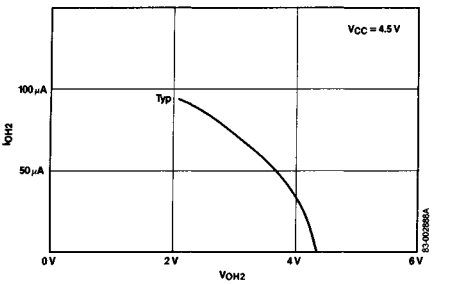
Symbol	Description
A	Accumulator
AC	Auxiliary carry flag
addr	Program memory address (12 bits)
B_b	Bit designator (b = 0–7)
BS	Bank switch
BUS	Bus port
C	Carry flag
CLK	Clock signal
CNT	Event counter
D	Nibble designator (4 bits)
data	Number of expression (8 bits)
DBF	Memory bank flip-flop
F0, F1	Flags 0, 1
I	Interrupt
P	"In-page" operation designator
Pp	Port designator (p = 1, 2 or 4–7)
PSW	Program status word
Rr	Register designator (r = 0, 1 or 0–7)
SP	Stack pointer
T	Timer
TF	Timer flag
T0, T1	Testable flags 0, 1
X	External RAM
#	Prefix for immediate data
@	Prefix for indirect address
$	Program counter's current value
(x)	Contents of external RAM location
((x))	Contents of memory location addressed by the contents of external RAM location
←	Replaced by
AND	Logical product (logical AND)
OR	Logical sum (logical OR)
XOR	Exclusive-OR

Operating Characteristics

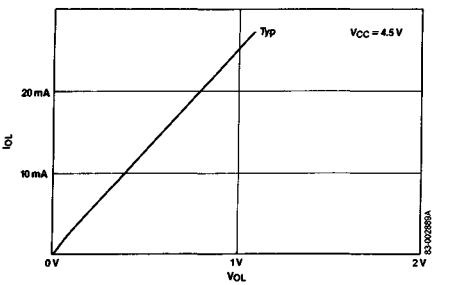
Bus Output High Voltage vs. Source Current



Port P1 & P2 Output High Voltage vs. Source Current



Bus Output Low Voltage vs. Sink Current



μPD80C35/C48, μPD48
8-BIT, SINGLE-CHIP
CMOS MICROCOMPUTERS

Description

The μPD80C35, μPD80C48, and μPD48 are true stand-alone 8-bit microcomputers fabricated using CMOS technology. All of the functional blocks necessary for an integrated microcomputer are incorporated, including a 1K-byte ROM (μPD80C48 only), a 64-byte RAM, 27 I/O lines, an 8-bit timer/event counter, and a clock generator. This integrated capability permits use in stand-alone applications. For designs requiring extra capability, the μPD80C35/μPD80C48 can be expanded using peripherals and is memory compatible with industry-standard 8080A/8085A processors.

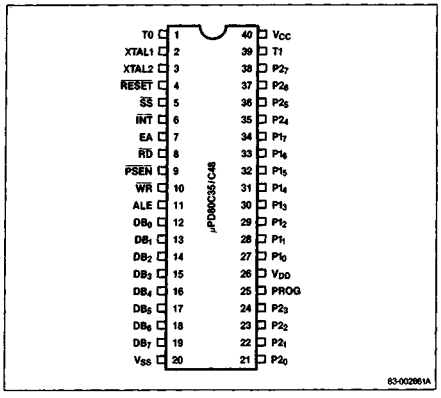
Providing compatibility with industry-standard 8048, 8748, and 8035 processors, the μPD80C35/μPD80C48 features significant savings in power consumption. In addition to the power savings gained through CMOS technology, the μPD80C35/μPD80C48 offers two standby modes (Halt and Stop modes) to further minimize power drain.

Features

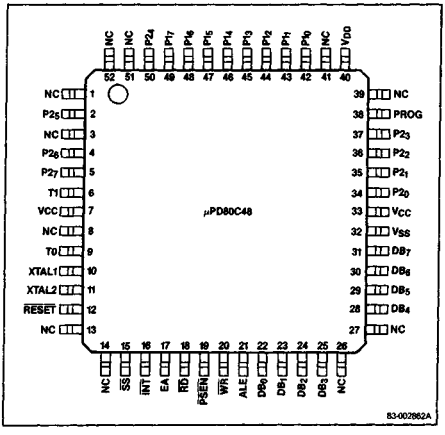
- ☐ 8-Bit CPU with memory and I/O on a single-chip
- ☐ Hardware/software-compatible with industry-standard 8048, 8748, and 8035 processors
- ☐ 1K x 8 ROM (μPD80C48 only)
- ☐ 64 x 8 RAM
- ☐ 27 I/O lines
- ☐ 2.5-μs cycle time (6-MHz crystal)
- ☐ All instructions executable in 1 or 2 cycles
- ☐ 97 instructions: 70 percent are single-byte instructions
- ☐ Internal timer/event counter
- ☐ Two interrupts (external and timer)
- ☐ Easily expandable memory and I/O
- ☐ Bus compatible with 8080A/8085A peripherals
- ☐ Power-efficient CMOS technology requiring a single +2.5 to +6.0 V power supply
- ☐ Halt mode
- ☐ Stop mode

Pin Configurations

40-Pin Plastic DIP

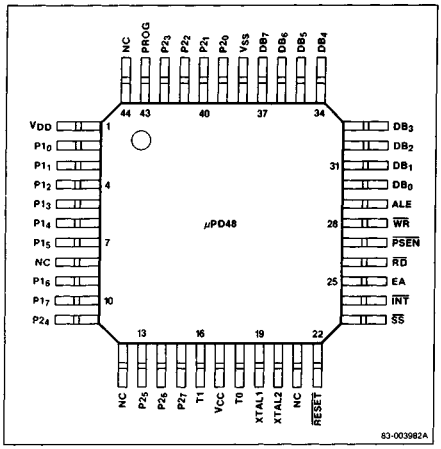


52-Pin Plastic Miniflat



Pin Configurations (cont)

44-Pin Plastic Miniflat



Ordering Information

Part Number	Package Type	Max Frequency of Operation	ROM
μPD80C35C	40-pin plastic DIP	6 MHz	None
μPD80C48C	40-pin plastic DIP	6 MHz	1K x 8
μPD80C48G-00	52-pin plastic miniflat	6 MHz	1K x 8
μPD48G-22	44-pin plastic miniflat	6 MHz	1K x 8

Note:

μPD80C48C, μPD80C48G-00, and μPD48G-22 have two optional port types: type 0, $I_{OH} = -5\,\mu A$; type 1, $I_{OH} = -50\,\mu A$. Type 0 or 1 can be selected independently for $P1_0$-$P1_7$, $P2_0$-$P2_3$, and $P2_4$-$P2_7$.

Pin Identification

Symbol	Function
T0	Test 0 input/clock output
XTAL1	Crystal 1 input
XTAL2	Crystal 2 input
$\overline{RESET}$	Reset input
$\overline{SS}$	Software stop input
$\overline{INT}$	Interrupt input
EA	External access input
$\overline{RD}$	Read output
$\overline{PSEN}$	Program store enable output
$\overline{WR}$	Write output
ALE	Address latch enable output
DB_0-DB_7	Bidirectional data bus
V_{SS}	Ground
$P2_0$-$P2_7$	Quasi-bidirectional port 2
PROG	Program output
V_{DD}	Oscillator control voltage
$P1_0$-$P1_7$	Quasi-bidirectional port 1
T1	Test 1 input
V_{CC}	Primary power supply
NC	No connection

Pin Functions

XTAL1, XTAL2 [Crystals 1, 2]

XTAL1 and XTAL2 are the crystal inputs for the internal clock oscillator. XTAL1 is also used as an input for external clock signals.

T0 [Test 0]

The JT0 and JNT0 instructions test the level of T0 and, if it is high, the program address jumps to the specified address. T0 becomes a clock output when the ENT0 CLK instruction is executed.

T1 [Test 1]

The JT1 and JNT1 instructions test the level of T1 and, if it is high, the program address jumps to the specified address. T1 becomes an internal counter input when the STRT CNT instruction is executed.

$\overline{RESET}$ [Reset]

$\overline{RESET}$ initializes the processor and is also used to verify the internal ROM. $\overline{RESET}$ determines the oscillation stabilizing time during the release of STOP mode. The $\overline{RESET}$ pulse width requires at least 5 machine cycles when the supply voltage is within specifications and the oscillation frequency is stable.

$\overline{SS}$ [Single Step]

$\overline{SS}$ causes the processor to execute the program one step at a time.

$\overline{INT}$ [Interrupt]

$\overline{INT}$ starts an interrupt if interrupts are enabled. A reset disables an interrupt. INT can be tested with the JNI instruction and, depending on the results, a jump to the specified address can occur.

EA [External Access]

EA disables internal program memory and fetches and accesses external program memory. EA is used for system testing and debugging.

$\overline{RD}$ [Read]

$\overline{RD}$ enables a data read from external memory.

$\overline{WR}$ [Write]

$\overline{WR}$ enables a data write to external memory.

$\overline{PSEN}$ [Program Store Enable]

$\overline{PSEN}$ fetches instructions only from external program memory.

ALE [Address Latch Enable]

ALE occurs at each cycle. The falling edge of ALE addresses external data memory or external program memory. ALE can also be used as a clock output.

DB_0-DB_7 [Data Bus]

DB_0-DB_7 is a bidirectional port, which reads and writes data using $\overline{RD}$ and $\overline{WR}$ for latching. During an external program memory fetch, DB_0-DB_7 output the low-order eight bits of the memory address. $\overline{PSEN}$ fetches the instruction. DB_0-DB_7 also output the address of an external data memory fetch. The addressed data is read and written by $\overline{RD}$ and $\overline{WR}$.

$P1_0$-$P1_7$ [Port 1]

$P1_0$-$P1_7$ is an 8-bit quasi-bidirectional port.

$P2_0$-$P2_7$ [Port 2]

$P2_0$-$P2_7$ is an 8-bit quasi-bidirectional port. $P2_0$-$P2_3$ output the high-order four bits of the address during an external program memory fetch. $P2_0$-$P2_3$ also function as a 4-bit I/O bus for the μPD82C43 I/O port expander.

PROG [Program Pulse]

PROG is used as an output pulse during a fetch when interfacing with the μPD82C43 I/O port expander.

V_{DD} [Oscillator Control Voltage]

V_{DD} stops and starts the oscillator in STOP mode. STOP mode is enabled by forcing V_{DD} low during a rest.

V_{CC} [Primary Power Supply]

V_{CC} is the primary power supply. V_{CC} must be between +2.5 V and +6.0 V for normal operation. In STOP mode, V_{CC} must be at least +2.0 V to ensure data retention.

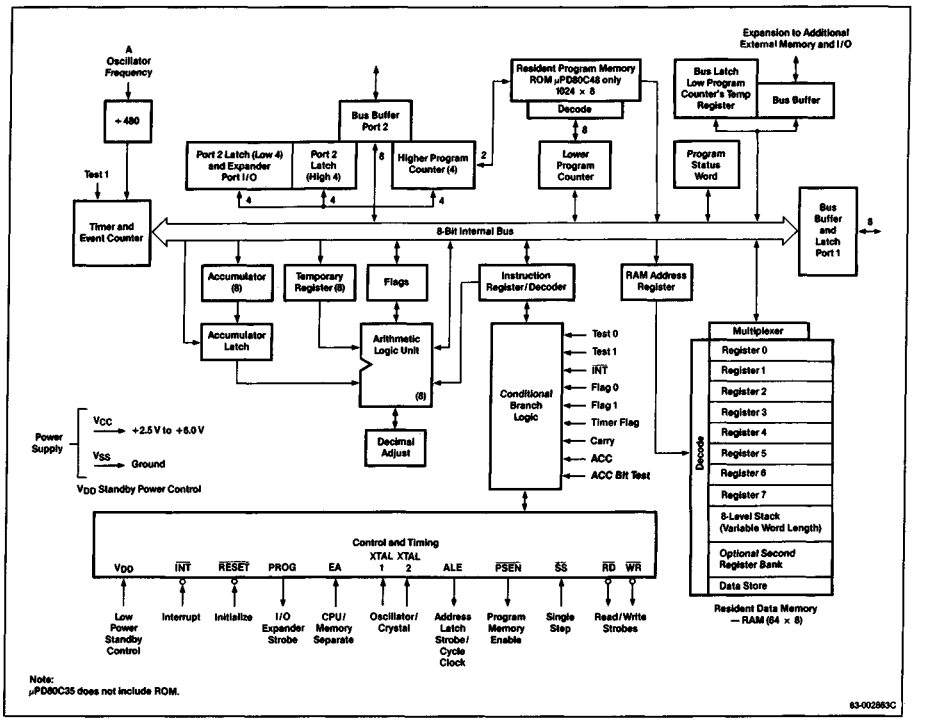
V_{SS} [Ground]

V_{SS} is ground potential.

NC [No Connection]

NC is no connection.

Block Diagram



Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{CC}	$V_{SS} - 0.3$ to $+10$ V
Input voltage, V_{IN}	$V_{SS} - 0.3$ to $V_{CC} + 0.3$ V
Output voltage, V_O	$V_{SS} - 0.3$ to $V_{CC} + 0.3$ V
Operating temperature, T_{OPT}	$-40°C$ to $+85°C$
Storage temperature, T_{STG}	$-65°C$ to $+150°C$

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Standard Voltage Range

$T_A = -40°C$ to $+85°C$, $V_{CC} = +5\,V \pm 10\%$, $V_{SS} = 0\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}	−0.3		+0.8	V	
Input voltage high	V_{IH}	$V_{CC}-2$		V_{CC}	V	Except XTAL1, XTAL2, $\overline{RESET}$
	V_{IH1}	$V_{CC}-1$		V_{CC}	V	$\overline{RESET}$, XTAL1, XTAL2
Output voltage low	V_{OL}			+0.45	V	$I_{OL} = 2.0$ mA
Output voltage high	V_{OH}	2.4			V	Bus, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0; $I_{OH} = -100\,\mu A$
	V_{OH1}(1)	2.4			V	$I_{OH} = -5\,\mu A$ (type 0) port 1, port 2
		2.4			V	$I_{OH} = -50\,\mu A$ (type 1) port 1, port 2
	V_{OH2}	$V_{CC}-0.5$			V	All outputs, $I_{OH} = -0.2\,\mu A$
Input current	I_{ILP}(1)		−15	−40	μA	Port 1, port 2; $V_{IN} \leq V_{IL}$ (type 0)
				−500	μA	Port 1, port 2; $V_{IN} \leq V_{IL}$ (type 1)
	I_{ILC}			−40	μA	$\overline{SS}$, $\overline{RESET}$; $V_{IN} \leq V_{IL}$
Input leakage current	I_{LI1}			±1	μA	T1, $\overline{INT}$, V_{CC}; $V_{SS} \leq V_{IN} \leq V_{CC}$
	I_{LI2}			±3	μA	EA; $V_{SS} \leq V_{IN} \leq V_{CC}$
Output leakage current	I_{LO}			±1	μA	$V_{SS} \leq V_O \leq V_{CC}$ High impedance, bus, T0
Standby current	I_{CC1}		0.4	0.8	mA	Halt mode $t_{CY} = 2.5\,\mu s$
	I_{CC2}		1	20	μA	Stop mode (Note 2)
Supply current	I_{CC}		4	8	mA	$t_{CY} = 2.5\,\mu s$
Data retention voltage	V_{CCDR}	2.0			V	Stop mode (V_{DD}, $\overline{RESET} \geq 0.4\,V$)

Extended Voltage Range

$T_A = -40°C$ to $+85°C$, $V_{CC} = +2.5\,V$ to $+6.0\,V$, $V_{SS} = 0\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}	−0.3		$+0.18V_{CC}$	V	
Input voltage high	V_{IH}	$0.7V_{CC}$		V_{CC}	V	Except XTAL1, XTAL2
	V_{IH1}	$0.8V_{CC}$		V_{CC}	V	XTAL1, XTAL2
Output voltage low	V_{OL}			+0.45	V	$I_{OL} = 1.0$ mA
Output voltage high	V_{OH}	$0.75V_{CC}$			V	Bus, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0; $I_{OH} = -100\,\mu A$
	V_{OH1}	$0.7V_{CC}$			V	All other outputs; $I_{OH} = -1\,\mu A$ (type 0) port 1, port 2
		$0.7V_{CC}$			V	All other outputs; $I_{OH} = -10\,\mu A$ (type 1) port 1, port 2
Input current	I_{ILP}		−15	−40	μA	Port 1, port 2; $V_{IN} \leq V_{IL}$ (type 0)
				−500	μA	Port 1, port 2; $V_{IN} \leq V_{IL}$ (type 1)
Input leakage current	I_{IL}			−40	μA	$\overline{SS}$, $\overline{RESET}$; $V_{IN} \leq V_{IL}$
	I_{LI1}			±1	μA	T1, $\overline{INT}$, $V_{SS} < V_{IN} < V_{CC}$
	I_{LI2}			±5	μA	EA; $V_{SS} < V_{IN} < V_{CC}$
Output leakage current	I_{LO}			±1	μA	$V_{SS} < V_O < V_{CC}$, Bus, T0 — high impedance state
Supply current	I_{CC}		0.8	1.6	mA	$V_{CC} = 3\,V$, $t_{CY} = 10\,\mu s$
			6	12	μA	$V_{CC} = 6\,V$, $t_{CY} = 25\,\mu s$
Standby current	I_{CC1}		100	200	μA	Halt mode; $V_{CC} = 3\,V$, $t_{CY} = 10\,\mu s$
			0.6	1.2	mA	$V_{CC} = 6\,V$, $t_{CY} = 2.5\,\mu s$
	I_{CC2}		1	20	μA	Stop mode, $V_{CC} = 3\,V$
			1	50	μA	$V_{CC} = 6\,V$

Note:

(1) Types 0, 1 for μPD80C48 only.
Type 0 for μPD80C35 only.

(2) Input pin voltage is $V_{IN} \leq V_{IL}$, or $V_{IN} \geq V_{IH}$.

AC Characteristics

Read, Write and Instruction Fetch: External Data and Program Memory

$T_A = -40°C$ to $+85°C$, $V_{CC} = V_{DD} = +5\,V \pm 10\%$; $V_{SS} = 0\,V$

		Limits					
		V_{CC} = +5 V ± 10%		V_{CC} = 2.5 V to 6.0 V			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
ALE pulse width	t_{LL}	400		2160		ns	
Address setup before ALE	t_{AL}	120		1620		ns	
Address hold from ALE	t_{LA}	80		330		ns	(Note 1)
Control pulse width ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$)	t_{CC}	700		3700		ns	
Data setup before $\overline{WR}$	t_{DW}	500		3500		ns	
Data hold after $\overline{WR}$	t_{WD}	120		370		ns	(Note 2)
Cycle time	t_{CY}	2.5	150	10	150	μs	6 MHz XTAL
Data hold	t_{DR}	0	200	0	950	ns	
$\overline{PSEN}$, $\overline{RD}$ to data in	t_{RD}		500		2750	ns	
Address setup before $\overline{WR}$	t_{AW}	230		3230		ns	(Note 1)
Address setup before data in	t_{AD}		950		5450		
Address float to $\overline{RD}$, $\overline{PSEN}$	t_{AFC}	0		500		ns	
Control pulse to ALE	t_{CA}	10		10		ns	

Port 2 Timing

$T_A = -40°C$ to $+85°C$, $V_{CC} = V_{DD} = +5\,V \pm 10\%$; $V_{SS} = 0\,V$

		Limits					
		V_{CC} = +5 V ± 10%		V_{CC} = 2.5 V to 6.0 V			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Port control setup before falling edge of PROG	t_{CP}	110		860		ns	
Port control hold after falling edge of PROG	t_{PC}	0	80	0	200	ns	(Note 4)
PROG to time P2 input must be valid	t_{PR}		810		5310	ns	
Output data setup time	t_{DP}	250		3250		ns	(Note 3)
Output data hold time	t_{PD}	65		820		ns	
Input data hold time	t_{PF}	0	150	0	900	ns	
PROG pulse width	t_{PP}	1200		6450		ns	
Port 2 I/O data setup time	t_{PL}	350		2100		ns	
Port 2 I/O data hold time	t_{LP}	150		1400		ns	

Note:

(1) Control outputs: $C_L = 80$ pF, bus outputs: $C_L = 150$ pF

(2) $C_L = 20$ pF

(3) Control outputs: $C_L = 80$ pF

(4) *Refer to the operating characteristics curves for supply voltage and port control hold.*

Bus Timing Requirements (Note 1)

Symbol	Timing Formula	Min/Max	Unit
t_{LL}	(7/30) t_{CY} − 170	Min	ns
t_{AL}	(1/5) t_{CY} − 380	Min	ns
t_{LA}	(1/30) t_{CY}	Min	ns
t_{CC}	(2/5) t_{CY} − 300	Min	ns
t_{DW}	(2/5) t_{CY} − 500	Min	ns
t_{WD}	(1/30) t_{CY} + 40	Min	ns
t_{DR}	(1/10) t_{CY} − 50	Max	ns
t_{RD}	(3/10) t_{CY} − 250	Max	ns
t_{AW}	(2/5) t_{CY} − 770	Min	ns
t_{AD}	(3/5) t_{CY} − 550	Max	ns
t_{AFC}	(1/15) t_{CY} − 165	Min	ns

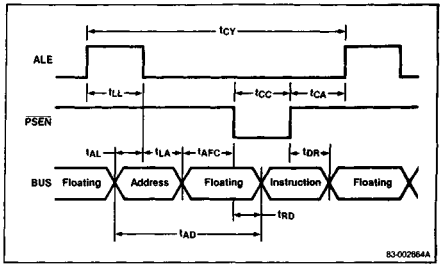
Symbol	Timing Formula	Min/Max	Unit
t_{CP}	(1/10) t_{CY} − 140	Min	ns
t_{PC2}	(4/15) t_{CY} − 200	Min	ns
t_{PR}	(3/5) t_{CY} − 690	Max	ns
t_{PF}	(1/10) t_{CY} − 100	Max	ns
t_{DP}	(2/5) t_{CY} − 750	Min	ns
t_{PD}	(1/10) t_{CY} − 180	Min	ns
t_{PP}	(7/10) t_{CY} − 550	Min	ns
t_{PL}	(7/30) t_{CY} − 230	Min	ns
t_{LP}	(1/6) t_{CY} − 265	Min	ns

Note:

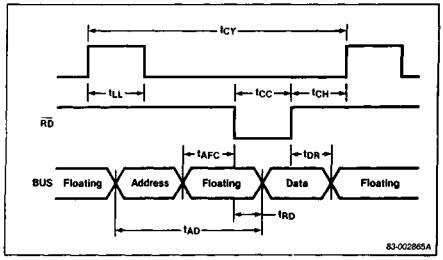
(1) Unlisted parameters are not affected by cycle time.

Timing Waveforms

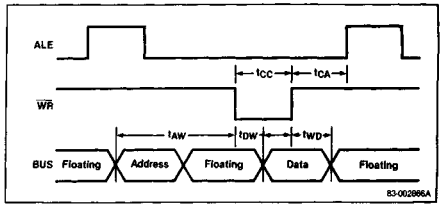
Instruction Fetch From External Memory



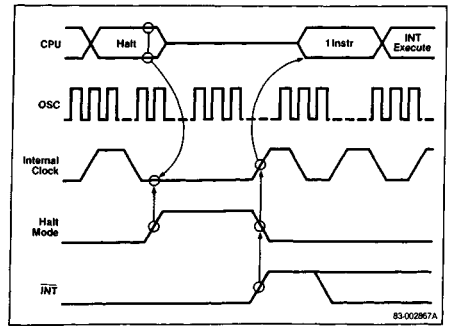
Read From External Data Memory



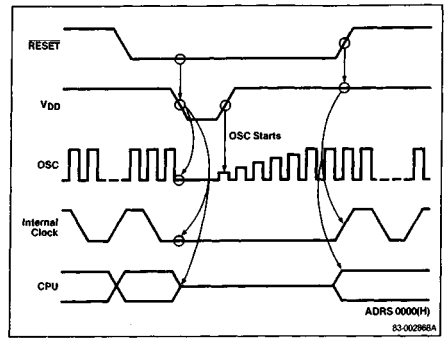
Write to External Memory



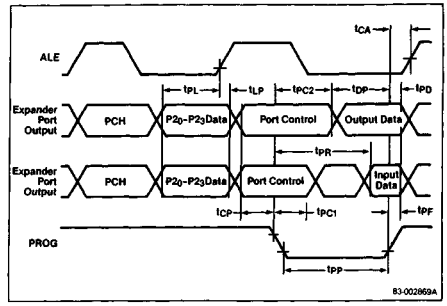
Low Power Standby Operation
1) Halt Mode (When EI)



2) Stop Mode



Port 2 Timing



Functional Description

Standby Function

Halt Mode

In Halt mode, the oscillator continues to operate, but the internal clock is disabled. The status of all internal logic just prior to execution of the HALT instruction is maintained by the CPU. In Halt mode, power consumption is less than 10 percent of normal μPD80C48 operation and less than 1 percent of normal 8048 operation.

The Halt mode is initiated by execution of the HALT instruction, and is released by either $\overline{INT}$ or $\overline{RESET}$ input.

INT Input. When the $\overline{INT}$ pin receives a low-level input, if interrupts are enabled, the internal clock is restarted and the interrupt is executed after the first or second instruction following the HALT instruction. However, if interrupts are disabled, program operation is resumed from the next address following the HALT instruction. The first instruction following a HALT instruction should be a NOP instruction to ensure proper program execution.

If the Halt mode is released when interrupts are enabled, the interrupt service routine is usually executed after the first or second instruction following the release of Halt mode. However, if either a timer or external interrupt is accepted within one machine cycle prior to a HALT instruction, the corresponding timer or external interrupt service routine is executed immediately following the release of Halt mode. It is important to note this sequence of execution when considering interrupt service routine execution following a HALT instruction.

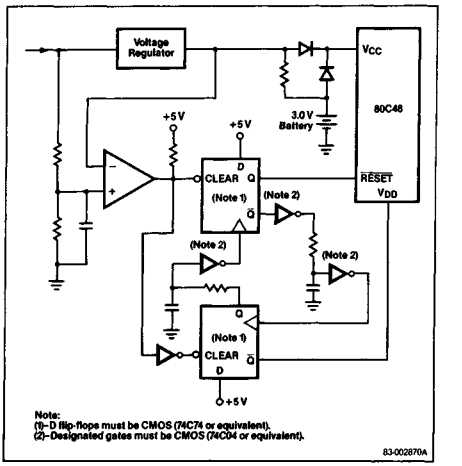
$\overline{RESET}$ Input. When a low-level input is received by the $\overline{RESET}$ pin, Halt mode is released and the normal reset operation is activated, restarting program operation from address 0.

Stop Mode

In Stop mode, the oscillator is deactivated and only the contents of RAM are maintained. The operation status of the μPD80C35/μPD80C48 resembles that of a reset condition. Because only the contents of RAM are maintained, Stop mode provides even lower power consumption than Halt mode, only requiring a minimum V_{CC} as low as +2 V.

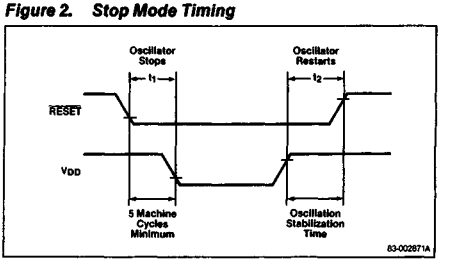
Stop mode is initiated by setting V_{DD} to low when $\overline{RESET}$ is low, to protect the contents of RAM. Stop mode is released by first raising the supply voltage at the V_{CC} pin from standby level to correct operating level and setting V_{DD} to high when $\overline{RESET}$ is low. After the oscillator has been restarted and the oscillation has stabilized, $\overline{RESET}$ must be set to high, whereby program operation is started from address 0. Figure 1 shows the Stop mode circuit.

Figure 1. Stop Mode Circuit



Stop Mode Circuit. Since V_{DD} controls the restarting of the oscillator, it is important that V_{DD} be protected from noise interference. The time required to reset the CPU is represented by t_1 (see figure 2), which is a minimum of 5 machine cycles. The reset operation will not be completed in less than 5 machine cycles. In Stop mode, it is important to note that if V_{DD} goes low before 5 machine cycles have elapsed, the CPU will be deactivated and the output of ALE, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, and PROG will not have been stabilized.

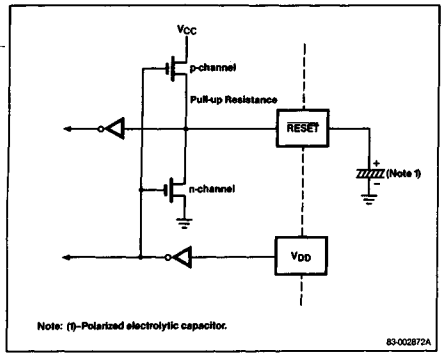
Figure 2. Stop Mode Timing



Oscillation stabilization time is represented by t_2 (see figure 2). When V_{DD} goes high, oscillator operation is reactivated, but it takes time before oscillation can be stabilized. In particular, such high Q resonators as crystals require longer periods to stabilize. Because there is a delay between restarting of the oscillator and oscillator stabilization, t_2 should be long enough to ensure that the oscillator has been fully stabilized.

To facilitate Stop mode control, an external capacitor can be connected to the $\overline{RESET}$ pin (see figure 3), affecting only t_2, allowing control of the oscillator stabilization time. When V_{DD} is asserted in Stop mode, the capacitor begins charging, pulling up $\overline{RESET}$. When $\overline{RESET}$ reaches a threshold level equivalent to a logic 1, Stop mode is released. The time it takes $\overline{RESET}$ to reach the threshold level of logic 1 determines the oscillator stabilization time, which is a function of the capacitance and pull-up resistance values.

Figure 3. Stop Mode Control Circuit

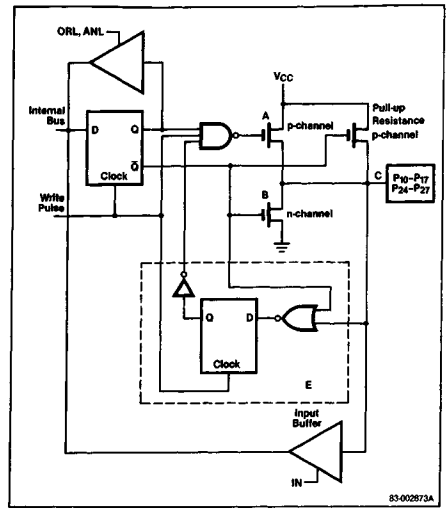


Port Operation

A port-loading option is offered at the time of ordering the mask. Individual source current requirements for Port 1 and the upper and lower halves of Port 2 may be factory set at either $-5\,\mu A$ or $-50\,\mu A$ (see Port-Loading Options table). The $-50\,\mu A$ option is required for interfacing with TTL/NMOS devices. The $-5\,\mu A$ option is recommended for interfacing to other CMOS devices. The CMOS option results in lower power consumption and greater noise immunity.

Port lines $P1_0$–$P1_7$ and $P2_4$–$P2_7$ include a protective circuit "E" to prevent a signal conflict at the port. The circuit prevents a logic 1 from being written to a line that is being pulled down externally (see figure 4, Port Protection Circuit E diagram). When a logic 0 is detected at the port line and a logic 1 is written from the bus, the NOR gate sends a logic 1 to the D input of the flip-flop. The output is inverted, forcing the NAND gate to send a high-level output. This turns off transistor A, preventing the output of a logic 1 from the port.

Figure 4. Port Protection Circuit E



Port-Loading Options

I_{OH} (min) $V_{CC} = V_{DD} = 5\,V \pm 10\%$; $V_{OH} = 2.4\,V$ (min)

Option Selected	$P1_0$-$P1_7$	$P2_0$-$P2_3$	$P2_4$-$P2_7$	Unit
A	−5	−5	−5	μA
B	−50	−5	−5	μA
C	−5	−50	−5	μA
D	−50	−50	−5	μA
E	−5	−5	−50	μA
F	−50	−5	−50	μA
G	−5	−50	−50	μA
H	−50	−50	−50	μA

Note:

(1) The selection of $I_{OH} = -5\,\mu A$ will result in a port source current of $I_{ILP} = -40\,\mu A$ max when used as input port.

(2) The selection of $I_{OH} = -50\,\mu A$ will result in a port source current of $I_{ILP} = -500\,\mu A$ max when used as input port.

Oscillator Operation

The oscillator maintains an internal frequency for clock generation and controls all system timing cycles. The oscillation is initiated by either a self-generating external resonator or external clock input. The oscillator acts as a high-gain amplifier which produces square-wave pulses at the frequency determined by the resonator or clock source to which it is connected.

To obtain the oscillation frequency, an external LC network (figure 5) may be connected to the oscillator, or, a ceramic or crystal external resonator (figure 6) may be connected.

Figure 5. LC Frequency Reference Circuit

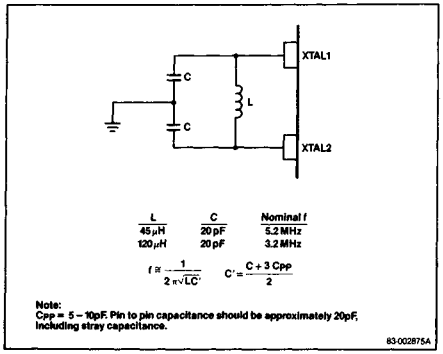
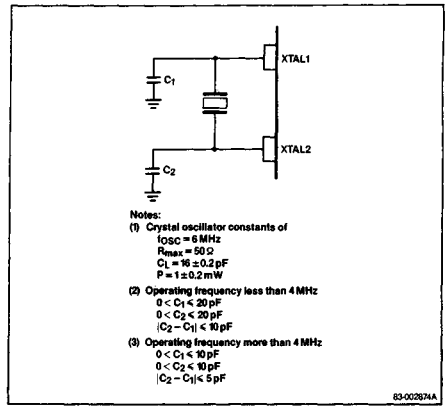


Figure 6. Crystal Frequency Reference Circuit



As the crystal frequency is lowered, there is an equivalent reduction in series resistance (R). As the temperature of the crystal is lowered, R is increased. Due to this relationship, it becomes difficult to stabilize oscillation when there is low power supply voltage. When V_{CC} is less than 2.7 V and the oscillator frequency is 3 MHz or less, T_A (ambient temperature) should not be less than −10°C.

Figures 7 and 8 show the ceramic resonator and external clock frequency reference circuits. Figure 9 shows the μPD80C35/μPD80C48 major I/O signals.

Figure 7. Ceramic Resonator Frequency Reference Circuit

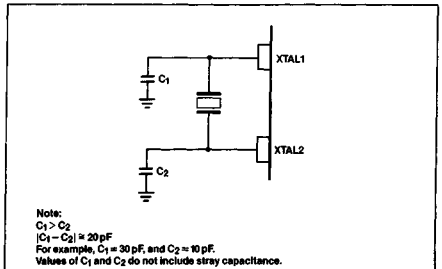


Figure 8. External Clock Frequency Reference Circuit

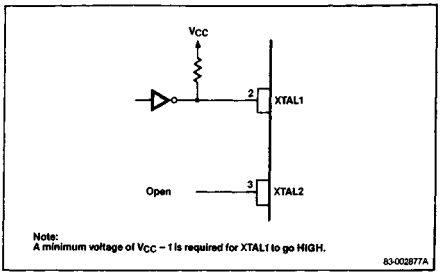
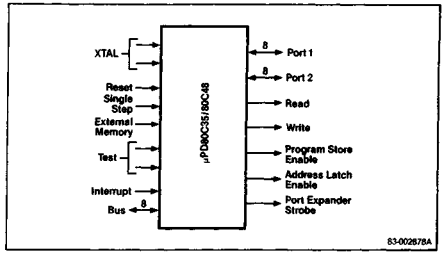


Figure 9. Major Input and Output Signals



Instruction Set

Instruction Set Symbol Definitions

Symbol	Description
A	Accumulator
AC	Auxiliary carry flag
addr	Program or data memory address (a_0–a_7) or (a_0–a_{10})
b	Accumulator bit (b = 0–7)
BS	Bank switch
BUS	Bus
C	Carry flag
CLK	Clock
CNT	Counter
data	8-bit binary data (d_0–d_7)
DBF	Memory bank flip-flop
F0, F1	Flag 0, flag 1
INT	Interrupt pin
n	Indicates the hex number of the specified register or port
PC	Program counter
Pp	Port 1, port 2, or ports 4–7 (p = 1, 2 or 4–7)
PSW	Program status word
Rr	Register (r = 0–7)

Symbol	Description
SP	Stack pointer
T	Timer
TF	Timer flag
T0, T1	Test 0, test 1 pin
#	Prefix for immediate data
@	Prefix for indirect address
x	Indicates the hex number corresponding to the accumulator bit or page number specified in the *operand*
(x)	Contents of RAM
((x))	Contents of memory location addressed by (x)
←	Transfer direction, result
AND	Logical product (logical AND)
OR	Logical sum (logical OR)
EXOR	Exclusive-OR
———	Complement

Instruction Set (cont)

Mnemonic	Function	Description	Hex Code	Operation Code								Cycles	Bytes
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
Accumulator													
ADD A, # data	(A) ← (A) + data	Adds immediate data d_0–d_7 to the accumulator. Sets or clears both carry flags. (Note 2)	03	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ADD A, Rr	(A) ← (A) + (Rr) r = 0–7	Adds the contents of register Rr to the accumulator. Sets or clears both carry flags. (Note 2)	6n(4)	0	1	1	0	1	r	r	r	1	1
ADD A, @ Rr	(A) ← (A) + ((Rr)) r = 0–1	Adds the contents of the internal data memory location specified by bits 0–5 of register Rr to the accumulator. Sets or clears both carry flags. (Note 2)	6n(4)	0	1	1	0	0	0	0	r	1	1
ADDC A, # data	(A) ← (A) + (C) + data	Adds, with carry, immediate data d_0–d_7 to the accumulator. Sets or clears both carry flags. (Note 2)	13	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ADDC A, Rr	(A) ← (A) + (C) + (Rr) r = 0–7	Adds, with carry, the contents of register Rr to the accumulator. Sets or clears both carry flags. (Note 2)	7n(4)	0	1	1	1	1	r	r	r	1	1
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) r = 0–1	Adds, with carry, the contents of the internal data memory location specified by bits 0–5 of register Rr, to the accumulator. Sets or clears both carry flags. (Note 2)	7n(4)	0	1	1	1	0	0	0	r	1	1
ANL A, # data	(A) ← (A) AND data	Takes the logical product (logical AND) of immediate data d_0–d_7 and the contents of the accumulator, and stores the result in the accumulator.	53	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ANL A, Rr	(A) ← (A) AND (Rr) r = 0–7	Takes the logical product (logical AND) of the contents of register Rr and the accumulator, and stores the result in the accumulator.	5n(4)	0	1	0	1	1	r	r	r	1	1
ANL A, @ Rr	(A) ← (A) AND ((Rr)) r = 0–1	Takes the logical product (logical AND) of the contents of the internal data memory location specified by bits 0–5 of register Rr, and the accumulator, and stores the result in the accumulator.	5n(4)	0	1	0	1	0	0	0	r	1	1
CPL A	(A) ← ($\overline{A}$)	Takes the complement of the contents of the accumulator.	37	0	0	1	1	0	1	1	1	1	1
CLR A	(A) ← 0	Clears the contents of the accumulator.	27	0	0	1	0	0	1	1	1	1	1
DA A		Converts the contents of the accumulator to BCD. Sets or clears the carry flags. When the lower 4 bits (A_0–A_3) are greater than 9, or if the auxiliary carry flag has been set, adds 6 to (A_0–A_3). When the upper 4 bits (A_4–A_7) are greater than 9 or if the carry flag (C) has been set, adds 6 to (A_4–A_7). If an overflow occurs at this point, C is set. (Note 2)	57	0	1	0	1	0	1	1	1	1	1
DEC A	(A) ← (A) – 1	Decrements the contents of the accumulator by 1.	07	0	0	0	0	0	1	1	1	1	1
INC A	(A) ← (A) + 1	Increments the contents of the accumulator by 1.	17	0	0	0	1	0	1	1	1	1	1
ORL A, # data	(A) ← (A) OR data	Takes the logical sum (logical OR) of immediate data d_0–d_7 and the contents of the accumulator, and stores the result in the accumulator.	43	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ORL A, Rr	(A) ← (A) OR (Rr) r = 0–7	Takes the logical sum (logical OR) of register Rr and the contents of the accumulator, and stores the result in the accumulator.	4n(4)	0	1	0	0	1	r	r	r	1	1

Instruction Set (cont)

Mnemonic	Function	Description	Hex Code	Operation Code								Cycles	Bytes
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
Accumulator (cont)													
ORL A, @ Rr	(A) ← (A) OR ((Rr)) r = 0–1	Takes the logical sum (logical OR) of the contents of the internal data memory location specified by bits 0–5 in register Rr, and the contents of the accumulator, and stores the result in the accumulator.	4n(4)	0	1	0	0	0	0	0	r	1	1
RL A	(AN + 1) ← (AN) (A_0) ← (A_7) N = 0–6	Rotates the contents of the accumulator one bit to the left. The MSB is rotated into the LSB.	E7	1	1	1	0	0	1	1	1	1	1
RLC A	(AN + 1) ← (AN); N = 0–6 (A_0) ← (C) (C) ← (A_7)	Rotates the contents of the accumulator one bit to the left through carry.	F7	1	1	1	1	0	1	1	1	1	1
RR A	(AN) ← (AN + 1); N = 0–6 (A_7) ← (A_0)	Rotates the contents of the accumulator one bit to the right. The LSB is rotated into the MSB.	77	0	1	1	1	0	1	1	1	1	1
RRC A	(AN) ← (AN + 1); N = 0–6 (A_7) ← (C) (C) ← (A_0)	Rotates the contents of the accumulator one bit to the right through carry.	67	0	1	1	0	0	1	1	1	1	1
SWAP A	(A_4–A_7) ⟷ (A_0–A_3)	Exchanges the contents of the lower 4 bits of the accumulator with the upper 4 bits of the accumulator.	47	0	1	0	0	0	1	1	1	1	1
XRL A, # data	(A) ← (A) XOR data	Takes the exclusive OR of immediate data d_0–d_7 and the contents of the accumulator, and stores the result in the accumulator.	D3	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
XRL A, Rr	(A) ← (A) XOR (Rr) r = 0–7	Takes the exclusive OR of the contents of register Rr and the accumulator, and stores the result in the accumulator.	Dn(4)	1	1	0	1	1	r	r	r	1	1
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) r = 0–1	Takes the exclusive OR of the contents of the location in data memory specified by bits 0–5 in register Rr, and the accumulator, and stores the result in the accumulator.	Dn(4)	1	1	0	1	0	0	0	r	1	1
Branch													
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0–7 If (Rr) ≠ 0; (PC_0–PC_7) ← addr	Decrements the contents of register Rr by 1, and if the result is not equal to 0, jumps to the address indicated by a_0–a_7.	En	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2
JBb addr	(PC_0–PC_7) ← addr if b = 1 (PC) = (PC) + 2 if b = 0	Jumps to the address specified by a_0–a_7 if the bit in the accumulator specified by b_0–b_2 is set.	x2(6)	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2

Instruction Set (cont)

Mnemonic	Function	Description	Hex Code	Operation Code								Cycles	Bytes
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
Branch (cont)													
JC addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if C = 1 $(PC) \leftarrow (PC) + 2$ if C = 0	Jumps to the address specified by $a_0\text{-}a_7$ if the carry flag is set.	F6	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JF0 addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if F0 = 1 $(PC) \leftarrow (PC) + 2$ if F0 = 0	Jumps to the address specified by $a_0\text{-}a_7$ if F0 is set.	B6	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JF1 addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if F1 = 1 $(PC) \leftarrow (PC) + 2$ if F1 = 0	Jumps to the address specified by $a_0\text{-}a_7$ if F1 is set.	76	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JMP addr	$(PC_8\text{-}PC_{10}) \leftarrow (addr_8\text{-}addr_{10})$ $(PC_0\text{-}PC_7) \leftarrow (addr_0\text{-}addr_7)$ $(PC_{11}) \leftarrow$ DBF	Jumps directly to the address specified by $a_0\text{-}a_{10}$ and the DBF.	x4(6)	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2
JMPP @ A	$(PC_0\text{-}PC_7) \leftarrow ((A))$	Replaces the lower 8 bits of the program counter with the contents of program memory specified by the contents of the accumulator, producing a jump to the specified address within the current page.	B3	1	0	1	1	0	0	1	1	2	1
JNC addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if C = 0 $(PC) \leftarrow (PC) + 2$ if C = 1	Jumps to the address specified by $a_0\text{-}a_7$ if the carry flag is not set.	E6	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNI addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if I = 0 $(PC) \leftarrow (PC) + 2$ if I = 1	Jumps to the address specified by $a_0\text{-}a_7$ if the interrupt flag is not set.	86	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNT0 addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if T0 = 0 $(PC) \leftarrow (PC) + 2$ if T0 = 1	Jumps to the address specified by $a_0\text{-}a_7$ if test 0 is low.	26	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNT1 addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if T1 = 0 $(PC) \leftarrow (PC) + 2$ if T1 = 1	Jumps to the address specified by $a_0\text{-}a_7$ if test 1 is low.	46	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNZ addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if A ≠ 0 $(PC) \leftarrow (PC) + 2$ if A = 0	Jumps to the address specified by $a_0\text{-}a_7$ if the contents of the accumulator are not equal to 0.	96	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JTF addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if TF = 1 $(PC) \leftarrow (PC) + 2$ if TF = 0	Jumps to the address specified by $a_0\text{-}a_7$ if the timer flag is set. The timer flag is cleared after the instruction is executed.	16	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JT0 addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if T0 = 1 $(PC) \leftarrow (PC) + 2$ if T0 = 0	Jumps to the address specified by $a_0\text{-}a_7$ if test 0 is high.	36	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JT1 addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if T1 = 1 $(PC) \leftarrow (PC) + 2$ if T1 = 0	Jumps to the address specified by $a_0\text{-}a_7$ if test 1 is high.	56	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JZ	$(PC_0\text{-}PC_7) \leftarrow$ addr if A = 0 $(PC) \leftarrow (PC) + 2$ if A = 1	Jump to the address specified by $a_0\text{-}a_7$ if the contents of the accumulator are equal to 0.	C6	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2

Instruction Set (cont)

Mnemonic	Function	Description	Hex Code	Operation Code								Cycles	Bytes
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
Control													
EN I		Enables external interrupts. When external interrupts are enabled, a low-level input to the INT pin causes the processor to vector to the interrupt service routine.	05	0	0	0	0	0	1	0	1	1	1
DIS I		Disables external interrupts. When external interrupts are disabled, low-level inputs to the INT pin have no effect on program execution.	15	0	0	0	1	0	1	0	1	1	1
ENTO CLK		Enables clock output to pin T0.	75	0	1	1	1	0	1	0	1	1	1
SEL MB0	(DBF) ← 0	Clears the memory bank flip-flop, selecting program memory bank 0 (program memory addresses $0–2047_{(10)}$). Clears PC_{11} after the next JMP or CALL instruction.	E5	1	1	1	0	0	1	0	1	1	1
SEL MB1	(DBF) ← 1	Sets the memory bank flip-flop, selecting program memory bank 1 (program memory addresses $2048–4095_{(10)}$). Sets PC_{11} after the next JMP or CALL instruction.	F5	1	1	1	1	0	1	0	1	1	1
SEL RB0	(BS) ← 0	Selects data memory bank 0 by clearing bit 4 (bank switch) of the PSW. Specifies data memory addresses $0–7_{(10)}$ as registers 0–7 of data memory bank 0.	C5	1	1	0	0	0	1	0	1	1	1
SEL RB1	(BS) ← 1	Selects data memory bank 1 by setting bit 4 (bank switch) of the PSW. Specifies data memory $24–31_{(10)}$ as registers 0–7 of data memory bank 1.	D5	1	1	0	1	0	1	0	1	1	1
HALT		Initiates halt mode.	01	0	0	0	0	0	0	0	1	1	1
Data Moves													
MOV A, # data	(A) ← data	Moves immediate data $d_0–d_7$ into the accumulator.	23	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
MOV A, Rr	(A) ← (Rr); r = 0–7	Moves the contents of register Rr into the accumulator.	Fn(4)	1	1	1	1	1	r	r	r	1	1
MOV A, @ Rr	(A) ← ((Rr)); r = 0–1	Moves the contents of internal data memory specified by bits 0–5 in register Rr, into the accumulator.	Fn(4)	1	1	1	1	0	0	0	r	1	1
MOV A, PSW	(A) ← (PSW)	Moves the contents of the program status word into the accumulator.	C7	1	1	0	0	0	1	1	1	1	1
MOV Rr, # data	(Rr) ← data; r = 0–7	Moves immediate data $d_0–d_7$ into register Rr.	Bn(4)	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2
MOV Rr, A	(Rr) ← (A); r = 0–7	Moves the contents of the accumulator into register Rr.	An(4)	1	0	1	0	1	r	r	r	1	1
MOV @ Rr, A	((Rr)) ← (A); r = 0–1	Moves the contents of the accumulator into the data memory location specified by bits 0–5 in register Rr.	An(4)	1	0	1	0	0	0	0	r	1	1
MOV @ Rr, # data	((Rr)) ← data; r = 0–1	Moves immediate data $d_0–d_7$ into the data memory location specified by bits 0–5 in register Rr.	Bn(4)	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2

Instruction Set (cont)

Mnemonic	Function	Description	Hex Code	Operation Code								Cycles	Bytes
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
Data Moves (cont)													
MOV PSW, A	(PSW) ← (A)	Moves the contents of the accumulator into the program status word.	D7	1	1	0	1	0	1	1	1	1	1
MOVP A, @ A	(PC_0–PC_7) ← (A) (A) ← ((PC))	Moves the contents of the program memory location specified by PC_8–PC_{11} concatenated with the contents of the accumulator, into the accumulator.	A3	1	0	1	0	0	0	1	1	2	1
MOVP3 A, @ A	(PC_0–PC_7) ← (A) (PC_8–PC_{11}) ← 001 (A) ← ((PC))	Moves the contents of the program memory location specified by 0011 (PC_8–PC_{11}, page 3 of program memory bank 0) and the contents of the accumulator, into the accumulator.	E3	1	1	1	0	0	0	1	1	2	1
MOVX A, @ R	(A) ← ((Rr)); r = 0–1	Moves the contents of the external data memory location specified by register Rr, into the accumulator.	8n(4)	1	0	0	0	0	0	0	r	2	1
MOVX @ R, A	((Rr)) ← (A); r = 0–1	Moves the contents of the accumulator into the external data memory location specified by register Rr.	9n(4)	1	0	0	1	0	0	0	r	2	1
XCH A, Rr	(A) ⟷ (Rr); r = 0–7	Exchanges the contents of the accumulator and register Rr.	2n(4)	0	0	1	0	1	r	r	r	1	1
XCH A, @ Rr	(A) ⟷ ((Rr)); r = 0–1	Exchanges the contents of the accumulator and the contents of the data memory location specified by bits 0–5 in register Rr.	2n(4)	0	0	1	0	0	0	0	r	1	1
XCHD A, @ Rr	(A_0–A_3) ⟷ $((Rr))_0$–$((Rr))_3$; r = 0–1	Exchanges the contents of the lower 4 bits of the accumulator with the contents of the lower 4 bits of the internal data memory location specified by bits 0–5 in register Rr.	3n(4)	0	0	1	1	0	0	0	r	1	1
Flags													
CPL C	(C) ← ($\overline{C}$)	Takes the complement of the carry bit.	A7	1	0	1	0	0	1	1	1	1	1
CPL F0	(F0) ← ($\overline{F0}$)	Takes the complement of flag 0.	95	1	0	0	1	0	1	0	1	1	1
CPL F1	(F1) ← ($\overline{F1}$)	Takes the complement of flag 1.	B5	1	0	1	1	0	1	0	1	1	1
CLR C	(C) ← 0	Clears the carry bit.	97	1	0	0	1	0	1	1	1	1	1
CLR F0	(F0) ← 0	Clears flag 0.	85	1	0	0	0	0	1	0	1	1	1
CLR F1	(F1) ← 0	Clears flag 1.	A5	1	0	1	0	0	1	0	1	1	1

NEC

Instruction Set (cont)

Mnemonic	Function	Description	Hex Code	Operation Code								Cycles	Bytes
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
Input / Output													
ANL BUS, # data	(bus) ← (bus) AND data	Takes the logical AND of the contents of the bus and immediate data d_0–d_7, and sends the result to the bus.	98	1	0	0	1	1	0	0	0	2	2
				d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0		
ANL Pp, # data	(Pp) ← (Pp) AND data; p = 1–2	Takes the logical AND of the contents of designated port Pp and immediate data d_0–d_7, and sends the result to port Pp for output.	9n(5)	1	0	0	1	1	0	p	p	2	2
				d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0		
ANLD Pp, A	(Pp) ← (Pp) AND (A_0–A_3); p = 4–7	Takes the logical AND of the contents of designated port Pp and the lower 4 bits of the accumulator, and sends the result to port Pp for output.	9n(5)	1	0	0	1	1	1	p	p	2	1
IN A, Pp	(A) ← (Pp); p = 1–2	Loads the accumulator with the contents of designated port Pp.	0n(5)	0	0	0	0	1	0	p	p	2	1
INS A, BUS	(A) ← (bus)	Loads the contents of the bus into the accumulator on the rising edge of $\overline{RD}$.	08	0	0	0	0	1	0	0	0	2	1
MOVD A, Pp	(A_0–A_3) ← (Pp); p = 4–7 (A_4–A_7) ← 0	Moves the contents of designated port Pp to the lower 4 bits of the accumulator, and clears the upper 4 bits.	0n(5)	0	0	0	0	1	1	p	p	2	1
MOVD Pp, A	(Pp) ← (A_0–A_3); p = 4–7	Moves the lower 4 bits of the accumulator to designated port Pp. The upper 4 bits of the accumulator are not changed.	3n(5)	0	0	1	1	1	1	p	p	2	1
ORL BUS, # data	(bus) ← (bus) OR data	Takes the logical OR of the contents of the bus and immediate data d_0–d_7, and sends the result to the bus.	88	1	0	0	0	1	0	0	0	2	2
				d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0		
ORLD Pp, A	(Pp) ← (Pp) OR (A_0–A_3); p = 4–7	Takes the logical OR of the contents of designated port Pp and the lower 4 bits of the accumulator, and sends the result to port Pp for output.	8n(5)	1	0	0	0	1	1	p	p	2	1
ORL Pp, # data	(Pp) ← (Pp) OR data; p = 1–2	Takes the logical OR of the contents of designated port Pp and immediate data d_0–d_7, and sends the result to port Pp for output.	9n(5)	1	0	0	0	1	0	p	p	2	2
				d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0		
OUTL BUS, A	(bus) ← (A)	Latches the contents of the accumulator onto the bus on the rising edge of $\overline{WR}$. Note: Never use the OUTL BUS instruction when using external program memory, as this will permanently latch the bus.	02	0	0	0	0	0	0	1	0	2	1
OUTL Pp,A	(Pp) ← (A); p = 1–2	Latches the contents of the accumulator into designated port Pp for output.	3n(5)	0	0	1	1	1	0	p	p	2	1
Registers													
DEC Rr	(Rr) ← (Rr) – 1; r = 0–7	Decrements the contents of register Rr by 1.	Cn(4)	1	1	0	0	1	r	r	r	1	1
INC Rr	(Rr) ← (Rr) + 1; r = 0–7	Increments the contents of register Rr by 1.	1n(4)	0	0	0	1	1	r	r	r	1	1
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0–1	Increments by 1 the contents of the data memory location specified by bits 0–5 in register Rr.	1n(4)	0	0	0	1	0	0	0	r	1	1

Instruction Set (cont)

Mnemonic	Function	Description	Hex Code	Operation Code								Cycles	Bytes
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
Subroutine													
CALL addr	$((SP)) \leftarrow (PC), (PSW_4\text{-}PSW_7)$ $(SP) \leftarrow (SP) + 1$ $(PC_8\text{-}PC_{10}) \leftarrow (addr_8\text{-}addr_{10})$ $(PC_0\text{-}PC_7) \leftarrow (addr_0\text{-}addr_7)$ $(PC_{11}) \leftarrow DBF$	Stores the contents of the program counter and the upper 4 bits of the PSW in the address indicated by the stack pointer, and increments the contents of the stack pointer, calling the subroutine specified by address a_0-a_{10} and the DBF.	x4(6)	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2
RET	$(SP) \leftarrow (SP) - 1$ $(PC) \leftarrow ((SP))$	Decrements the contents of the stack pointer by 1 and stores, in the program counter, the contents of the location specified by the stack pointer, executing a return from subroutine without restoring the PSW.	83	1	0	0	0	0	0	1	1	2	1
RETR	$(SP) \leftarrow (SP) - 1$ $(PC) \leftarrow ((SP))$ $(PSW_4\text{-}PSW_7) \leftarrow ((SP))$	Decrements the contents of the stack pointer by 1 and stores, in the program counter, the contents of the upper 4 bits of the PSW and the contents of the location specified by the stack pointer, executing a return from subroutine with restoration of the PSW.	93	1	0	0	1	0	0	1	1	2	1
Timer / Counter													
EN TCNTI		Enables internal interrupt of timer / event counter. If an overflow condition occurs, then an interrupt will be generated.	25	0	0	1	0	0	1	0	1	1	1
DIS TCNTI		Disables internal interrupt of timer / event counter.	35	0	0	1	1	0	1	0	1	1	1
MOV A, T	$(A) \leftarrow (T)$	Moves the contents of the timer / counter into the accumulator.	42	0	1	0	0	0	0	1	0	1	1
MOV T, A	$(T) \leftarrow (A)$	Moves the contents of the accumulator into the timer / counter.	62	0	1	1	0	0	0	1	0	1	1
STOP TCNT		Stops the operation of the timer / event counter.	65	0	1	1	0	0	1	0	1	1	1
STRT CNT		Starts the event counter operation of the timer / counter when T1 changes from a low-level input to a high-level input.	45	0	1	0	0	0	1	0	1	1	1
STRT T		Starts the timer operation of the timer / counter. The timer is incremented every 32 machine cycles.	55	0	1	0	1	0	1	0	1	1	1
Miscellaneous													
NOP		Uses one machine cycle without performing any operation.	00	0	0	0	0	0	0	0	0	1	1

Instruction Set (cont)

Note:

(1) Binary operation code designations r and p represent encoded values or the lowest-order bit value of specified registers and ports, respectively.

(2) Execution of the ADD, ADDC, and DA instructions affect the carry flags, which are not shown in the respective function equations. These instructions set the carry flags when there is an overflow in the accumulator (the auxiliary carry flag is set when there is an overflow of bit 3 of the accumulator) and clear the carry flags when there is no overflow. Flags that are specifically addressed by flag instructions are shown in the function equations for those instructions.

(3) References to addresses and data are specified in byte 1 and/or 2 in the opcode of the corresponding instruction.

(4) The hex value of n for specific registers is as follows:

a) Direct addressing

R0: n = 8 R2: n = A R4: n = C R6: n = E
R1: n = 9 R3: n = B R5: n = D R7: n = F

b) Indirect addressing

@ R0: n = 0 @ R1: n = 1

(5) The hex value of n for specific ports is as follows:

P1: n = 9 P4: n = C P6: n = E
P2: n = A P5: n = D P7: n = F

(6) The hex value of x for specific accumulator or address bits is as follows:

a) JBb instruction

B_0: x = 1 B_2: x = 5 B_4: x = 9 B_6: x = D
B_1: x = 3 B_3: x = 7 B_5: x = B B_7: x = F

b) JMP instruction

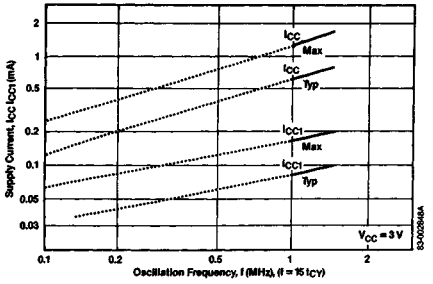
Page 0: x = 0 Page 2: x = 4 Page 4: x = 8 Page 6: x = C
Page 1: x = 2 Page 3: x = 6 Page 5: x = A Page 7: x = E

c) CALL instruction

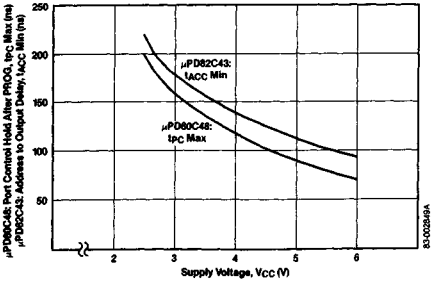
Page 0: x = 1 Page 2: x = 5 Page 4: x = 9 Page 6: x = D
Page 1: x = 3 Page 3: x = 7 Page 5: x = B Page 7: x = F

Operating Characteristics

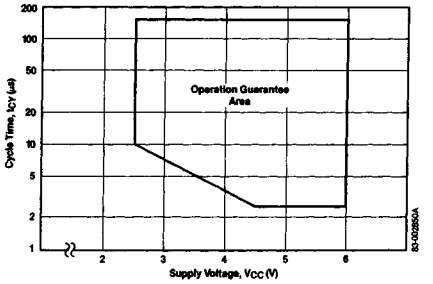
Supply Current vs. Oscillation Frequency



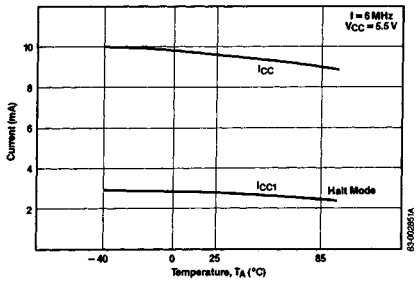
Port Control Hold After PROG, t_{PC} Max (μPD80C48), and Address to Output Delay, t_{ACC} Min (μPD82C43), vs. Supply Voltage



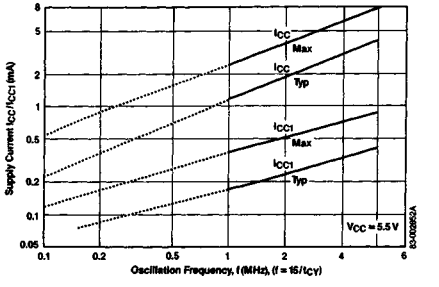
Cycle Time vs. Supply Voltage



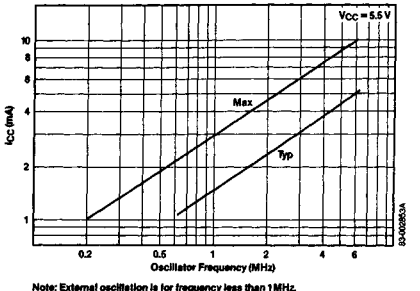
Current Consumption as a Function of Temperature — Normal Operating Mode



Supply Current vs. Oscillation Frequency



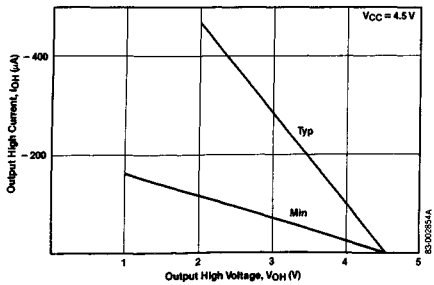
Current Consumption as a Function of Operating Frequency — Normal Operating Mode



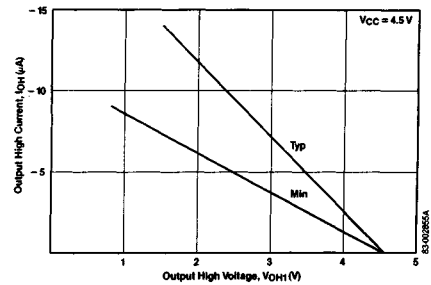
Note: External oscillation is for frequency less than 1 MHz. Internal oscillation requires more power.

Operating Characteristics (cont)

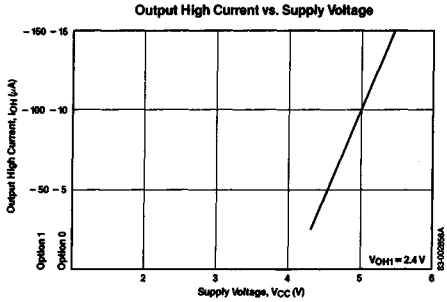
Output High Current vs. Output High Voltage



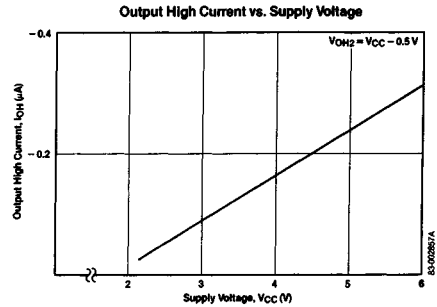
Output High Current vs. Output High Voltage



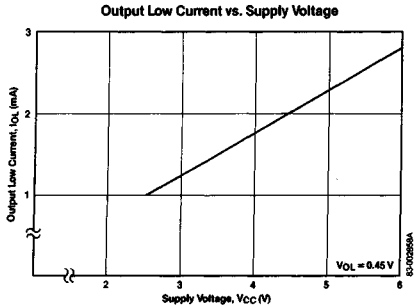
Output High Current vs. Supply Voltage



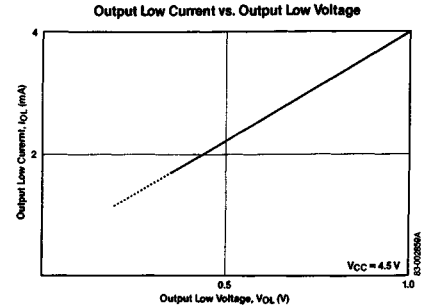
Output High Current vs. Supply Voltage



Output Low Current vs. Supply Voltage

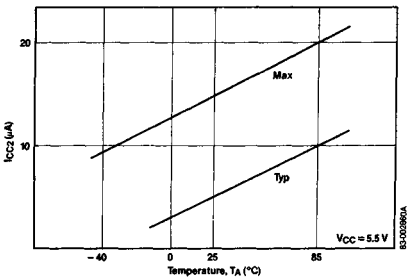


Output Low Current vs. Output Low Voltage



Operating Characteristics (cont)

Current Consumption as a Function of Temperature — Stop Mode



NEC
NEC Electronics Inc.

μPD765A/μPD7265
SINGLE/DOUBLE DENSITY FLOPPY DISK CONTROLLER

Revision 2 — November 1985

Description

The μPD765A is an LSI floppy disk controller (FDC) chip which contains the circuitry and control functions for interfacing a processor to 4 floppy disk drives. It is capable of either IBM 3740 single density format (FM), or IBM System 34 double density format (MFM) including double-sided recording. The μPD765A provides control signals which simplify the design of an external phase-locked loop and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a floppy disk interface.

The μPD7265 is an addition to the FDC family that has been designed specifically for the Sony Micro Floppydisk® drive. The μPD7265 is pin-compatible and electrically equivalent to the 765A but utilizes the Sony recording format. The μPD7265 can read a diskette that has been formatted by the μPD765A.

Each of these devices is also available in a -2 version. The -2 versions represent a reduction from 4-micron to 3-micron design rule. Functionality is the same. Minor differences between the two versions are detailed in the AC Characteristics table. The -2 versions are only available in the plastic package at this time.

Hand-shaking signals are provided in the μPD765A/μPD7265 which make DMA operation easy to incorporate with the aid of an external DMA controller chip, such as the μPD8257. The FDC will operate in either the DMA or non-DMA mode. In the non-DMA mode the FDC generates interrupts to the processor every time a data byte is to be transferred. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the FDC and DMA controllers.

There are 15 commands which the μPD765A/μPD7265 will execute. Each of these commands requires multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

Read Data	Read Deleted Data
Read ID	Write Data
Specify	Format Track
Read Track	Write Deleted Data
Scan Equal	Seek
Scan High or Equal	Recalibrate
Scan Low or Equal	Sense Interrupt Status
	Sense Drive Status.

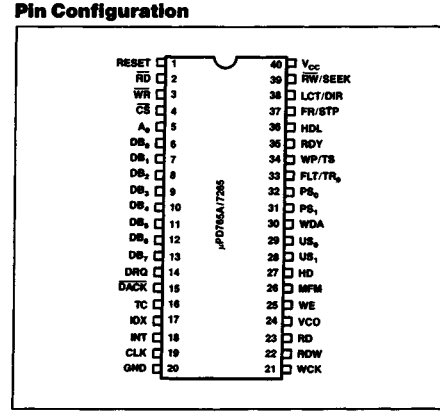
Features

Address mark detection circuitry is internal to the FDC which simplifies the phase-locked loop and read electronics. The track stepping rate, head load time, and head unload time are user-programmable. The μPD765A/μPD7265 offers additional features such as multi-track and multi-side read and write commands and single and double density capabilities.

- ☐ Sony (EMCA)-compatible recording format (μPD7265)
- ☐ IBM-compatible format (single and double density) (μPD765A)
- ☐ Multi-sector and multi-track transfer capability
- ☐ Drive Up to 4 floppy or micro floppydisk drives
- ☐ Data scan capability — will scan a single sector or an entire cylinder comparing byte-for-byte host memory and disk data
- ☐ Data transfers in DMA or non-DMA mode
- ☐ Parallel seek operations on up to four drives
- ☐ Compatible with μPD8080/85, μPD8086/88 and μPD780 (Z80®) microprocessors
- ☐ Single-phase clock (8 MHz)
- ☐ +5 V only

* Z80 is a registered trademark of the Zilog Corporation.

Pin Configuration



Ordering Information

Device Number	Package Type	Max Freq. of Operation
μPD765AC, μPD765A-2C	40-Pin plastic DIP	8 MHz
μPD7265C, μPD7265-2C	40-Pin plastic DIP	8 MHz
μPD765AD	40-Pin ceramic DIP	8 MHz
μPD7265D	40-Pin ceramic DIP	8 MHz

Pin Identification

No.	Symbol	Function
1	RESET	Reset input
2	$\overline{RD}$	Read control input
3	$\overline{WR}$	Write control input
4	$\overline{CS}$	Chip select input
5	A_0	Data or status select input
6–13	DB_0–DB_7	Bidirectional data bus
14	DRQ	DMA request output
15	$\overline{DACK}$	DMA acknowledge input
16	TC	Terminal count input
17	IDX	Index input
18	INT	Interrupt request output
19	CLK	Clock input
20	GND	Ground
21	WCK	Write clock input
22	RDW	Read data window input
23	RDD	Read data input
24	VCO	VCO sync output
25	WE	Write enable output
26	MFM	MFM output
27	HD	Head select output
28, 29	US_0, US_1	FDD unit select output
30	WDA	Write data output
31, 32	PS_0, PS_1	Preshift output
33	FLT / TR_0	Fault / track zero input
34	WP / TS	Write protect / two side input
35	RDY	Ready input
36	HDL	Head load output
37	FR / STP	Fault reset / step output
38	LCT / DIR	Low current direction output
39	RW / SEEK	Read / write / seek output
40	V_{CC}	DC power

Pin Functions

RESET (Reset)

The RESET input places the FDC in the idle state. It resets the output lines to the FDD to 0 (low). It does not affect SRT, HUT, or HLT in the Specify command. If the RDY input is held high during reset, the FDC will generate an interrupt within 1.024 ms. To clear this interrupt, use the Sense Interrupt Status command.

$\overline{RD}$ (Read Strobe)

The $\overline{RD}$ input allows the transfer of data from the FDC to the data bus when low. Disabled when $\overline{CS}$ is high.

$\overline{WR}$ (Write Strobe)

The $\overline{WR}$ input allows the transfer of data to the FDC from the data bus when low. Disabled when $\overline{CS}$ is high.

A_0 (Data / Status Select)

The A_0 input selects the data register ($A_0 = 1$) or status register ($A_0 = 0$) contents to be sent to the data bus.

$\overline{CS}$ (Chip Select)

The FDC is selected when $\overline{CS}$ is low, enabling $\overline{RD}$, $\overline{WR}$, and A_0.

DB_0–DB_7 (Data Bus)

DB_0–DB_7 are a bidirectional 8-bit data bus. Disabled when $\overline{CS}$ is high.

DRQ (DMA Request)

The FDC asserts the DRQ output high to request a DMA transfer.

$\overline{DACK}$ (DMA Acknowledge)

When the $\overline{DACK}$ input is low, a DMA cycle is active and the controller is performing a DMA transfer.

TC (Terminal Count)

When the TC input is high, it indicates the termination of a DMA transfer. It terminates data transfer during Read/Write/Scan commands in DMA or interrupt mode.

IDX (Index)

The IDX input goes high at the beginning of a disk track.

INT (Interrupt)

The INT output is FDC's interrupt request.

CLK (Clock)

CLK is the input for the FDC's single-phase, 8 MHz squarewave clock.

WCK (Write Clock)

The WCK input sets the data write rate to the FDD. It is 500 kHz for FM, 1 MHz for MFM drives, with a 250 ns pulse for both FM and MFM.

RDW (Read Data Window)

The RDW input is generated by the phase-locked loop (PLL). It is used to sample data from the FDD.

RDD (Read Data)

The RDD input is the read data from the FDD, containing clock and data bits.

WDA (Write Data)

WDA is the serial clock and data output to the FDD.

WE (Write Enable)

The WE output enables write data into the FDD.

VCO (VCO Sync)

The VCO output inhibits the VCO in the PLL when low, enables it when high.

MFM (MFM Mode)

The MFM output shows the FDD's mode. It is high for MFM, low for FM.

HD (Head Select)

Head 1 is selected when the HD output is 1 (high), head 0 is selected when HD is 0 (low).

US_0, US_1 (Unit Select 0, 1)

The US_0 and US_1 outputs select the floppy disk drive unit.

PS_0, PS_1 (Preshift 0, 1)

The PS_0 and PS_1 outputs are the write precompensation status for MFM mode. They determine early, late, and normal times.

RDY (Ready)

The RDY input indicates that the FDD is ready to receive data.

HDL (Head Load)

The HDL output is the command which causes the read/write head in the FDD to contact the diskette.

FLT/TR0 (Fault/Track 0)

In the read/write mode, the FLT input detects FDD fault conditions. In the seek mode, TR0 detects track 0.

WP/TS (Write Protect/Two Side)

In the read/write mode, the WP input senses write protected status. In the seek mode, TS senses two-sided media.

FR/STP (Fault Reset/Step)

In the read/write mode, the FR output resets the fault flip-flop in the FDD. In the seek mode, STP outputs step pulses to move the head to another cylinder. A fault reset pulse (FR) is issued at the beginning or each Read or Write command prior to the HDL signal.

LCT/DIR (Low Current/Direction)

In the read/write mode, the LCT output lowers the write current on the inner tracks. In the seek mode, the DIR output determines the direction the head will move in when it receives a step pulse.

$\overline{RW}$/SEEK (Read/Write/Seek)

The $\overline{RW}$/SEEK output specifies the read/write mode when low, and the seek mode when high.

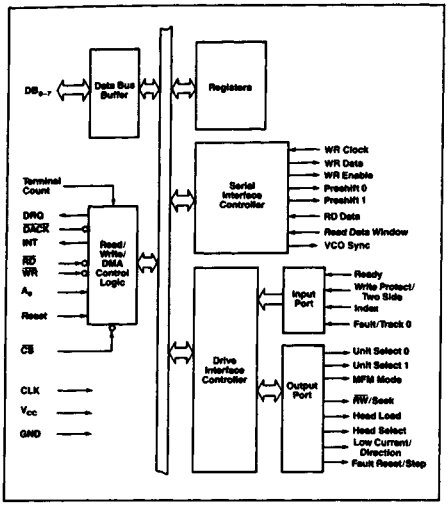
GND (Ground)

Ground.

V_{CC} (+5 V)

+5 V power supply.

Block Diagram



Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{CC}	−0.5 to +7 V
Input voltage, V_I	−0.5 to +7 V
Output voltage, V_O	−0.5 to +7 V
Operating temperature, T_{OPT}	−10°C to +70°C
Storage temperature, T_{STG}	−40°C to +125°C
Power dissipation, P_D	1 W

Comment: Exposing the device to stresses above those listed in the Absolute Maximum Ratings could cause permanent damage. The device should not be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = -10°C$ to $+70°C$, $V_{CC} = +5\,V \pm 5\%$ unless otherwise specified

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}	−0.5		+0.8	V	
Input voltage high	V_{IH}	2.0		$V_{CC}+0.5$	V	
Output voltage low	V_{OL}			0.45	V	$I_{OL} = 2.0$ mA
Output voltage high	V_{OH}	2.4		V_{CC}	V	$I_{OH} = -200\,\mu A$
Input voltage low (CLK + $\overline{WR}$ clock)	$V_{IL}(\Phi)$	−0.5		0.65	V	
Input voltage high (CLK + $\overline{WR}$ clock)	$V_{IH}(\Phi)$	2.4		$V_{CC}+0.5$	V	
Supply current (V_{CC})	I_{CC}			150	mA	
Input load current high	I_{LIH}			10	μA	$V_{IN} = V_{CC}$
Input load current low	I_{LIL}			−10	μA	$V_{IN} = 0$ V
Output leakage current high	I_{LOH}			10	μA	$V_{OUT} = V_{CC}$
Output leakage current low	I_{LOL}			−10	μA	$V_{OUT} = +0.45$ V

Capacitance

$T_A = 25°C$, $f_C = 1$ MHz, $V_{CC} = 0$ V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input clock capacitance	$C_{IN}(\Phi)$			20	pF	(Note 1)
Input capacitance	C_{IN}			10	pF	(Note 1)
Output capacitance	C_{OUT}			20	pF	(Note 1)

Note:
(1) All pins except pin under test tied to AC ground

AC Characteristics

$T_A = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$ unless otherwise specified

Parameter	Symbol	Limits						Unit	Test Conditions
		765A, 7265			765A-2, 7265-2				
		Min	Typ (1)	Max	Min	Typ (1)	Max		
Clock period	Φ_{CY}	120	125	500	120	125	500	ns	(Note 4)
			125			125		ns	8" FDD
			250			250		ns	5¼" FDD
			125			125		ns	3½" Sony (3)
Clock active (high)	Φ_0	40			40			ns	
Clock rise time	Φ_r			20			20	ns	
Clock fall time	Φ_f			20			20	ns	
A_0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{RD}\downarrow$	t_{AR}	0			0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ hold time from $\overline{RD}\uparrow$	t_{RA}	0			0			ns	
$\overline{RD}$ width	t_{RR}	250			200			ns	
Data access time from $\overline{RD}\downarrow$	t_{RD}			200			140	ns	$C_L = 100$ pF
DB to float delay time from $\overline{RD}\uparrow$	t_{DF}	20		100	10		85	ns	$C_L = 100$ pF
A_0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{WR}\downarrow$	t_{AW}	0			0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ hold time to $\overline{WR}\uparrow$	t_{WA}	0			0			ns	
$\overline{WR}$ width	t_{WW}	250			200			ns	
Data setup time to $\overline{WR}\uparrow$	t_{DW}	150			100			ns	
Data hold time from $\overline{WR}\uparrow$	t_{WD}	5			0			ns	
INT delay time from $\overline{RD}\uparrow$	t_{RI}			500			400	ns	
INT delay time from $\overline{WR}\uparrow$	t_{WI}			500			400	ns	
DRQ cycle time	t_{MCY}	13			13			μs	$\Phi_{CY} = 125$ ns (4)
$\overline{DACK}\downarrow \rightarrow$ DRQ↓ delay	t_{AM}			200			140	ns	
DRQ↑ $\rightarrow \overline{DACK}\downarrow$ delay	t_{MA}	200			200			ns	$\Phi_{CY} = 125$ ns (4)
$\overline{DACK}$ width	t_{AA}	2			2			Φ_{CY}	
TC width	t_{TC}	1			1			Φ_{CY}	
Reset width	t_{RST}	14			14			Φ_{CY}	
WCK cycle time	t_{CY}		4			16		Φ_{CY}	MFM = 0, 5¼"
			2			8		Φ_{CY}	MFM = 1, 5¼"
			2			8		Φ_{CY}	MFM = 0, 8"
			1			4		Φ_{CY}	MFM = 1, 8"
			2			8		Φ_{CY}	MFM = 0, 3½" (3)
			1			4		Φ_{CY}	MFM = 1, 3½"(3)
WCK active time (high)	t_0		2			2		Φ_{CY}	
CLK↑ $\rightarrow$ WCK↑ delay	t_{CWH}	0		40	0		40	ns	
CLK↑ $\rightarrow$ WCK↓ delay	t_{CWL}	0		40	0		40	ns	
WCK rise time	t_r			20			20	ns	
WCK fall time	t_f			20			20	ns	
Preshift delay time from WCK↑	t_{CP}	20		100	20		100	ns	
WCK↑ $\rightarrow$ WE↑ delay	t_{CWE}	20		100	20		100	ns	
WDA delay time from WCK↑	t_{CD}	20		100	20		100	ns	
RDD active time (high)	t_{RDD}	40			40			ns	

AC Characteristics (cont)

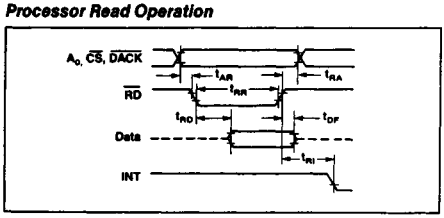
$T_A = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$ unless otherwise specified

Parameter	Symbol	Limits 765A, 7265 Min	Typ(1)	Max	765A-2, 7265-2 Min	Typ(1)	Max	Unit	Test Conditions
Window cycle time	t_{WCY}		4			4		μs	MFM=0, 5¼"
			2			2		μs	MFM=1, 5¼"
			2			2		μs	MFM=0, 8"
			1			1		μs	MFM=1, 8"
			2			2		μs	MFM=0, 3½" (3)
			1			1		μs	MFM=1, 3½"(3)
Window hold time to RDD	t_{RDW}	15			15			ns	
Window hold time from RDD	t_{WRD}	15			15			ns	
$US_{0,1}$ hold time to $\overline{RW}$ / seek↑	t_{US}	12			12			μs	8 MHz clock period(4)
$\overline{RW}$ / seek hold time to low current / direction↑	t_{SD}	7			7			μs	8 MHz clock period(4)
Low current / direction hold time to fault reset / step↑	t_{DST}	1.0			1.0			μs	8 MHz clock period(4)
$US_{0,1}$ hold time from fault reset / step↑	t_{STU}	5.0			5.0			μs	8 MHz clock period(4)
Step active time (high)	t_{STP}	6	7	8	6	7	8	μs	(Note 4)
Step cycle time	t_{SC}	33	(Note 2)	(Note 2)	33	(Note 2)	(Note 2)	μs	(Note 4)
Fault reset active time (high)	t_{FR}	8.0		10	8.0		10	μs	(Note 4)
Write data width	t_{WDD}	t_0-50			t_0-50			ns	
$US_{0,1}$ hold time after seek	t_{SU}	15			15			μs	8 MHz clock period(4)
Seek hold time from DIR	t_{DS}	30			30			μs	8 MHz clock period(4)
DIR hold time after step	t_{STD}	24			24			μs	8 MHz clock period(4)
Index pulse width	t_{IDX}	4			4			Φ_{CY}	
$\overline{RD}$↓ delay from DRQ	t_{MR}	800			800			ns	8 MHz clock period(4)
$\overline{WR}$↓ delay from DRQ	t_{MW}	250			250			ns	8 MHz clock period(4)
WE or $\overline{RD}$ response time from DRQ↑	t_{MRW}			12			12	μs	8 MHz clock period(4)

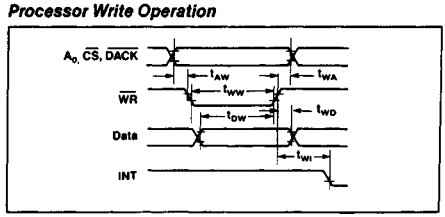
Note:
(1) Typical values for $T_A = 25°C$ and nominal supply voltage.
(2) Under software control. The range is from 1 ms to 16 ms at 8 MHz clock period, and 2 ms to 32 ms at 4 MHz clock period.
(3) Sony Micro Floppydisk 3½" drive.
(4) Double these values for a 4 MHz clock period.

Timing Waveforms

Processor Read Operation

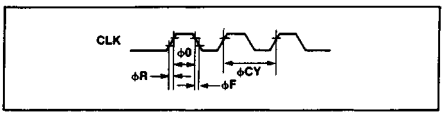


Processor Write Operation

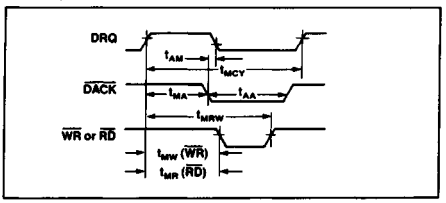


Timing Waveforms (cont)

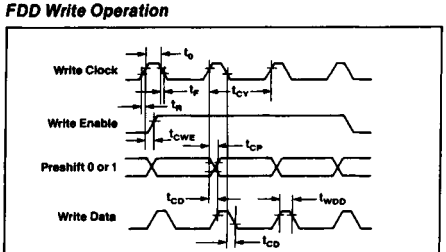
Clock



DMA Operation

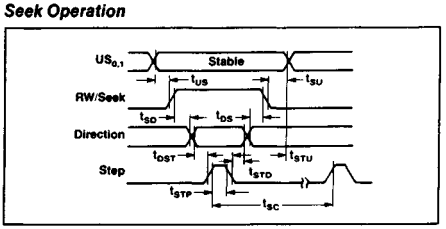


FDD Write Operation

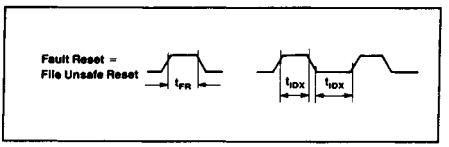


	Preshift 0	Preshift 1
Normal	0	0
Late	0	1
Early	1	0
Invalid	1	1

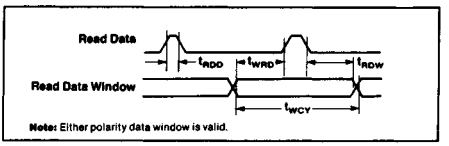
Seek Operation



FLT Reset

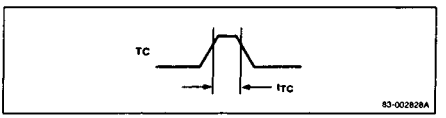


FDD Read Operation

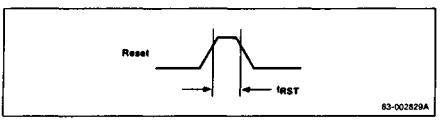


Note: Either polarity data window is valid.

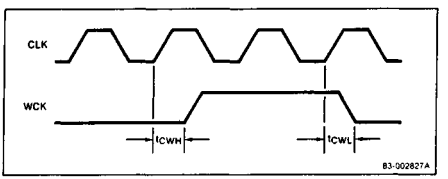
Terminal Count



Reset



Write Clock



Internal Registers

The μPD765A/μPD7265 contains two registers which may be accessed by the main system processor: a status register and a data register. The 8-bit main status register contains the status information of the FDC, and may be accessed at any time. The 8-bit data register (which actually consists of four registers, ST0-ST3, in a stack with only one register presented to the data bus at a time), stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the data register in order to program or obtain the results after a particular command (table 3). Only the status register may be read and used to facilitate the transfer of data between the processor and μPD765A/μPD7265.

The relationship between the status/data registers and the signals $\overline{RD}$, $\overline{WR}$, and A_0 is shown in table 1.

Table 1. Status/Data Register Addressing

A_0	$\overline{RD}$	$\overline{WR}$	Function
0	0	1	Read main status register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from data register
1	1	0	Write into data register

The bits in the main status register are defined in table 2.

Table 2. Main Status Register

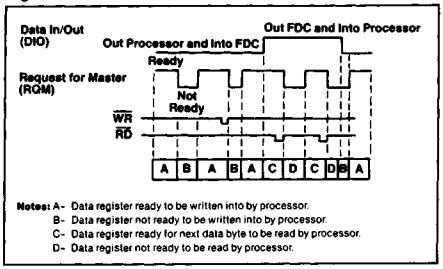
Pin No.	Pin Name	Function
DB_0	D_0B (FDD 0 Busy)	FDD number 0 is in the seek mode. If any of the D_nB bits is set FDC will not accept read or write command.
DB_1	D_1B (FDD 1 Busy)	FDD number 1 is in the seek mode. If any of the D_nB bits is set FDC will not accept read or write command.
DB_2	D_2B (FDD 2 Busy)	FDD number 2 is in the seek mode. If any of the D_nB bits is set FDC will not accept read or write command.
DB_3	D_3B (FDD 3 Busy)	FDD number 3 is in the seek mode. If any of the D_nB bits is set FDC will not accept read or write command.
DB_4	CB (FDC Busy)	A Read or Write command is in process. FDC will not accept any other command.
DB_5	EXM (Execution Mode)	This bit is set only during execution phase in non-DMA mode. When DB_5 goes low, execution phase has ended and result phase has started. It operates only during non-DMA mode of operation.

Table 2. Main Status Register (cont)

Pin No.	Pin Name	Function
DB_6	DIO (Data Input / Output)	Indicates direction of data transfer between FDC and data register. If DIO = 1, then transfer is from data register to the processor. If DIO = 0, then transfer is from the processor to data register.
DB_7	RQM (Request for Master)	Indicates data register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor.

The DIO and RQM bits in the status register indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last $\overline{RD}$ or $\overline{WR}$ during a command or result phase and DIO and RQM getting set or reset is 12 μs. For this reason every time the main status register is read the CPU should wait 12 μs. The maximum time from the trailing edge of the last $\overline{RD}$ in the result phase to when DB_4 (FDC busy) goes low is 12 μs. See figure 1.

Figure 1. DIO and RQM



Notes: A- Data register ready to be written into by processor.
B- Data register not ready to be written into by processor.
C- Data register ready for next data byte to be read by processor.
D- Data register not ready to be read by processor.

Table 3. Status Register Identification

Pin No.	Name	Function
Status Register 0		
D_7, D_6	IC (Interrupt Code)	$D_7 = 0$ and $D_6 = 0$ Normal termination of command, (NT). Command was completed and properly executed.
		$D_7 = 0$ and $D_6 = 1$ Abnormal termination of command, (AT). Execution of command was started but was not successfully completed.
		$D_7 = 1$ and $D_6 = 0$ Invalid command issue, (IC). Command which was issued was never started.
		$D_7 = 1$ and $D_6 = 1$ Abnormal termination because during command execution the ready signal from FDD changed state.
D_5	SE (Seek End)	When the FDC completes the Seek command, this flag is set to 1 (high).
D_4	EC (Equipment Check)	If a fault signal is received from the FDD, or if the track 0 signal fails to occur after 77 step pulses (Recalibrate Command) then this flag is set.
D_3	NR (Not Ready)	When the FDD is in the not-ready state and a Read or Write command is issued, this flag is set. If a Read or Write command is issued to side 1 of a single-sided drive, then this flag is set.
D_2	HD (Head Address)	This flag is used to indicate the state of the head at interrupt.
D_1	US_1 (Unit Select 1)	This flag is used to indicate a drive unit number at interrupt.
D_0	US_0 (Unit Select 0)	This flag is used to indicate a drive unit number at interrupt.
Status Register 1		
D_7	EN (End of Cylinder)	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
D_6		Not used. This bit is always 0 (low).
D_5	DE (Data Error)	When the FDC detects a CRC(1) error in either the ID field or the data field, this flag is set.
D_4	OR (Overrun)	If the FDC is not serviced by the host system during data transfers within a certain time interval, this flag is set.
D_3		Not used. This bit is always 0 (low).

Table 3. Status Register Identification (cont)

Pin No.	Name	Function
Status Register 1 (cont)		
D_2	ND (No Data)	During execution of Read Data, Write Deleted Data or Scan command, if the FDC cannot find the sector specified in the IDR(2) Register, this flag is set.
		During execution of the Read ID command, if the FDC cannot read the ID field without an error, then this flag is set.
		During execution of the Read A Cylinder command, if the starting sector cannot be found, then this flag is set.
D_1	NW (Not Writable)	During execution of Write Data, Write Deleted Data or Format A Cylinder command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	MA (Missing Address Mark)	If the FDC cannot detect the data address mark or deleted data address mark, this flag is set. Also at the same time, the MD (missing address mark in data field) of status register 2 is set.
Status Register 2		
D_7		Not used. This bit is always 0 (low).
D_6	CM (Control Mark)	During execution of the Read Data or Scan command, if the FDC encounters a sector which contains a deleted data address mark, this flag is set.
D_5	DD (Data Error in Data Field)	If the FDC detects a CRC error in the data field then this flag is set.
D_4	WC (Wrong Cylinder)	This bit is related to the ND bit, and when the contents of C(3) on the medium is different from that stored in the IDR, this flag is set.
D_3	SH (Scan Equal Hit)	During execution of the Scan command, if the condition of "equal" is satisfied, this flag is set.
D_2	SN (Scan Not Satisfied)	During execution of the Scan command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set.
D_1	BC (Bad Cylinder)	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FFH, then this flag is set.
D_0	MD (Missing Address Mark in Data Field)	When data is read from the medium, if the FDC cannot find a data address mark or deleted data address mark, then this flag is set.

Table 3. Status Register Identification (cont)

Pin No.	Pin Name	Function
Status Register 3		
D_7	FT (Fault)	This bit is used to indicate the status of the fault signal from the FDD.
D_6	WP (Write Protected)	This bit is used to indicate the status of the write protected signal from the FDD.
D_5	RY (Ready)	This bit is used to indicate the status of the ready signal from the FDD.
D_4	T0 (Track 0)	This bit is used to indicate the status of the track 0 signal from the FDD.
D_3	TS (Two-Side)	This bit is used to indicate the status of the two-side signal from the FDD.
D_2	HD (Head Address)	This bit is used to indicate the status of the side select signal to the FDD.
D_1	US_1 (Unit Select 1)	This bit is used to indicate the status of the unit select 1 signal to the FDD.
D_0	US_0 (Unit Select 0)	This bit is used to indicate the status of the unit select 0 signal to the FDD.

Note:
(1) CRC = Cyclic Redundancy Check
(2) IDR = Internal Data Register
(3) Cylinder (C) is described more fully in the Command Symbol Description.

Command Sequence

The μPD765A/μPD7265 is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the processor, and the result after execution of the command may also be a multibyte transfer back to the processor. Because of this multibyte interchange of information between the μPD765A/μPD7265 and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase:	The FDC receives all information required to perform a particular operation from the processor.
Execution Phase:	The FDC performs the operation it was instructed to do.
Result Phase:	After completion of the operation, status and other housekeeping information are made available to the processor.

Table 4 shows the required preset parameters and results for each command. Most commands require 9 command bytes and return 7 bytes during the result phase. The "W" to the left of each byte indicates a command phase byte to be written, and an "R" indicates a result byte. The definitions of other abbriviations used in table are given in the Command Symbol Description table.

Command Symbol Description

Name	Function
A_0 (Address Line 0)	A_0 controls selection of main status register ($A_0 = 0$) or data register ($A_0 = 1$).
C (Cylinder Number)	C stands for the current/selected cylinder (track) numbers 0 through 76 of the medium.
D (Data)	D stands for the data pattern which is going to be written into a sector.
D_7–D_0 (Data Bus)	8-bit data bus, where D_7 stands for a most significant bit, and D_0 stands for a least significant bit.
DTL (Data Length)	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the sector.
EOT (End of Track)	EOT stands for the final sector number on a cylinder. During read or write operations, FDC will stop data transfer after a sector number equal to EOT.
GPL (Gap Length)	GPL stands for the length of gap 3. During Read/Write commands this value determines the number of bytes that VCO sync will stay low after two CRC bytes. During Format command it determines the size of gap 3.
H (Head Address)	H stands for head number 0 or 1, as specified in ID field.
HD (Head)	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
HLT (Head Load Time)	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT (Head Unload Time)	HUT stands for the head unload time after a Read or Write operation has occurred (16 to 240 ms in 16 ms increments).
MF (FM or MFM Mode)	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT (Multitrack)	If MT is high, a multitrack operation is performed. If MT = 1 after finishing read/write operation on side 0, FDC will automatically start searching for sector 1 on side 1.
N (Number)	N stands for the number of data bytes written in a sector.
NCN (New Cylinder Number)	NCN stands for a new cylinder number which is going to be reached as a result of the seek operation; desired position of head.
ND (Non-DMA Mode)	ND stands for operation in the non-DMA mode.
PCN (Present Cylinder Number)	PCN stands for the cylinder number at the completion of Sense Interrupt Status command, position of head at present time.
R (Record)	R stands for the sector number which will be read or written.
R/W (Read/Write)	R/W stands for either Read (R) or Write (W) signal.
SC (Sector)	SC indicates the number of sectors per cylinder.
SK (Skip)	SK stands for skip deleted data address mark.

Command Symbol Description (cont)

Name	Function
SRT (Step Rate Time)	SRT stands for the stepping rate for the FDD (1 to 16 ms in 1 ms increments). Stepping rate applies to all drives (FH = 1 ms, EH = 2 ms, etc.).
ST0–ST3 (Status 0–3)	ST0–ST3 stands for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by $A_0 = 0$). ST0–ST3 may be read only after a command has been executed and contains information relevant to that particular command.

Command Symbol Description (cont)

Name	Function
STP	During a scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
US_0, US_1 (Unit Select)	US stands for a selected drive number 0 or 1.

Table 4. Instruction Set (Notes 1, 2)

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Read Data										
Command	W	MT	MF	SK	0	0	1	1	0	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	(Note 3)
	W	←				C			→	Sector ID information prior to command execution. The 4 bytes
	W	←				H			→	are compared against header on floppy disk.
	W	←				R			→	
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				DTL			→	
Execution										Data transfer between the FDD and main system
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	
Read Deleted Data										
Command	W	MT	MF	SK	0	1	1	0	0	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				C			→	Sector ID information prior to command execution. The 4 bytes
	W	←				H			→	are compared against header on floppy disk.
	W	←				R			→	
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				DTL			→	
Execution										Data transfer between the FDD and main system
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	

Note:

(1) Symbols used in this table are described at the end of this section.

(2) A_0 should equal 1 for all operations.

(3) X = Don't care, usually made to equal 0.

Table 4. Instruction Set (Notes 1, 2) (cont)

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Write Data										
Command	W	MT	MF	0	0	0	1	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior to command execution. The 4 bytes
	W	←			H				→	are compared against header on floppy disk.
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			DTL				→	
Execution										Data transfer between the main system and FDD
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	
Write Deleted Data										
Command	W	MT	MF	0	0	1	0	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior to command execution. The 4 bytes
	W	←			H				→	are compared against header on floppy disk.
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			DTL				→	
Execution										Data transfer between the FDD and main system
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	
Read A Track										
Command	W	0	MF	SK	0	0	0	1	0	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior to command execution
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			DTL				→	
Execution										Data transfer between the FDD and main system. FDC reads all data fields from index hole to EOT.
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	

Table 4. Instruction Set (Notes 1, 2) (cont)

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Read ID										
Command	W	0	MF	0	0	1	0	1	0	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
Execution										The first correct ID information on the cylinder is stored in data register.
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information read during execution phase from floppy disk.
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	
Format A Track										
Command	W	0	MF	0	0	1	1	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			N				→	Bytes / sector
	W	←			SC				→	Sectors / track
	W	←			GPL				→	Gap 3
	W	←			D				→	Filler byte
Execution										FDC formats an entire track.
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	In this case, the ID information has no meaning
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	
Scan Equal										
Command	W	MT	MF	SK	1	0	0	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior to command execution
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			STP				→	
Execution										Data compared between the FDD and main system
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	

Note:
(1) Symbols used in this table are described at the end of this section.
(2) A_0 should equal 1 for all operations.
(3) X = Don't care, usually made to equal 0.

Table 4. Instruction Set (Notes 1, 2) (cont)

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Scan Low or Equal										
Command	W	MT	MF	SK	1	1	0	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior to command execution
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			STP				→	
Execution										Data compared between the FDD and main system
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	
Scan High or Equal										
Command	W	MT	MF	SK	1	1	1	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior to command execution
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			STP				→	
Execution										Data compared between the FDD and main system
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	
Recalibrate										
Command	W	0	0	0	0	0	1	1	1	Command codes
	W	X	X	X	X	X	0	US_1	US_0	
Execution										Head retracted to track 0
Sense Interrupt Status										
Command	W	0	0	0	0	1	0	0	0	Command codes
Result	R	←			ST0				→	Status information about the FDC at the end of seek operation
	R	←			PCN				→	
Specify										
Command	W	0	0	0	0	0	0	1	1	Command codes
	W	←	SRT	→		←	HUT	→		
	W	←		HLT	→				ND	
Sense Drive Status										
Command	W	0	0	0	0	0	1	0	0	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
Result	R	←			ST3				→	Status information about FDD

Table 4. Instruction Set (Notes 1, 2) (cont)

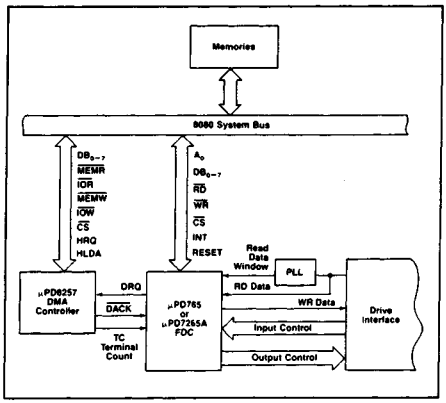
Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Seek										
Command	W	0	0	0	0	1	1	1	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	← NCN →								
Execution										Head is positioned over proper cylinder on diskette
Invalid										
Command	W	← Invalid Codes →								Invalid Command codes (No op — FDC goes into standby state)
Result	R	← ST0 →								ST0 = 80H

Note:
(1) Symbols used in this table are described at the end of this section.
(2) A_0 should equal 1 for all operations.
(3) X = Don't care, usually made to equal 0.

System Configuration

Figure 2 shows an example of a system using a μPD765A/μPD7265.

Figure 2. System Configuration



Processor Interface

During command or result phases the main status register (described earlier) must be read by the processor before each byte of information is written into or read from the data register. After each byte of data read or written to the data register, CPU should wait for 12 μs before reading main status register, bits D_6 and D_7 in the main status register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the μPD765A/μPD7265. Many of the commands require multiple bytes and, as a result, the main status register must be read prior to each byte transfer to the μPD765A/μPD7265. On the other hand, during the result phase, D_6 and D_7 in the main status register must both be 1's ($D_6 = 1$ and $D_7 = 1$) before reading each byte from the data register. Note that this reading of the main status register before each byte transfer to the μPD765A/μPD7265 is required only in the command and result phases, and *not* during the execution phase.

During the execution phase, the main status register need not be read. If the μPD765A/μPD7265 is in the non-DMA mode, then the receipt of each data byte (if μPD765A/μPD7265 is reading data from FDD) is indicated by an interrupt signal on pin 18 (INT = 1). The generation of a read signal ($\overline{RD} = 0$) or write signal ($\overline{WR} = 0$) will clear the interrupt as well as output the data onto the data bus. If the processor cannot handle interrupts fast enough (every 13 μs for the MFM mode and 27 μs for the FM mode), then it may poll the main status register and bit D_7 (RQM) functions as the interrupt signal. If a write command is in process then the $\overline{WR}$ signal negates the reset to the interrupt signal.

Note that in the non-DMA mode it is necessary to examine the main status register to determine the cause of the interrupt, since it could be a data interrupt or a command termination interrupt, either normal or abnormal.

If the μPD765A/μPD7265 is in the DMA mode, no interrupts are generated during the execution phase. The μPD765A/μPD7265 generates DRQs (DMA requests) when each byte of data is available. The DMA controller responds to this request with both a $\overline{DACK} = 0$ (DMA acknowledge) and an RD = 0 (read signal). When the DMA acknowledge signal goes low ($\overline{DACK} = 0$), then the DMA request is cleared (DRQ = 0). If a write command has been issued then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the execution phase has been completed (terminal count has occurred) or the EOT sector read/written, then an interrupt will occur (INT = 1). This signifies the beginning of the result phase. When the first byte of

data is read during the result phase, the interrupt is automatically cleared (INT = 0).

The $\overline{RD}$ or $\overline{WR}$ signals should be asserted while $\overline{DACK}$ is true. The $\overline{CS}$ signal is used in conjunction with $\overline{RD}$ and $\overline{WR}$ as a gating function during programmed I/O operations. $\overline{CS}$ has no effect during DMA operations. If the non-DMA mode is chosen, the $\overline{DACK}$ signal should be pulled up to V_{CC}.

It is important to note that during the result phase all bytes shown in the command table (table 4) must be read. The read data command, for example, has seven bytes of data in the result phase. All seven bytes must be read in order to successfully complete the Read Data command. The μPD765A/μPD7265 will not accept a new comand until all seven bytes have been read. Other commands may require fewer bytes to be read during the result phase.

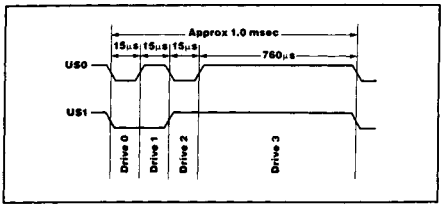
The μPD765A/μPD7265 contains five status registers. The main status register mentioned above may be read by the processor at any time. The other four status registers (ST0, ST1, ST2, and ST3) are available only during the result phase and may be read only after completing a command. The particular command that has been executed determines how many of the status registers will be read.

The bytes of data which are sent to the μPD765A/μPD7265 to form the command phase and are read out of the μPD765A/μPD7265 in the result phase must occur in the order shown in table 4. That is, the command code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the command or result phases is allowed. After the last byte of data in the command phase is sent to the μPD765A/μPD7265, the execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the result phase, the command is automatically ended and the μPD765A/μPD7265 is ready for a new command.

Polling

After reset has been sent to the μPD765A/μPD7265, the unit select lines US_0 and US_1 will automatically go into a polling mode. In between commands (and between step pulses in the Seek command) the μPD765A/μPD7265 polls all four FDDs looking for a change in the ready line from any of the drives. If the ready line changes state (usually due to a door opening or closing), then the μPD765A/μPD7265 will generate an interrupt. When status register 0 (ST0) is read (after Sense Interrupt Status is issued), not ready (NR) will be indicated. The polling of the ready line by the μPD765A/μPD7265 occurs continuously between commands, thus notifying the processor which drives are on or off line. Each drive is polled every 1.024 ms except during the Read/Write commands. When used with a 4 MHz clock for interfacing to minifloppies, the polling rate is 2.048 ms. See figure 3.

Figure 3. Polling Feature



Read Data

A set of nine (9) byte words are required to place the FDC into the read data mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID address marks and ID fields. When the current sector number (R) stored in the ID register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the sector number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a multi-sector read operation. The Read Data command may be terminated by the receipt of a terminal count signal. $\overline{TC}$ should be issued at the same time that the $\overline{DACK}$ for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (cyclic redundancy count) bytes, and then at the end of the sector terminate the Read Data command. The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MF (MFM/FM), and N (number of bytes/sector). Table 5 shows the transfer capacity.

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at sector 1, side 0 and completing at sector L, side 1 (sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a sector, the data beyond DTL in the sector is not sent to the data bus. The FDC reads (internally) the complete sector performing the CRC check and, depending upon the manner of command

termination, may perform a multi-sector read operation. When N is non-zero, then DTL has no meaning and should be set to FFH.

Table 5. Transfer Capacity

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskettes
0	0	00	(128) (26) = 3,328	26 at side 0
0	1	01	(256) (26) = 6,656	or 26 at side 1
1	0	00	(128) (52) = 6,656	26 at side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at side 0
0	1	02	(512) (15) = 7,680	or 15 at side 1
1	0	01	(256) (30) = 7,680	15 at side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at side 0
0	1	03	(1024) (8) = 8,192	or 8 at side 1
1	0	02	(512) (16) = 8,192	8 at side 1
1	1	03	(1024) (16) = 16,384	

At the completion of the Read Data command, the head is not unloaded until after head unload time interval (specified in the Specify command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the index hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No data) flag in status register 1 to a 1 (high), and terminates the Read Data command. (Status register 0 also has bits 7 and 6 set to 0 and 1, respectively.)

After reading the ID and data fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (data error) flag in status register 1 to a 1 (high), and if a CRC error occurs in the data field, the FDC also sets the DD (data error in data field) flag in status register 2 to a 1 (high), and terminates the Read Data command. (Status register 0 also has bits 7 and 6 set to 0 and 1, respectively.)

If the FDC reads a deleted data address mark off the diskette, and the SK bit (bit D_5 in the first command word) is not set (SK = 0), then the FDC sets the CM (control mark) flag in status register 2 to a 1 (high), and terminates the Read Data command, after reading all the data in the sector. If SK = 1, the FDC skips the sector with the deleted data address mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 μs in the FM mode, and every 13 μs in the MFM mode, or the FDC sets the OR (Overrun) flag in status register 1 to a 1 (high), and terminates the Read Data command.

If the processor terminates a read (or write) operation in the FDC, then the ID information in the result phase is dependent upon the state of the MT bit and EOT byte. Table 2 shows the values for C, H, R, and N, when the processor terminates the command.

Functional Description of Commands

Write Data

A set of nine (9) bytes is required to set the FDC into the write data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus and outputs it to the FDD. See table 6.

Table 6. Command Description

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase C	H	R	N
0	0	Less than EOT	NC	NC	R+1	NC
0	0	Equal to EOT	C+1	NC	R=01	NC
0	1	Less than EOT	NC	NC	R+1	NC
0	1	Equal to EOT	C+1	NC	R=01	NC
1	0	Less than EOT	NC	NC	R+1	NC
1	0	Equal to EOT	NC	LSB	R=01	NC
1	1	Less than EOT	NC	NC	R+1	NC
1	1	Equal to EOT	C+1	LSB	R=01	NC

Note:
(1) NC (No Change): The same value as the one at the beginning of command execution.
(2) LSB (Least Significant Bit): The least significant bit of H is complemented.

After writing data into the current sector, the sector number stored in R is incremented by one, and the next data field is written into. The FDC continues this multi-sector write operation until the issuance of a terminal count signal. If a terminal count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the terminal count signal is received while a data field is being written then the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (CRC error) in one of the ID fields, it sets the DE (Data Error) flag of status register 1 to a 1 (high) and terminates the Write

Data command. (Status register 0 also has bits 7 and 6 set to 0 and 1, respectively.)

The Write command operates in much the same manner as the Read command. The following items are the same, and one should refer to the Read Data command for details:

- Transfer capacity
- EN (end of cylinder) flag
- ND (no data) flag
- Head unload time interval
- ID information when the processor terminates command
- Definition of DTL when N = 0 and when N≠0

In the write data mode, data transfers between the processor and FDC, via the data bus, must occur every 27 μs in the FM mode and every 13 μs in the MFM mode. If the time interval between data transfers is longer than this, the FDC sets the OR (overrun) flag in status register 1 to a 1 (high) and terminates the Write Data command. (Status register 0 also has bits 7 and 6 set to 0 and 1, respectively.)

Write Deleted Data

This command is the same as the Write Data command except a deleted data address mark is written at the beginning of the data field instead of the normal data address mark.

Read Deleted Data

This command is the same as the Read Data command except that when the FDC detects a data address mark at the beginning of a data field (and SK = 0 (low)), it will read all the data in the sector and set the CM flag in status register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the data address mark and reads the next sector.

Read a Track

This command is similar to the Read Data command except that this is a continuous read operation where the entire data field from each of the sectors is read. Immediately after sensing the index hole, the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or data CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR and sets the ND flag of status register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT. If the FDC does not find an ID address mark on the diskette after it senses the index hole for the second time, it sets the MA (missing address mark) flag in status register 1 to a 1 (high) and terminates the command. (Status register 0 has bits 7 and 6 set to 0 and 1, respectively.)

Read ID

The Read ID command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read. If no proper ID address mark is found on the diskette before the index hole is encountered for the second time, then the MA (missing address mark) flag in status register 1 is set to a 1 (high), and if no data is found then the ND (No data) flag is also set in status register 1 to a 1 (high). The command is then terminated with bits 7 and 6 in status register 0 set to 0 and 1, respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

Format a Track

The Format a Track command allows an entire track to be formatted. After the index hole is detected, data is written on the diskette; gaps, address marks, ID fields, and data fields, all per the IBM System 34 (double density) or System 3740 (single density) format, are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (gap length), and D (data pattern) which are supplied by the processor during the command phase. The data field is filled with the byte of data stored in D. The ID field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (cylinder number), H (head number), R (sector number), and N (number of bytes/sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the μPD765A/μPD7265 for each sector on the track. If FDC is set for the DMA mode, it will issue four DMA requests per sector. If it is set for the interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R, and N loads for each sector. The contents of the R register are incremented by 1 after each sector is formatted; thus, the R register contains a value of R when it is read during the result phase. This incrementing and formatting continues for the whole track until the FDC detects the index hole for the second time, whereupon it terminates the command.

If a fault signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of status register 0 to a 1 (high) and terminates the command after setting bits 7 and 6 of status register 0 to 0 and 1, respec-

tively. Also, the loss of a ready signal at the beginning of a command execution phase causes bits 7 and 6 of status register 0 to be set to 0 and 1, respectively.

Table 7 shows the relationship between N, SC, and GPL for various sector sizes.

Table 7. Sector Size

Format	Sector Size	N	SC	GPL(1)	GPL(2, 3)
8" Standard Floppy					
FM Mode	128 Bytes / Sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode(4)	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5¼" Minifloppy					
FM Mode	128 Bytes / Sector	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode(4)	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3½" Sony Micro Floppydisk					
FM Mode	128 Bytes / Sector	0	0F	07	1B
	256	1	09	0E	2A
	512	2	05	1B	3A
MFM Mode(4)	256	1	0F	0E	36
	512	2	09	1B	54
	1024	3	05	35	74

Note:
(1) Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections.
(2) Suggested values of GPL in format command.
(3) All values except sector size are hexidecimal.
(4) In MFM mode FDC cannot perform a Read/Write/Format operation with 128 bytes/sector. (N = 00).

Scan Commands

The Scan commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} < D_{Processor}$, or $D_{FDD} > D_{Processor}$. The hexidecimal byte of FF either from memory or from FDD can be used as a mask byte because it always meets the condition of the comparison. One's complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur: the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met, then the FDC sets the SH (scan hit) flag of status register 2 to a 1 (high) and terminates the Scan command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (scan not satisfied) flag of status register 2 to a 1 (high) and terminates the Scan command. The receipt of a terminal count signal from the processor or DMA controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process and then to terminate the command. Table 8 shows the status of bits SH and SN under various conditions of Scan.

Table 8. Scan Conditions

Command	Status Register 2		Comments
	Bit 2 = SN	Bit 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} > D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} < D_{Processor}$

If the FDC encounters a deleted data address mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets the CM (control mark) flag of status register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the deleted address mark and reads the next sector. In the second case (SK = 1), the FDC sets the CM

(control mark) flag of status register 2 to a 1 (high) in order to show that a deleted sector has been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02) sectors are read or the MT (multi-track) is programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26 and the Scan command is started at sector 21, the following will happen: sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the index hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan command would be completed in a normal manner.

During the Scan command, data is supplied by either the processor or DMA controller for comparison against the data read from the diskette. In order to avoid having the OR (overrun) flag set in status register 1, it is necessary to have the data available in less than 27 μs (FM mode) or 13 μs (MFM mode). If an overrun occurs, the FDC ends the command with bits 7 and 6 of status register 0 set to 0 and 1, respectively.

Seek

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek command. FDC has four independent present cylinder registers for each drive. They are cleared only after the Recalibrate command. The FDC compares the PCN (present cylinder number) which is the current head position with the NCN (new cylinder number), and if there is a difference, performs the following operations:

PCN < NCN: Direction signal to FDD set to a 1 (high), and step pulses are issued. (Step in)

PCN > NCN: Direction signal to FDD set to a 0 (low), and step pulses are issued. (Step out)

The rate at which step pulses are issued is controlled by SRT (stepping rate time) in the Specify command. After each step pulse is issued NCN is compared against PCN, and when NCN = PCN, the SE (seek end) flag is set in status register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits D_0B-D_3B in the main status register are set during the seek operation and are cleared by the Sense Interrupt Status command.

During the command phase of the seek operation the FDC is in the FDC busy state, but during the execution phase it is in the non-busy state. While the FDC is in the non-busy state, another Seek command may be issued, and in this manner parallel seek operations may be done on up to four drives at once. No other command can be issued for as long as the FDC is in the process of sending step pulses to any drive.

If an FDD is in a not ready state at the beginning of the command execution phase or during the seek operation, then the NR (not ready) flag is set in status register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of status register 0 are set to 0 and 1, respectively.

If the time to write three bytes of Seek command exceeds 150 μs, the timing between the first two step pulses may be shorter than set in the Specify command by as much as 1 ms.

Recalibrate

The function of this command is to retract the read/write head within the FDD to the track 0 position. The FDC clears the contents of the PCN counter and checks the status of the track 0 signal from the FDD. As long as the track 0 signal is low, the direction signal remains 0 (low) and step pulses are issued. When the track 0 signal goes high, the SE (seek end) flag in status register 0 is set to a 1 (high) and the command is terminated. If the track 0 signal is still low after 77 step pulses have been issued, the FDC sets the SE (seek end) and EC (equipment check) flags of status register 0 to both 1s (highs) and terminates the command after bits 7 and 6 of status register 0 are set to 0 and 1, respectively.

The ability to do overlapping Recalibrate commands to multiple FDDs and the loss of the ready signal, as described in the Seek command, also applies to the Recalibrate command. If the diskette has more than 77 tracks, then Recalibrate command should be issued twice, in order to position the read/write head to the track 0.

Sense Interrupt Status

An interrupt signal is generated by the FDC for one of the following reasons:

(1) Upon entering the result phase of:
  (a) Read Data command
  (b) Read a Track command
  (c) Read ID command
  (d) Read Deleted Data command
  (e) Write Data command
  (f) Format a Cylinder command
  (g) Write Deleted Data command
  (h) Scan commands
(2) Ready line of FDD changes state
(3) End of Seek or Recalibrate command
(4) During execution phase in the non-DMA mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in non-

DMA mode, DB_5 in the main status register is high. Upon entering the result phase this bit gets cleared. Reasons 1 and 4 do not require Sense Interrupt Status commands. The interrupt is cleared by reading/writing data to the FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status command. This command, when issued, resets the Interrupt signal and, via bits 5, 6, and 7 of status register 0, identifies the cause of the interrupt. See table 9.

Table 9. Interrupt Status

Seek End Bit 5	Interrupt Code Bit 6	Interrupt Code Bit 7	Cause
0	1	1	Ready line changed state, either polarity
1	0	0	Normal termination of Seek or Recalibrate command
1	1	0	Abnormal termination of Seek or Recalibrate command

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no result phase. When the disk drive has reached the desired head position the μPD765A/μPD7265 will set the interrupt line true. The host CPU must then issue a Sense Interrupt Status command to determine the actual cause of the interrupt, which could be seek end or a change in ready status from one of the drives. A graphic example is shown in figure 4.

Specify

The Specify command sets the initial values for each of the three internal timers. The HUT (head unload time) defines the time from the end of the execution phase of one of the Read/Write commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms... 0FH = 240 ms). The SRT (step rate time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (head load time) defines the time between when the head load signal goes high and the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms... 7F = 254 ms).

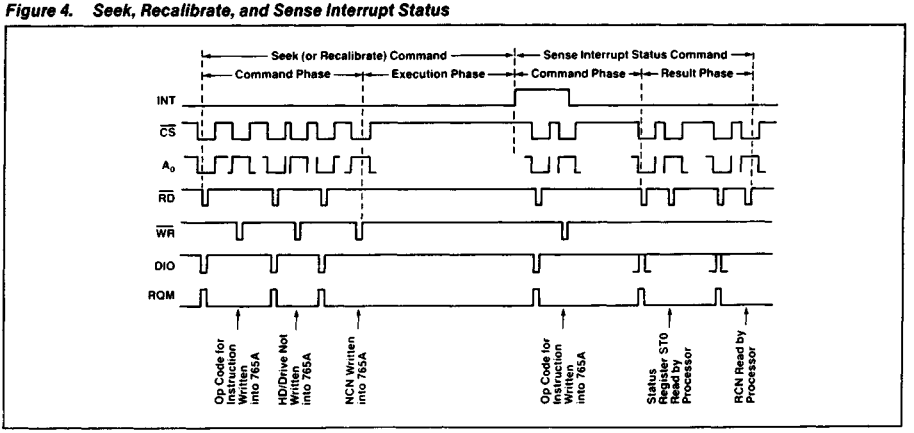
The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock; if the clock was reduced to 4 MHz (minifloppy application), then all time intervals are increased by a factor of 2.

The choice of a DMA or non-DMA operation is made by the ND (non-DMA) bit. When this bit is high (ND = 1) the non-DMA mode is selected, and when ND = 0 the DMA mode is selected.

Sense Drive Status

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status regis-

Figure 4. Seek, Recalibrate, and Sense Interrupt Status



ter 3 contains the drive status information stored internally in FDC registers.

Invalid

If an Invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of status register 0 are set to 1 and 0, respectively. No interrupt is generated by the μPD765A/μPD7265 during this condition. Bits 6 and 7 (DIO and RQM) in the main status register are both 1 (high), indicating to the processor that the μPD765A/μPD7265 is in the result phase and the contents of status register 0 (ST0) must be read. When the processor reads status register 0 it will find an 80H, indicating an Invalid command was received.

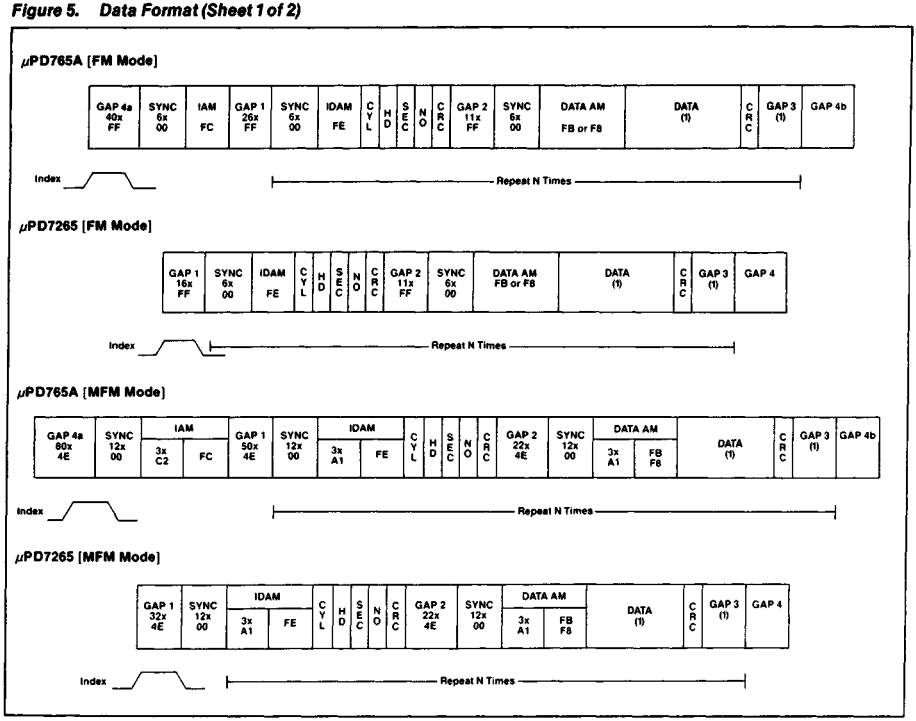
A Sense Interrupt Status command must be sent after a seek or recalibrate interrupt, otherwise the FDC will consider the next command to be an Invalid command.

In some applications the user may wish to use this command as a No-Op command to place the FDC in a standby or no operation state.

Data Format

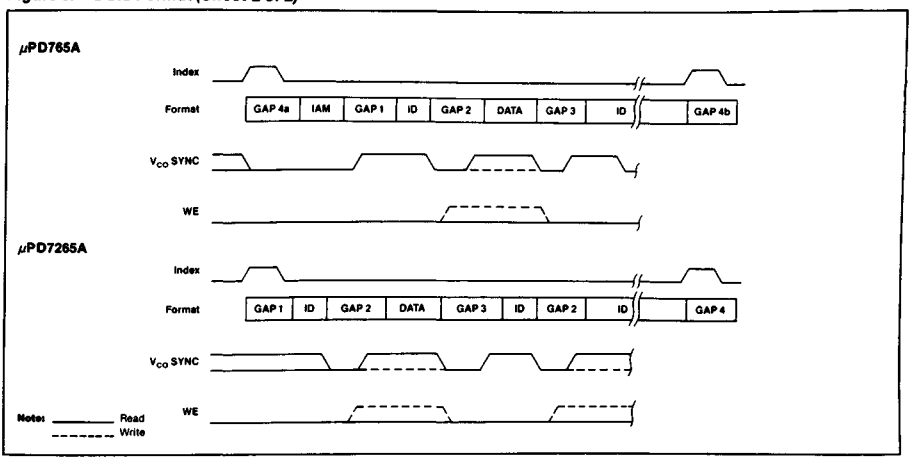
Figure 5 shows the data transfer format for the μPD765A and μPD7265 in various modes.

Figure 5. Data Format (Sheet 1 of 2)



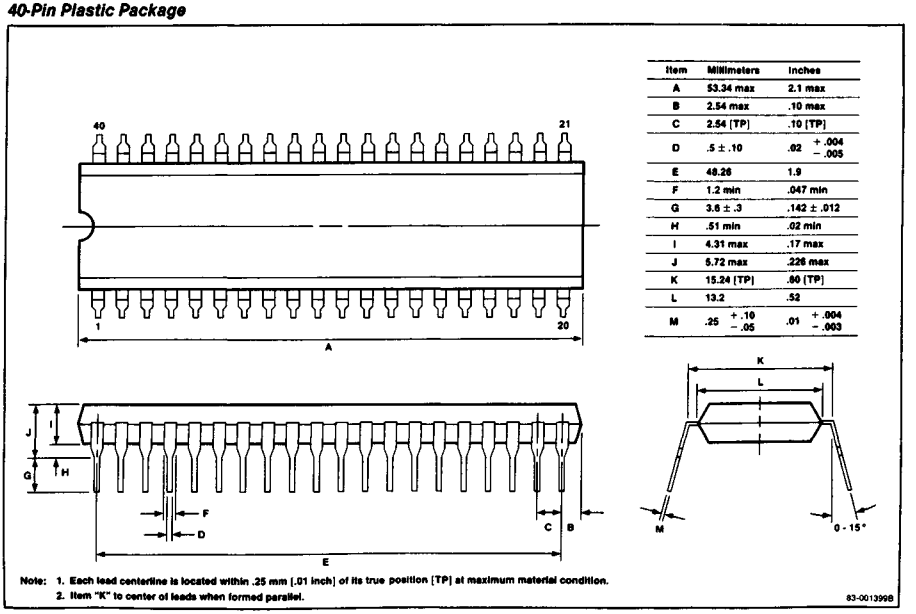
Note: It is suggested that the user refer to the following application notes:
(1) #6 — for an example of an actual interface, as well as a "theoretical" data separator.
(2) #10 — for a well documented example of a working phase-locked loop.

Figure 5. Data Format (Sheet 2 of 2)



Packaging Information

40-Pin Plastic Package



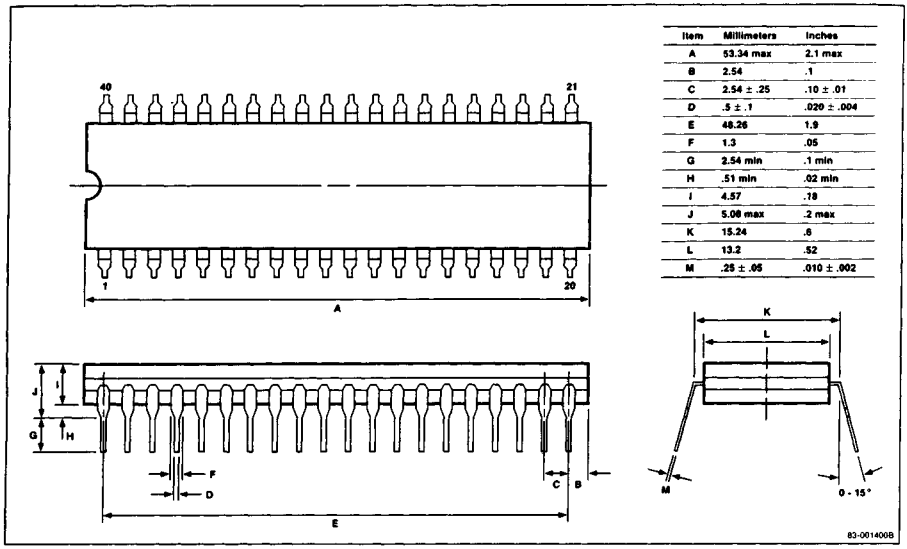
Item	Millimeters	Inches
A	53.34 max	2.1 max
B	2.54 max	.10 max
C	2.54 [TP]	.10 [TP]
D	.5 ± .10	.02 $^{+.004}_{-.005}$
E	48.26	1.9
F	1.2 min	.047 min
G	3.6 ± .3	.142 ± .012
H	.51 min	.02 min
I	4.31 max	.17 max
J	5.72 max	.226 max
K	15.24 [TP]	.60 [TP]
L	13.2	.52
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.003}$

Note: 1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.

83-0013998

Packaging Information (cont)

40-Pin Ceramic Package



Item	Millimeters	Inches
A	53.34 max	2.1 max
B	2.54	.1
C	2.54 ± .25	.10 ± .01
D	.5 ± .1	.020 ± .004
E	48.26	1.9
F	1.3	.05
G	2.54 min	.1 min
H	.51 min	.02 min
I	4.57	.18
J	5.08 max	.2 max
K	15.24	.6
L	13.2	.52
M	.25 ± .05	.010 ± .002

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DMA Chip Specification

DMA Chip Specification
Contents

DMA CHIP SPECIFICATION

GENERAL DESCRIPTION

The DMA Chip is an Intel 8237A-5 (AMD 9517) DMA Controller plus associated support circuity to integrate the TANDY 1000 External Memory function into a single ASIC part. The support circuity is divided into the five functional sections. The ADDRESS DECODE-MEMORY and ADDRESS DECODE-IO are independent of the DMA function and interface directly into the bus. The TIMING and DMA RDY sections are DMA support functions. The BUFFERS support the in/out pins.

The functional configuration of the 8237 for the DMA Chip is a fixed subset of its total capability. It is configured via the BIOS ROM for: normal timing, fixed priority, late write, high DREQ sense, low DACK sense.

ADDRESS DECODE - MEMORY

Provides RAM Memory access decode and address generation. Bus addresses A19-A15 determine which segment(bank) of memory is being accessed based on one of four possible memory configurations. (see memory map Figure 1). This is combined with Bus strobes MEMWB or MEMRB and CLK to create one of the three RAS strobes (RAS0B, RAS1B or RAS2B), MUX, CAS, data directional controls DBDIR, DBENB and the multiplexed RAM addresses MA0-MA8. The signals CAS and MUX will occur for all access's except REFRESH. The address lines MA0-MA8 are Bus addresses A0-A8 and A9-A17 multiplexed together by the signal MUX. These will occur for all access's including REFRESH (since MUX does not occur during REFRESH, MA0-MA8 will be only A0-A8). The selection of MA8 will be made externally since Bank 0 and Bank 1 can be either 64K or 265K DRAM IC's.

	MCF0,MCF1 CODE	MEMORY ORGANIZATION	ADDRESS	ACCESS CONTROL SIGNAL
OPTION #1	00	BANK 0 64K x 8	0.0000-0.FFFF	RAS0
		BANK 1 64K x 8	1.0000-1.FFFF	RAS1
		BANK 2 EMPTY		
OPTION #2	01	BANK 0 256K x 8	0.0000-3.FFFF	RAS0
		BANK 1 EMPTY		
		BANK 2 EMPTY		
OPTION #3	10	BANK 0 256K x 8	0.0000-3.FFFF	RAS0
		BANK 1 256K x 8	4.0000-7.FFFF	RAS1
		BANK 2 EMPTY		
OPTION #4	11	BANK 0 64K x 8	0.0000-0.FFFF	RAS0
		BANK 1 64K x 8	1.0000-1.FFFF	RAS1
		BANK 2 256K x 8	2.0000-5.FFFF	RAS2

Figure 1 MEMORY CONFIGURATION MAP

EQUATIONS FOR RAS-B

64K DRAMS require address A0-A15, therefore A19-A16 determine access.
256K DRAMS require address A0-A17, therefore A19-A18 determine access.

```
RAS0B = /MCF1./MCF0./19./18./17./16./REFRESH.(MEMRB+MEMWB)   OPTION #1
      + /MCF1. MCF0./19./18.        /REFRESH.(MEMRB+MEMWB)   OPTION #2
      +  MCF1./MCF0./19./18.        /REFRESH.(MEMRB+MEMWB)   OPTION #3
      +  MCF1. MCF0./19./18./17./16./REFRESH.(MEMRB+MEMWB)   OPTION #4
      +  REFRESH.MEMRB

RAS1B = /MCF1./MCF0./19./18./17. 16./REFRESH.(MEMRB+MEMWB)   OPTION #1
      +  MCF1./MCF0./19. 18.        /REFRESH.(MEMRB+MEMWB)   OPTION #3,
                                                    NO OPTION #2
      +  MCF1. MCF0./19./18./17. 16./REFRESH.(MEMRB+MEMWB)   OPTION #4
      +  REFRESH.MEMRB

RAS3B =  MCF1. MCF0./19./18. 17     /REFRESH.(MEMRB+MEMWB)   OPTION #4,
                                                 NO OPTION #1,#2,#3
      +  MCF1. MCF0./19. 18./17     /REFRESH.(MEMRB+MEMWB)
      +  REFRESH.MEMRB
```

EQUATIONS FOR MULTIPLEXED ADDRESSES MA-

	ROW ADDRESS (FIRST)	COLUMN ADDRESS (SECOND)	
MA0 :	A0	A8	Since these addresses will
MA1 :	A1	A9	be used for either/both
MA2 :	A2	A10	64K and 256K DRAMS, MA8
MA3 :	A3	A11	will be A16,A17 instead
MA4 :	A4	A12	of two sets of MAs.
MA5 :	A5	A13	(i.e. 64K MA0=A0/A8,
MA6 :	A6	A14	256K MA0=A0/A9,...etc.)
MA7 :	A7	A15	
MA8 :	A16	A17	

ADDRESS DECODE - I/O

Provides I/O decode for generating the chip selects for the DMA Controller and the DMA Segment Address Register plus the data directional control signals DBDIR and DBENB. Bus addresses A0-A15 are decoded and combined with Bus strobes IORB or IOWB to create the chip selects.

CHIP SELECT FUNCTION	ADDRESS	SIGNAL	EQUATION (A19-A16 = don't care) (A15,...,A8 = 0, ALWAYS)
DMA	X.0000-X.000F	DMACSB =	/A7./A6./A5./A4./AEN.(IORB + IOWB)
DMA SEGMENT REGISTER	X.0080-X.0083	WPRCSB =	A7./A6./A5./A4./A4./AEN.IOWB

Figure 2 I/O CONFIGURATION MAP

DMA READY

A system requirement is to have one WAIT cycle automatically inserted into each I/O transfer. When an IORB occurs, WAIT cycles will continually be inserted until IORB returns inactive or until a MEMWB or MEMRB occurs.

This one WAIT cycle is inserted automatically when the CPU is Bus Master. Therefore when the DMA is a Bus Master, it is necessary to insert one WAIT cycle into each DMA I.O transfer (that is every transfer) and honor any additional WAIT requests from the system.

TIMING GENERATOR

The input clock is OSC (= 14.31818 MHZ).

1.) It is divided by three to recreate the 4.77 MHz system processor clock which is used as the clock for the 8237.

2.) It is used to delay the memory access strobe MEM-B twice to create the timing for RAS-, MUX, and CAS.

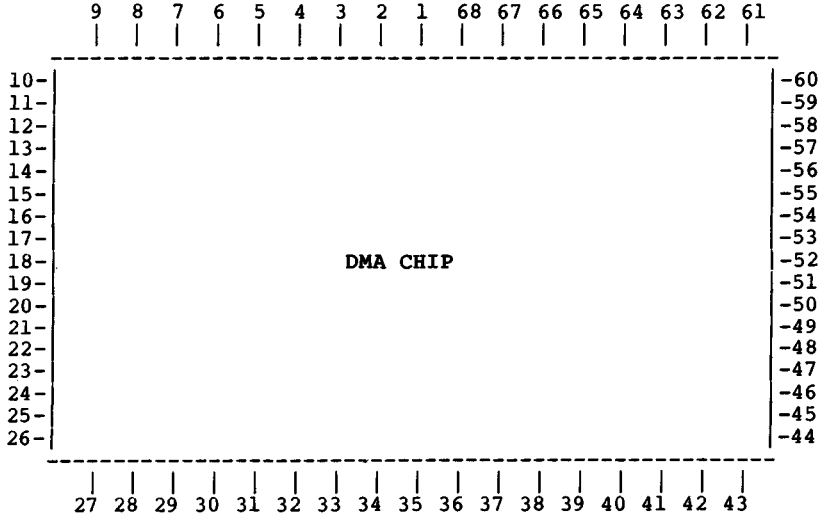
BUFFERS

Provide isolation and drive capability since this circuit will interface directly onto the system bus. These buffers include the bi-directional buffers for address and control strobes (CPU Bus Master - Receive control,address, DMA Bus Master - transmit control,address) but excludes the bi-directional data buffer. Since it must be shared by the memory, this part will be provided externally. Decoding from the ADDRESS DECODE I/O and MEMORY circuitry are combined to provide directional control signals DBDIR, DBENB for this data bus buffer.

FUNCTION	SIGNAL	EQUATION
DATA BUS DIRECTIONAL CONTROL	DBDIR	= DMACSB.IORB + /MCF1./MCF0./19./18./17. /REFRESH. MEMRB + /MCF1. MCF0./19./18. /REFRESH. MEMRB + MCF1. /MCF0./19. /REFRESH. MEMRB + MCF1. MCF0./19.(/18 + 18./17)./REFRESH. MEMRB
DATA BUS BUFFER ENABLE	DBENB	= DMACSB + WPRCSB + /MCF1./MCF0./19./18./17. /REFRESH. MEM-B + /MCF1. MCF0./19./18. /REFRESH. MEM-B + MCF1. /MCF0./19. /REFRESH. MEM-B + MCF1. MCF0./19.(/18 + 18./17)./REFRESH. MEM-B
ADDRESS BUS, CONTROL BUS DIRECTIONAL CONTROL	DMAAENB	= 8257 Signal AEN inverted

Figure 3 BUFFER CONTROL SIGNALS

PIN LIST


9 8 7 6 5 4 3 2 1 68 67 66 65 64 63 62 61
10- -60
11- -59
12- -58
13- -57
14- -56
15- -55
16- -54
17- -53
18- DMA CHIP -52
19- -51
20- -50
21- -49
22- -48
23- -47
24- -46
25- -45
26- -44
27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43

DESCRIPTION OF EACH PIN FUNCTION

FUNCTION	PIN NUMBER	FUNCTION	PIN NUMBER
VSS	1	VDD	35
RFSHB	2	CASB	36
REFRESHB	3	RAS0B	37
MCF1	4	RAS1B	38
MCF0	5	RAS2B	39
WRB	6	MA0	40
FDCDMACKB	7	MA1	41
DACK1B	8	MA2	42
DACK3B	9	MA3	43
DMATC	10	MA4	44
FDCDMARQB	11	MA5	45
DRQ1B	12	MA6	46
DRQ3B	13	MA7	47
DBDIR	14	MA8	48
DBEN	15	A19	49
MEGAPIN	16	A18	50
OSC	17	A17	51
VSS2	18	A16	52
BREQB	19	A15	53
RESET	20	A14	54
AENA	21	A13	55
BRDY	22	A12	56
MEMWB	23	A11	57
MEMRB	24	A10	58
IOWB	25	A9	59
IORB	26	A8	60
D7	27	A7	61
D6	28	A6	62
D5	29	A5	63
D4	30	A4	64
D3	31	A3	65
D2	32	A2	66
D1	33	A1	67
D0	34	A0	68

PIN DEFINITIONS

NOTE: All negative true signals use the suffix "B".

INPUTS: (11 pins)

MCF0	Memory configuration OPTION Select.
MCF1	(See Figure 1 for details.)
RFSH	8237 CHANNEL 0 REQUEST (DREQ2) Input from timer. Set up as 16 microsec interval timer for REFRESH.
DRQ1	8237 CHANNEL 1 REQUEST (DREQ1)
FDCDMARQ	8237 CHANNEL 2 REQUEST (DREQ2) dedicated to FDC.
DRQ3	8237 CHANNEL 3 REQUEST (DREQ3)
READY	System READY signal for DMA.
RESET	System hardware master RESET.
OSC	Memory timing clock. Currently CLK14M.
AEN	CPU Bus Grant (8237 HLDA)
TEST	Input for TEST mode used by IC mfg.

BI-DIRECTIONAL: (32 pins)

BUSA19-BUSA16	System Segment Address (CPU BUS MASTER- INPUT, DMA BUS MASTER- OUTPUT)
BUSA15-BUSA0	System Address (CPU BUS MASTER- INPUT, DMA BUS MASTER- OUTPUT)
D00-D07	System Data Bus (WRITE-OUTPUT, READ- INPUT)
MRB	System Memory Read strobe (CPU BUS MASTER- INPUT, DMA BUS MASTER- OUTPUT)
MWB	System Memory Write strobe (CPU BUS MASTER- INPUT, DMA BUS MASTER- OUTPUT)
IRB	System Memory Read strobe (CPU BUS MASTER- INPUT, DMA BUS MASTER- OUTPUT)
IWB	System Memory Write strobe (CPU BUS MASTER- INPUT, DMA BUS MASTER- OUTPUT)

OUTPUTS: (20 pins)

MA00-MA08	External Memory multiplexed address
RAS0B-RAS2B	External Memory ROW strobes.
CASB	External Memory COLUMN strobe.
WRB	External Memory WRITE strobe.
DBDIR	Data Buffer directional control (Read=1).
DBENB	Data Buffer enable.
REFRESHB	8237 CHANNEL 0 ACKNOWLEDGE (DREQ0) Acknowledge from DMA channel 0 setup for refresh.
DACK1B	8237 CHANNEL 1 ACKNOWLEDGE (DREQ1)
FDCDMACKB	8237 CHANNEL 2 ACKNOWLEDGE (DREQ2)
DACK3B	8237 CHANNEL 3 ACKNOWLEDGE (DREQ3)
DMATC	8237 EOP (output only)
BREQB	CPU Bus Request (8237 HRQ)

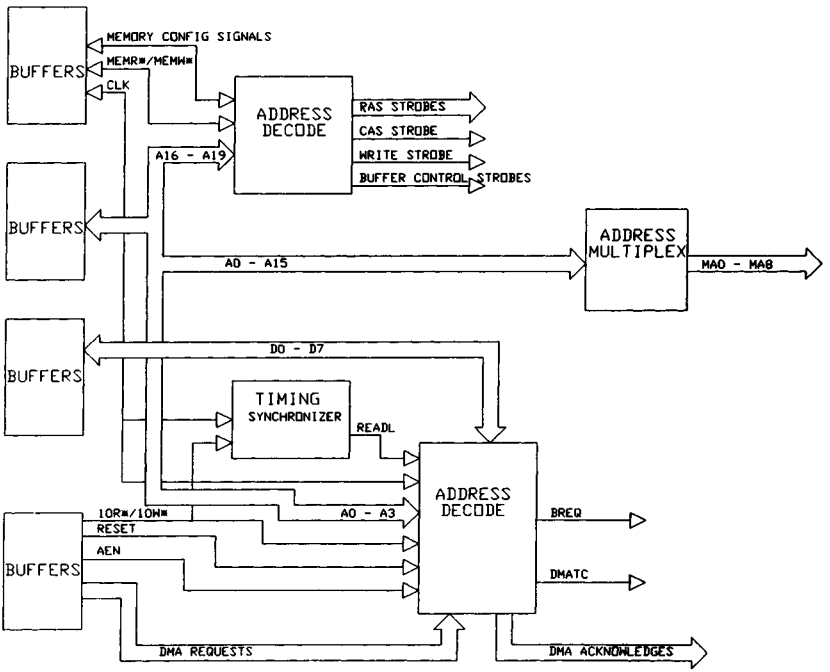
POWER: (4 pins)

VDD	+5 VDC
VSS	GND

TOTAL PIN COUNT = 68

PIN SENSE	DMA PINOUT	8237 PINOUT
BIDIR	A0	A0
BIDIR	A1 (BIDIR ENA = DMAAEN)	A1 (BIDIR ENA =8237 CNTL)
BIDIR	A2	A2
BIDIR	A3	A3
TSFBAK	A4	A4
TSFBAK	A5 (TS ENA = DMAAEN)	A5 (TS ENA = LOGIC 1)
TSFBAK	A6	A6
TSFBAK	A7	A7
TSFBAK	A8	
TSFBAK	A9	
TSFBAK	A10	
TSFBAK	A11	
TSFBAK	A12	
TSFBAK	A13	
TSFBAK	A14	
TSFBAK	A15	
TSFBAK	A16	
TSFBAK	A17	
TSFBAK	A18	
TSFBAK	A19	

PIN SENSE	DMA PINOUT	8237 PINOUT
BIDIR	D0	D0
BIDIR	D1	D1
BIDIR	D2	D2
BIDIR	D3	D3
BIDIR	D4	D4
BIDIR	D5	D5
BIDIR	D6	D6
BIDIR	D7	D7
OUTPUT	MAD0	
OUTPUT	MAD1	
OUTPUT	MAD2	
OUTPUT	MAD3	
OUTPUT	MAD4	
OUTPUT	MAD5	
OUTPUT	MAD6	
OUTPUT	MAD7	
TRISTATE	MAD8	
INPUT	RESET	RESET
INPUT	READY	RDY (MUXED)
OUTPUT	DMATC	EOP* (INVERTED)
OUTPUT	BREQ*	HRQ (INVERTED)
INPUT	OSC	CLK (MUXED)
INPUT	DRQ3	DREQ3
INPUT	FDCDMARQ*	DREQ2
INPUT	DRQ1*	DREQ1
INPUT	RFSH*	DREQ0 (MUXED)
OUTPUT	REFRESH*	DACK0
OUTPUT	DACK1*	DACK1
OUTPUT	FDCDMACK*	DACK2
OUTPUT	DACK3*	DACK3
OUTPUT	RAS0	
OUTPUT	RAS1	
OUTPUT	RAS2	
OUTPUT	CAS	AS (MUXED)
OUTPUT	WR*	AEN (MUXED)
INPUT	MCF1	CS (MUXED)
INPUT	MCF0	
OUTPUT	DBDIR	
OUTPUT	DBEN	
INPUT	AEN (SYSTEM)	HLDA
BIDIR	MEMW* -	MW* -
BIDIR	MEMR* | (BIDIR ENA	MR* | (BIDIR ENA
BIDIR	IOW* | = DMAAEN)	IOW* |- =8237 CNTL)
BIDIR	IOR* -	IOR* -
POWER	VDD	VDD
POWER	VDD	VDD
GROUND	VSS	VSS
GROUND	VSS	
	68 PINS	40 PINS



LOGIC BLOCK DIAGRAM

ELECTRICAL SPECIFICATIONS - DMA

ELECTRICAL PARAMETERS

ABSOLUTE MAX RATINGS (NON-OPERATING, VSS=0.0V)

	MIN	MAX	UNITS
STORAGE TEMPERATURE	-65	+150	DEGREES C.
VOLTAGE ON ANY PIN W.R.T.GROUND	-0.5	7.0	VOLTS

OPERATING ELECTRICAL SPECIFICATIONS:

OPERATING AMBIENT	MIN	TYP	MAX	UNITS
AIR TEMP. RANGE	0	25	70	DEGREES C
POWER SUPPLIES				
VDD	4.5	5.0	5.5	VOLTS
VSS	0	0	0	VOLTS
ICC			100	MILLIAMPS

NOTE: INCLUDE ALL RELEVENT CONDITIONS UNDER WHICH ICC IS TO BE MEASURED; IE, ALL INPUTS AT VSS OR VCC, CLOCK FREQUENCY, ETC.

TOTAL POWER DISSIPATION (Include output loading)			700	MILLIWATTS

LEAKAGE CURRENT	MIN	TYP	MAX
Vin = 0.0 v		20	microamps
Vin = 5.0 v		-20	microamps

INPUT VOLTAGES			
LOGIC "0" (Vil)		0.8	volts
LOGIC "1" (Vih)	2.0		volts

OUTPUT VOLTAGES	CURRENT LOADING	MIN	TYP	MAX	UNITS
LOGIC "0" (Vol) @ 4.0 MA LOAD				0.4	volts
LOGIC "1" (Voh) @ 0.4 MA LOAD		2.4			volts

INPUT CAPACITANCE	MIN	TYP	MAX
All inputs 0.0 < Vin < 5.0	10	picofarads	

OUTPUT CAPACITANCE			
All outputs Except Data (bi-directional)	50	picofarads	

BI-DIRECTIONAL CAPACITANCE

SEE NOTES 3-6 IN THE FOLLOWING SECTION.

TIMING SPECIFICATION

MAXIMUM LOADING FOR EACH OUTPUT

Capacitive Load:50pf
Current Load: Ioh = 4.0 MA
Iol = 0.4 MA

INPUT/OUTPUT TIMING

(NOTE: ALL AC TESTING AND TIMING MEASUREMENTS WILL BE AT THE FOLLOWING CONDITIONS: VOH (OUTPUT 1 LEVEL) = 2.0V, AND VOL (OUTPUT 0 LEVEL) = .8V)

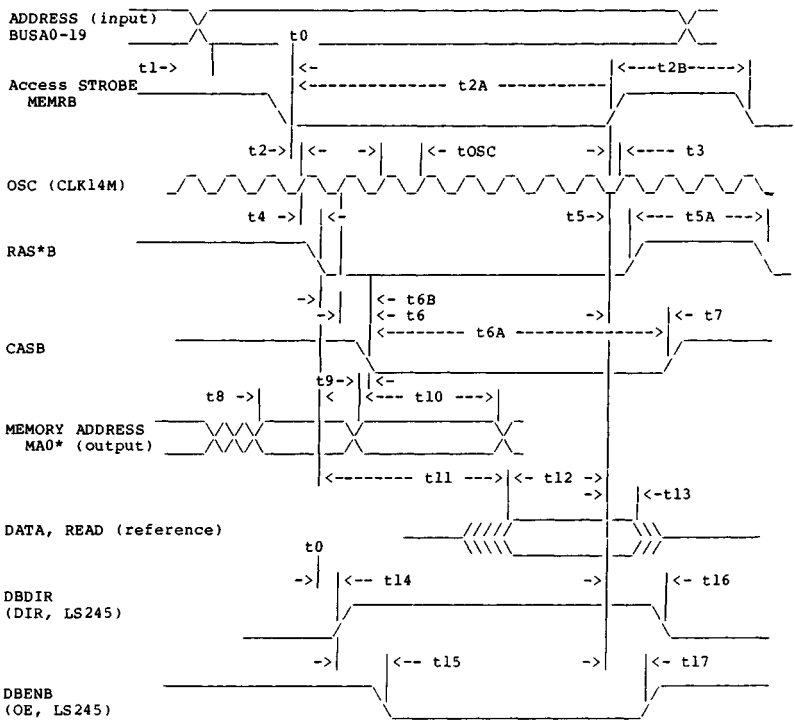


Figure 1. MEMORY TIMING PARAMETERS, READ

MEMORY TIMING PARAMETERS , READ

	min	typ	max	
t0 Reference time zero, STROBE lo tOSC Period of 14.31818 MHz		69.8		
t1 ADDRESS Setup to STROBE lo	50			
t2 STROBE lo Setup to OSC hi	15			
t2A STROBE lo Length		250		
t2B STROBE hi Length		250		
t3 STROBE hi Setup to OSC hi	don't care			
t4 RAS*B lo Delay from OSC hi	0		40	
t5 RAS*B hi Delay from STROBE hi	0		40	
t5A RAS*B hi Length	100			
t6 CAS*B lo Delay from OSC hi	0		40	
t6A CAS*B lo Length	75			
t6B CAS*B lo Delay from RAS*B lo		69.8	70	
t7 CAS*B hi Delay from STROBE hi		69.8	70	
t8 MA*-Row Address Valid Setup to RAS*B lo	20			NOTE 2
t9 MA*-Column Address Valid Setup to CAS*B lo	20			NOTE 2
t10 MA*-Column Address Hold	35			
t11 DATA Valid Delay from RAS*B True (reference)		150		NOTE 6
t12 DATA Valid Setup to STROBE hi	70			NOTE 3
t13 DATA Hold from STROBE False hi	0			
t14 DBDIR lo Delay from STROBE lo			40	
t15 DBENB lo Delay after DBDIR hi		70		NOTE 4
t16 DBENB Hold from STROBE hi	0			
t17 DBDIR Hold from DBENB hi	0			NOTE 5

NOTE 1 Setup time t2 will be defined by the ASIC design. It should be of sufficient length to allow Clear on RAS flip-flop to go false and still meet setup time before next clock rising edge.

NOTE 2 Address outputs are loaded with 3 row x 8 DRAMS = 24 x 8 pf = 192 pf. each.

NOTE 3 Additional delay through LS245 needs to be added to match Bus Specs.
Bus requires +75 ns setup. LS245 into 45pf requires 20 ns. Therefore 75+20=95 ns.

NOTE 4 Applying the DIRection signal to the LS245 and allowing the part to settle before applying OUTput ENable reduces Bus and power noise. Also OUTput ENable should be removed first.

NOTE 5 OUTput ENable should be removed first before changing DIRection.

NOTE 6 Depends upon DRAM used.

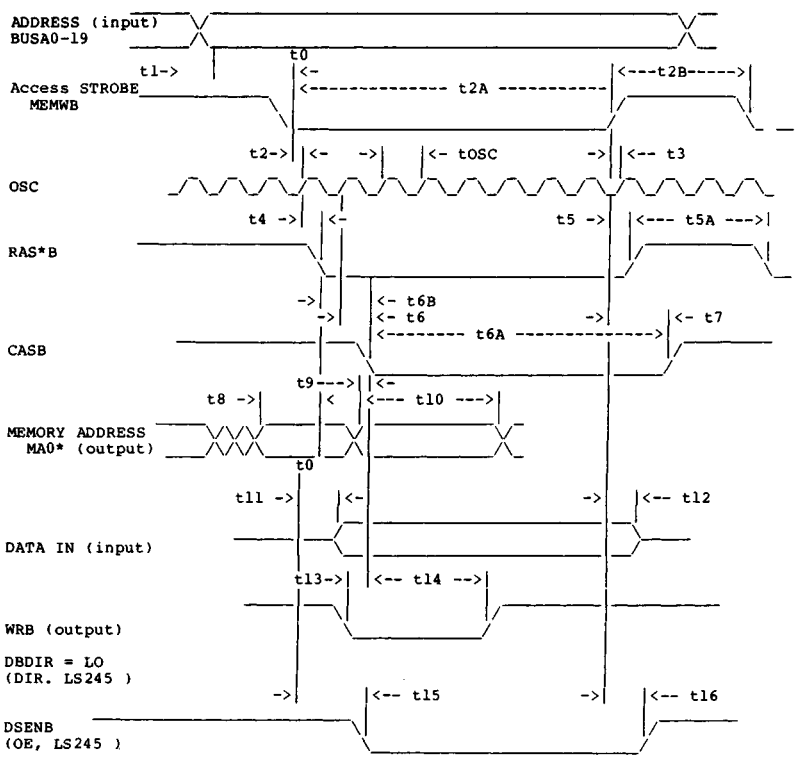


Figure 2. MEMORY TIMING PARAMETERS, WRITE

MEMORY TIMING PARAMETERS, WRITE

	min	typ	max	
t1 thru t10, see MEMORY TIMING PARAMETERS, READ				
t11 DATA Valid Delay after STROBE lo			50	NOTE 1 [1]
t12 DATA Valid Hold after STROBE hi	20			{2}
t13 WRB lo Setup to CASB lo	30			(3)
t14 WRB lo Hold after CASB lo	70			(3)
t15 DBENB lo Delay after STROBE lo		70		[1]
t16 DBENB Hold from STROBE hi	0			[1]

NOTE 1 For CPU generated MEMWB, data will appear about the same time as the STROBE, but for DMA generated MEMWB, data will appear before MEMWB.

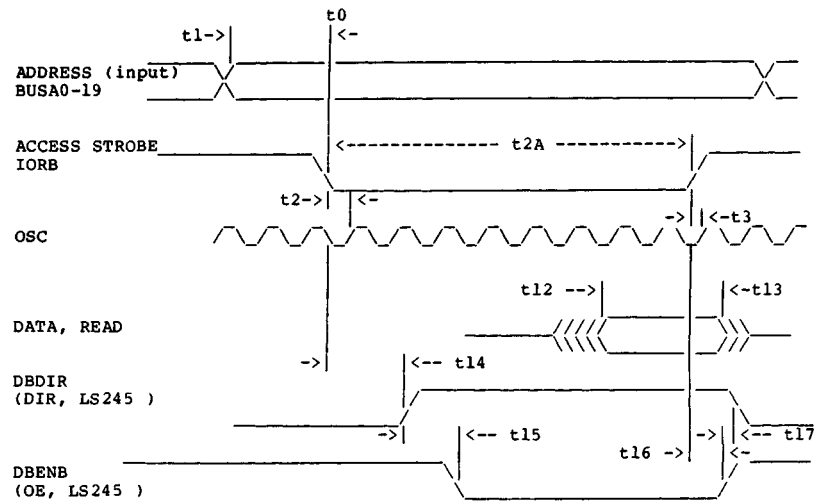


Figure 3. I/O CHIP SELECT PARAMETERS, READ

I/O CHIP SELECT PARAMETERS, READ

	min	typ	max	
t1 ADDRESS Valid Setup to STROBE lo	50			
t2 STROBE lo Setup to OSC hi	15			
t2A STROBE lo Length	420			
t3 STROBE hi Setup to OSC hi	20			
t12 DATA Valid Setup to STROBE hi	90			
t13 DATA Hold from STROBE hi	0			
t14 DBDIR hi Delay from STROBE lo			70	
t15 DBENB lo Delay after DBDIR hi		70		NOTE 1
t16 DBENB Hold from STROBE hi	0			
t17 DBDIR Hold after DBENB hi	0			NOTE 1

NOTE 1 ENable should be removed first before changing DIRection.

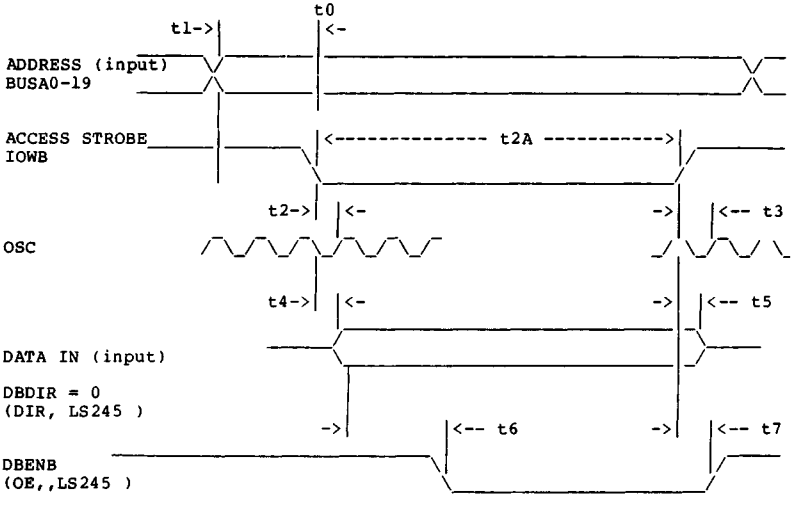


Figure 4. I/O CHIP SELECT PARAMETERS, WRITE

I/O CHIP SELECT PARAMETERS, WRITE

		min	typ	max
t1	ADDRESS Valid Setup to STROBE lo	50		
t2	STROBE lo Setup to OSC hi	15		
t2A	STROBE lo Length	420		
t3	STROBE hi Setup to OSC hi	20		
t4	DATA Valid Setup to STROBE lo		0	
t5	DATA Hold from STROBE hi	0		
t6	DBENB Delay after STROBE lo			70
t7	DBENB Hold from STROBE hi	0		

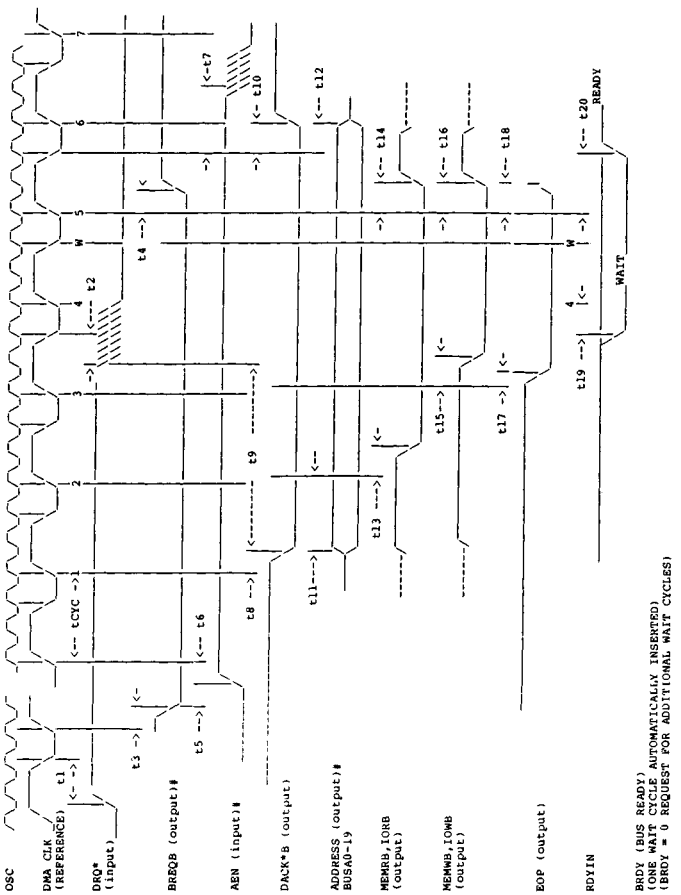


Figure 5. DMA BUS MASTER TIMING, READ / WRITE

DMA BUS MASTER TIMING, READ / WRITE

	min	typ	max	
t1 DRQ* True Setup to CLK lo	30			
t2 DRQ* False Setup to CLK lo	30			
t3 BREQB True Delay from CLK hi			120	8237A-5 tDQl
t4 BREQB False Delay from CLK hi			120	8237A-5 tDQl
t5 AEN True Delay after BREQB True	N x tCYC		+30	N =
t6 AEN True Setup to CLK Hi			40	
t7 AEN False delay from CLK hi			40	
t8 DACK*B True Delay from CLK lo			170	8237A-5 tAK
t9 DACK*B True Hold from AEN True	0			8237A-5 NOTE 6
t10 DACK*B False delay from CLK lo			170	8237A-5 tAK
t11 ADDRESS Valid Setup to CLK Hi	50			System Spec
t12 ADDRESS False delay from CLK hi	0			
t12 MEMRB or IORB True Delay from CLK hi			40	
t13 MEMRB or IORB False Delay after CLK hi			40	
t14 MEMWB or IOWB True Delay from CLK hi			40	
t15 MEMWB or IOWB False Delay after CLK hi			40	
t16 EOP True Delay after CLK hi			40	
t17 EOP False Delay after CLK hi			40	
t18 BRDY False Setup to CLK hi	30			
t19 BRDY False Hold after CLK hi	30			

Printer Interface Chip Specification

Printer Interface Chip Specification
Contents

PRINTER INTERFACE SPECIFICATION
TANDY PART # 8075068
APRIL 30, 1986

1. GENERAL DESCRIPTION

1.1 The Tandy part# 8075068 - Printer Interface I.C provides the interface between the system I/O bus and the printer. Figure 1 shows Block diagram of Printer Interface chip. Figure 2 shows pin configurations of Printer interface chip.

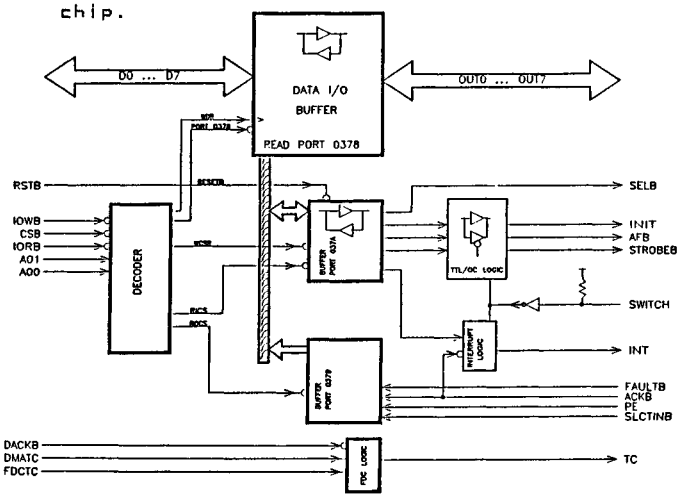


Figure 1.

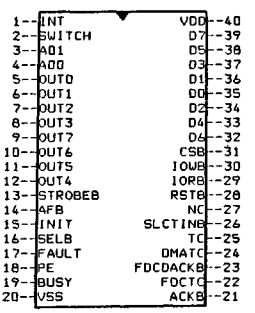


Figure 2.

1.2 DESCRIPTION OF EACH PINS:

Pin#	Pin Name	Type	Description
1	INT	output	Interrupt signal
2	SWITCH	input	Switch for totem pole output or open collector output on INITB, AF, STROBEB.
3	A01	input	CPU address line
4	A00	input	CPU address line
5	OUT0	input/output	Data I/O line
6	OUT1	input/output	Data I/O line
7	OUT2	input/output	Data I/O line
8	OUT3	input/output	Data I/O line
9	OUT7	input/output	Data I/O line
10	OUT6	input/output	Data I/O line
11	OUT5	input/output	Data I/O line
12	OUT4	input/output	Data I/O line
13	STROBEB	output	Printer Strobe signal
14	AFB	output	Printer Autofeed signal
15	INITB	output	Printer Initialize signal
16	SEL	output	Printer Select signal
17	FAULTB	input	Printer Fault signal
18	PE	input	Printer Paper empty signal
19	BUSY	input	Printer Busy signal
20	VSS	ground	Ground
21	ACKB	input	Printer Acknowledge signal
22	FDCTC	input	FDC Terminal Count
23	FDCDACKB	input	FDC-DMA Acknowledge signal
24	DMATC	input	DMA Terminal Count
25	TC	output	FDC Terminal Count signal
26	SLCTINB	input	Printer Select input
27	NC	--	Not used
28	RSTB	input	System Reset
29	IORB	input	CPU I/O Read strobe
30	IOWB	input	CPU I/O Write strobe
31	CSB	input	Chip select signal
32	D6	Input/output	CPU Data I/O
33	D4	Input/output	CPU Data I/O
34	D2	Input/output	CPU Data I/O
35	D0	Input/output	CPU Data I/O
36	D1	Input/output	CPU Data I/O
37	D3	Input/output	CPU Data I/O
38	D5	Input/output	CPU Data I/O
39	D7	Input/output	CPU Data I/O
40	VDD	power	+5 Volt Power Supply

2. ENVIRONMENTAL SPECIFICATIONS

2.1 Storage Temperature -65 C to 150 C
2.2 Operating Temperature 0 C to 70 C

3. ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Rating

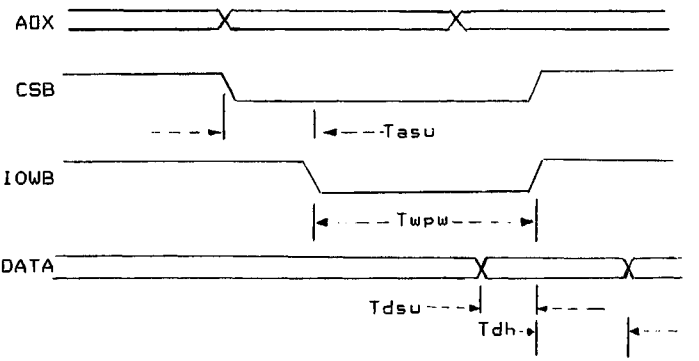
Parameter	Min.	Typ.	Max.	Units	Cond.
Voltage, any pin	-1.0		7.0	Volts	W.R.T ground
Power Dissipation			0.5	Watts	

3.2 D.C. Electrical Characteristics

Symb.	Parameter	Min.	Typ.	Max.	Units	Cond.
VDD	Supply Voltage	4.5	5.0	5.5	Volts	
Icc(q)	Quiescent current			50	uA	
Icc(o)	Operating Current			40	mA	
Vil	Input Low Voltage			0.8	Volts	TTL inputs
Vih	Input High Voltage	2.0			Volts	TTL inputs
Iin	Input Leakage	-10		10	uA	
Cin	Input Capacitance			7	pF	
Vol	Output Low Voltage			0.4	Volts	@4 mA
Voh	Output High Voltage	2.4			Volts	@-2 mA
Ioz	High Impedance Leak	-10		10	uA	

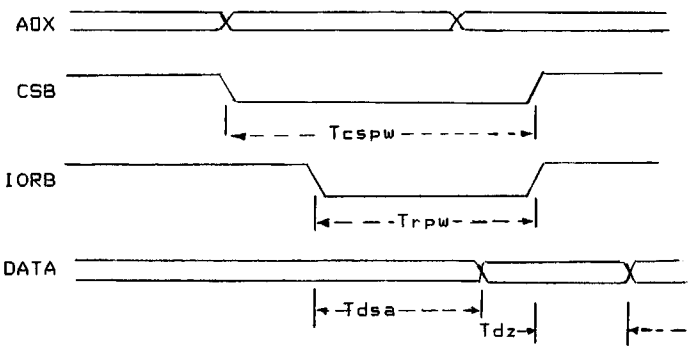
3.3 A.C Electrical Characteristics

3.3.1 Write Cycle



Symb.	Parameter	Min.	Typ.	Max.	Units	Cond.
Tasu	Address Setup	15			nS	
Twpw	Write Pulse Width	69			nS	
Tdsu	Data Setup	29			nS	
Tdh	Data Hold	6			nS	

3.3.2 Read Cycle



Symb.	Parameter	Min.	Typ.	Max.	Units	Cond.
Tcspw	Chip Select Width	69			nS	
Trpw	Read Pulse Width	69			nS	
Tda	Data Access			69	nS	
Tdz	Bus Hold/release	6		25	ns	

Timing Control Generator Chip Specification

Timing Control Generator Chip Specification
Contents

TIMING CONTROL GENERATOR
TANDY PART # 8075306
MAY 07, 1986
REV 050886

1.0 GENERAL DESCRIPTION

1.1 The Tandy part # 8075306 - Timing Control Generator:
- creates eight clock outputs from two independent oscillator inputs.
- synchronizes the ready signals.
- synthesizes the system control strobes from the CPU status signals.
- interfaces the system signals (HOLD, HLDA) with the CPU signals (RQ/GT).
- creates two FDC chip selects and the DMA request delay.

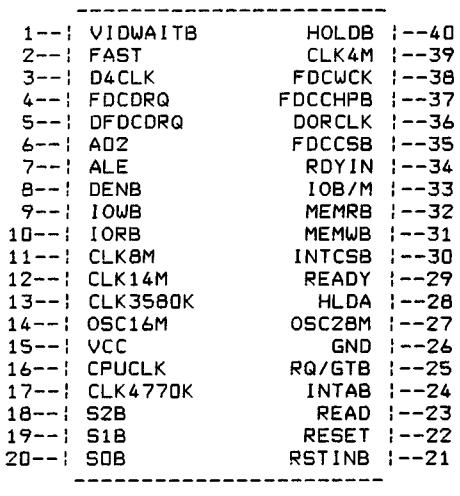
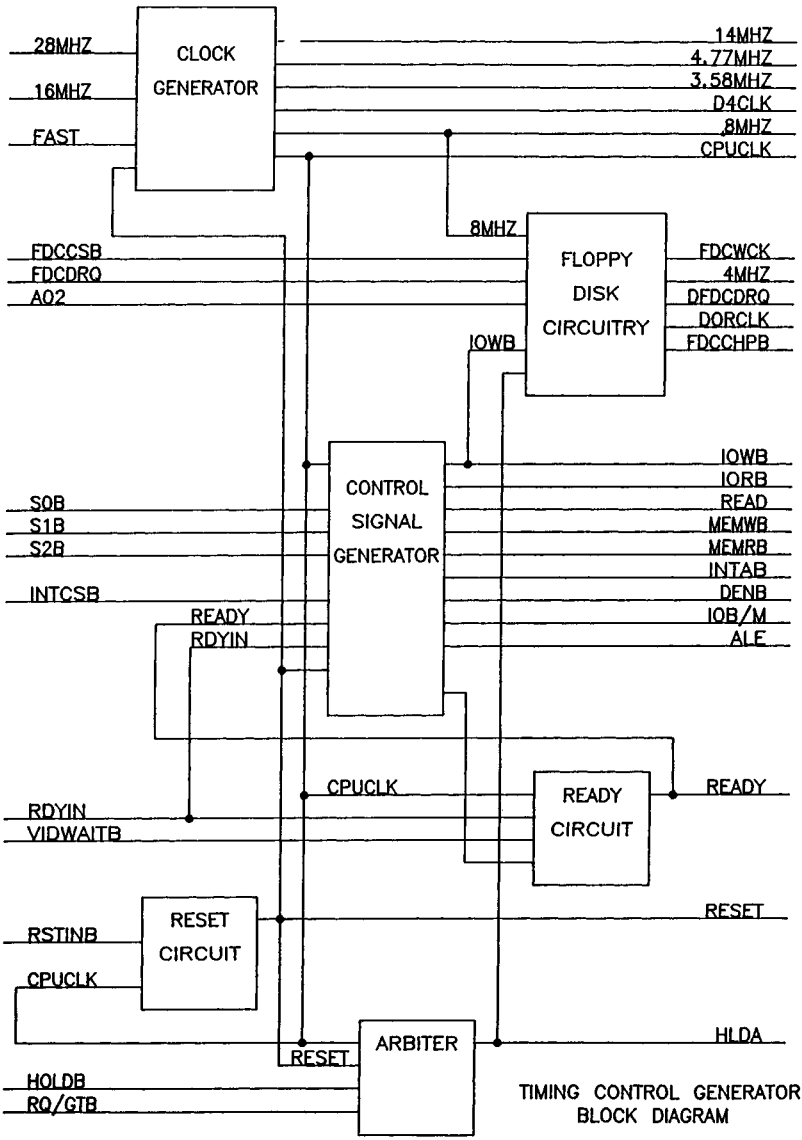


Figure 1. Pin Assignment

1.2 DESCRIPTION OF PINS:

Pin #	Pin Name	Type	Description
1	VIDWAITB	INPUT	Wait signal from video system (0 = Wait)
2	FAST	INPUT	Clock speed select
3	D4CLK	OUTPUT	CLK477M/4, Squarewave
4	FDCDRQ	INPUT	FDC DMA Request
5	DFDCDRQ	OUTPUT	Beginning of FDCDRQ delayed 1.0 microsec
6	A02	INPUT	System Address
7	ALE	OUTPUT	Address Latch Enable
8	DENB	OUTPUT	Data Enable
9	IOWB	OUTPUT	I/O Write
10	IORB	OUTPUT	I/O Read
11	CLK8M	OUTPUT	OSC16M/2, Squarewave
12	CLK14M	OUTPUT	OSC28M/2, Squarewave
13	CLK3580K	OUTPUT	OSC28M/8, Squarewave
14	OSC16M	INPUT	Input Frequency = 16.00000 MHz
15	VDD	POWER	
16	CPUCLK	OUTPUT	FAST=1, CPUCLK=7.16MHz (OSC28M/4, 50-50 cycle) FAST=0, CPUCLK=4.77MHz (OSC28M/6, 33-67 cycle)
17	CLK4770K	OUTPUT	CLK14M/3, 33% duty cycle
18	S2B	INPUT	8088 Status Signal
19	S1B	INPUT	8088 Status Signal
20	S0B	INPUT	8088 Status Signal
21	RSTINB	INPUT	Asynchronous system input
22	RESET	OUTPUT	8088 CPU Reset input
23	READ	OUTPUT	Directional Control for CPU Data buffer
24	INTAB	OUTPUT	Interrupt Acknowledge
25	RQ/GTB	INPUT/OUTPUT	Request/Acknowledge/Release
26	VSS	GROUND	
27	OSC28M	INPUT	Input frequency = 28.63636 MHz
28	HLDA	OUTPUT	Bus Acknowledge
29	READY	OUTPUT	8088 CPU READY input
30	INTCSB	INPUT	8257 Interrupt Controller Chip Select
31	MEMWB	OUTPUT	Memory Write
32	MEMRB	OUTPUT	Memory Read
33	IOB/M	OUTPUT	1 = Memory access, 0 = I/O access
34	RDYIN	INPUT	Asynchronous system input (0 = Wait condition)
35	FDCCSB	INPUT	Previously decoded FDC Function I/O chip select
36	DORCLK	OUTPUT	Configuration register Chip Select
37	FDCCHPB	OUTPUT	FDC Chip Select
38	FDCWCK	OUTPUT	Pulse, Period = 2 microsec, 250(nom) pulse
39	CLK4M	OUTPUT	OSC16M/4, Squarewave
40	HOLDB	INPUT	Bus Request



TIMING CONTROL GENERATOR BLOCK DIAGRAM

2.0 ENVIRONMENTAL SPECIFICATIONS

2.1 Storage Temperature: -65 min, +150 max degrees C
2.2 Operating temperature: 0 min, +25 typ, + 70 max degrees C

3.0 ELECTRICAL SPECIFICATIONS

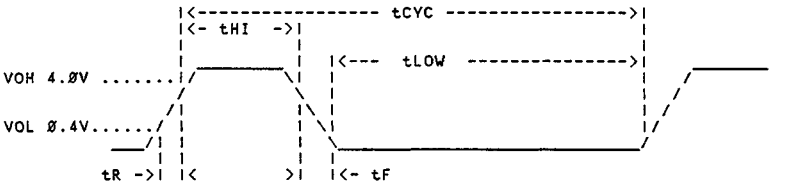
3.1 Absolute Maximum Rating:
Voltage on any pin w.r.t. Ground: -0.5 min, 7.0 max volts

3.2 Operating Electrical Specifications:

	min	typ	max	units
3.2.1 Operating Ambient:				
Air Temp. Range	0	25	70	degrees C
3.2.2 Power Supplies:				
VDD	4.5	5.0	5.5	volts
VSS	0	0	0	volts
ICC			100	milliamps
Total Power			700	milliwatts
3.2.3 Leakage Current, All Inputs:				
Vin = 0.0 v			-10	microamps
Vin = 5.0 v			+10	microamps
3.2.4 Input voltages:				
Logic "0"			.8	volts
Except RSTIN			.5	volts
Logic "1"	2.0			volts
Except RSTIN	3.5			volts
3.2.5 Output Voltages:				
logic "0" @ 4.0 mA load			.4	volts
logic "1" @ 4.0 mA load	2.4			volts
except all clocks	4.0			volts
3.2.6 INPUT CAPACITANCE (0.0 < Vin < 5.0)				
All inputs			10	pf
3.2.7 OUTPUT CAPACITANCE				
All loads			50	pf

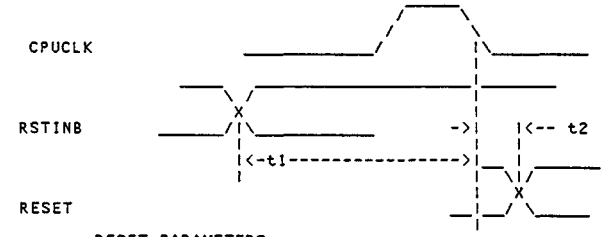
TIMING DIAGRAMS

FIGURE 1. CPUCLK



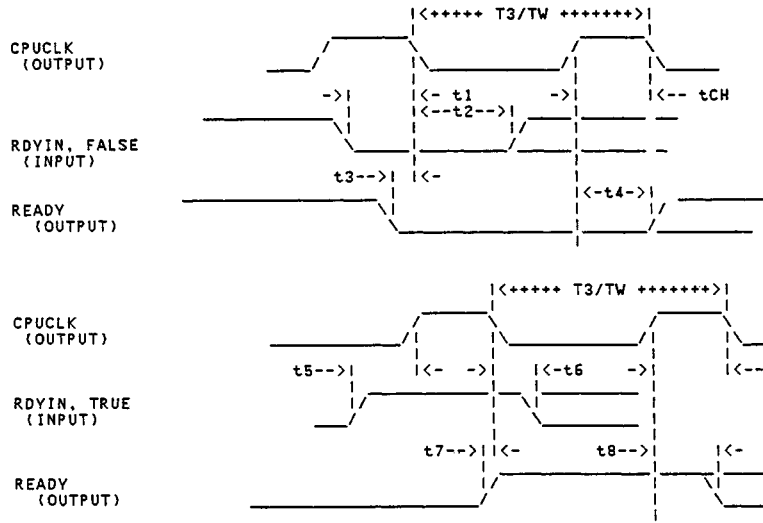
CLOCK PARAMETER		7.16 MHZ			4.77MHZ			
		min	typ	max	min	typ	max	
tHI	Level at least 4.Øv	44	(69.5-tR-tF)		69	69.5		ns
tLOW	Level not greater than Ø.4v	68	69.5		118	(14Ø-tR-tF)		ns
tR	Rise time , Ø.4 to 4.Øv			8			1Ø	ns
tF	fall time , 4.Ø to Ø.4v			7			1Ø	ns
tCYC			14Ø			21Ø		ns

FIGURE 2. RESET



RESET PARAMETERS	
t1 RSTIN Setup to CPUCLK low	Asynchronous input
t2 RESET Delay from CPUCLK low	4Ø ns max

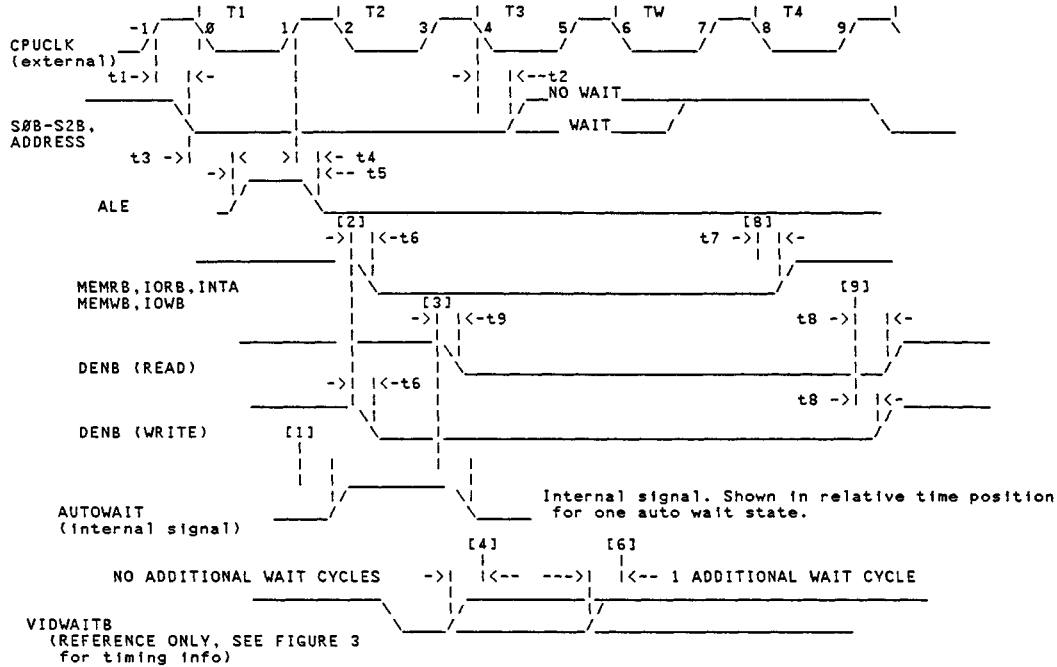
FIGURE 3. READY



READY PARAMETER

	min	max		
t1 RDYIN False Setup to CPUCLK low	35		ns	
t2 RDYIN False Hold after CPUCLK low	10		ns	
t3 READY False before CPUCLK low	-8		ns	tRYLCL 8088
t4 READY False Hold after CPUCLK hi		tCH + 8	ns	tCHRYX 8088
t5 RDYIN True Setup to CPUCLK hi	35		ns	
t6 RDYIN True Hold after CPUCLK low	10		ns	
t7 READY True before CPUCLK low	0		ns	tRYHCH 8088
t8 READY True Hold after CPUCLK hi		tCH + 8	ns	tCHRYX 8088

FIGURE 4. CONTROL GENERATOR



CONTROL GENERATOR

	min	max		
t1 STATUS Active Delay from CLK hi	1Ø	6Ø	ns	tCHSV 8Ø88
t2 STATUS Inactive Delay from CLK low	1Ø	7Ø	ns	tCLSH 8Ø88
t3 ALE True Delay from Status Active		2Ø	ns	tSVLH 8288

t4 ALE False Delay from CLK hi		2Ø	ns
t5 ALE Pulse Width	55		ns
t6 STROBE True Delay from CLK low		3Ø	ns
t7 STROBE False Delay from CLK low		3Ø	ns
t8 STROBE False Delay from CLK hi		3Ø	ns
t9 STROBE True Delay from Clk hi		3Ø	ns

FIGURE 5A. ARBITTER/REQUEST

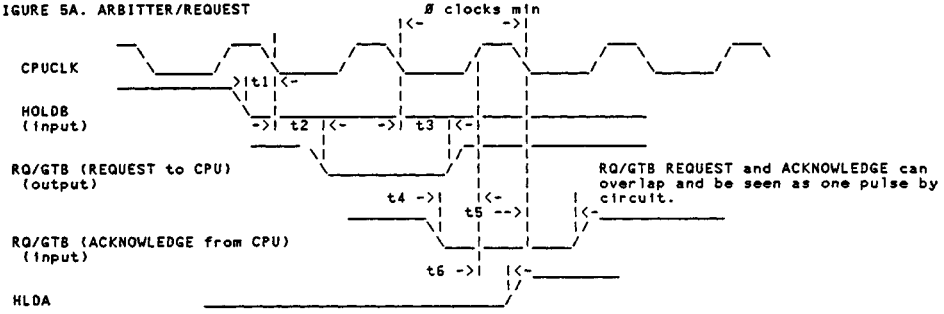
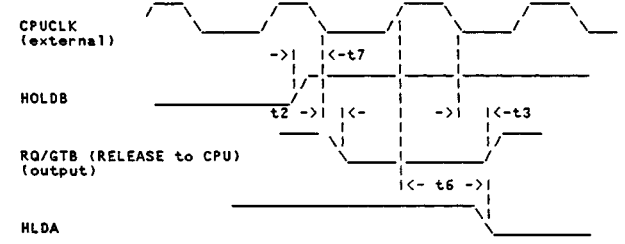


FIGURE 5B. ARBITTER/RELEASE

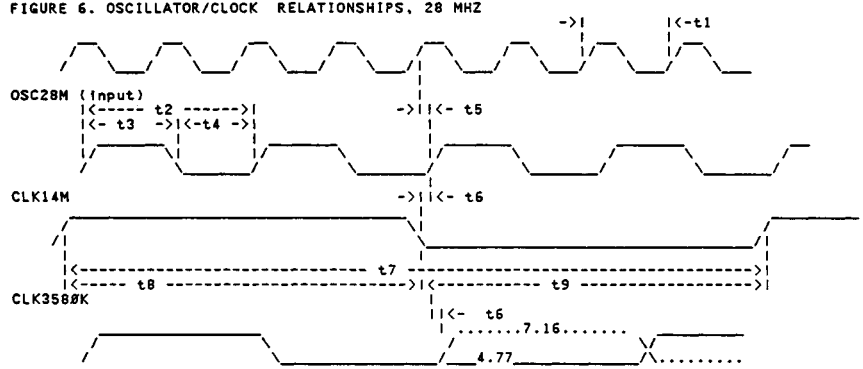


ABRITTER PARAMETER

	min	max		
t1 HOLDB (True) setup to CPUCLK low	2Ø		ns	
t2 CPUCLK low to RQ/GTB active (REQ/REL pulse)		5Ø	ns	tGVCH 8Ø88

t3 CPUCLK low to RQ/GTB inactive (REQ/REL pulse)		5Ø	ns	tCHGX 8Ø88
t4 RQ/GTB (True) setup to CPUCLK hi (ACK pulse)	2Ø		ns	tCLGL 8Ø88
t5 RQ/GTB (False) hold from CPUCLK low (ACK pulse)		5Ø	ns	tCLGH 8Ø88
t6 CPUCLK hi to HLDA Delay		3Ø	ns	
t7 HOLDB (False) Setup to CPUCLK low	2Ø		ns	

FIGURE 6. OSCILLATOR/CLOCK RELATIONSHIPS, 28 MHZ



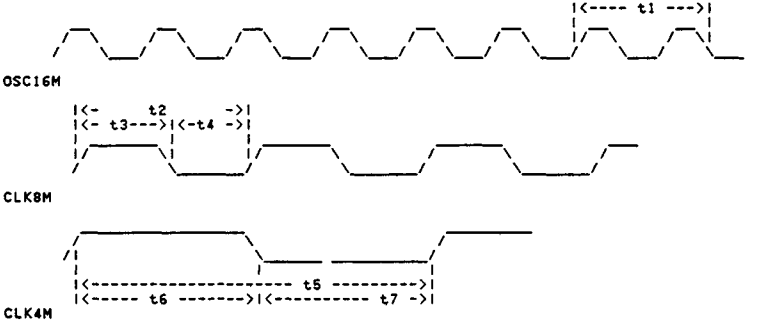
CPUCLK (See Fig. 1 for Specs)

CLOCK PARAMETER	min	typ	max	
t1 OSC28M Period		34.9		NOTE 1
t2 CLK14M Period		t1 x 2		
t3 CLK14M high (includes tRISE)	-1Ø%	t2/2	+1Ø%	
t4 CLK14M low (includes tFALL)		(t2-t3)		
t5 OSC28M to CLK*M Output Delay skew		15		
t6 CLK*M to CLK*M Output Delay skew		15		
t7 CLK358ØK Period		t1 x 8		
t8 CLK358ØK high (includes tRISE)	-1Ø%	t7/2	+1Ø%	

t9 CLK3580K low (includes tFALL)	(t7-t8)	
tR CLK*M		10 ns
tF CLK*M		10 ns

NOTE 1 Use only one edge because the oscillator duty cycle symmetery can not be specified.
NOTE 2 Phase Relationship is important between the CLK14M clock and the outputs it generates.

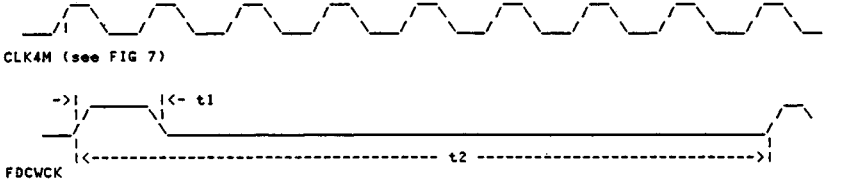
FIGURE 7. OSCILLATOR/CLOCK RELATIONSHIPS, 8MHZ



CLOCK PARAMETER	min	typ	max
t1 OSC16M Period		62.5	
t2 CLK8M Period		t1 x 2	
t3 CLK8M High (includes tRISE)	-10%	t2/2	+10%
t4 CLK8M Low (includes tFALL)		t2-t3	
t5 CLK4M Period		t1 x 4	
t6 CLK4M High (includes tRISE)	-10%	t5/2	+10%
t7 CLK4M Low (includes tFALL)		t5-t6	

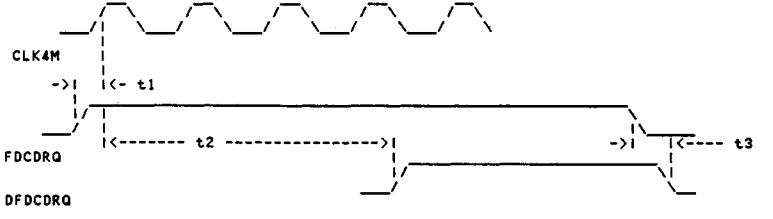
tR		10 ns
tF		10 ns

FIGURE 8. FDCCLK/FDWCK RELATIONSHIPS



CLOCK PARAMETER	min	typ	max	
t1 FDCWCK High (includes tRISE)		250		ns
t2 FDCWCK Period		2.0		us

FIGURE 9. CLK4M/FDDMAREQ RELATIONSHIPS



CLOCK PARAMETER	min	typ	max	
t1 FDCDRQ Setup to CLK4M	2Ø		ns	Asynchronous
t2 DFDCDRQ Delay TRUE	.75 us	1.Ø us	1.1 us	
t3 FDCDRQ False to DFDCDRQ False Delay			3Ø ns	

Video Controller Chip Specification

Video Controller Chip Specification
Contents

VIDEO CONTROLLER CHIP SPECIFICATION

GENERAL DESCRIPTION

The Tandy 1000 video controller chip is designed to operate with three types of display devices: A standard TV using an RF modulator, a composite monitor, and an RGBI 200 line Color monitor. This custom controller chip implements all of the video logic for the Tandy 1000 plus most of the system decode logic. Figure 1 shows a block diagram of the controller chip.

The video display system is very flexible and can be programmed for a number of video modes. These modes use varying numbers of colors (2,4 or 16). These 16 colors are defined by combinations of the RGBI as shown in the color chart below and can be used for the foreground color or background color. If you are using a black and white monitor, these colors will appear as shades of gray. In addition, any 1 of the 16 colors or shades of gray can be used for the screen border.

I	R	G	B	Color
0	0	0	0	Black
0	0	0	1	Blue
0	0	1	0	Green
0	0	1	1	Cyan
0	1	0	0	Red
0	1	0	1	Magenta
0	1	1	0	Brown
0	1	1	1	Light Gray
1	0	0	0	Dark Gray
1	0	0	1	Light Blue
1	0	1	0	Light Green
1	0	1	1	Light Cyan
1	1	0	0	Pink
1	1	0	1	Light Magenta
1	1	1	0	Yellow
1	1	1	1	White

TABLE 1 AVAILABLE COLORS TABLE

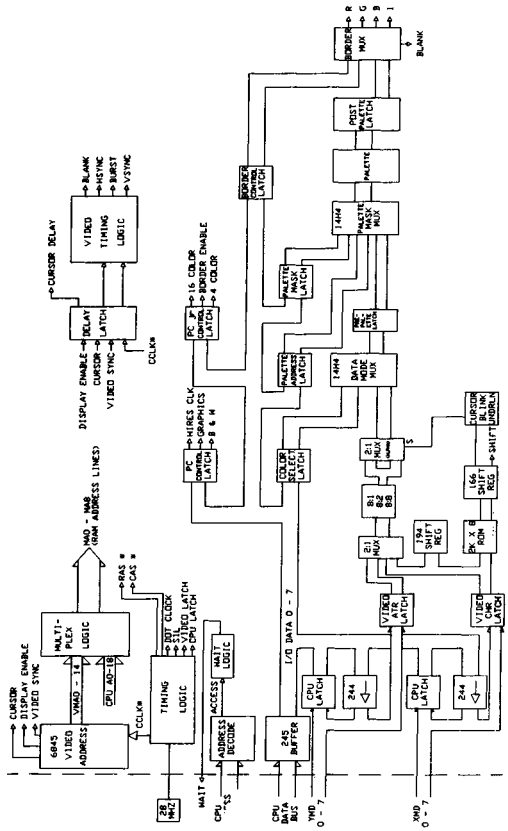


Figure 1. VIDEO CONTROLLER CHIP BLOCK DIAGRAM

OPERATING MODES

The operating modes supported by the Tandy 1000 video controller may be grouped in two categories: Alphanumeric and Graphic.

ALPHANUMERIC MODE

The Alphanumeric mode has two basic types of operation: 80 character by 25 rows, and 40 character by 25 rows. In both modes the characters are generated by a 256 character ROM. The character ROM is divided into the following groups:

* 96 Standard ASCII characters
* 48 Block Graphics characters
* 64 Foreign Language/Greek characters
* 16 Special Graphics characters.
* 32 Word Processing/Scientific Notation characters

In both modes all characters are 7 dots wide by 7 dots high and are placed in an 8 dot wide by 8 or 9 dot high matrix. In both the 40x25 and the 80x25 modes, two bytes of data are used to define each character on the screen. The even address (0,2,4 etc.) is the character code and is used in addressing the character generating ROM. The odd address (1,3,5 etc.) is the attribute byte, that defines the foreground and the background color of the character. The following chart shows how the attribute byte controls colors.

ATTRIBUTE BYTE							
7	6	5	4	3	2	1	0
Background				Foreground			
I	R	G	B	I	R	G	B
.	R	G	B	I	R	G	B

+---> =1 Selects Blinking of foreground if enabled

Table 2 ALPHANUMERIC MODE ATTRIBUTE BYTE DEFINITION

* Writing a 1 in bit 5 of register 'H3D8 enables Blinking

GRAPHICS MODE

The Tandy 1000 Video Controller chip can be programmed for a variety of modes.
The Tandy 1000 Computer family supports the following Graphics Modes:

MODE		IBM PCJR	IBM PC
4 Color Medium Resolution	320 x 200	X	X
16 Color Medium Resolution	320 x 200	X	
16 Color Low Resolution	160 x 200	X	
2 Color High Resolution	640 x 200	X	X
4 Color High Resolution	640 x 200	X	

GRAPHICS MEMORY USAGE

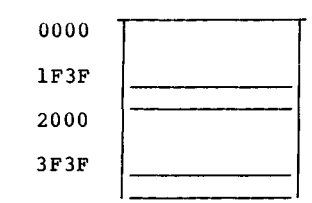
* 200 line Graphics Memory uses either 2 or 4 banks of 8000 bytes. In either case, pixel information for the display's upper left corner is found at address 0000.

```
####   The  4 Color High Resolution 640 X 200 and
####   The 16 Color Medium Resolution 320 X 200
####   use 4 banks of 8000 bytes as follows

(Hex) | <------160 Bytes------>

0000  ┌──────────────────────┐   00 Scans
      │                      │   (0,4,8,...,196)
1F3F  ├──────────────────────┤
2000  ├──────────────────────┤   01 Scans
      │                      │   (1,5,9,...,197)
3F3F  ├──────────────────────┤
4000  ├──────────────────────┤   10 Scans
      │                      │   (2,6,10,...,198)
5F3F  ├──────────────────────┤
6000  ├──────────────────────┤   11 Scans
      │                      │   (3,7,11,...,199)
7F3F  └──────────────────────┘
```

```
####   The  2 Color High Resolution 640 X 200 and
####   The  4 Color Medium Resolution 640 X 200 and
####   The 16 Color Low Resolution 640 X 200
####   use only 2 banks of 8000 bytes as follows
```



2 COLOR HIGH RESOLUTION 640 X 200 GRAPHICS MODE

The 2 Color High Resolution 640 X 200 Graphics mode may require a high resolution monitor for proper operation. Available in the IBMPC and IBM PCjr, this mode has the following characteristics:

Contains a maximum of 200 rows of 640 PELs
Can display 2 of 16 possible colors
Requires 16K bytes of read/write memory
Formats 8 PELs per byte for each byte in the following manner:

7	6	5	4	3	2	1	0
PA3	PA2	PA1	PA0	PA3	PA2	PA1	PA0
First Display PEL	Second Display PEL	Third Display PEL	Fourth Display PEL	Fifth Display PEL	Sixth Display PEL	Seventh Display PEL	Eighth Display PEL

4 COLOR HIGH RESOLUTION 640 X 200 GRAPHICS MODE

The 4 Color High Resolution 640 X 200 Graphics mode may require a high resolution monitor for proper operation. Only supported on the IBM PCjr, this mode has the following characteristics:

Contains a maximum of 200 rows of 640 PELs
Can display 4 of 16 possible colors
Each pixel selects 1 of 4 colors
Requires 32K bytes of read/write memory
Formats 8 PELs per two bytes (1 even byte and 1 odd byte) in the following manner:

EVEN BYTES

7	6	5	4	3	2	1	0
PA0	PA0	PA0	PA0	PA0	PA0	PA0	PA0
First Display PEL	Second Display PEL	Third Display PEL	Fourth Display PEL	Fifth Display PEL	Sixth Display PEL	Seventh Display PEL	Eighth Display PEL
PA1	PA1	PA1	PA1	PA1	PA1	PA1	PA1
7	6	5	4	3	2	1	0

ODD BYTES

16 COLOR MEDIUM RESOLUTION 320 X 200 GRAPHICS MODE

The 16 Color Medium Resolution 320 X 200 Graphics mode works with all types of display devices. This mode is available in the IBM PCjr only and has the following characteristics:

Contains a maximum of 200 rows of 320 PELs
Can display 16 of 16 possible colors
Each pixel selects 1 of 16 colors
Requires 32K bytes of read/write memory
Formats 2 PELs per byte in the following manner:

7	6	5	4	3	2	1	0
PA3	PA2	PA1	PA0	PA3	PA2	PA1	PA0
First Display PEL				Second Display PEL			

16 COLOR LOW RESOLUTION 160 X 200 GRAPHICS MODE

The 16 Color Low Resolution 160 X 200 Graphics mode works with all types of display devices. This mode is available in the IBM PCjr only, with the following characteristics:

Contains a maximum of 200 rows of 160 PELs
Can display 16 of 16 possible colors
Each pixel selects 1 of 16 colors
Requires 16K bytes of read/write memory
Formats 2 PELs per byte in the following manner:

7	6	5	4	3	2	1	0
PA3	PA2	PA1	PA0	PA3	PA2	PA1	PA0
First Display PEL				Second Display PEL			

4 COLOR MEDIUM RESOLUTION 320 X 200 GRAPHICS MODE

The 4 Color Medium Resolution 320 X 200 Graphics mode works with all types of display devices. It is available in the IBM PC and PCjr. This mode has the following characteristics:

Contains a maximum of 200 rows of 320 PELs
Can display 4 of 16 possible colors
Each pixel selects 1 of 4 colors
Requires 16K bytes of read/write memory
Formats 4 PELs per byte in the following manner:

7 PA1	6 PA0	5 PA1	4 PA0	3 PA1	2 PA0	1 PA1	0 PA0
First Display PEL		Second Display PEL		Third Display PEL		Fourth Display PEL	

VIDEO MEMORY MAP AND GRAPHICS USAGE

Hex Address	Register
3D0	Not Used
3D1	Not Used
3D2	Not Used
3D3	Not Used
3D4	6845 Address Register
3D5	6845 Data Register
3D6	Not Used
3D7	Not Used
3D8	Mode Select Register
3D9	Color Select Register
3DA	Video Array Address & Status
3DB	Not Used
3DC	Not Used
3DD	Extended RAM Page Register
3DE	Video Array Data
3DF	CRT Processor Page Register

VIDEO ARRAY REGISTERS

The following registers can be accessed by writing their Hex Address to 3DA and their Data to 3DE

Hex Address	Video Array Register
01	Palette Mask
02	Border Color
03	Mode Control
10-1F	Palette Registers

ARRAY PALETTE MASK REGISTER

Bit Programming

Hex Address	Array Register	7	6	5	4	3	2	1	0	Notes
01	Palette Mask	X	X	X	X					Write Only
MSK[3]	Palette Mask 3									
MSK[2]	Palette Mask 2									
MSK[1]	Palette Mask 1									
MSK[0]	Palette Mask 0									

When bits 0-3 are 0, they force the appropriate palette address to be 0 regardless of the incoming color information. This can be used to make some information in memory a 'don't care' condition until it is requested.

ARRAY BORDER COLOR

Hex Address	Array Register	7	6	5	4	3	2	1	0	Notes
02	Border Color	X	X	0	X					Write Only
	Reserved = 0									
BORI	I (Intensity) Border Color Select									
BORR	R (Red) Border Color Select									
BORG	G (Green) Border Color Select									
BORB	B (Blue) Border Color Select									
	A combination of bits 0-3 selects the screen border as one of 16 colors, as listed in Table 1 "Available Colors Table" at the beginning of this section.									

ARRAY MODE CONTROL REGISTER

Hex Address	Array Register	Bit Programming 7	6	5	4	3	2	1	0	Notes
03	Mode Control	X	X					0	X	Write Only
NVDM	Set to 1 for 640x200 secondary pixel organization									
C16COL	Set to 1 for 16 Color Modes									
C4COLHR	Set to 1 for 4 Color 640x200 Mode									
BORENB	Enables the border color register For PC compatibility, this bit should be 0. For PCjr compatibility, this bit should be 1.									
	Reserved for future implementations. Must always be set to zero.									

ARRAY PALETTE REGISTERS

There are sixteen 4 bit wide palette registers implemented by a 16x4 bit RAM. These registers are 'write' only; they cannot be 'read'. Their address in the Video Array are from hex 10 to 1F. They can be used to redefine any color.

To load the palette, write the hex address to the Video Array register at 3DA. Then, the new palette color is written to 3DE.

Palette address hex 10 is accessed whenever the color code from memory is a hex 0, address hex 11 is accessed whenever the color code from memory is a hex 1, and so forth. A description of the color codes is in Table 1 "Available Colors Table" at the beginning of this section.

Note: The palette address can be 'masked' by using the palette mask register.

The following is a description of the register's bit functions:

Bit Number	Function
0	Blue
1	Green
2	Red
3	Intensity

When loading the palette, the video is 'disabled' and the color viewed on the screen is the data contained in the register being addressed by the processor.

When the program has completed loading the palette, it must change the hex address to some address less than hex 10 for video to be 'enabled' again.

If a programmer does not wish a user to see the adverse effects of loading the palette, the palette should be loaded during the vertical retrace time. The program must modify the palette and change the address to less than hex 10 within the vertical retrace time. A vertical retrace interrupt and a status bit are provided to facilitate this procedure.

In two color modes, the palette is defined by using one bit (PA0), with the following logic:

PALETTE ADDRESS BIT

PA0	Function
0	Palette Register 0
1	Palette Register 1

In four color modes, the palette is defined by using two bits (PA1 and PA0), with the following logic:

PALETTE ADDRESS BITS

PA1	PA0	Function
0	0	Palette Register 0
0	1	Palette Register 1
1	0	Palette Register 2
1	1	Palette Register 3

In sixteen color modes, the palette is defined by using four bits (PA3,PA2,PA1 and PA0), with the following logic:

PALETTE ADDRESS BITS

PA3 (I)	PA2 (R)	PA1 (G)	PA0 (B)	Function
0	0	0	0	Palette Register 0
0	0	0	1	Palette Register 1
0	0	1	0	Palette Register 2
0	0	1	1	Palette Register 3
0	1	0	0	Palette Register 4
0	1	0	1	Palette Register 5
0	1	1	0	Palette Register 6
0	1	1	1	Palette Register 7
1	0	0	0	Palette Register 8
1	0	0	1	Palette Register 9
1	0	1	0	Palette Register 10
1	0	1	1	Palette Register 11
1	1	0	0	Palette Register 12
1	1	0	1	Palette Register 13
1	1	1	0	Palette Register 14
1	1	1	1	Palette Register 15

DETAILED I/O REGISTER INFORMATION

Bit Programming

Hex Address	Register	7	6	5	4	3	2	1	0	Notes
3D4	6845 Address Register	X	X	X						Write Only
					<- 5 bit address ->					Addresses 1 of 18 6845 Registers
Hex Address	Register	7	6	5	4	3	2	1	0	Notes
3D5	6845 Data Register									Write Only
		<------ 8 bit Data ---->								Data placed in 1 of 18 6845 Registers

Hex Address	Register	Bit Programming 7	6	5	4	3	2	1	0	Notes
3D8	Mode Register	X	X							Write Only
ENABLINKCR	Alpha Blink Enable. A logical 1 selects blink if attribute bit 7 is set. A logical 0 selects 16 background colors. A logical 1 selects 0 background colors.									
HRESAD	640 Dot Graphics. A logical 1 selects 640 X 200 (2 or 4 Color)									
VIDENBCR	Video Enable. A logical 1 enables the Video display.									
BW	Black & White Select. Selects B&W or color mode for TV or composite monitors. In RGB monitors, a different color palette is selected by this bit in 320 x 200 4 Col Mode. This bit will have no other effect on RGB operation									
GRPH	Graphics Select. A logical 0 selects Alphanumeric Mode. A logical selects Graphics Mode.									
HRESCK	High Resolution Dot Clock. A logical 0 selects the lower speed for 40 character text or low resolution graphics mode. A logical 1 selects the lower speed for 80 character text or low resolution graphics mode.									

Bit Programming

Hex Address	Register	7	6	5	4	3	2	1	0	Notes
3D9	Color Select Register	X	X							Write Only
COLSEL	320 X 200 4 Color Blue Control									
BACKGROUNDI	Alpha Background/320 Graphics Foreground Intensity. When Blink is enabled in alpha mode, this bit is used to select intensity. In the 320 X 200 4 color mode, it selects the intensity of the foreground									
OVERSCANI	In Alpha mode screen Border intensity In 320x200 4 Col Background intensity if PA0=PA1=0 In 640x200 2 Col Foreground intensity									
OVERSCANR	In Alpha mode screen Border Red In 320x200 4 Col Background Red if PA0=PA1=0 In 640x200 2 Col Foreground Red									
OVERSCANG	In Alpha mode screen Border Green In 320x200 4 Col Background Green if PA0=PA1=0 In 640x200 2 Col Foreground Green									
OVERSCANB	In Alpha mode screen Border Blue In 320x200 4 Col Background Blue if PA0=PA1=0 In 640x200 2 Col Foreground Blue									

Hex Address	Register	Bit Programming 7	6	5	4	3	2	1	0	Notes
3DA	Video/Light Pen Status	X	X	X	X					Read Only
CVSYNC	When 1 Vertical retrace is active									
LPSWB	Not Used									
LPSTRB	Not Used									
DISPENB	When 0 Display is active When 1 Video is not displayed									

Bit Programming

Hex Address	Register	7	6	5	4	3	2	1	0	Notes
3DD	Extended Ram Page Reg	X					X	X		Write Only
	PG18 (#) CPU Page Address 18									
	PG17 CPU Page Address 17									All bits
	VPG18 (#) Video Page Address 18									cleared
	VPG17 Video Page Address 17									by a System Reset
	EXTADR Extended Addressing Mode for 256K systems									

Note (#) Not implemented in current design but reserved for future implementations

Bit Programming

Hex Address	Register	7	6	5	4	3	2	1	0	Notes
3DF	CRT/Processor Page Reg									Write Only
ADRM1(**)	Video Address Mode 1 with Reg 3DD bit0 selects Video Address supplied to RAM									
ADRM0(**)	Video Address Mode 0 with Reg 3DD bit0 selects Video Address supplied to RAM									
	Processor Page 2									
	Processor Page 1									
	Processor Page 0									
CRTPG2	CRT Page 2									
CRTPG1	CRT Page 1									
CRTPG0	CRT Page 0									

The processor page bits are combined with the CPU address to select the 32K segment of memory accessed at B8000. If an odd page number is selected, the window is reduced to 16K.

The CRT Page bits select the 16K Page used by the Video. In 32K modes bit 0 is ignored.

Note (**) :
These bits are used in conjunction with Reg 3DD bit 0 to select the Video addresses to the RAM. See the Video Memory Addressing Modes Table. Also the Graphics control bit 3D8 bit 1 (GRPH) will force the same condition as setting ADRM0.

Bit Programming

Hex Address	Register	7	6	5	4	3	2	1	0	Notes
00A0-00A7	NMI Mask Register		X	X						Write Only
NMIEN	Enable Non Maskable Interrupt									
PORTMD	Enable 256K Video RAM									All bits
MC3	Memory Configuration 3									cleared
MC2	Memory Configuration 2									by a
MC1	Memory Configuration 1									System
XTERNVID	Disables all video Accesses to Video Memory at B8000-BFFFF and video I/O locations 3D0-3D7									Reset

6845 PROGRAMMING TABLE FOR ALL MODES

*	REGISTER	40X25 ALPHANUM	80X25 ALPHANUM	160X200 16 Col 320X200 4 Col 640X200 2 Col	640X200 4 Col 320X200 16 Col
0	Horizontal Total	38 (56)	71 (113)	38 (56)	71 (113)
1	Horiz. Displayed	28 (40)	50 (80)	28 (40)	50 (80)
2	Horiz. Sync. Pos	2D (45)	5A (90)	2D (45)	5A (90)
3	Horiz. Sync. Width	08 (8)	0E (14)	08 (8)	0E (14)
4	Vertical Total-1	1C (28)	1C (28)	7F (127)	3F (63)
5	Vert. Total Adjust	01 (1)	01 (1)	06 (6)	06 (6)
6	Vertic. Displayed	19 (25)	19 (25)	64 (100)	32 (50)
7	Vert. Sync Pos.	1A (26)	1A (26)	70 (112)	38 (56)
8	Interlace Mode	02 (2)	02 (2)	02 (2)	02 (2)
9	MaxScanLineAdd -1	08 (8)	08 (8)	01 (1)	03 (3)
10	Cursor Start	06 (6)	06 (6)	06 (6)	06 (6)
11	Cursor End	07 (7)	07 (7)	07 (7)	07 (7)
12	StartAddresss High	00 (0)	00 (0)	00 (0)	00 (0)
13	StartAddress Low	00 (0)	00 (0)	00 (0)	00 (0)

MODE SELECTION SUMMARY

MODE	'H3D8 BIT 0 HRESCK	'H3D8 BIT 4 HRESAD	'H3DE REG3 BIT 3 C4COLHR	'H3DE REG3 BIT 4 C16COL	'H3DE REG3 BIT 5 NVDM	'H3D8 BIT 1 GRPH	'H3DD BIT 0 EXTADR	'H3DF BIT 7 ADRM1	'H3DF BIT 6 ADRM0
40X25 ALPHA	0	0	0	0	0	0	0	0	0
80X25 ALPHA	1	0	0	0	0	0	0	0	0
160X200 16 COL	0	0	0	1	0	1	0	0	1
320X200 4 COL	0	0	0	0	0	1	0	0	1
320X200 16 COL	1	0	0	1	0	1	0	1	1
640X200 2 COL	0	1	0	0	0	1	0	0	1
640X200 4 COL	1	1	1	0	0	1	0	1	1

VIDEO/SYSTEM MEMORY ADDRESS MAP

'H0A0 BITS 4 3 2 1	VIDEO/SYSTEM MEMORY START ADDRESS	VIDEO/SYSTEM MEMORY LENGTH	VIDEO/SYSTEM MEMORY ADDRESS RANGE
0 0 0 0	0 0 0 0 0	128K	0 0 0 0 0 - 1 F F F F
0 0 0 1	2 0 0 0 0	128K	2 0 0 0 0 - 3 F F F F
0 0 1 0	4 0 0 0 0	128K	4 0 0 0 0 - 5 F F F F
0 0 1 1	6 0 0 0 0	128K	6 0 0 0 0 - 7 F F F F
0 1 0 0	8 0 0 0 0	128K	8 0 0 0 0 - 9 F F F F
1 0 0 1	0 0 0 0 0	256K	0 0 0 0 0 - 3 F F F F
1 0 1 0	2 0 0 0 0	256K	2 0 0 0 0 - 5 F F F F
1 0 1 1	4 0 0 0 0	256K	4 0 0 0 0 - 7 F F F F
1 1 0 0	6 0 0 0 0	256K	6 0 0 0 0 - 9 F F F F

VIDEO MEMORY ADDRESSING MODES

'H3DD BIT 0 EXTADR	'H3DF BIT 7 ADRM1	'H3DF BIT 6 ADRM0	VIDEO MEMORY ORGANIZATION (128)
0	0	0	1 16K Segment of Memory (8 Pages)
0	0	1	2 8K Segments of Memory (8 Pages) Switched on RA[0]
0	1	0	2 16K Segments of Memory (4 Pages) Switched on RA[0]
0	1	1	4 8K Segments of Memory (4 Pages) Switched on RA[0],RA[1]
1	0	0	1 32K Segment of Memory (4 Pages)
1	0	1	2 32K Segments of Memory (2 Pages) Switched on RA[0]

For 8 Page Modes CRTPG[2:0] select the Video Page
For 4 Page Modes CRTPG[2:1] select the Video Page
For 2 Page Modes CRTPG[2] select the Video Page

OTHER CHIP FUNCTIONS

In addition to the video controller functions, the Tandy 1000 video controller chip also provides most of the system address decode functions. These decode and chip select functions are described as follows:
A, B, C outputs are encoded device select lines and are connected to an external LS138.

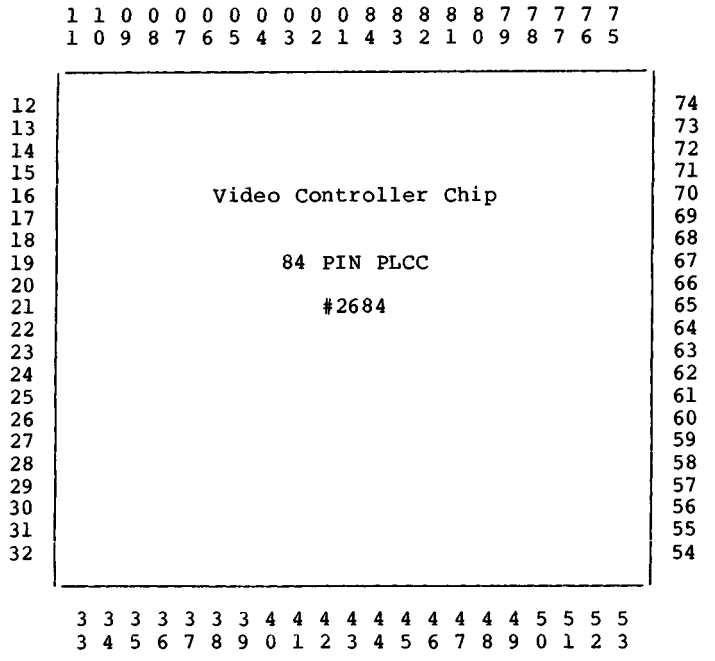
C	B	A	IOMB	BA0-15(HEX)	DESCRIPTION
1	1	1		NONE OF BELOW	
1	1	0	1	0020-0027	INTCSB
1	0	1	1	0040-0047	TMRCSB
1	0	0	1	0060-0067	PIOCSB
0	1	1	1	0200-0207	JOYSTKCSB
0	1	0	1	00C0-00C7	SNDCSB
0	0	1	1	03F0-03F7	FDCCSB
0	0	0	1	0378-037F	PRINTCSB

The output signal ROMIOSELB is the enable signal for an LS245 that controls all of the data flow to devices on the main logic board. This signal is active low and will be activated for any of the following conditions:

1. Video/System Memory Read or Write
2. Video Access at B8000-BFFFF
3. Rom Access at F0000-FFFFF
4. Video I/O access at 03D0-03DF
5. I/O access to any of the following addresses:

   0040-0047
   0060-0067
   00A0-00A7
   00C0-00C7
   0200-0207
   0378-037F
   03F0-03F7

PIN LIST


1 1 0 0 0 0 0 0 0 0 0 8 8 8 8 8 7 7 7 7 7
1 0 9 8 7 6 5 4 3 2 1 4 3 2 1 0 9 8 7 6 5
12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
74 73 72 71 70 69 68 67 66 65 64 63 62 61 60 59 58 57 56 55 54
Video Controller Chip
84 PIN PLCC
#2684
3 3 3 3 3 3 3 4 4 4 4 4 4 4 4 4 4 5 5 5 5
3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3

DESCRIPTION OF EACH PIN FUNCTION

PIN#	PIN NAME	TYPE	DESCRIPTION
1	VSS	Ground	Ground
2	XMD[2]	Input/Output	External Memory Data I/O Bank 0
3	XMD[3]	Input/Output	External Memory Data I/O Bank 0
4	XMD[4]	Input/Output	External Memory Data I/O Bank 0
5	XMD[5]	Input/Output	External Memory Data I/O Bank 0
6	XMD[6]	Input/Output	External Memory Data I/O Bank 0
7	XMD[7]	Input/Output	External Memory Data I/O Bank 0
8	YMD[0]	Input/Output	External Memory Data I/O Bank 1
9	YMD[1]	Input/Output	External Memory Data I/O Bank 1
10	YMD[2]	Input/Output	External Memory Data I/O Bank 1
11	YMD[3]	Input/Output	External Memory Data I/O Bank 1
12	YMD[4]	Input/Output	External Memory Data I/O Bank 1
13	YMD[5]	Input/Output	External Memory Data I/O Bank 1
14	YMD[6]	Input/Output	External Memory Data I/O Bank 1
15	YMD[7]	Input/Output	External Memory Data I/O Bank 1
16	RFSHB	Input	Memory Refresh Strobe Input
17	MWE1B	Output	Ram Bank 1 Write Enable Signal
18	MWE0B	Output	Ram Bank 0 Write Enable Signal
19	RASB	Output	Ram Row Address Strobe
20	CASB	Output	Ram Column Address Strobe
21	BMEMRB	Input	CPU Memory Read Strobe
22	VDD	Power	5 Volts Supply
23	BMEMWB	Input	CPU Memory Write Strobe
24	CK28M	Clock	28.63636 Mhz Clock Input
25	VIDEOWAIT	Output(OpenDrain)	Video Wait Signal
26	SYSRSTB	Input	System Reset
27	IOMB	Input	CPU I/O-Memory Signal (Memory ->1, I/O -> 0)
28	A	Output	Encoded Peripheral Select Line
29	B	Output	Encoded Peripheral Select Line
30	C	Output	Encoded Peripheral Select Line
31	IOMEMSELB	Output	External Buffer Enable
32	NMIEN	Output	Nonmaskable Interrupt Enable
33	BIORB	Input	CPU I/O Read Strobe
34	BIOWB	Input	CPU I/O Write Strobe
35	LPIN	Input	Not Used
36	LPSWB	Input	Not Used
37	OUTVSYNC	Output	Vertical Sync Output
38	OUTHSYNC	Output	Horizontal Sync Output
39	COMPCOLOR	Output	Composite Color Signal
40	COMPSYNC	Output	Composite Sync Signal
41	OUTI	Output	Intensity Out
42	OUTR	Output	Red Video Out
43	VSS1	Ground	Ground
44	OUTB	Output	Blue Video Out/Monochrome Dotclock

45	OUTG	Output	Green Video Out/Monochrome Video
46	BA[19]	Input	CPU Address Line
47	BA[18]	Input	CPU Address Line
48	BA[17]	Input	CPU Address Line
49	BA[16]	Input	CPU Address Line
50	BA[157	Input	CPU Address Line
51	BA[14]	Input	CPU Address Line
52	BA[13]	Input	CPU Address Line
53	BA[12]	Input	CPU Address Line
54	BA[11]	Input	CPU Address Line
55	BA[10]	Input	CPU Address Line
56	BA[9]	Input	CPU Address Line
57	BA[8]	Input	CPU Address Line
58	BA[7]	Input	CPU Address Line
59	BA[6]	Input	CPU Address Line
60	BA[5]	Input	CPU Address Line
61	BA[4]	Input	CPU Address Line
62	BA[3]	Input	CPU Address Line
63	BA[2]	Input	CPU Address Line
64	BA[1]	Input	CPU Address Line
65	BA[0]	Input	CPU Address Line
66	DB[7]	Input/Output	CPU Data I/O
67	DB[6]	Input/Output	CPU Data I/O
68	DB[5]	Input/Output	CPU Data I/O
69	DB[4]	Input/Output	CPU Data I/O
70	DB[3]	Input/Output	CPU Data I/O
71	DB[2]	Input/Output	CPU Data I/O
72	DB[1]	Input/Output	CPU Data I/O
73	DB[0]	Input/Output	CPU Data I/O
74	MA[0]	Output	Memory Address Line
75	MA[1]	Output	Memory Address Line
76	MA[2]	Output	Memory Address Line
77	MA[3]	Output	Memory Address Line
78	MA[4]	Output	Memory Address Line
79	MA[5]	Output	Memory Address Line
80	MA[6]	Output	Memory Address Line
81	MA[7]	Output	Memory Address Line
82	BANKSL	Output	Memory Address Line
83	XMD[0]	Input/Output	External Memory Data I/O Bank 0
84	XMD[1]	Input/Output	External Memory Data I/O Bank 0

LOGIC BLOCK DIAGRAM

TEST MODES AND THEIR OPERATIONS

There are four Test Modes that the chip can be placed into to make the part easily and efficiently testable. All these Test Modes use conditions that can never occur in a System environment, therefore avoiding accidental entry in Test Mode. All the test modes are entered when both MEMRB and MEMWB are active. The selection of the different tests is done by an additional decode on some bits of the BA lines according to the following chart:

TEST MODE	ENABLED WHEN						OPERATION PERFORMED
	BMEMRB	BMEMWB	BA15	BA14	BA13	BA12	
1	0	0	1	X	X	X	Pinout the 6845 Megacell on external pins and/or Start Self Test Rom. While the testing of the Megacell is in progress, the Rom is performing a signature analysis. At the end of 4500 clocks, a PASS/FAIL bit is set, if the Self Test was successful.
2	0	0	0	1	X	X	Enable a Software Reset on the 6845.
3	0	0	0	X	1	X	Clear the Clock generators & blink counter to start from a known condition.
4	0	0	0	X	X	0/1	A logical 1 writes a bit that forces Display Enable constantly. A 0 removes forced Display Enable. Cleared by SYSRSTB.

TEST MODE 1 PINOUT THAT EMULATES THE 6845 STANDARD PRODUCT

The following signals of the Megacell are available on the following pins in Test Mode 1:

6845 SIGNAL	VIDEO SIGNAL
RESETB	SYSRSTB
LPSTB (Not Used)	LPIN (Not Used)
MA[7:0]	MA[7:0]
MA[8]	BANKSL
MA[9]	MWE1B
MA[10]	ROMIOSELB
MA[11]	A
MA[12]	B
MA[13]	C
DE	COMPSYNC
CURSOR	COMPCOLOR
CLK	IOMB (See Note ***)
RNW	BIOWB
E	RFSHB
RS	BA[0]
CSB	LPSWB (Not Used)
DB[7:0]	DB[7:0]
RA[0]	RASB
RA[1]	CASB
RA[2]	OUTR
RA[3]	OUTI
RA[4]	MWE0B
HS	OUTHSYNC
VS	OUTVSYNC

Also the Pass/Fail bit for the Self Test ROM can be tested on the OUTG outputpin during TEST MODE 1. Note that at least 4,500 clocks must be given in Test Mode 1 before checking the Pass/Fail bit. These clock times could be used to exercise the 6845 as a standard part according to the previous pinout.

Note***: IOMB is in fact CLK Bar so in order to test it using the standard part's test program, there is a need to invert the clock coming in the Test program.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAX RATINGS (NON-OPERATING, VSS=0v)

	MIN	MAX	UNITS
STORAGE TEMPERATURE	-65	150	DEGREES C.
VOLTAGE ON ANY PIN W.R.T.GROUND	-0.5	7.0	VOLTS

OPERATING ELECTRICAL SPECIFICATIONS

OPERATING AMBIENT AIR TEMP. RANGE	MIN	TYP	MAX	UNITS
	0	25	70	DEGREES C.

POWER SUPPLIES				
VCC SUPPLY VOLTAGE	4.5	5.0	5.5	VOLTS
VSS SUPPLY VOLTAGE	0	0	0	VOLTS
ICC SUPPLY CURRENT		20	35	MILLIAMPS
TOTAL POWER DISSIPATION (INCLUDE LOADING ON OUTPUTS)		100	175	MILLIWATTS

LEAKAGE CURRENT ALL INPUTS AND TRISTATE OUTPUTS	MIN	TYP	MAX	
	-10		10	MICROAMPS

INPUT VOLTAGES LOGIC "0" (Vil) ALL INPUTS	0.8	VOLTS
LOGIC "1" (Vih) ALL INPUTS	2.0	VOLTS

OUTPUT VOLTAGES	CURRENT LOADING	MIN	TYP	MAX	UNITS
LOGIC"0" (Vol) ALL OUTPUTS	2.0 MA			0.4	VOLTS
LOGIC"1" (Voh) ALL OUTPUTS	0.4 MA	2.4			VOLTS

INPUT CAPACITANCE	MIN	TYP	MAX	
ALL INPUTS			10	PICOFARADS

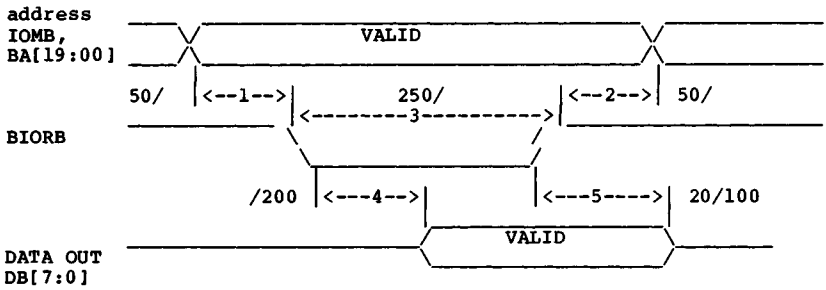
TIMING SPECIFICATION

MAXIMUM LOADING FOR EACH OUTPUT

MA[8]-MA[0]	100 pF
ALL OTHER OUTPUTS	20 pF

CHARACTERISTICS

READ Operation



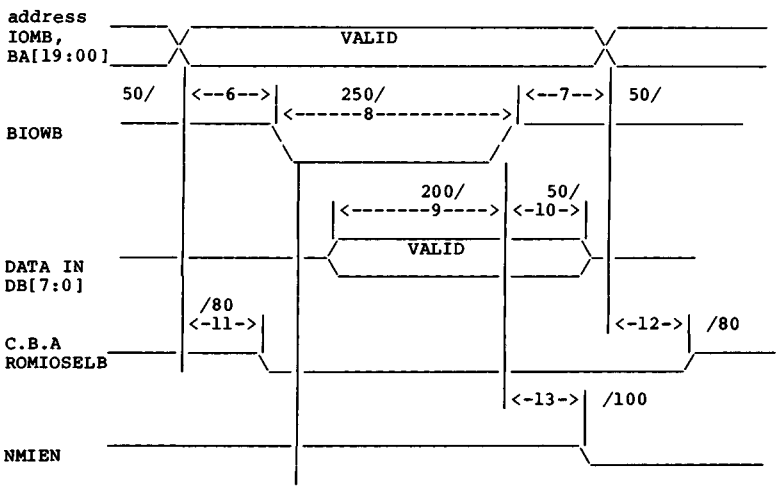
I/O TIMING

#	DESCRIPTION	MIN	MAX	UNITS	NOTE
1	ADDRESS VALID TO BIORB ACTIVE SETUP	50		NS	
2	ADDRESS VALID HOLD AFTER BIORB INACTIVE	50		NS	
3	BIORB PULSE WIDTH LOW	250		NS	
4	BIORB ACTIVE TO DATA OUT VALID		200	NS	
5	BIORB INACTIVE TO DATA OUT TRISTATE	20	100	NS	

READ OPERATION

READ OPERATION

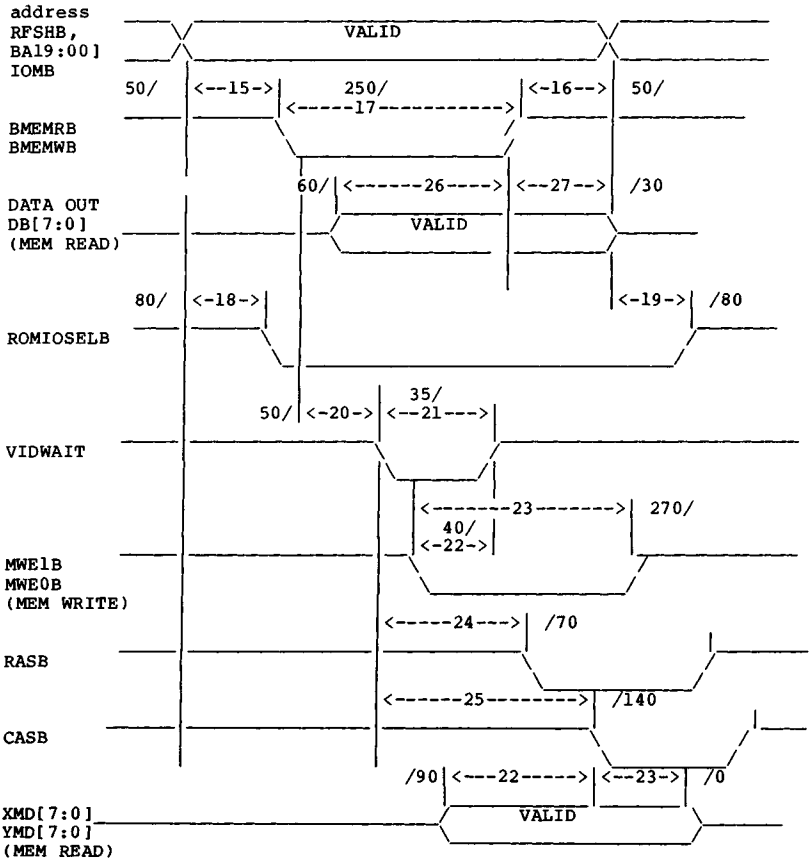
WRITE OPERATION AND I/O OUTPUT TIMING



#	DESCRIPTION	MIN	MAX	UNITS	NOTE
6	ADDRESS VALID TO BIOWB ACTIVE SETUP	50		NS	
7	ADDRESS VALID HOLD AFTER BIOWB INACTIVE	50		NS	
8	BIOWB PULSE WIDTH LOW	250		NS	
9	DATA IN VALID TO BIOWB INACTIVE SETUP	200		NS	
10	BIOWB INACTIVE TO DATA IN VALID HOLD	50		NS	
11	ADDRESS VALID TO C,B,A,ROMIOSELB OUTPUT DELAY		80	NS	
12	ADDRESS NOT VALID TO ROMIOSELB INACTIVE OUT DELAY		80	NS	
13	BIOWB INACTIVE TO NMIEN LATCHED OUTPUT DELAY		100	NS	

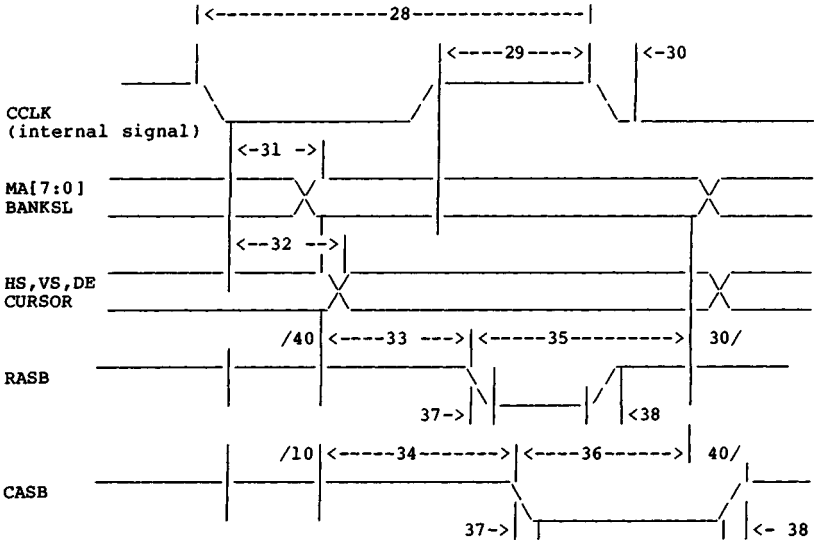
MEMORY DECODE TIMING

MEMORY READ OR WRITE OPERATION



*	DESCRIPTION	MIN	MAX	UNITS	NOTE
15	ADDRESS VALID TO BMEMRB ACTIVE SETUP	50		NS	
16	ADDRESS VALID HOLD AFTER BMEMRB INACTIVE	50		NS	
17	BMEMRB PULSE WIDTH LOW	250		NS	
18	ADDRESS VALID TO ROMIOSELB OUTPUT DELAY		80	NS	
19	ADDRESS NOT VALID TO ROMIOSELB INACTIVE OUT DELAY		80	NS	
20	VIDWAIT DELAY FROM BMEMRB READ LOW		50	NS	
21	VIDWAIT PULSE WIDTH	35	600	NS	
22	XMD, YMD SETUP TO CASB LOW (MEM READ)	90		NS	
23	XMD, YMD HOLD TO CASB LOW (MEM READ)	0		NS	
24	VIDWAIT LOW DELAY TO RASB LOW		70	NS	
25	VIDWAIT LOW DELAY TO CASB LOW	0	140	NS	
26	I/O DATA BUS OUT SETUP TO BMEMRB HIGH	60		NS	
27	I/O DATA BUS OUT HOLD TO BMEMRB HIGH	0	30	NS	

CRTC TIMING


28
29
30
CCLK
(internal signal)
31
MA[7:0]
BANKSL
32
HS,VS,DE
CURSOR
/40
33
35
30/
RASB
37
38
/10
34
36
40/
CASB
37
38

CRTC TIMING

	Characteristics	Symbol	Min	Nom	Max	Units
28	CCLK frequency	Fcyc			2	MHz
29	CCLK width	PWcl	100			nS
30	CCLK rise and fall time	Tcr,Tcf			5	nS
31	CLK fall to MA[7:0]RA0-4 delay time	Tmad,Trad			50	nS
32	CLK fall to HS, VS, DE,CURSOR delay time	Thsd,Tvsd Tdtd,Tcdd			50	nS
33	MA[7:0],BANKSL setup to RASB low		40			nS
34	MA[7:0],BANKSL setup to CASB low		10			nS
35	MA[7:0],BANKSL hold from RASB low		30			nS
36	MA[7:0],BANKSL hold from CASB low		40			nS
37	RASB,CASB fall				20	nS
38	RASB,CASB rise				5	nS

OTHER TIMING SPECS

	Characteristics	Symbol	Min	Nom	Max	Units
39	Relative Skew of R,G,B,I				10	nS
40	Relative Skew of R,G,B,I With respect to Compcol				20	nS
41	Relative Skew of R,G,B,I With respect to CompSync OutHsync,OutVsync				35	nS
42	Relative Skew of R,G,B,I With respect to CompSync				35	nS

MEGACELL 6845R1 SPECIFICATION DATASHEET FOR 6845 MEGACELL

VE 68C45 MEGACELL DESIGN KIT
CRT CONTROLLER MEGACELL

FEATURES

- Completely integrated with VTI's extensive IC design tools and libraries
- CMOS (2-micron) M68C45 Megacell configurable as:
  - -- 68C45R - CMOS equivalent of Motorola 6845R CRTC
  - -- 68C45R1 - CMOS equivalent of Motorola 6845R1 Enhanced CRTC
  - -- 68C45S - CMOS equivalent of Hitachi 6845S CRTC
  - -- 68C45SY - CMOS CRTC similar to Synertek 6545 CRTC
- 4.5 MHz video memory interface
- 3 MHz system processor interface
- Compatible with the VTI bus architecture
- Programmable Display Enable and Cursor delays (standard for S and SY versions -- optional for R and R1 versions)
- Programmable Vertical Sync pulse width (standard for S version -- optional for R, R1 and SY versions)
- Row/Column display memory addressing (SY version)
- Double Width character control

OPTIONAL FEATURES

- 16K, 32K, or 64K display Memory Address range (14, 15, or 16 bits)
- 7, 8, or 9-bit Vertical Row counter

VTI MEGACELLS

Megacells are building block equivalents of standard LSI functions that can be combined with other megacells, standard cells or compiled cells to create custom User-Specific ICs (USICs). Megacells are fully compatible with VTI's other cell technologies and design tools.

The VTI bus (TM) architecture allows multiple megacells to be combined on a single IC, along with additional cells from VTI's extensive libraries -- decreasing the design time, design cost, and size of complex systems. A detailed Functional Model provided with each megacell further reduces design verification time.

SIGNAL DESCRIPTIONS

The following signals function the same on the M68C45 Megacells and on the standard VL6845 family of CRT Controller ICs.

Signal	I/O	Description
RS	IP	Register Select
E	IP	Enable
RNW	IP	Specify READ (high) or WRITE (low) operation
CSB	IP	Chip (6845 megacell) select, low true
CCLK	IP	Character Clock
LPSTB	IP	Not Used
D0-D7	I/O	Data Bus
RA0-RA4	OP	Raster Address
HS	OP	Horizontal Sync
RESETB	IP	Reset, low true

The following signals are unique to the VE68C45 Megacells, or are functionally different on the VE68C45 Megacells and the VL6845 ICs.

Signal	I/O	Description
DE	OP	Display Enable output - active (DE = "1") when the VE68C45 is generating active display information. The S version can be programmed with a 0, 1, or 2 character delay. The SY version can be programmed for a 0 or 1 character delay.
CURSOR	OP	Cursor output - this signal is high when the raster scan coincides with the programmed cursor position. The S version can be programmed with a 0, 1, or 2 character delay. The SY version can be programmed for a 0 or 1 character delay.
VS	OP	Vertical Sync output - active high pulse which determines the vertical placement of the video data. An optional feature permits programming the Vertical Sync pulse width.

MA0-MA13, 14,15	OP	14, 15, or 16- bit Video Memory Address bus. These tri-state outputs provide the binary address to the external video RAM. If row/column addressing is selected (SY version only) this bus will provide row/column addressing to the external RAM instead of binary addressing. The AENB input signal can be used to place the MA bus in the high impedance state.
AENB	IP	Address Enable input - when asserted low (AENB = "0") the MA outputs are enabled. AENB = "1" forces the MA outputs into a high impedance state.
LD0-LD13, 14,15	I/O	14, 15, or 16-bit Advanced Memory Address bus - separate video memory address information on this bus precedes the information on the MA bus by one character clock. This bus is provided to interface with a separate strip of logic for split display capability.
LOAD	IP	When asserted (high) a new value is loaded into the RA counter. Tie to VSS when not used.
BREAK	IP	To be used for splitted screen format. Tie to VSS when not used.
READB	OP	This signal goes LOW during a legitimate read operation.
VDRA (reserved)	n/c	Reserved for future expansion. To be left unconnected.
DW	IP	Double Width input - this input puts the VE68C45 in a double-width display mode. Tie to VSS when not used.

6845R, 6845S, 6545SY	IP	One of these three inputs is tied high to select the version of the VE68C45 used in your application. The remaining two inputs must be grounded. NOTE: the VE68C45SY does not provide 6545 transparent addressing or the 6545 status register.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Ambient temperature under bias	0 C to 70 C
Storage temperature	-65 C to +150 C
Voltage on any signal with respect to Gnd	-0.5V to +7V
Power dissipation	750mW

DC characteristics (Ta = 0 - 70 degree C, Vss=0v, Vcc=+5 +/- 10%)

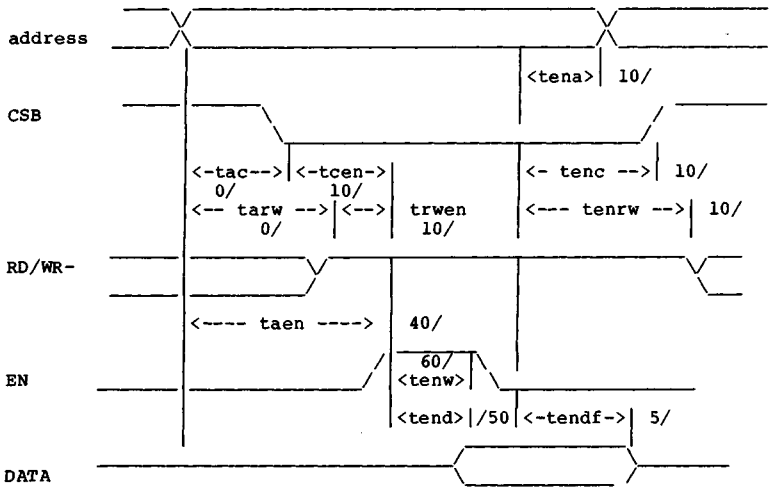
Characteristics	Symbol	Min	Typ	Max	Units
Input High Voltage					
Inputs,I/O	Vih	3.0		Vcc	Volts
Input Low Voltage					
Inputs,I/O	Vil	Vss		0.8	Volts
Output High Voltage					
Outputs,I/O	Voh	3.0		Vcc	Volts
Output Low Voltage					
Outputs,I/O	Vol			0.4	Volts

Capacitance

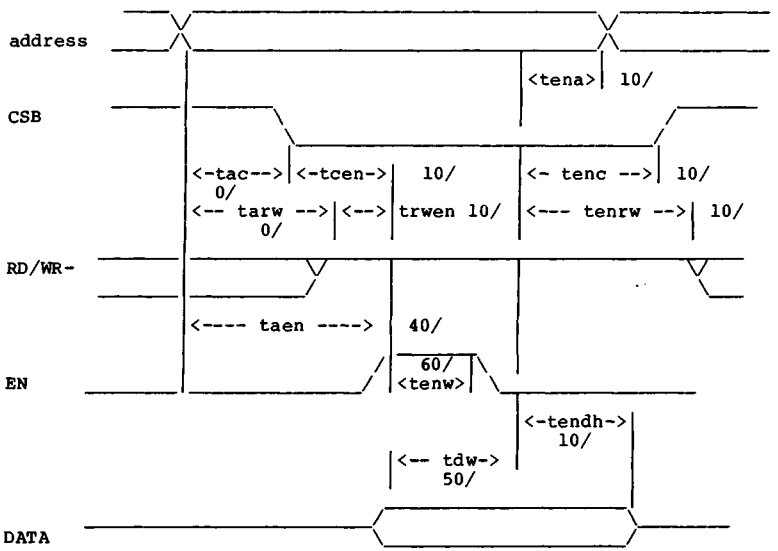
Input Capacitance					
CLK input	Cin			6	pF
remaining inputs	Cin			.7	pF
Output Loading					
MA0-13,D0-7	Cout			9	pF
RA0-4,HS,VS,DE, Cursor	Cout			3	pF

AC CHARACTERISTICS (Vcc=+5v +/- 10%, Vss=0v, Ta=0 C to 70 C)

VTI BUS TIMING



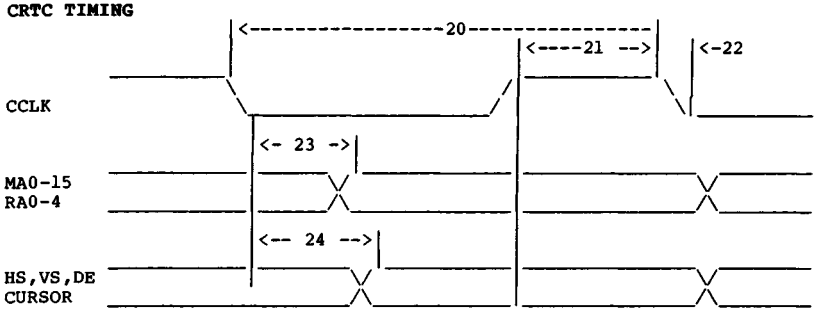
WRITE


address
CSB
RD/WR-
EN
DATA
<tena> 10/
<-tac--> 0/
<-tcen-> 10/
<- tenc --> 10/
<-- tarw --> 0/
<--> trwen 10/
<--- tenrw --> 10/
<---- taen ----> 40/
60/
<tenw>
<-tendh-> 10/
<-- tdw-> 50/

VTI BUS TIMING

	MIN(ns)	MAX(ns)
TAC address to CS delay	0	
TARW address to read/write delay	0	
TAEN address to enable set up	40	
TCEN CS to enable delay	10	
TRWEN read/write to enable set up	10	
TENW enable pulse width	100	
TENA enable to address hold time	10	
TENC enable to cs hold time	10	
TENRW enable to read/write hold time	10	
read:		
TEND enable to read data delay		50
TENDF enable to data bus float	5	30
write:		
TDEN write data to enable setup time	50	
TENDH enable to write data hold time	10	

CRTC TIMING



CRTC TIMING

	Characteristics	Symbol	Min	Nom	Max	Units
20	CLK frequency	Fcyc			4.5	MHz
21	CLK width	PWcl	100			nS
22	CLK rise and fall time	Tcr,Tcf			5	nS
23	CLK fall to MA0-15,RA0-4 delay time	Tmad,Trad			50	nS
24	CLK fall to HS, VS, DE,CURSOR delay time	Thsd,Tvsd Tdtd,Tcdd			50	nS

NCR

MICROELECTRONICS DIVISION

NCR 8496
SOUND GENERATOR
DATA SHEET

NCR 8496 SOUND GENERATOR

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

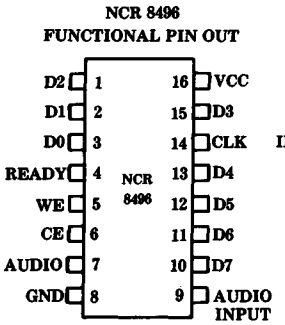
SECTION 1

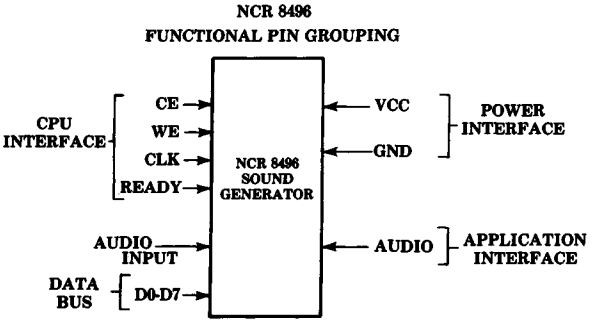
GENERAL DESCRIPTION

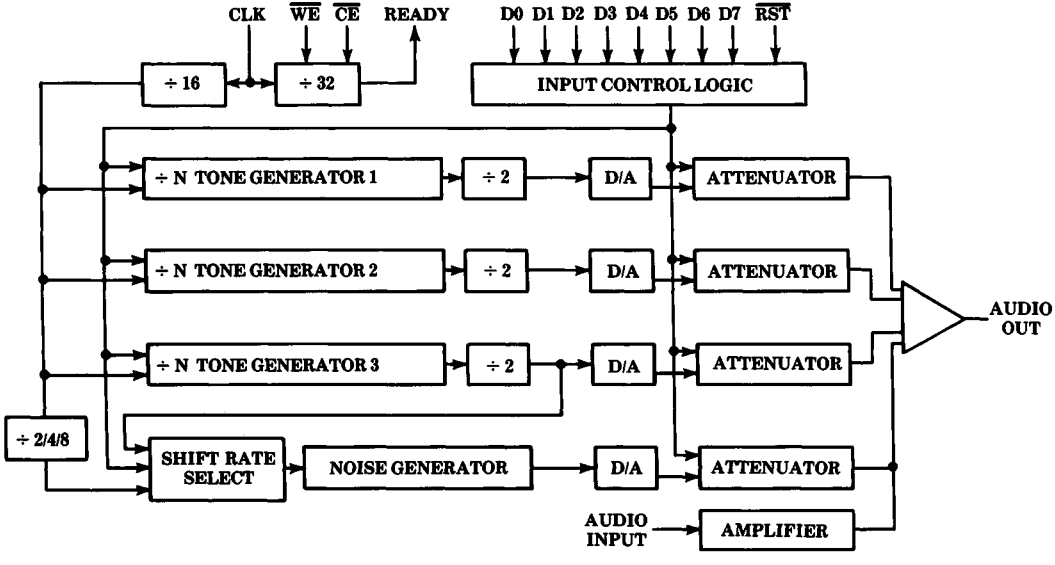
The NCR 8496 is an NMOS digital sound generator capable of providing applications with a low cost solution for noise and sound generation.

FEATURES

- Functionally and Pin compatible with the SNR76496
- Programmable white or periodic noise generator
- Three programmable tone generators
- Programmable attenuation values
- Simultaneous multiple sound generation
- TTL compatible
- 4 MHz maximum clock input
- External audio input added to Internal Generators







NCR 8496 FUNCTIONAL BLOCK DIAGRAM

SECTION 2

FUNCTIONAL DESCRIPTIONS

2.1 Control Registers

The NCR 8496 Sound Generator has eight (8) internal registers used to control three (3) tone generators and one (1) noise generator. A three (3) bit data word used to determine the destination control register is contained in the first byte of data for all data transfers. The internal register designations are as follows:

Address Bits			Register Destination
RO	R1	R2	Description
0	0	0	Tone 1: Frequency
0	0	1	Tone 1: Attenuation
0	1	0	Tone 2: Frequency
0	1	1	Tone 2: Attenuation
1	0	0	Tone 3: Frequency
1	0	1	Tone 3: Attenuation
1	1	0	Noise : Control
1	1	1	Noise : Attenuation

Note: RO is the most significant address bit

2.2 Tone Generation

The NCR 8496 sound generator has three (3) programmable tone generators, each with separate frequency synthesis and attenuation sections. The frequency synthesis section requires ten (10) bits of data (F0 to F9) to define half the period of the desired frequency. This data is entered into a ten (10) stage tone counter, which is decremented at a rate of N/16 where N is the clock input frequency. A signal is produced when this tone counter decrements to one, which toggles a divide by two counter and reloads the tone counter. Therefore, the period of the desired frequency is twice the value of the tone generator.

The frequency of each tone generation is calculated using the equation:

$$f=N/32n$$

N = the clock input frequency
n = a 10 bit binary number [2 < n < 1023]

The divide by two counter is directly connected to a four stage attenuator whose values and bit position in the data word are shown in the following table:

ATTENUATION CONTROL

Data				Value	Data				Value
A0	A1	A2	A3	dB	A0	A1	A2	A3	dB
0	0	0	0	0	1	0	0	0	-16
0	0	0	1	-2	1	0	0	1	-18
0	0	1	0	-4	1	0	1	0	-20
0	0	1	1	-6	1	0	1	1	-22
0	1	0	0	-8	1	1	0	0	-24
0	1	0	1	-10	1	1	0	1	-26
0	1	1	0	-12	1	1	1	0	-28
0	1	1	1	-14	1	1	1	1	OFF

Note: A0 is the most significant bit of data

2.3 Noise Generation

The NCR Sound Generator has two (2) noise sources (periodic and white), which share a common attenuator. These noise sources are shift registers with an exclusive NOR feedback network. One (1) of four (4) noise generator shift rates, each rate being derived from the input clock, will be controlled by the two (2) NF bits, as is shown in the following table:

NOISE GENERATOR FREQUENCY CONTROL

NF BITS		FREQUENCY CONTROL
NF0	NF1	SHIFT RATE
0	0	N/512
0	1	N/1024
1	0	N/2048
1	1	Tone Generator #3 Output

Note: NF0 is the most significant bit

The choice of either periodic or white noise is controlled by the noise feedback control bit FB, as is shown in the following table:

NOISE FEEDBACK CONTROL

FB	CONFIGURATION
0	Periodic Noise
1	White Noise

2.4 Data Transfer

The NCR 8496 Sound Generator is enabled by the CPU by asserting a low logic level to $\overline{CE}$. $\overline{WE}$ strobes the contents of the data bus to the appropriate control register. Data bus contents must be valid at this time. Data transfers cannot occur unless $\overline{CE}$ is true.

Thirty two (32) clock cycles are required by the NCR 8496 to load data into the control register. The READY output used as a handshake signal to synchronize the CPU, is asserted to a low logic level immediately following the leading edge of $\overline{CE}$. READY assumes a true state via an external pull up register once the data transfer has been completed.

Formats for Data Transfer are as follows:

FREQUENCY UPDATE (Double Byte Transfer)

FIRST BYTE

DATA				REGISTER ADDRESS			BIT 0
F9	F8	F7	F6	R2	R1	R0	1
D7							D0

SECOND BYTE

DATA							BIT 0
F5	F4	F3	F2	F1	F0	X	0
D7							D0

NOISE SOURCE UPDATE (Single Byte Transfer)

SHIFT RATE		FEEDBACK			REGISTER ADDRESS			BIT 0
NF1	NF0	FB		X	R2	R1	R0	1
D7								D0

ATTENUATOR UPDATE (Single Byte Transfer)

DATA				REGISTER ADDRESS			BIT 0
A3	A2	A1	A0	R2	R1	R0	1
D7							D0

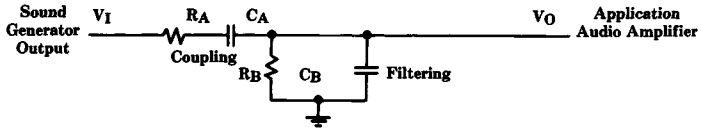
2.5 CPU INTERFACE

Eight (8) data lines (D0-D7) and three (3) control lines ($\overline{WE}$, $\overline{CE}$, READY) interface the NCR 8496 Sound Generator to the CPU. As indicated in Section 2.2, Tone Generation, ten (10) bits of data are required by each tone generator in selecting frequency values. Frequency updates require double byte data transfers. An additional four (4) bits of data are required to select the attenuation values. Attenuation updates require only single byte data transfers. (See Section 2.4: Data Transfer).

Tone generators can be quickly updated by initially sending both bytes of frequency and register data, followed by only the second byte of data for succeeding values only if no other control registers are accessed at the time of generator updating. This action is accomplished by latching the register address and permitting the continued transfer of data into the same register. This updating feature permits the expedited modification of the six (6) most significant bits of data needed for frequency sweeps.

2.6 OUTPUT CIRCUITRY

The NCR 8496 Sound Generator output circuitry, emulating a conventional op amp summing circuit, sums the three (3) tone and one (1) noise generator outputs, and will source/sink current to 2 mA. The 0 dB output signal per generator is nominally a 450 mV square in the negative direction from a 2V quiescent level. The output should be OR coupled into the application audio circuit via a filtering network similar to the following:



The upper and lower frequency poles for the application are determined from the following equations:

Lower Pole

$$f \cong \frac{1}{2\pi(R_A + R_B)\,C_A}$$

Upper Pole

$$f \cong \frac{1}{2\pi(R_A \,//\, R_B)\,C_B}$$

Attenuation of the output signal is:

$$\frac{V_O}{V_I} = \frac{R_B}{R_A + R_B}$$

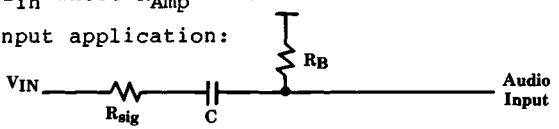
Typically $R_B \geq 10\ R_A$ so that the attenuation can be small while achieving desired filtering at the same time.

2.7 AUDIO INPUT CIRCUIT

This input node can be biased on with a current to give an approximate transfer function at the output of :

$V_O = R_{Amp} I_{in}$ where R_{Amp} is on the order of 1K Ohms

Typical input application:



R_B provides the bias current to put the amplifier in the linear range.

R_{sig} controls the input current causing the signal swing.

SECTION 3

INTERFACE DEFINITION

3.1 MICROPROCESSOR INTERFACE

Signal	Pin	Description
READY	4	OUTPUT: Open collector, READY indicates that data has been read when true (high). The CPU must be placed in a wait state until READY is true.
$\overline{WE}$	5	INPUT: Write Enable $\overline{WE}$ indicates that data is available to the NCR 8496 when true (low).
$\overline{CE}$	6	INPUT: Chip Enable $\overline{CE}$ indicates that data may be transferred to the NCR 8496.
$\overline{RST}$	9	INPUT: Master Reset $\overline{RST}$ is used for testing purposes only. This pin is a no connect on the SN 76489A and is internally pulled high.
D7	10	Inputs: D0-D7 is the data bust through which data is transferred. D0 is the most significant data bit. D7 is the least significant data bit.
D6	11	
D5	12	
D4	13	
D3	15	
D2	1	
D1	2	
D0	3	
CLK	14	Input Clock

3.2 AUDIO APPLICATION INTERFACE

Signal	Pin	Description
Audio	7	OUTPUT: Audio signal to application. Refer to section 2.6. Output Circuitry for recommended output connections.
Audio In	9	INPUT: Audio input signal from application. Refer to section 2.7.

3.3 POWER INTERFACE

Signal	Pin	Description
VCC	16	Supply Voltage
GND	8	Ground Reference

SECTION 4

ELECTRICAL CHARACTERISTICS

4.1 OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Max	Units
Supply Voltage	V_{CC}		4.5	5.5	V
Supply Current	I_{CC}	Outputs Open		40	mA
Operating Temperature	T_O		0	+70	°C
Storage Temperature	T_S		-65	+150	°C
Absolute Maximum	V_{max}	To Any Pin		7.0	V

4.2 INPUT CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Max	Units
Input Voltage Low	V_{IL}	D0-D7, $\overline{WE}$, $\overline{CE}$, CLK		0.8	V
Input Voltage High	V_{IH}	D0-D7, $\overline{WE}$, $\overline{CE}$, CLK	2.0		V
Input Current	I_I	V_{in}-GND→V_{CC}	-10	+10	uA
Input Capacitance	C_I			15	pf

4.3 OUTPUT CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Max	Units
Output Voltage Low	V_{OL}	I_{OUT}=-2mA (READY)		0.4	V

4.4 AUDIO CHARACTERISTICS

Parameter	Symbol	Conditions	Typ	Max	Units
Audio Input Current		Causing half scale output swing		2.0	mA
Source Current	I_{SO}	Over Output Voltage Swing		-3	mA
Sink Current	I_{SO}	Over Output Voltage Swing		2	mA
Quiescent Output	V_{OQ}		2.1		V
Maximum Output	V_{OM}	Generators at 0dB	0.5		V
Signal Swing	V_{SW}	Generators at 0dB	450		mV
Capacitance Loading *	C_{OL}	From Pin 7 to Ground for Stability		200	pf
Audio Input Bias Voltage		R=4.7k ohms	1.0V	1.2V	

* Does not apply to coupling capacitors which are connected to loads >500 ohms. It is recommended that capacitors to ground be isolated by a series resistance of 500 ohms for stability.

SECTION 5

TIMING REQUIREMENTS

Parameter	Symbol	Conditions	Min	Max	Units
CE READY	t_{CER}	CL=225pf RL=2K to VCC		150	nS
Frequency Input	CLOCK	Transition Time	.05	4	MHz
Set up Time	t_{su2} t_{sul}	Data $\rightarrow\overline{WE}$ $\overline{CE}\rightarrow\overline{WE}$	0		nS
Hold Time	t_h	Data $\rightarrow$READY	0		nS

DATA TRANSFER TIMING

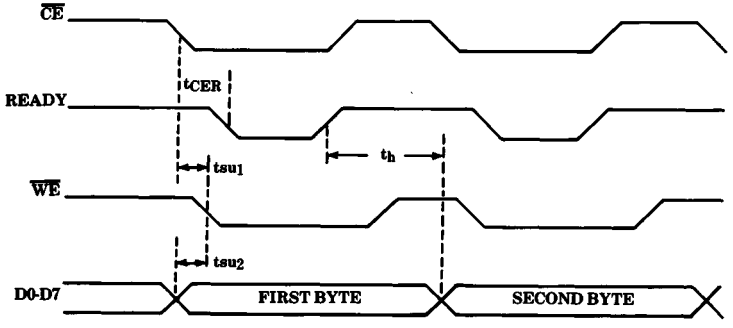


FIGURE 4

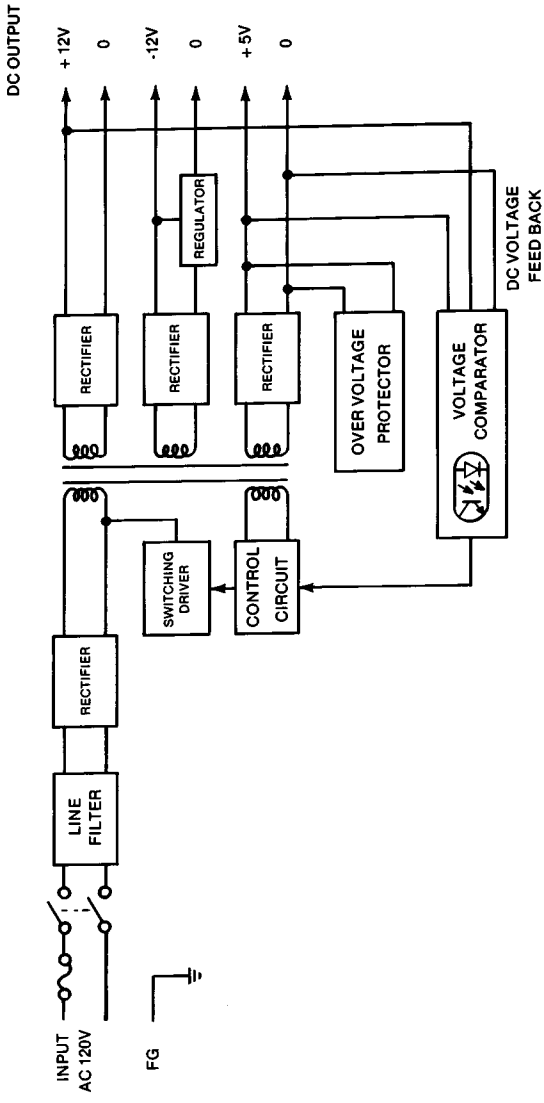
1000 HX Power Supply
(Single and Dual Input)

1000 HX 28 Watt Single Input Power Supply

1000 HX 28 Watt Single Input Power Supply
Contents

OPERATING CHARACTERISTICS

	MINIMUM	TYPICAL	MAXIMUM	UNITS
Operating Voltage Range	90	120	135	VAC
Line Frequency	47	50/60	63	Hz
Output Voltage				
Vol	4.85	5.00	5.15	V
Vo2	11.40	12.00	12.60	V
Vo3	-13.20	-12.00	-10.80	V
Output Loads				
Iol	1.25	-	3.0	A
Io2	0.1	-	1.25	A
Io3	0	-	0.1	A
Over Current Protection				
Current Limit ICL1	-	-	6.0	A
ICL2	-	-	2.5	A
ICL3	-	-	1.0	A
Over Voltage Protection				
Crowbar	5.8	-	6.8	V
Output Noise				
Vol	-	-	50	mV P-P
Vo2	-	-	100	mV P-P
Vo3	-	-	150	mV P-P
Efficiency	65	69	-	%
Holdup Time				
Full Load at Nominal Line	16	-	-	mSec
Insulation Resistance				
Input to Output	7	1000	-	M ohms
Input to Ground	7	1000	-	M ohms
Isolation				
Input to Ground	1.7	-	-	KVDC



Power Supply Block Diagram

Theory of Operation

AC Input Circuit

This circuit is composed of an AC Power Switch, a fuse, a line filter, and an inrush current limiting circuit and rectifying smoothing circuit. The inrush current limiting circuit controls the charging current to electrolytic capacitors when power is ON. The line filter reduces noise that leaks from the power source to the AC line or that returns from the unit to the power souce; it satisfies the specifications of noise regulations.

Control Circuit & Power Converter Circuit

This circuit is a self oscillation switching system, generally called an R.C.C. (Ringing Choke Converter). The R.C.C. circuit does not fix the oscillating frequency. Whenever input voltage is high or the load becomes light, the oscillating frequency will be high.

The current through R2 supplies transistor Q1's base, then Q1 turns ON. When transistor Q1 is On, the Q1 current excites the transformer T1 and voltage rises in the bias coil of T1(5-6) which leads transistor Q1 positive bias, then transistor Q1 turns ON.

When transistor Q1 turns ON, collector current charges the energy to primary inductance of transformer T1 (1-3). Increasing the collector current of transistor Q1 to the point of:

$$I_C = I_B .h_{fe}$$

Then, transistor Q1 immediately turns OFF. In a moment, transformer T1 will have negative voltage which will be supplied to the secondary circuit through a rectifier. A Short Circuit Protector is provided to protect transistor Q1 from excess amounts of current when the secondary circuit becomes shorted. When transistor Q2 detects the voltage drop at R8, the collector of Q2 shorts the base and emitter of Q1. Then Q1 stops working so that the circuit protects Q1 from over current.

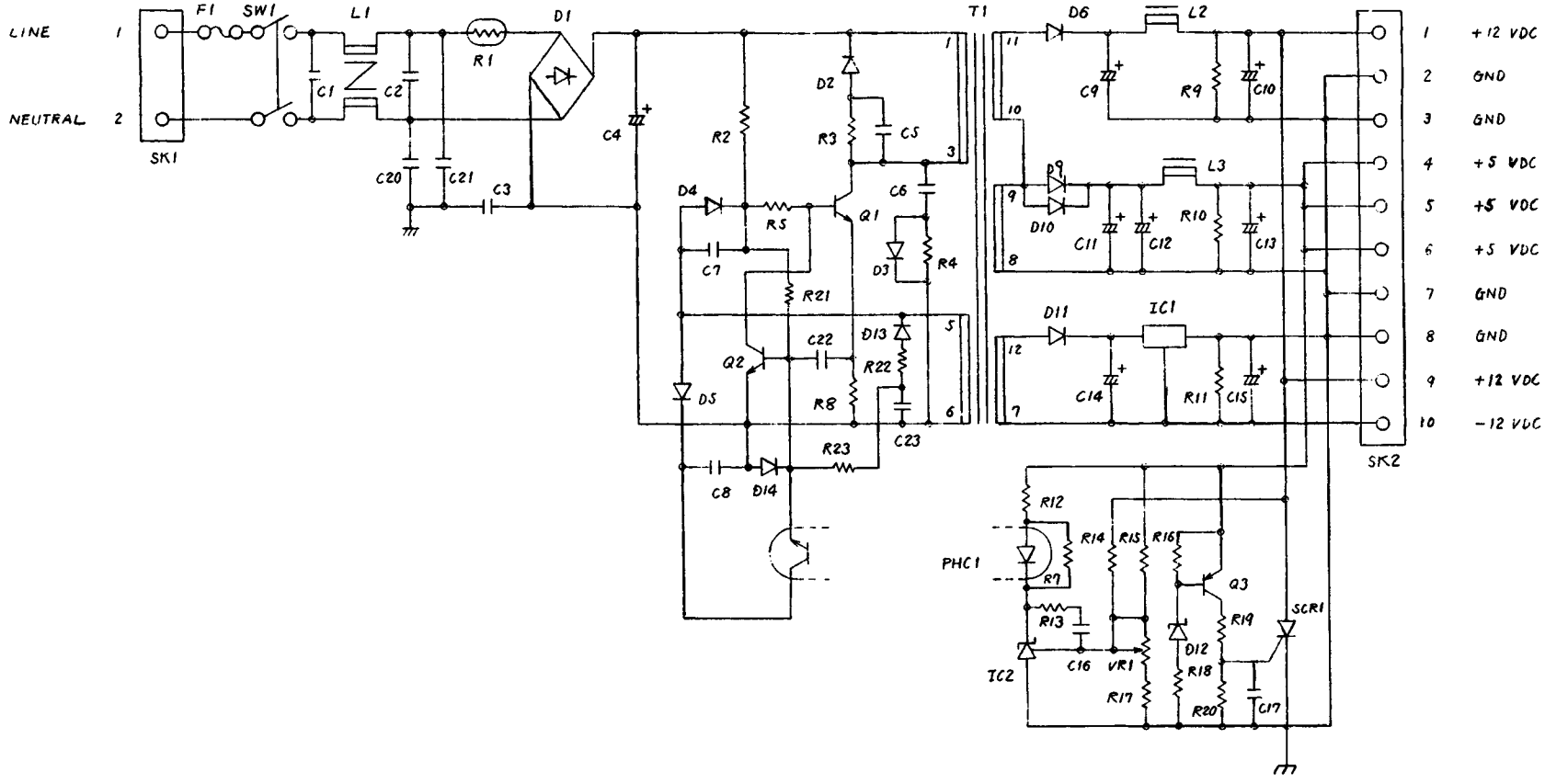
The over current protector in the -12V line is provided by the three terminal positive voltage regulator IC1 (built-in current fold back protection), which protects Q1 against excessive current from the -12V line.

5V Output Voltage Detecting Circuit

The circuit detects the change of output load current comparing with the output voltage and AC line input voltage, which feeds back to the control circuit through a photo coupler to keep the output voltage stable. The Photo coupler isolates the primary and secondary circuits.

Over-Voltage Protection

When the +5 output voltage rises, between 5.8V to 6.8V, the +12V circuit will be shorted by the Thyristor SCR1 under the control of zener diode D12, and then the supply shuts down because of the over current protection. In the above case, correct the cause of the failure, and reinput the power. The overvoltage protection circuit will reset automatically under good conditions.



DWN	K.Miyajima	8790083	3P-M1-0163
CHKD	A.Imura		
APPD	T.Fukayama		

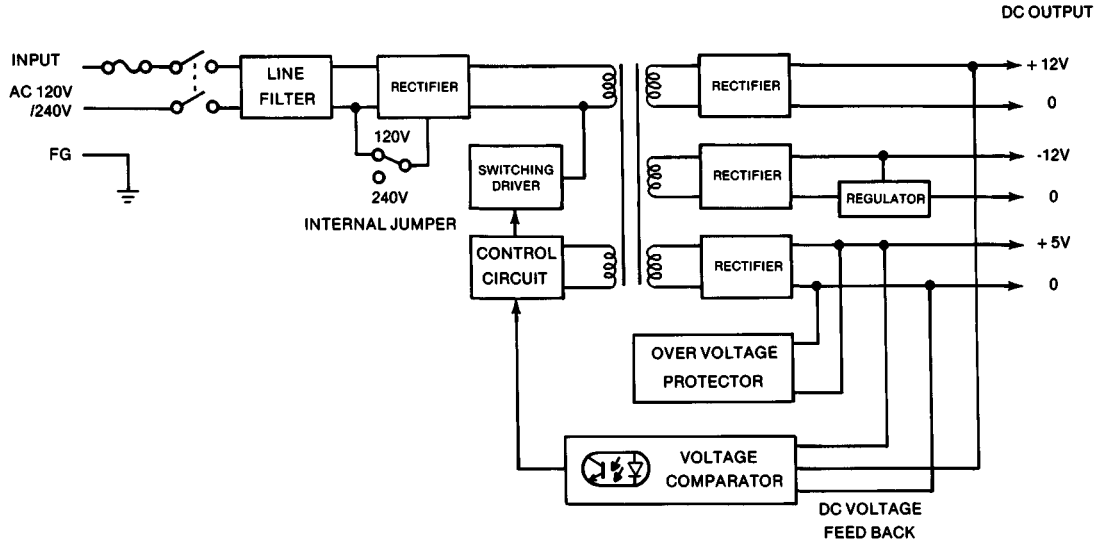
TAMURA SEISAKUSHO CO., LTD.

1000 HX 28 Watt Dual Input Power Supply

1000 HX 28 Watt Dual Input Power Supply
Contents

OPERATING CHARACTERISTICS

	MINIMUM	TYPICAL	MAXIMUM	UNITS
Operating Voltage Range	90 198	120 240	135 264	VAC
Line Frequency	47	50/60	63	Hz
Output Voltages				
Vol	4.85	5.00	5.15	V
Vo2	11.40	12.00	12.60	V
Vo3	-13.20	-12.00	-10.80	V
Output Loads				
Iol	1.25	-	3.0	A
Io2	0.1	-	1.25	A
Io3	0	-	0.1	A
Over Current Protection				
Current Limit ICL1	-	-	6.0	A
ICL2	-	-	2.5	A
ICL3	-	-	1.0	A
Over Voltage Protection				
Crowbar	5.8	-	6.8	V
Output Noise				
Vol	-	-	50	mV P-P
Vo2	-	-	100	mV P-P
Vo3	-	-	150	mV P-P
Efficiency	65	69	-	%
Holdup Time				
Full Load at Nominal Line	16	-	-	mSec
Insulation Resistance				
Input to Output	7	1000	-	M ohms
Input to Ground	7	1000	-	M ohms
Isolation				
Input to Ground	1.25	-	-	KVAC
Input to Output	3.75	-	-	KVAC



POWER SUPPLY BLOCK DIAGRAM

Theory of Operation

AC Input Circuit

This circuit is composed of an AC Power Switch, a fuse, a line filter, and an inrush current limiting circuit and rectifying smoothing circuit. The inrush current limiting circuit controls the charging current to electrolytic capacitors when power is ON. The line filter reduces noise that leaks from the power source to the AC line or that returns from the unit to the power souce; it satisfies the specifications of noise regulations.

Control Circuit & Power Converter Circuit

This circuit is a self oscillation switching system, generally called an R.C.C. (Ringing Choke Converter). The R.C.C. circuit does not fix the oscillating frequency. Whenever input voltage is high or the load becomes light, the oscillating frequency will be high.

The current through R3 supplies transistor Q1's base, then Q1 turns ON. When transistor Q1 is On, the Q1 current excites the transformer T1 and voltage rises in the bias coil of T1(5-6) which leads transistor Q1 positive bias, then transistor Q1 turns ON.

When transistor Q1 turns ON, collector current charges the energy to primary inductance of transformer T1 (1-3). Increasing the collector current of transistor Q1 to the point of:

$I_C = I_B .hfe$

Then, transistor Q1 immediately turns OFF. In a moment, transformer T1 will have negative voltage which will be supplied to the secondary circuit through a rectifier. A Short Circuit Protector is provided to protect transistor Q1 from excess amounts of current when the secondary circuit becomes shorted. When transistor Q2 detects the voltage drop at R8, the collector of Q2 shorts the base and emitter of Q1. Then Q1 stops working so that the circuit protects Q1 from over current.

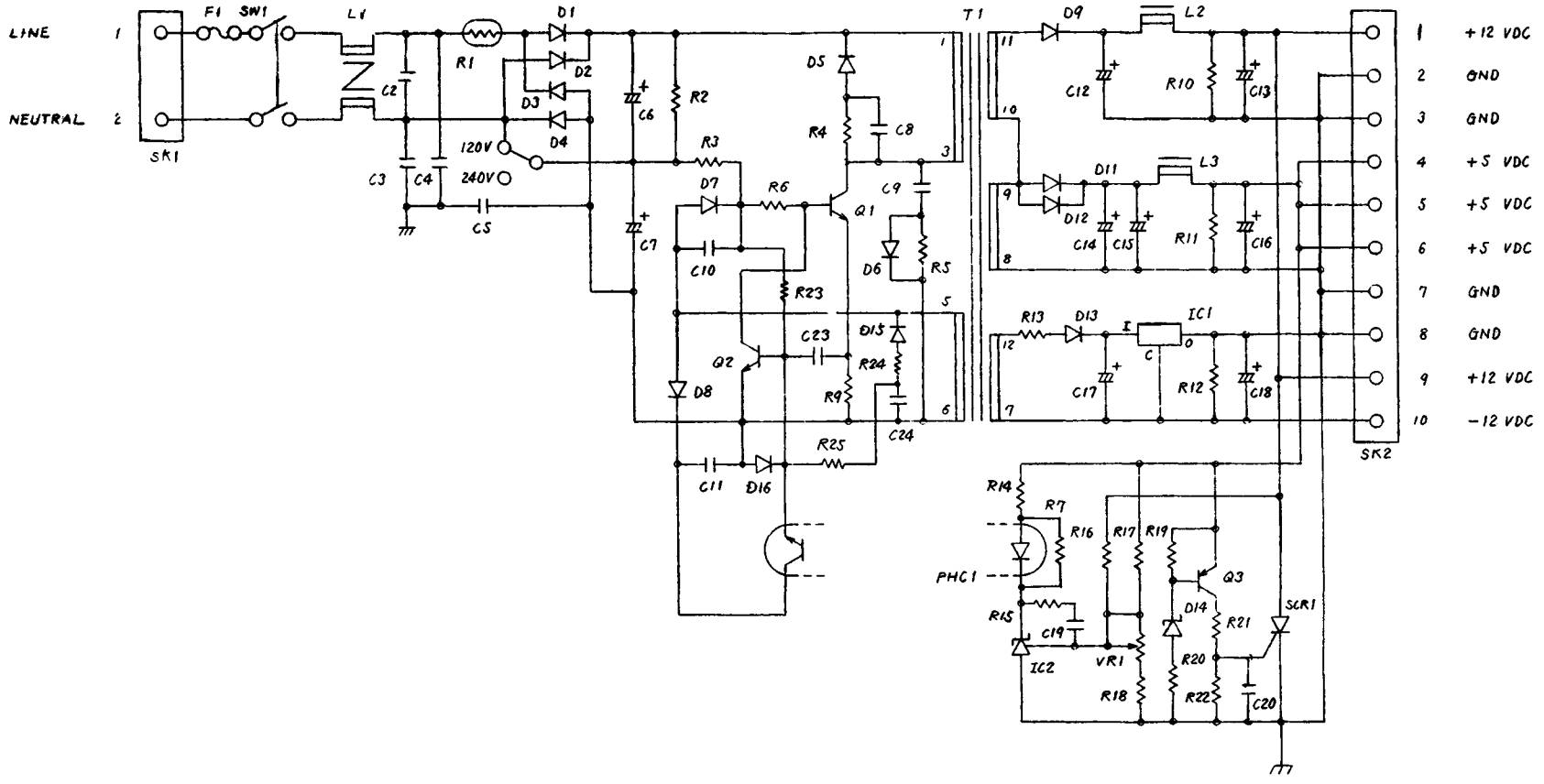
The over current protector in the -12V line is provided by the three terminal positive voltage regulator IC1 (built-in current fold back protection), which protects Q1 against excessive current from the -12V line.

5V Output Voltage Detecting Circuit

The circuit detects the change of output load current compared with the output voltage and AC line input voltage, which feeds back to the control circuit through a photo coupler to keep the output voltage stable. The Photo coupler isolates the primary and secondary circuits.

Over-Voltage Protection

When the +5 output voltage rises, between 5.8V to 6.8V, the +12V circuit will be shorted by the Thyristor SCR1 under the control of zener diode D14, and then the supply shuts down because of the over current protection. In the above case, correct the cause of the failure, and reinput the power. The overvoltage protection circuit will reset automatically under good conditions.



DWN	K. Miyajima	8790086	3P-M1-0159
CHKD	A. Miura		
APPD	T. Yokoyama		

TAMURA SEISAKUSHO CO., LTD.

1000 HX 25.6 Watt Power Supply

1000 HX 25.6 Watt Power Supply
Contents

ELECTRICAL SPECIFICATION

INPUT VOLTAGE:

Min. 90 at 47 Hz
Nominal 120 at 60 Hz
Max. 135 at 63Hz

INPUT SURGE CURRENT:

Limit ---------- 25A max.

EFFICIENCY:

At full rated load with 120 VAC input at 50/60 Hz.
Nominal ---------- 69%
Limit ---------- 65% min.

OUTPUT VOLTAGE:

	NOMINAL VOLTAGE	REGULATION TOLERANCE	LIMITS
Vo1	+5.0 VDC	+/- 3%	4.85 to 5.15 VDC
Vo2	+12.0 VDC	+/- 5%	11.4 to 12.6 VDC
Vo3	-12.0 VDC	+/- 10%	-13.2 to -10.8 VDC

OUTPUT RIPPLE AND NOISE VOLTAGE:

OUTPUT		RIPPLE AND NOISE VOLTAGE
Vo1	+5V	50mV p-p
Vo2	+12V	100mV p-p
Vo3	-12V	150mV p-p

Note: Ripple is defined as a composite of a power line frequency component plus a high frequency component due to the power oscillator. Common mode noise which may be observed due to oscilloscope connections will be ignored.

OUTPUT OVER VOLTAGE PROTECTION:

The +5V output shall be protected from over voltage fault conditions crowbar circuitry that is set to trip in the range of 5.6 to 6.8V.

OUTPUT STABILITY:

The power supply must remain stable for any step load current change during any combination of input line voltage and output current loading between and including rated minimum and maximum values. The output loads may include capacitance of up to 500 microfarads on the +5V output, up to 250 microfarads on either +/- 12V output.

OUTPUT TRANSIENT RESPONCE:

For a step load current change of the positive twelve volt output between rated minimum and maximum values, the maximum voltage excursion of the positive twelve volt output shall be 600 millivolts and of the positivre five volt output shall be 150 millivolts.

OUTPUT HOLDUP TIME

Nominal Line ------- 16msec. min.
Low Line ---------- 10msec. min.

OUTPUT CURRENT

OUTPUT		MINIMUM LOAD	MAXIMUM LOAD
Vol	-5V	1.25A	2.6A(3.2A Surge for 400 msec.)
Vo2	-12V	0.1A	1.0A(1.8A Surge for 400 msec.)
Vo3	+12V	0	0.05A

The maximum continuous output is 25.6 Watts.

OUTPUT CURRENT LIMITING

Over current protection wil prevent damage to the power supply when any output is short circuited continuously with 100 milliohms or less. Protection circuitry shall shutdown the output if the continuous output current level should exceed 200% or more of its maximum output rating. Damage to the power supply should not occur if operated up to its maximum over current limit.

ENVIRONMEMTAL REQUIREMENTS

Operating Temperature Range	0 ° C to +50 ° C
Storage Temperature Range	-40 ° C to +70 °
Operating Humidity	90% RH at 50 ° C
Storage Humidity	95% RH at 50 ° C

SAFTEY REQUIREMENT

The P.S.U. is compiled with U.L. standard 114 and compiled with CSA standard 22.2 No. 154-M1983.

LINE CONDUCTED EMI

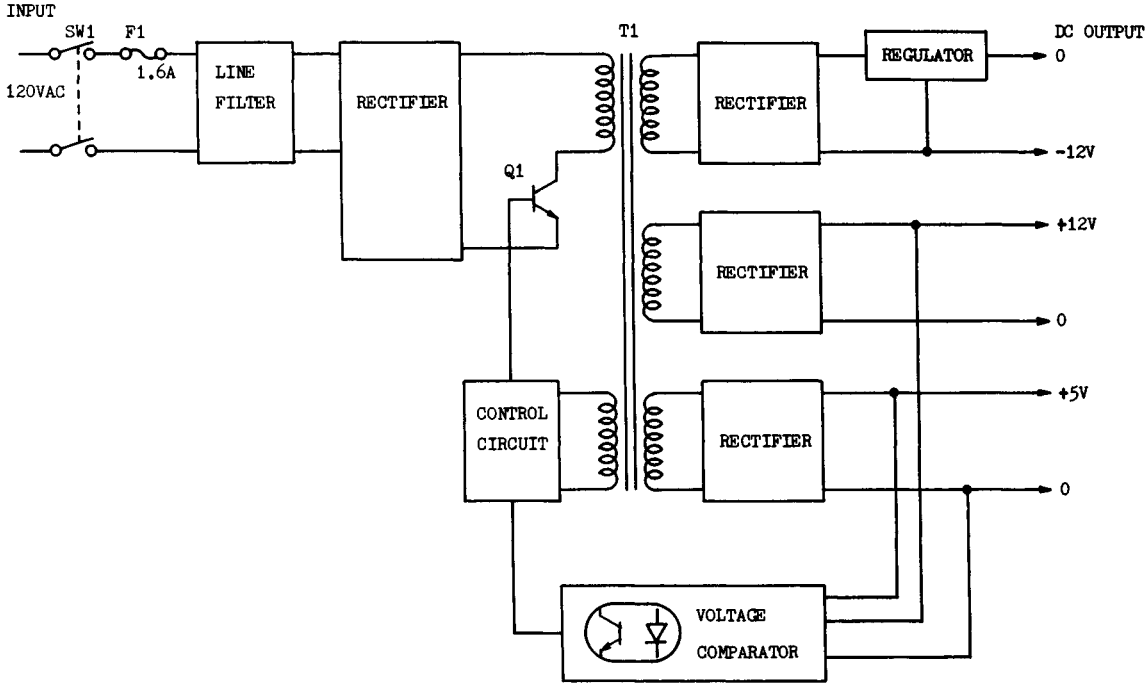
For 120VAC input operation the power supply must exceed the FCC Part 15J class B, computing device with 3dB margin at 450 kHz increasing linearly to 8dB margin at 1.0 MHz and with 8dB margin from 1.0 to 30 MHz. Line conducted noise is measured at the operating AC input for all output loads from minimum to maximum. Line conducted EMI shall be measured in a configuration representative of the intended application and in compliance with the required standards.

LINE TRANSIENT

The power supply shall meet the line transient requirements of IEE 472-1974 for the Common Mode and Differential Mode operation.

MECHANICAL SPECIFICATIONS

Dimension: 3P-K1-0268
Weight: Approx. 220g



POWER SUPPLY BLOCK DIAGRAM

Theory of Operation

AC Input Circuit

This circuit is composed of an AC power switch, a fuse, a line filter, an inrush current limiting circuit and rectifying smoothing circuit. The inrush current limiting circuit controls the charging current to the electrolytic capacitors when power is ON.
The line filter reduces noise from the power source to the AC line and return noise from the unit to the power source; it satisfies the specifications of the noise regulations.

Control Circuit and Power Converter Circuit

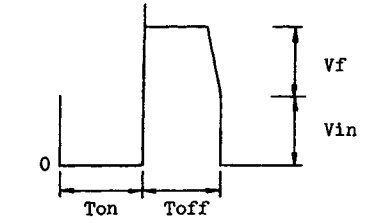
This circuit is an oscillation switching system, generally called R.C.C. (Ringing Choke Converter). The R.C.C. circuit does not operate at a fixed oscillating frequency. Whenever the input increases and the load decreases, the oscillating frequency will increase.
The circuit system feeds the current through R2 suppling transistor Q1's base, then Q1 turns ON. When transistor Q1 is set to ON, the Q1 current excites transformer T1 and the voltage rises in the bias coil of T1 (4-5) which leads transistor Q1 positive bias, then transistor Q1 turns ON.

When the transistor Q1 becomes ON, the Collector current changes the energy to primary inductance of transformer T1 (1-3). Increasing the collector current of transistor Q1 to the point of:

$I_C > I_B$:hfe

Then, transistor Q1 immediately turns OFF. In a moment, transformer T1 will have negative voltage which will be supplied to the secondary circuit.
A Short Circuit Protector is provided for protection of transistor Q1 from excess amounts of current when the secondary circuit is shorted. When transistor Q2 detects the voltage drop at R8, the collector of Q2 shorts the base and emitter of Q1. Then Q1 stops working so that the circuit protects Q1 from excess current.
The over current protector in the -12V line is provided by the three terminal positive voltage regulator IC1 (built-in current fold back protection), which protects Q1 against excessive current from the -12V line.

Power Converter Circuit



Collector Voltage Waveform


Collector Current Waveform

The input and output voltage are represented by the following equations:

Vo = n x Vf

Vo : Output Voltage
n : Turn ratio of transformer Tl
Vf : Collector voltage at turn-off time

Vin x Ton = Vf x Toff

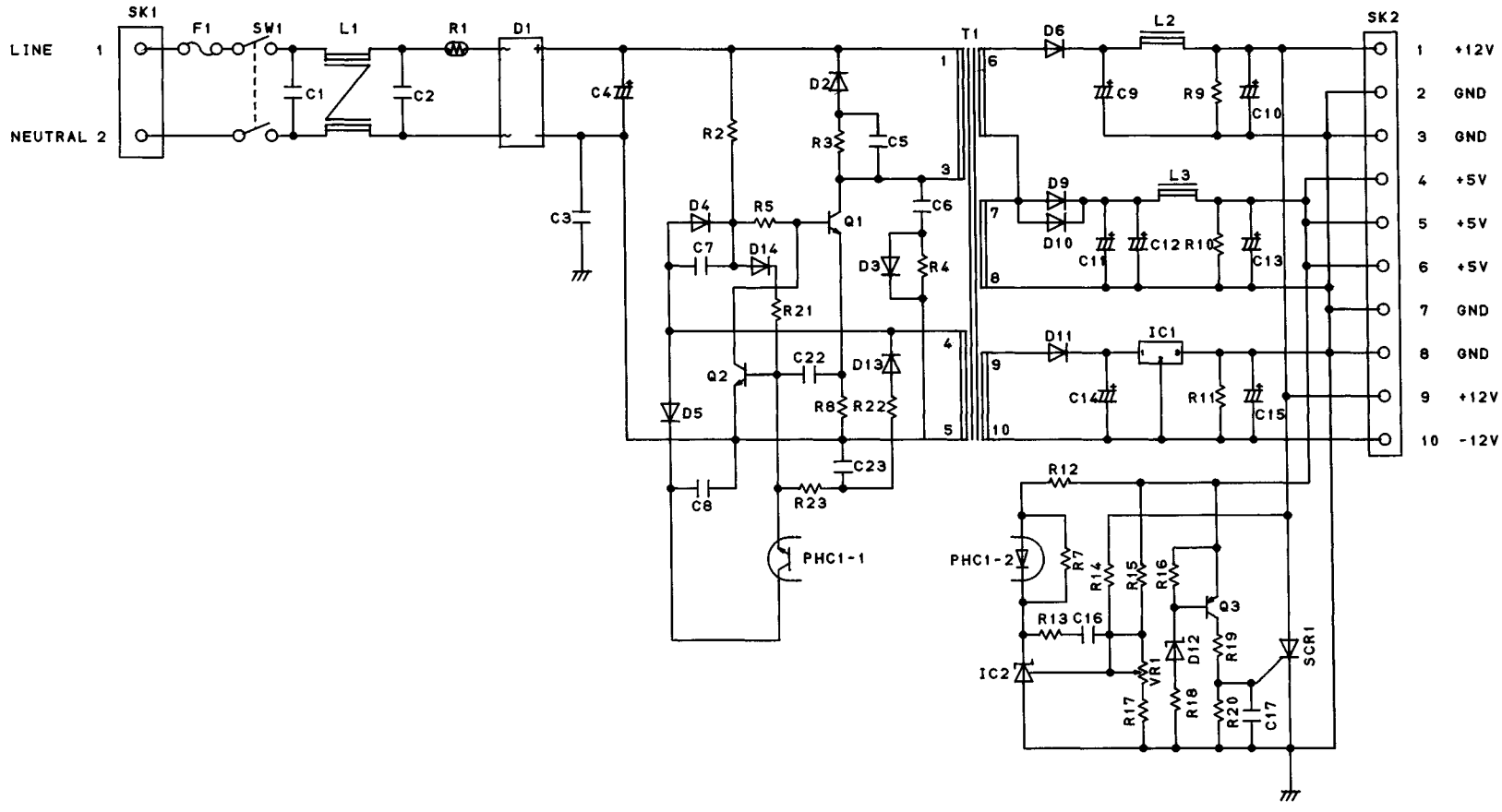
Vin : Input voltage
Ton : Turn-on time of transistor
Toff: Turn-off time of transistor

5V Output Voltage Detecting Circuit

The circuit detects the change of output load current by comparing the output voltage and AC line input voltage, which feeds back to the control circuit through a photo coupler to keep the output voltage stable.

Over Voltage Protection

When the output voltage is 5.8V to 6.8V, the +12V circuit is shorted by thyristor SCR1 under the control of zener diode D12, and then the supply shuts down because of the over current protection.



model no. 8790093

1000 HX Keyboard

1000 HX Keyboard
Contents

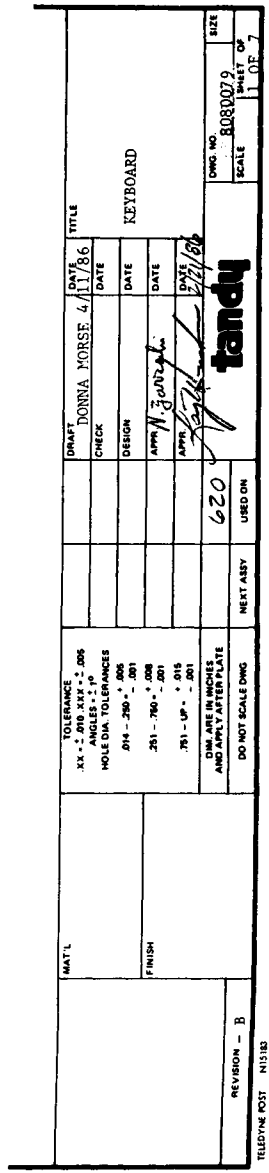
SPECIFICATION

NON-ENCODED KEYBOARD MATRIX

* REV-A 12-18-85

* REV-B 2-11-86

SEE SHEET 1A FOR REVISIONS



REV.	DESCRIPTION	DATE	APPD
C	PAGE 6: 11/5/85 REMOVED LEDS FROM KEYCAPS; DELETED NOTE OF LEDS; ADDED LED FLANGE & .150 SLOTS; .438 WAS .563; ADDED SH. 2. 11/5/85 RELEASED FOR QUOTATION ONLY 12/2/85 ADDED 3RD LED MOUNTING HOLE; MOVED J1 OFF C.L.; 5.81 WAS 5.75; ADDED SPLIT CABLE OPTION AND INCREASED OVERALL WIDTH & MOUNTING DIMS; DWG. WAS #8010010. 1/10/86 DELETED SINGLE CABLE OPTION; CHG'D 8 & 12 POSITION CABLES TO 12 & 13 POSITION CABLES, RESPECTIVELY. 2/20/86 SPACE BAR WAS CHANGED FROM 9 KEY LENGTH TO 8 KEY LENGTH. 4/11/86 ADDED PAGE 7. 4/11/86 REVISED CABLE ASSY., ADDED "J1" & "J2" DETAIL. RELEASED FOR PRODUCTION	4/11/86	
D	REVISED CABLE LENGTHS: 5.84 WAS 6.43, 6.11 WAS 6.70, 6.39 WAS 6.98, 6.63 WAS 7.22.	5/15/86	

SPECIFICATION
NON-ENCODED KEYBOARD MATRIX

1. Scope

This specification covers a keyboard.

2. Electrical Characteristics

2-1 Contact Resistance :

500 Ohm Max.,5Vdc 1mA

2-2 Contact Bounce :

10msec Max. (operating speed at 250 mm/sec)

2-3 Insulation Resistance :

50Mohm Min. at 250Vdc (between switch contacts)

2-4 Dielectric Withstand Voltage :

250 Vdc for 1 minute (betweem PCB pattern and iron panel)

150 Vdc for 1 minute (between switch contacts)

3. Mechanical Characteristics

3-1 Operating Force :

70g+/-25g at full stroke (at center of keycap)

3-2 Plunger Stroke :

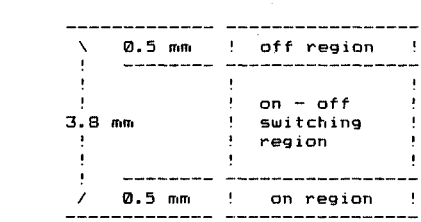
3.8mm+/-0.5

3-3 Operating Point :

0.5mm Mim. to full stroke

3-4 Release Point :

0.5mm Min. to free position



4. Operating Life *

4-1 Life :

10Meg (10 million operation)

4-2 Contact Resistance :

500ohm Max. (upto 10 million), 800ohm (after 10 million)

4-3 Contact Bounce :

10msec Max. (after 10Meg)

* Conditions

(1) 5Vdc 1mA (resistive load)

(2) Operation Speed : 5 Hz

(3) Depression Force: 200g Max. (at center of keyboard)

5. Environmental Characteristics

5-1 Operating Temperature Range :

0 to 55 degrees C

5-2 Storage temperature Range :

-10 to 65 degrees C

5-3 Humidity :

10% to 95% RH (non-condensing), 45 degrees C Max.

5-4 Altitude :

-1000ft to 10000ft

5-5 Vibration :

10 to 55 Hz 1.5mm (along each of the orthogonal axis)

5-6 Shock :

50G, 11 msec 1/2 sine wave, 3 directions each 3 times.

6. Safety Standards

Keyboard must meet; UL standard 114
, CSA SPEC: C22.2 NO.0-M1982
, CSA SPEC: C22.2 NO.154-M1983

Detailed material specification will be determinded at the approval time.

7. Keycaps

7-1 Keycaps Configuration :

Keycaps must be detachable. Keycaps are preferred to look exactly the same as they are shown on.D-size drawing NO. 8080079.

7-2 Keycaps Color :

Keycaps colors are specified on the D-size drawing NO.8080079

7-3 Legends :

Legends must be in black and are printed flat on the keycaps as they appear on the D-size drawing. Two shot molding or sublimation printing is preferred.

8. Drawings

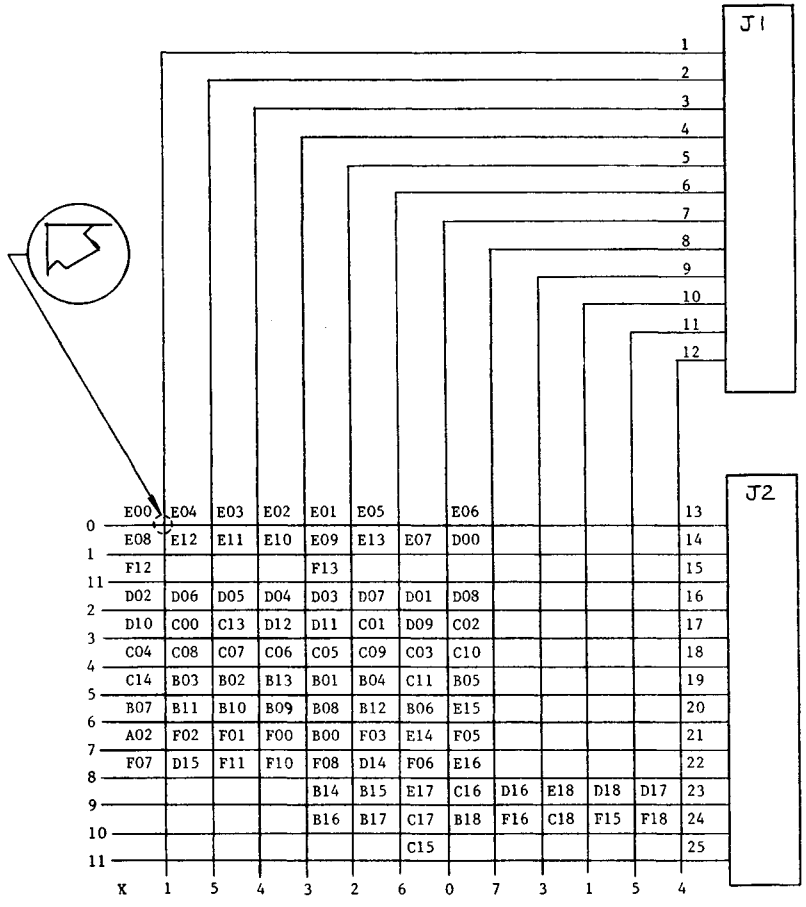
8-1 Mechanical Specifications & Keytop Arrangement :

D-8080079 Sheets 6 and 7 of 7

8-2 Circuit Specification :

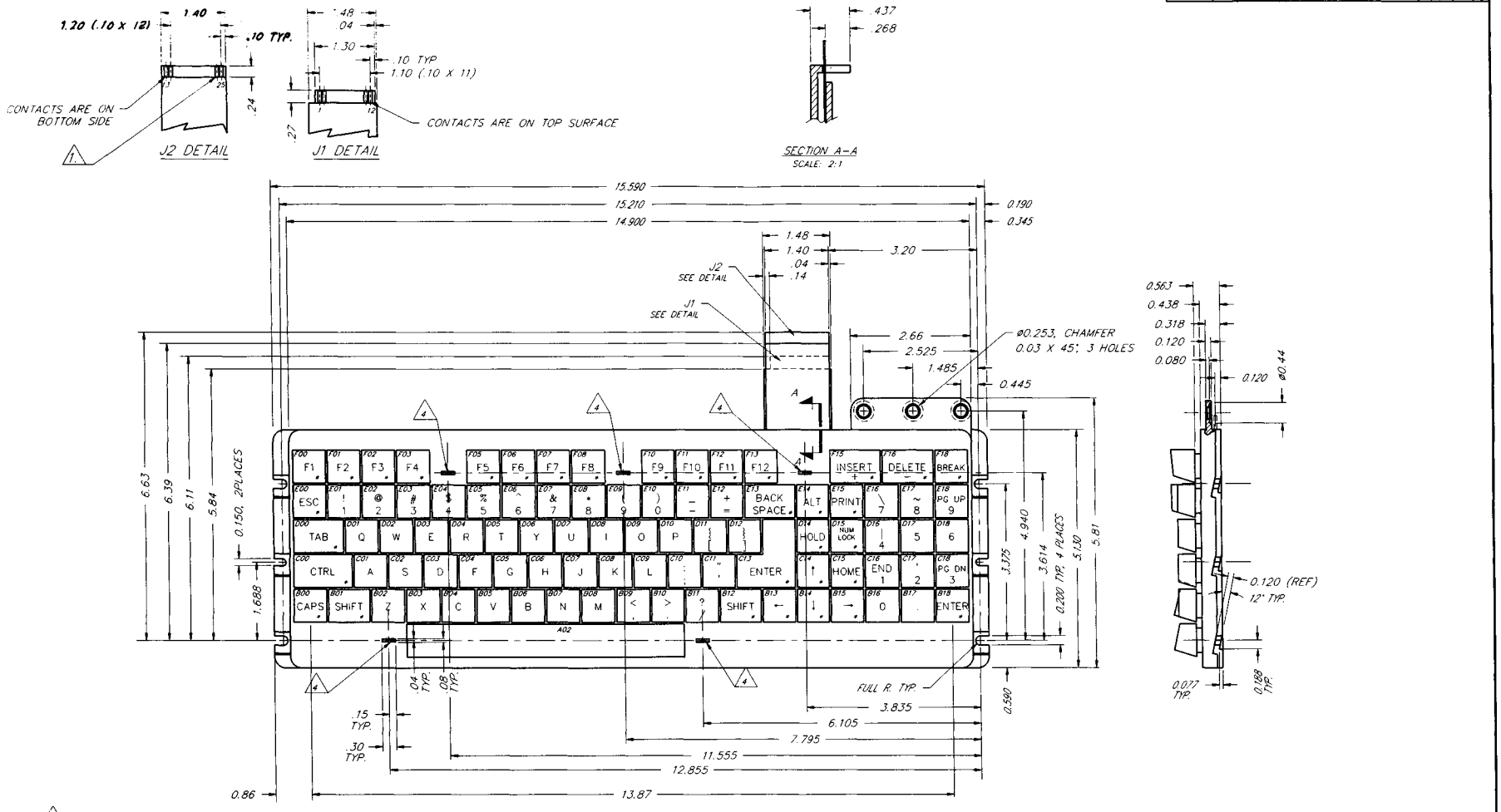
B-8080079 Sheet 5 of 7

REVISION			
LTR	DESCRIPTION	DATE	APPD
–	RFQ	2-12-86	



NOTES (UNLESS OTHERWISE SPECIFIED)

MAT'L	UNLESS OTHERWISE SPECIFIED		DRAFT	DATE 2-12-86	TITLE SPECIFICATION- KEYBOARD CIRCUIT
	TOLERANCE XX = ± .010 XXX = ± .005 ANGLES = ± 1°		CHECK	DATE	
			DESIGN	DATE	
FINISH			APPD	DATE	
			APPD	DATE 2/11/86	
	DIM. ARE IN INCHES AND APPLY AFTER PLATING		TANDY	DWG. NO. B-8080079	
	DO NOT SCALE DWG.	USED ON		SCALE NTS	SHEET 5 OF 7



4. NO SCREWS, ETC. IN THIS AREA.
3. SHEETS 1, 2, & 3 ARE "A" SIZE; SHEET 5 IS "B" SIZE.
2. KEYCAPS COLOR: ALL KEYCAPS WITH "•" IN RIGHT CORNER HAVE THE COLOR CODE: UBE CYCON AM-134914-3
ALL OTHERS (UNMARKED) HAVE THE COLOR CODE: UBE CYCON EX 111-124369-2.
1. RIBBON CONNECTOR TRACES TO BE ON .100 CENTERS, POLARITY AS SHOWN.

NOTES:

MATERIAL	UNLESS OTHERWISE SPECIFIED TOLERANCES		DRAFT	DATE 10/4/85	TITLE LAYOUT — KEYBOARD
Finish			CHECK	DATE 12/11/86	
			DESIGN	DATE	
			APPD	DATE	
			APPD	DATE 12/11/86	
	DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING				
	DO NOT SCALE THIS DRAWING	USED ON	TANDY		DRAWING NO. 8080079
					SCALE 1:1 SHEET 6 OF 7

1000 HX Disk Drive

1000 HX Disk Drive
Contents

Specifications

of

MP-F63W-72D

Double Sided 80 Tracks
Recording Capacity 1MBytes
Transfer Rate 250 Kbits/sec
[TTL interface, without Ready signal]

VALID for MP-F63W-72D,
with the following serial numbers :

_____	_____	_____	_____	_____
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____
_____	_____	_____	_____	_____

SONY CORPORATION

MFD TECHNICAL INFORMATION 00-0054 REV. 11-87 Apr. 6, '87

*** Contents ***

1. Description

This document describes the specifications for the MP-F63W-72D of which the recording capacity is 1MB, the maximum track-to-track access time is 3 msec and a TTL compatible signal interface.
The main features of the MP-F63W-72D are low power consumption, low height, and nigh reliability with a simple mechanism and electric circuit.

NB: The specifications defined in this booklet are valid only if the drive is used with Sony media or any other ANSI specification media agreed upon by Sony and the drive customer.

2. Specifications

2.1 Configuration

The drive consists of Read/Write heads, head positioning mechanism, disk motor, interface logic circuit and Read/Write circuit.

2.2 Physical Dimensions

The detailed physical dimensions are shown in Figure 2.1.
The main dimensions are:

1) Height : 30 mm
2) Width : 101.6 mm
3) Depth : 150 mm
4) Weight : 480 g max.

2.3 Performance

2.3.1 Recording Capacity

Unformated capacity : 1.0 Mbyte/disk for MFM
0.5 Mbyte/surface for MFM
6.25 Kbyte/track for MFM

2.3.2 Transfer Rate

Burst transfer rate : 250 Kbits/sec for MFM

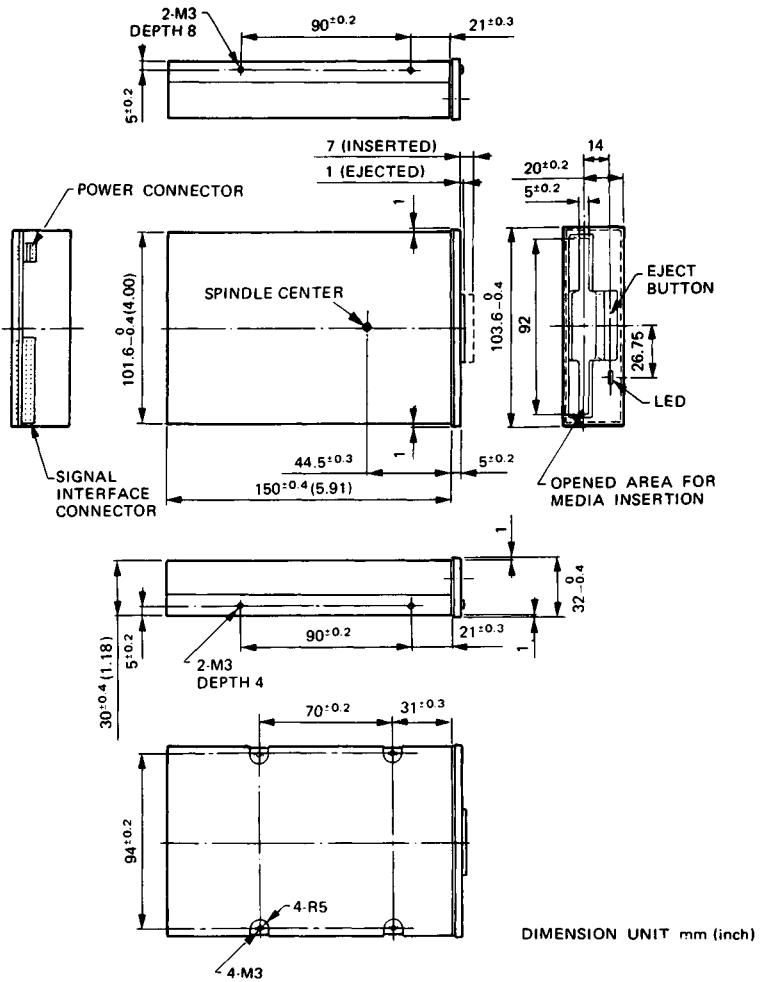


Figure 2-1. PHYSICAL DIMENSIONS

2.3.3 Access Time

a. Track to Track Slew Rate : 3 msec max.

b. Head Settling Time : 15 msec max.

c. Motor Start Time : 500 msec max.
(700 msec max.*)

Motor start time is defined as the time period necessary to stabilise the Motor Rotational Speed variance to less than +/-1.5% after turning the MOTOR ON signal on.

NB. When a disk is inserted in the drive, the Motor Start Time will be 700 msec at maximum, but, after that it will be 500 msec max. as the disk is kept inserted.

2.3.4 Functional

a. Rotation Speed : 300 rpm
The continuous speed variation is within +/-1.5%.
The instantanuous speed variation is within +/-1.0%.

b. Recording Density : 8717 BPI (Side 1, Track 79) in a 1MB mode

c. Track Density : 135 TPI

d. Cylinders : 80

e. Tracks : 160

f. R/W Heads : 2

2.3.5 Reliability

a. Mean Time Between Failures (MTBF) : 10,000 POH

b. Mean Time to Repair (MTTR) : 30 minutes

c. Preventive Maintenance (PM) : Not Required

d. Components life : 5 years or 15000 POH

e. Error Rate :

1. Soft Read Error : Less than 1 per 10^9 bits read

2. Hard Read Error : Less than 1 per 10^{12} bits read

3. Seek Error : Less than 1 per 10^6 seeks

2.4 Input Power Requirements

2.4.1 Power Consumption

	TTL Interface
Standby	250 mW
Operation (read/write mode)	2.8 W

2.4.2 Supply Voltages

Voltage	Max. Ripple	Current
+12.0V +/-5%	0.1Vpp	Standby 0.3 mA Average 130 mA (Read) Peak 500 mA (Motor Start) Peak 450 mA (stepping during Motor On)
+5.0V +/-5%	0.1Vpp	Standby 50 mA Operating 240 mA

2.5 Environmental Limits

2.5.1 Temperature Range

Operating : $5^{o}C$ to $50^{o}C$ ambient ($40^{o}F$ to $122^{o}F$)

Transportation : $-40^{o}C$ to $60^{o}C$ ($-40^{o}F$ to $140^{o}F$)

Storage : $-20^{o}C$ to $60^{o}C$ ($-20^{o}F$ to $140^{o}F$)

2.5.2 Humidity Range

Operating : 8% to 80% relative humidity with a wet bulb temperature of $29^{o}C$ (85F) and no condensation.

Transportation and Storage : 5% to 95% relative humidity and no condensation

2.5.3 Vibration

Operating : The unit can perform Read/Write operations without errors at continuous vibration from 10 to 500 Hz at a maximum of 0.5G along each of the three mutually perpendicular axes.

Transportation and Storage : The unit can withstand continuous vibration from 10 to 300 Hz with a maximum level of 2.0G along each of the three mutually perpendicular axes without any degradation of any characteristics below the performance specifications.

2.5.4 Shock

Operating : The unit can withstand a shock of 5.0G shock for 11 msec with a 1/2 sine wave shape in each of the three mutually perpendicular axis while performing normal read/write functions without damage or any loss of data.

Transportation and Storage : The unit when unpacked can withstand an 11 msec with a 1/2 sine wave shock of 60G on any of the three mutually perpendicular axes.

2.5.5 Orientation

The drive does not necessarily need to be horizontally positioned. In fact, as seen in figure 2-3, there are many other possible orientations.

3. Signal Interface

3.1 Connector and Pin Assignments

3.1.1 Signal connector

Receptacle : 3M 3414-6500xx or Equivalent

Cable : 3M 3365/34 or Equivalent

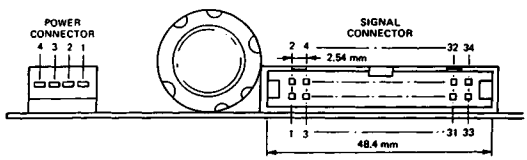


Figure 3-1. PIN ASSIGNMENT (REAR VIEW OF DRIVE)

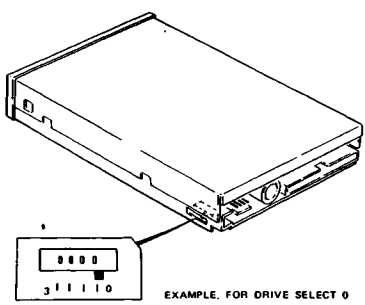


Figure 3-2. DRIVE SELECT SWITCH

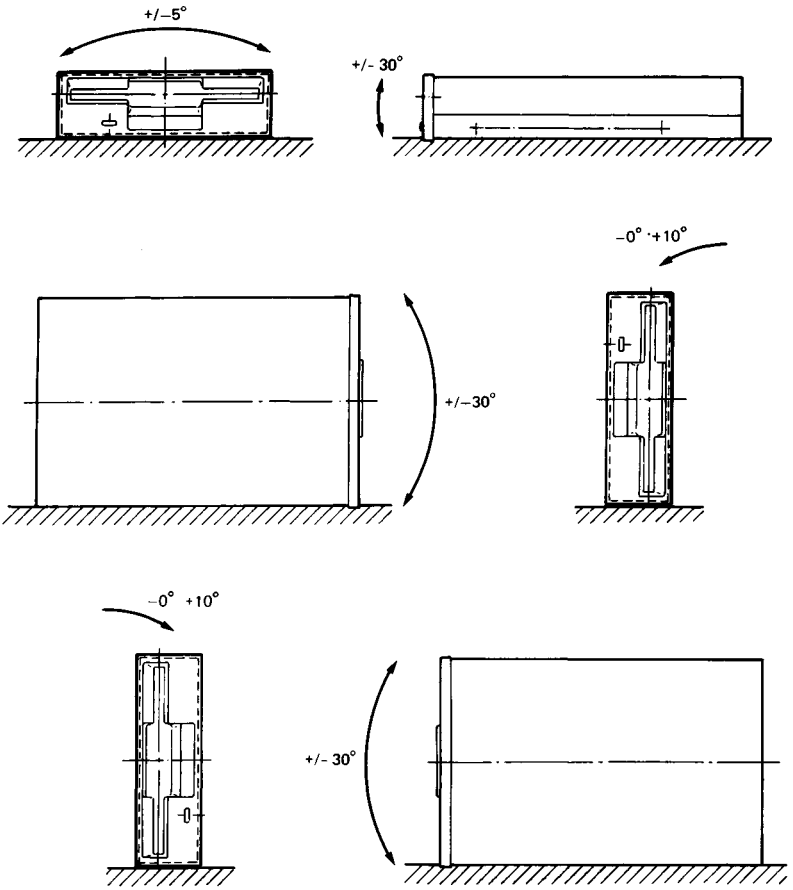


Figure 2-3. ORIENTATIONS

3.1.2 Signal Connector Pin Assignment

PIN	SIGNAL DESCRIPTION	PIN	SIGNAL DESCRIPTION
1	CN	2	N.C.
3	5V	4	N.C.
5	5V	6	DRIVE SELECT 3
7	5V	8	INDEX
9	5V	10	DRIVE SELECT 0
11	5V	12	DRIVE SELECT 1
13	RETURN	14	DRIVE SELECT 2
15	RETURN	16	MOTOR ON
17	RETURN	18	DIRECTION
19	RETURN	20	STEP
21	RETURN	22	WRITE DATA
23	RETURN	24	WRITE GATE
25	RETURN	26	TRACK 00
27	RETURN	28	WRITE PROTECT
29	12V	30	READ DATA
31	12V	32	HEAD SELECT
33	12V	34	DISK CHANGE

3.1.3 Power Supply Connector

Receptacle : AMP 171822-4 or Equivalent

Contact : AMP 170262-1 or Equivalent

Wire : AWG 20

3.1.4 Power Supply Connector Pin Assignment

PIN	SIGNAL DESCRIPTION
1	+5V
2	GND (+5V Return)
3	GND (+12V Return)
4	+12V

3.2 DC Characteristics of Interface Signals

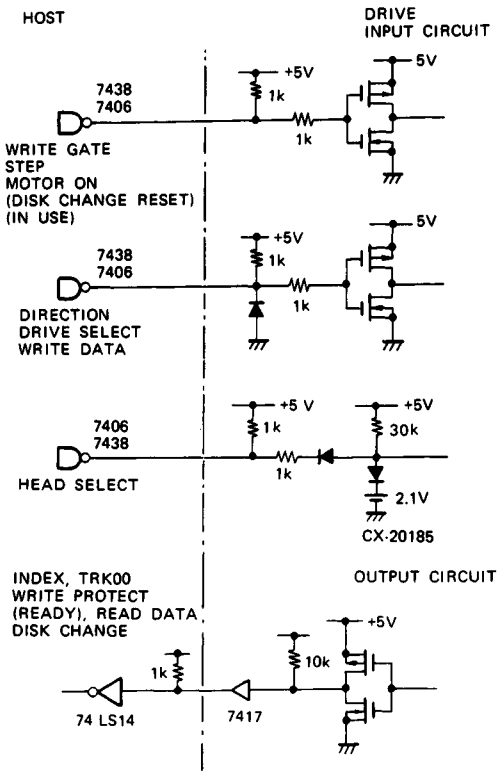
3.2.1 Output Signal from Drive

Name	Output Current IOH(mA)	IOL(mA)	Output Voltage VOH(V)	VOL(V)
TTL interface All outputs	0.25	40		0.7

3.2.2 Input Signal to Drive

Name	Input Current VIN=0.4V IIL(mA)	Input Voltage Threshold VIH(V)	VIL(V)
TTL interface All inputs	-5.0 (at +0.4V)	2.2	0.8

3.2.3 Recommended Circuit for Signal Interface



The Interface signals in parethesis are only for MP-F63W-72D The line from the drive to the controller should be pulled up by a resistor of 1K ohm.

The cable length must be less than 1.5m. (4.92ft.)

Recommended driver IC : 7406, 7438

3.3 Signal Definitions

3.3.1 DRIVE SELECT 0,1,2,3

The select lines are used to enable or disable all other interface lines except a MOTOR ON line. When the SELECT line is true (low), the drive is enabled and is considered active. When the SELECT line is false (high), all controller inputs except the MOTOR ON line are ignored and all output lines are disabled.

NB. IN USE (LED) lamp:
When a drive is selected, the IN USE lamp on the selected drive is turned on, and when a drive is not selected, it is turned off.

3.3.2 MOTOR ON

When this input is true (low) and a disk is inserted, the spindle motor will start to run. When this line is made false (high) or a disk is ejected, the spindle motor will decelerate and stop.

However, if the MOTOR ON signal becomes false (high) during either a write or erase operation, the disk motor will not stop rotating until both the ERASE GATE signal and the WRITE GATE signal become false (high).

3.3.3 STEP

When a drive is selected, a true (low) pulse on this line will cause the Read/Write head to move to the adjacent track. The direction of the head movement is determined by the DIRECTION input at the trailing edge of the pulse.
The step operation can be performed even if there is no disk inserted in the drive.

3.3.4 DIRECTION

When a drive is selected, a false (high) level on this input will cause a STEP pulse input to move the Read/Write head away from the disk spindle. A true (low) level will cause a STEP input to move the Read/Write head toward the drive spindle.

3.3.5 HEAD SELECT

When a drive is selected, a true (low) level on this input will cause Head 1 (upper) to be selected. A false (high) level on this input will cause Head 0 (lower) to be selected.

If the HEAD SELECT signal changes during either write or erase operation, the head will not be changed until both ERASE GATE and WRITE GATE signal becomes high (false).

3.3.6 WRITE GATE

When this line is made true (low) while a drive is selected, the write current circuits are enabled and information may be written under control of the WRITE DATA input.

3.3.7 WRITE DATA

If the WRITE GATE is true (low), a true pulse (low) on the WRITE DATA line causes a bit to be written on the disk. Pulses on this line are neglected when WRITE GATE signal is false (high).
No pre-compensation is required.

3.3.8 INDEX

When the drive is selected, a true (low) pulse is generated on this line by each revolution of the spindle.

3.3.9 TRACK 00

This line is true (low) when the drive is selected and the Read/Write head is positioned on track 00.

3.3.10 WRITE PROTECT

If a write-protect disk is inserted while a drive is selected, this line will be true (low) and the drive will not be able to write data. At all other times, except when a disk is ejected while the drive is selected, this line will be false (high).

3.3.11 READ DATA

When the drive is selected, a true (low) pulse is generated on this line every time a bit is detected.

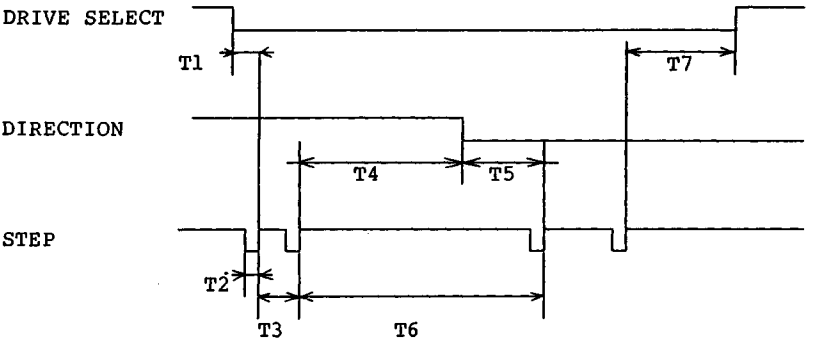
3.3.12 DISK CHANGE

This line is true (low) whenever a disk is removed from the drive. The line remains true (low) until both the following conditions have been met:

1. A disk is inserted,
and
2. A STEP pulse has been received when the drive is selected.

3.4 Timing Requirements

3.4.1 Head Access



T1 : 0.5 us min.

T2 : 1.3 us min.

T3 : 3.0 ms min.

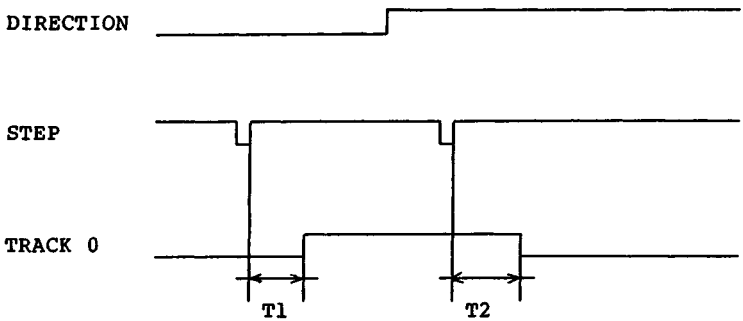
T4 : 2.4 us min.

T5 : 0.5 us min.

T6 : 18 ms min.

T7 : 2.5 us min.

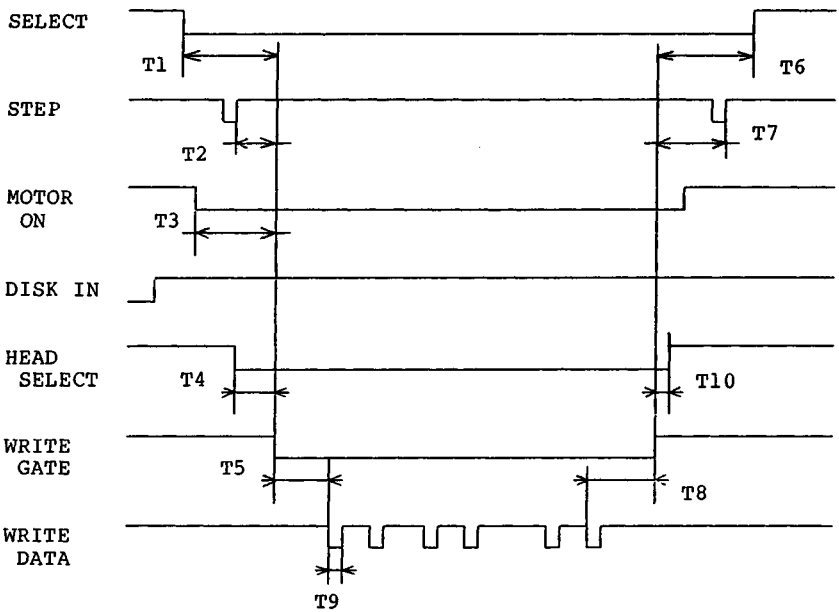
3.4.2 TRACK 00 Signal



T1 : 2.9 msec max.

T2 : 2.9 msec max.

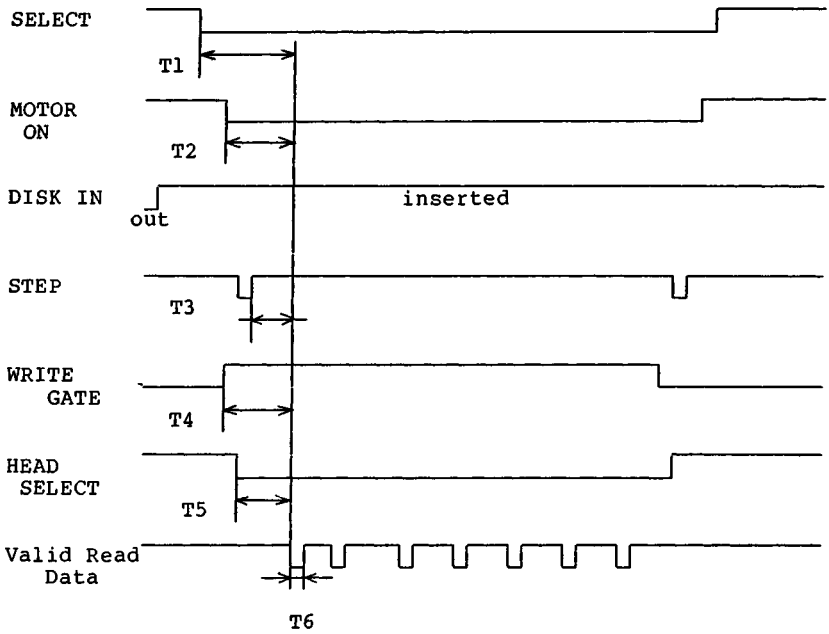
3.4.3 Write Data Timing



T1	:	0.5 us min.	T6	:	0.5 us min.
T2	:	18 ms min.	T7	:	1020 us min.
T3	:	500 ms max.*	T8	:	8.0 us min.
T4	:	100 us min.	T9	:	150 ns min., 2000 ns max.
T5	:	8 us max.	T10	:	See 3.3.5

***NB.** When a disk is inserted in the drive, the Motor Start Time is 700 msec at maximum, but, after that, it is 500 msec max. as the disk is kept inserted.

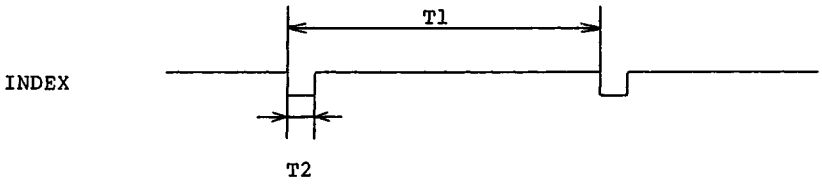
3.4.4 Read Data Timing



T1	:	0.5 us max.	T4	:	1050 us max.
T2	:	500 ms max.*	T5	:	100 us max.
T3	:	18 ms max.	T6	:	550 ns min., 1200 ns max.

NB. When a disk is inserted in the drive, the T2 is 700 msec at maximum, but, after that it is 500 msec max. as the disk is kept inserted.

3.4.5 Index Pulse

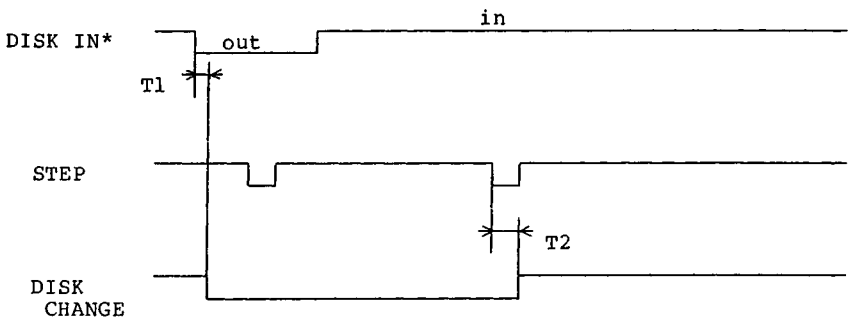


T1* : 197 ms min., 203 ms max.

T2 : 1.25 ms min., 1.45 ms max.

*When the disk motor rotation is at the stable state.

3.4.6 Disk Change



T1 : 0.5 us max. T2 : 1.6 us max.

*DISK IN, the disk-in sensor signal inside the drive, is high when a disk is inserted in the drive.

3.5 Power On and Power off Requirements

3.5.1 Data Protection

Turning power on or off does not cause any damage to recorded data on the disk as the drive is not in the midst of writing when the power is shut off or supplied.

3.5.2 Power Supply Sequencing

No special supply sequencing is required by the disk drive as long as both the 5V and 12V power supplies have a monotonic rise time of less than 100msec. When the power is turned off, although there are no sequencing or timing requirements, both power supplies must fall monotonically to 0V.

3.6 Disk motor rotation and Disk Insertion.

Even if the MOTOR ON signal is true (low), the disk motor does not rotate until a disk is inserted.

4. Safety

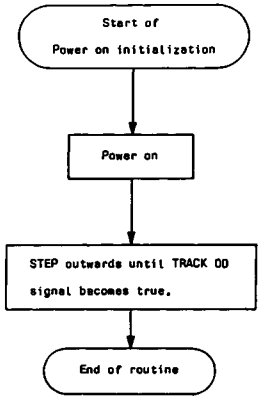
MP-F63W-00D will meet the following product safety regulations:

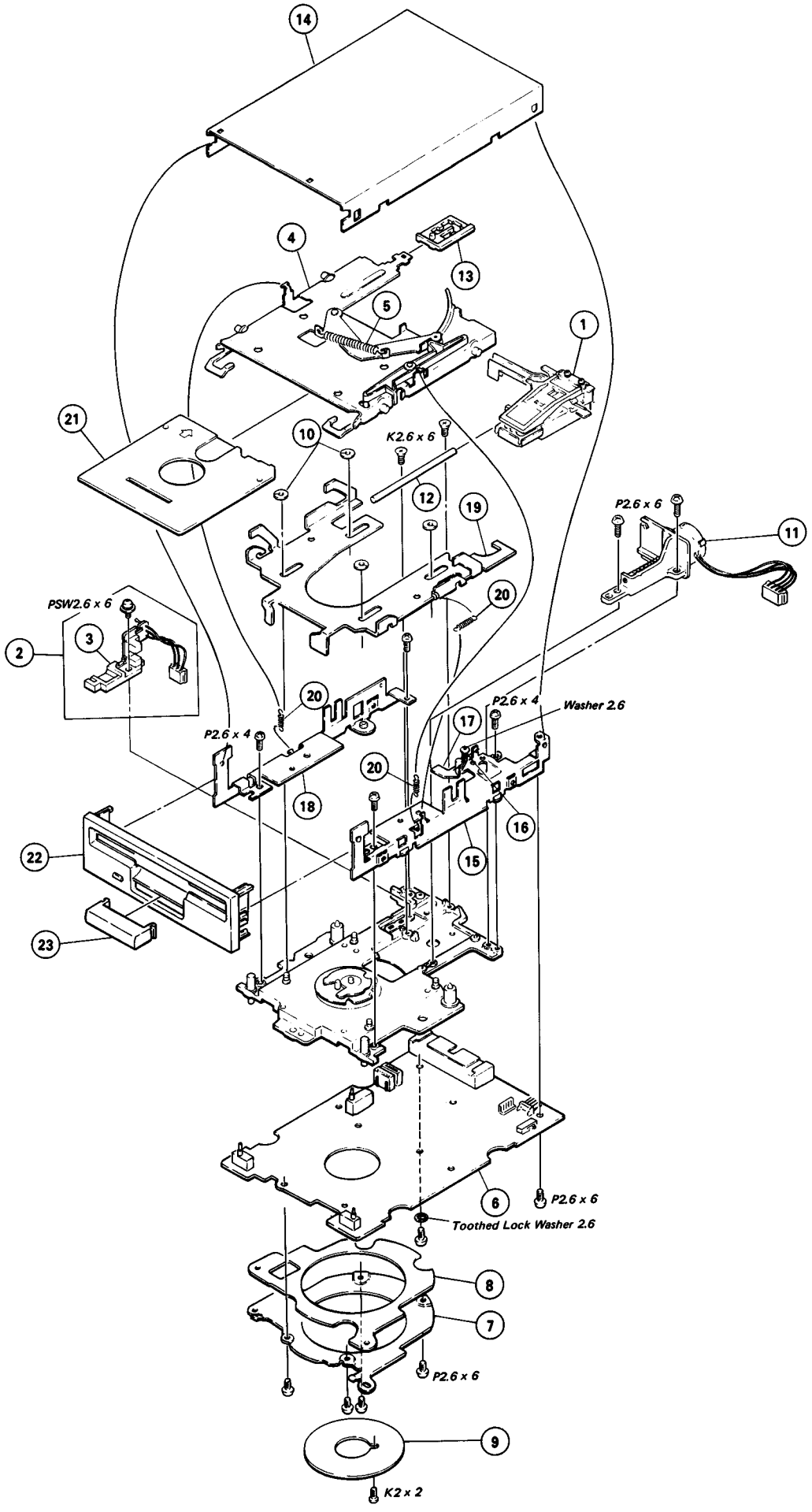
U.L. 478
C.S.A. C.22.2, No.154
U.L. 94V-0 for Front Bezel

5. Power On Initialization

In order to reduce the peak current requirement when used in a daisy chain, the MP-F63W-72D has been disigned not to seek track 00 automatically. If all the drives connected in the daisy chain sought track 00 simultaneously, this would place a significant power drain on the host system. Thus, the host system must perform the following routine just after power on in order to reset the track counter inside the drive.

Power On Initialization




14
4
13
5
1
21
10
K2.6 x 6
12
19
P2.6 x 6
11
PSW2.6 x 6
3
2
20
20
P2.6 x 4
Washer 2.6
17
P2.6 x 4
18
20
16
15
22
23
6
P2.6 x 6
Toothed Lock Washer 2.6
8
7
P2.6 x 6
9
K2 x 2

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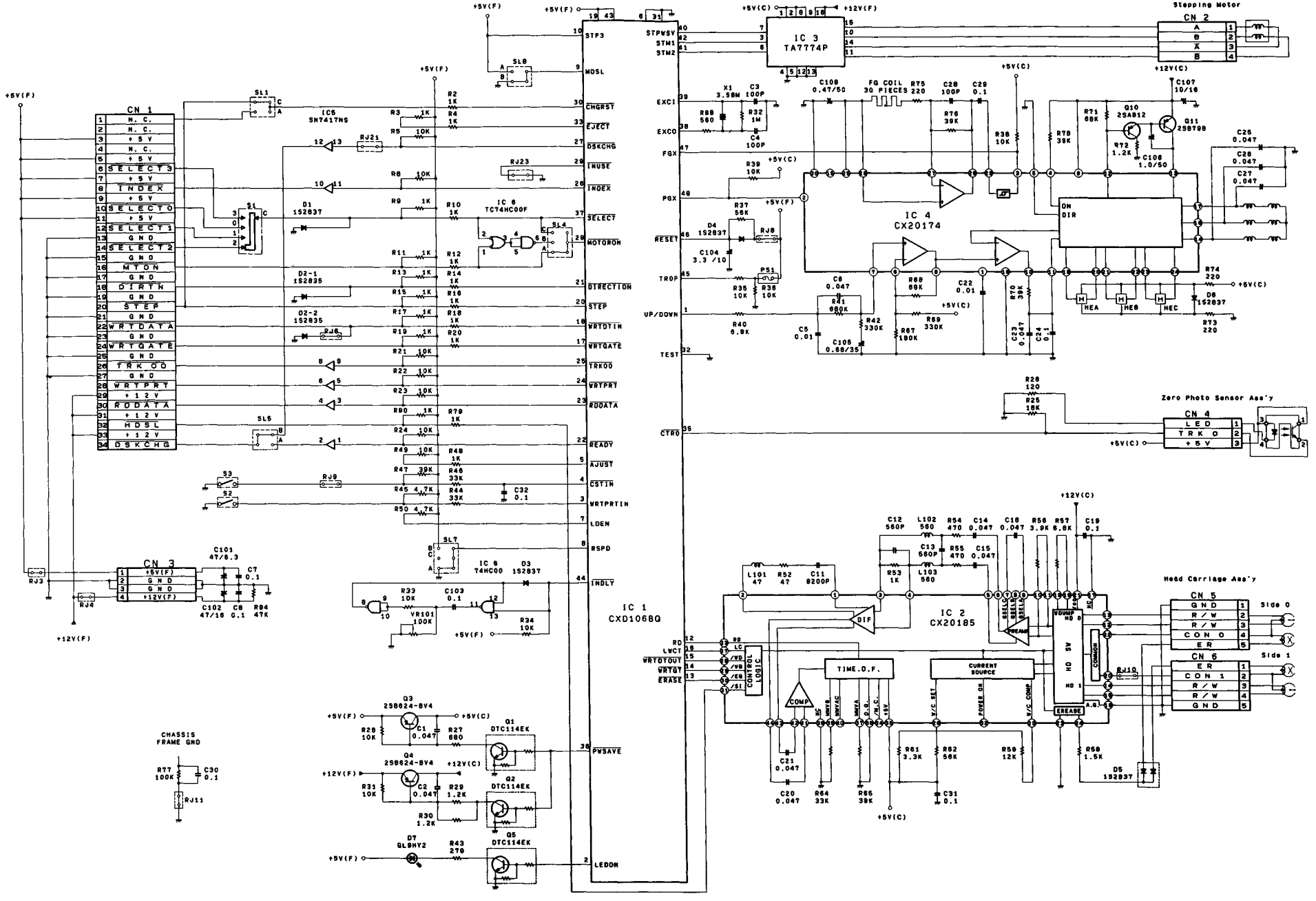
CN 1
CN 2
CN 3
CN 4
CN 5
CN 6
IC 1
CXD1068Q
IC 2
CX20185
IC 3
TA7774P
IC 4
CX20174
IC 5
SN7417NS
IC 6
TC74HC00F
74HC00
Stepping Motor
Zero Photo Sensor Ass'y
Head Carriage Ass'y
Side 0
Side 1
CHASSIS
FRAME GND
+5V(F)
+5V(C)
+12V(F)
+12V(C)
N. C.
+ 5 V
SELECT3
INDEX
SELECT0
SELECT1
GND
SELECT2
MTON
DIRTN
STEP
WRTDATA
WRTGATE
TRK 00
WRTPRT
+ 1 2 V
RDDATA
HDSL
DSKCHG
STP3
MDSL
CHGRST
EJECT
DSKCHG
INUSE
INDEX
SELECT
MOTORON
DIRECTION
STEP
WRTDTIN
WRTGATE
TRK00
WRTPRT
RDDATA
READY
AJUST
CSTIN
WRTPRTIN
LDEN
RSPD
INDLY
PWSAVE
LEDON
STPWSV
STM1
STM2
EXCI
EXCO
FGX
PGX
RESET
TROP
UP/DOWN
TEST
CTR0
RD
LWCT
WRTDTOUT
WRTGT
ERASE
LED
TRK 0
HEA
HEB
HEC
Side 0
Side 1
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1000 HX Options

SOFTWARE

Software Contents

BIOS Services

Keyboard ASCII and Scan Codes

MS-DOS Memory Map

Device I/O Services

Introduction

The BIOS (Basic Input/Output System) is the lowest-level interface between other software (application programs and the operating system itself) and the hardware. The BIOS routines provide various device input/output services, as well as boot strap and print screen and other services. Some of the services that BIOS provides are not available through the operating system, such as the graphics routines.

All calls to the BIOS are made through software interrupts (that is, by means of assembly language "INT x" instructions). Each I/O device is provided with a software interrupt, which transfers execution to the routine.

Entry parameters to BIOS routines are normally passed in CPU registers. Similarly, exit parameters are generally returned from these routines to the caller in CPU registers. To insure BIOS compatibility with other machines, the register usage and conventions are, for the most part, identical.

The following pages describe the entry and exit requirements for each BIOS rutine. To execute a BIOS call, load the registers as indicated under the "Entry Conditions." (Register AH will contain the function number in cases where a single interrupt can perform more than one operation.) Then issue the interrupt given for the call. The example, the following can be used to read a character from the keyboard:

```
MOV AH,0
INT 16H
```

Upon return, AL contains the ASCII character and AH the keyboard scan code.

Note: All registers except those used to return parameters to the caller are saved and restored by the BIOS routines.

Below is a quick reference list of software interrupts for all device I/O and system status services.

Service	Software Interrupts
Keyboard	16 hex (22 dec)
Video Display	10 hex (16 dec)
Serial Communications	14 hex (20 dec)
Line Printer	17 hex (23 dec)
System Clock	1A hex (26 dec)
Floppy Disk	13 hex (19 dec)
Equipment	11 hex (17 dec)
Memory Size	12 hex (18 dec)

Keyboard

16 hex (22 dec)

Function Summary:

AH = 0: Read Keyboard (destructive with wait)
AH = 1: Scan Keyboard (nondestructive, no wait)
AH = 2: Get Current Shift Status

Function Descriptions:

Read Keyboard

Read the next character typed at the keyboard. Return the ASCII value of the character and the keyboard scan code, removing the entry from the keyboard buffer (destructive read).

Entry Conditions:

AH = 0

Exit Conditions:

AL = *ASCII value of character*
AH = *keyboard scan code*

Scan Keyboard

Set up the zero flag (Z flag) to indicate whether a character is available to be read from the keyboard or not. If a character is available, return the ASCII value of the character and the keyboard scan code. The entry remains in the keyboard buffer (nondestructive read).

Entry Conditions:

AH = 1

Exit Conditions:

Z = no character is available
NZ = a character is available, in which case:
AL = *ASCII value of character*
AH = *keyboard scan code*

Get Shift Status

Return the current shift status.

Entry Conditions:

AH = 2

Exit Conditions:

AL = *current shift status (bit settings: set = true, reset = false)*
bit 0 = RIGHT SHIFT key depressed
bit 1 = LEFT SHIFT key depressed
bit 2 = CTRL (control) key depressed
bit 3 = ALT (alternate mode) key depressed
bit 4 = SCROLL state active
bit 5 = NUMBER lock engaged
bit 6 = CAPS lock engaged
bit 7 = INSERT state active

Video Display

These routines provide an interface to the video display, which is the output half of the console (CON) device. MS-DOS considers the video display to be the default standard output (STDOUT) device.

Software Interrupts:

10 hex (16 dec)

Function Summary:

Control Routines:

AH = 0: Set CRT Mode
AH = 1: Set Cursor Type
AH = 2: Set Cursor Position
AH = 3: Get Cursor Position
AH = 4: Read Light Pen Position
AH = 5: Select Active Page
AH = 6: Scroll Active Page Up
AH = 7: Scroll Active Page Down

Text Routines:

AH = 8: Read Attribute/Character
AH = 9: Write Attribute/Character
AH = 10: Write Character Only

Graphics Routines:

AH = 11: Set Color Palette
AH = 12: Write Dot
AH = 13: Read Dot

Other Routines:

AH = 14: Write TTY* to active page
AH = 15: Get CRT Mode
AH = 16: Set Palette Registers

*Screen width is determined by the mode previously set. Some "control" characters (ASCII 00H-1FH) perform the usual special terminal function. These include (but are not limited to) BEL (07H), BS (08H), LF (0AH), and CR (0DH).

Function Descriptions:

Set CRT Mode

Entry Conditions:

AH = 0
AL = *mode value, as follows:*

Alpha Modes
- AL = 0: 40x25 black and white
- AL = 1: 40x25 color
- AL = 2: 80x25 black and white
- AL = 3: 80x25 color

Graphics Modes
- AL = 4: 320x200 color graphics
- AL = 5: 320x200 black and white graphics with 4 shades
- AL = 6: 640x200 black and white graphics with 2 shades
- AL = 7: Reserved

Additional Modes
- AL = 8: 160x200 color graphics with 16 colors
- AL = 9: 320x200 color graphics with 16 colors
- AH = A: 640x200 color graphics with 4 colors

Note: If the high order bit of the AL register is 1 then the video buffer is not cleared.

Set Cursor Type

Set the cursor type and attribute.

Entry Conditions:

AH = 1
CH = *bit values:*
bits 5-6 = cause an invisible or erratically blinking cursor
bits 5-6 = 00 produces a visible, blinking cursor.
bits 4-0 = start line for cursor within character cell
CL = *bit values:*
bits 4-0 = end line for cursor within character cell

Set Cursor Position

Write (set) cursor position.

Entry Conditions:

AH = 2
BH = *page number (must be 0 for graphics modes)*
DH = *row (0 = top row)*
DL = *column (0 = leftmost column)*

Get Cursor Position

Read (get) cursor position.

Entry Conditions:

AH = 3
BH = *page number (must be 0 for graphics modes)*

Exit Conditions:

DH = *row of current cursor position (0 = top row)*
DL = *column of current cursor position (0 = leftmost column)*
CX = *cursor type currently set [1]:*

See Set Cursor Type (AH = 1) above.

Read Light Pen Position

Reads light pen position.

Entry Conditions:

AH = 4

Exit Conditions:

AH = 0: light pen switch not activated
AH = 1: light pen values in registers
DH = *row of current light pen position*
DL = *column of current light pen position*
CH = *raster line (0-199)*
BX = *pixel column (0-319 or 0-639)*

Select Active Page

Select active display page (valid in alpha mode only).

Entry Conditions:

AH = 5
AL = 0 through 7: *new page value for modes 0, 1*
AL = 0 through 3: *new page value for modes 2, 3*
AL = 80H: *read CRT/CPU page registers*
AL = 81H: *set CPU page register to value in BL*
AL = 82H: *set CRT page register to value in BH*
AL = 83H: *set both CRT and CPU page registers in BH and BL*

Exit Conditions:

If bit 7 of AL = 1 upon entry, BH = *contents of CRT page register*
BL = *contents of CPU page register*

Scroll Up

Scroll active page up.

Entry Conditions:

AH = 6
AL = *numbers of lines to scroll. The number of lines that will be left blank at the bottom of the window. (0 means blank entire window)*
CH = *row of upper left corner of scroll window*
CL = *column of upper left corner of scroll window*
DH = *row of lower right corner of scroll window*
DL = *column of lower right corner of scroll window*
BH = *attribute (alpha modes) or color (graphics modes) to be used on blank line*

Attributes:

Color modes:

foreground color:

bit 0 = blue
bit 1 = green
bit 2 = red

bit 3 = intensity
All bits off = black

background color:

bit 4 = blue
bit 5 = green
bit 6 = red

bit 7 = blink
All bits off = white

Scroll Down

Scroll active page down.

Entry Conditions:

AH = 7
AL = *number of lines to scroll (0 means blank entire window)*
CH = *row of upper left corner of scroll window*
CL = *column of upper left corner of scroll window*
DH = *row of lower right corner of scroll window*
DL = *column of lower right corner of scroll window*
BH = *attribute (alpha modes) or color (graphics modes) to be used on blank line. See Scroll Up (AH = 6) for attribute values and Set Color Palette (AH = 11) for color values.*

Read Attribute or Color/Character

Read a character and its attribute or color at the current cursor position.

Entry Conditions:

AH = 8
BH = *display page number (not used in graphics modes)*

Exit Conditions:

AL = *character read*
AH = *attribute of character (alpha modes only)*

Write Attribute or Color/Character

Write a character and its attribute or color at the current cursor position.

Entry Conditions:

AH = 9
BH = *display page number (not used in graphics modes)*
CX = *number of characters to write*
AL = *character to write*
BL = *attribute of character (for alpha modes) or color of character (for graphics modes; if bit 7 of BL is set, the color of the character is XOR'ed with the color value). See Scroll Up (AH = 6) for attribute values and Set Color Palette (AH = 11) for color values.*

Write Character Only

Write character only at current cursor position.

Entry Conditions:

AH = 10
BH = *display page number (valid for alpha modes only*
CX = *number of characters to write*
AL = *character to write*
BL = *color of character (graphics mode)*

Set Color Palette [3]

Select the color palette.

Entry Conditions:

AH = 11
BH = 0 Set background color (0-15) to color value in BL.
BL = *color value* (0 = black / 1 = blue / 2 = green / 3 = cyan / 4 = red / 5 = magenta / 6 = yellow / 7 = gray / 8 = dark gray / 9 = light blue / 10 = light green / 11 = light cyan / 12 = light red / 13 = light magenta / 14 = light yellow / 15 = white)

or
BH = 1 Set default palette to the number (0 or 1) in BL.

In black and white modes:

BL = 0: 1 for white
BL = 1: 1 for black

In 4 color graphics modes:

BL = 0 (1 = green / 2 = red / 3 = yellow)
BL = 1 (1 = cyan / 2 = magenta / 3 = white)

In 16 color graphics modes:

(1 = blue / 2 = green / 3 = cyan / 4 = red / 5 = magenta / 6 = yellow / 7 = light gray / 8 = dark gray / 9 = light blue / 10 = light green / 11 = light cyan / 12 = light red / 13 = light magenta / 14 = yellow / 15 = white)

Note: For alpha modes palette entry 0 indicates the border color. For graphics mode palette entry 0 indicates the border and the background color.

Write Dot

Write a pixel (dot).

Entry Conditions:

AH = 12
DX = *row number*
CX = *column number*
AL = *color value (When bit 7 of AL is set, the resultant color value of the dot is the exclusive OR of the current dot color value and the value in AL.)*

Read Dot

Read a pixel (dot).

Entry Conditions:

AH = 13
DX = *row number*
CX = *column number*

Exit Conditions:

AL = *color value of dot read*

Write TTY

Write a character in teletype fashion. (Control characters are interpreted in the normal manner.)

Entry Conditions:

AH = 14
AL = *character to write*
BL = *foreground color (graphics mode)*

Get CRT Mode

Get the current video mode.

Entry Conditions:

AH = 15

Exit Conditions:

AL = *current video mode; see Set CRT Mode (AH = 0) above for values*
AH = *number of columns on screen*
BH = *current active display page*

Set Palette Registers

Sets palette registers.

Entry Conditions:

AH = 16
AL = 0 Set Palette register
BL = *number of the palette register (0-15) to set*
BH = *color value to store*
AL = 1 Set border color register
BH = *color value to store*
AL = 2 Set palette color value to store and border registers
ES:DX :points to a 17 byte list.
bytes 0-15 = *values for palette registers 0-15*
byte 16 = *value for the border register*

Note: CS,SS,DS,ES,BX,CX,DX are preserved.

Serial Communications

These routines provide asynchronous byte stream I/O from and to the RS-232C serial communications port. This device is labeled the auxiliary (AUX) I/O device in the device list maintained by MS-DOS.

Software Interrupts:

14 hex (20 dec)

Function Summary:

AH = 0: Reset Comm Port
AH = 1: Transmit Character
AH = 2: Receive Character
AH = 3: Get Current Comm Status
DX = communication port number (0 or 1).

Function Descriptions:

Reset Comm Port

Reset (or initialize) the communication port according to the parameters in AL, DL, and DH.

Entry Conditions:

AH = 0
AL = *RS-232C parameters, as follows:*
DX = *port number (0 or 1)*

7 6 5	*4 3*	*2*	*1 0*
Baud Rate	*Parity*	*Stop Bits*	*Word Length*

000 = *110 baud*
001 = *150 baud*
010 = *300 baud*
011 = *600 baud*
100 = *1200 baud*
101 = *2400 baud*
110 = *4800 baud*
111 = *9600 baud*

x0 = none
01 = odd
11 = even

0 = 1 bit
1 = 2 bits

10 = 7 bits
11 = 8 bits

Exit Conditions:

AX = *RS-232 status; see Get Current Comm Status (AH = 3) following*

Transmit Character

Transmit (output) the character in AL (which is preserved).

Entry Conditions:

AH = 1
AL = *character to transmit*
DX = *port number* (0 or 1)

Exit Conditions:

AH = *RS-232 status; see Get Current Comm Status (AH = 3) below* (If bit 7 is set, the routine was unable to transmit the character because of a timeout error.)
AL is preserved.

Receive Character

Receive (input) a character in AL (wait for a character, if necessary). On exit, AH will contain the RS-232 status, except that only the error bits (1,2,3,4,7) may be set; the timeout bit (7), if set, indicates that data set ready was not received and the bits in AH are not meaningful. Thus, AH is non-zero only when an error occurred.

Entry Conditions:

AH = 2
DX = *port number* (0 or 1)

Exit Conditions:

AL = *character received*
AH = *RS-232 status; see Get Current Comm Status (AH = 3) below*

Get Current Comm Status

Read the communication status into AX.

Entry Conditions:

AH = 3
DX = *port number* (0 or 1)

Exit Conditions:

AH = *RS-232 status, as follows (set = true):*
- bit 0 = data ready
- bit 1 = overrun error
- bit 2 = parity error
- bit 3 = framing error
- bit 4 = break detect
- bit 5 = transmitter holding register empty
- bit 6 = transmitter shift register empty
- bit 7 = timeout occurred

AL = *modem status, as follows (set = true):*
- bit 0 = delta clear to send
- bit 1 = delta data set ready
- bit 2 = trailing edge ring detector
- bit 3 = delta receive line signal detect
- bit 4 = clear to send
- bit 5 = data set ready
- bit 6 = ring indicator
- bit 7 = receive line signal detect

Line Printer

These routines provide an interface to the parallel line printer. This device is labeled "PRN" in the device list maintained by the operating system.

Software Interrupts:

17 hex (23 dec)

Function Summary:

AH = 0: Print Character
AH = 1: Reset Printer Port
AH = 2: Get Current Printer Status

Function Descriptions:

Print Character

Print a character.

Entry Conditions:

AH = 0
AL = *character to print*
DX = *printer to be used (0-2)*

Exit Conditions:

0AH = *printer status; see Get Current Printer Status (AH = 2) below*
(If bit 0 is set, the character could not be printed because of a timeout error.)

Reset Printer Port

Reset (or initialize) the printer port.

Entry Conditions:

AH = 1
DX = *printer to be used (0-2)*

Exit Conditions:

AH = *printer status; see Get Current Printer Status (AH = 2) below*

Get Current Printer Status

Read the printer status into AH.

Entry Conditions:

AH = 2

Exit Conditions:

DX = *printer to be used (0-2)*
AH = *printer status, as follows (set = true):*
bit 0 = timeout occurred
bit 1 = [unused]
bit 2 = [unused]
bit 3 = I/O error
bit 4 = selected
bit 5 = out of paper
bit 6 = acknowledge
bit 7 = not busy

System Clock

These routines provide methods of reading and setting the clock maintained by the system. This device is labeled CLOCK in the device list of the operating system. An interface for setting the multiplexer for audio source is also provided.

Software Interrupts:

1A hex (26 dec)

Function Summary:

AH = 0: Get Time of Day
AH = 1: Set Time Of Day
AH = 80H: Set Up Sound Multiplexer

The clock runs at the rate of 1,193,180/65,536 per second (about 18.2 times per second).

Function Descriptions:

Get Time Of Day

Get (read) the time of day in binary format.

Entry Conditions:

AH = 0

Exit Conditions:

CX = *high (most significant) portion of clock count*
DX = *low (least significant) portion of clock count*
AL = Ø of the clock was read or written (via AH = Ø,1) within the current 24-hour period; othrwise, AL > Ø

Set Time Of Day

Set (write) the time of day using binary format.

Entry Conditions:

AH = 1
CX = *high (most significant) portion of clock count*
DX = *low (least significant) portion of clock count*

Sound Multiplexer

Sets the multiplexer for audio source.

Entry Conditions:

AH = 8Ø
AL = *source of sound*
ØØ = 8253 channel 2
Ø2 = audio in
Ø3 = complex sound generator chip

Disk I/O Support for the Floppy Only System Configuration

Software Interrupt:

13 hex (19 dec)

Function Summary:

AH = 0: Reset Floppy Disk
AH = 1: Return Status of Last Floppy Disk Operation
AH = 2: Read Sector(s) from Floppy Disk
AH = 3: Write Sector(s) to Floppy Disk
AH = 4: Verify Sector(s) on Floppy Disk
AH = 5: Format Track on Floppy Disk

Function Descriptions:

Reset Floppy Disk

Reset the diskette system. Resets associated hardware and recalibrates all diskette drives.

Entry Conditions:

AH = 0

Exit Conditions:

See "Exits From All Calls" below.

Return Status of Last Floppy Disk Operation

Return the diskette status of the last operation in AH.

Entry Conditions

AH = 1

Exit Conditions:

AL = *status of the last operation; see "Exits From All Calls" below for values*

Read Sector(s) from Floppy Disk

Read the desired sector(s) from disk into RAM.

Entry Conditions:

AH = 2
DL = *drive number (0-1)*
DH = *head number (0-1)*
CH = *track number (0-79)*
CL = *sector number (1 to 9)*
AL = *sector count (1 to 9)*
ES:BX = *pointer to disk buffer*

Exit Conditions:

See "Exits From All Calls" below.
AL = *number of sectors read*

Write Sector(s) to Floppy Disk

Write the desired sector(s) from RAM to disk.

Entry Conditions:

AH = 3
DL = *drive number (0-1)*
DH = *head number (0-1)*
CH = *track number (0-79)*
CL = *sector number (1 to 9)*
AL = *sector count (1 to 9)*
ES:BX = *pointer to disk buffer*

Exit Conditions:

See "Exits From All Calls" below.
AL = *number of sectors written*

Verify Sector(s) on Floppy Disk

Verify the desired sector(s).

Entry Conditions:

AH = 4
DL = *drive number (0-1)*
DH = *head number (0-1)*
CH = *track number (0-79)*
CL = *sector number (1 to 9)*
AL = *sector count (1 to 9)*

Exit Conditions:

See "Exits From All Calls" below.
AL = number of sectors verified

Format on Floppy Disk

Format the desired track.

Entry Conditions:

AH = 5
DL = *drive number (0-1)*
DH = *head number (0-1)*
CH = *track number (0-79)*
CL = *sector number (1-9)*
ES:BX = *pointer to a group of address fields for each track.* Each address field is made up of 4 bytes. These are C, H, R, and N, where:
C = track number
H = head number
R = sector number
N = the number of bytes per sector (00 = 128, 01 = 256, 02 = 512, 03 = 1024)
There is one entry for every sector on a given track.

Exit Conditions:

See "Exits From All Calls" below.

Exits From All Calls:

AH = *Status of operation, where set = true:*

Error Code	Condition
01H	Illegal Function
02H	Address Mark Not Found
03H	Write Protect Error
04H	Sector Not Found
08H	DMA Overrun
09H	Attempt To DMA Across A 64K Boundary
10H	Bad CRC on Disk Read
20H	Controller Failure
40H	Seek Failure
80H	Device Timeout, Device Failed To Respond

[NC] = operation successful (AH = 0)
[C] = operation failed (AH = error status)

Equipment

This service returns the "equipment flag" (hardware configuration of the computer system) in the AX register.

Software Interrupts:

11 hex (17 dec)

The "equipment flag" returned in the AX register has the meanings listed below for each bit:

Reset = the indicated equipment is not in the system
Set = the indicated equipment is in the system

bit 0	diskette installed
bit 1	math coprocessor
bit 2,3	always = 11
bit 4,5	initial video mode
	01 = 40x25 BW
	10 = 80x25 BW
bit 6,7	number of diskette drives (only if bit 0 = 1)
	00 = 1
	01 = 2
bit 8	0 = dma present
	1 = no dma on system
bit 9, 10, 11	number of RS 232 cards
bit 12	game I/O attached
bit 13	not used
bit 14, 15	number of printers

Memory Size

This service returns the total number of kilobytes of RAM in the computer system (contiguous starting from address 0) in the AX register. The maximum value returned is 640.

Software Interrupts:

12 hex (18 dec)

EEROM (Tandy 1000 HX only)

15 hex (21 dec)

Function Summary

AH = 70H, AL = 0: Read a 16 bit word from EEROM
AH = 70H, AL = 1: Write a 16 bit word to EEROM

Function Descriptions

Read From EEROM

Read the 16 bit value from the indicated EEROM word.

Entry Conditions:

AH = 70H
AL = 0
BL = word number to read (0 -15)

Exit Conditions:

DX = word value
Carry Flag set indicates EEROM call not supported, system is not a 1000HX

Write To EEROM

Write a 16 bit value to the indicated EEROM word

Entry Conditions:

AH = 70H
AL = 1
BL = word number to write (0-15)
DX = word value to write

Exit Conditions:

Carry Flag set indicates EEROM call not supported, system is not a 1000HX

KEYBOARD ASCII AND SCAN CODES

The table in this appendix lists the keys on the Tandy 1000 keyboard in scan code order, along with the ASCII codes they generate. For each key, the following entries are given:

Scan Code — A value in the range 01H-5AH which uniquely identifies the physical key on the keyboard that is pressed.

Keyboard Legend — The physical marking(s) on the key. If there is more than one marking, the upper one is listed first.

ASCII Code — The ASCII codes associated with the key. The four modes are:

Normal — The normal ASCII value (returned when only the indicated key is depressed).

SHIFT — The shifted ASCII value (returned when SHIFT is also depressed).

CTRL — The control ASCII value (returned when CTRL is also depressed).

ALT — The alternate ASCII value (returned when ALT is also depressed).

Remarks — Any remarks or special functions.

The following special symbols appear in the table:

x	Values preceded by "x" are extended ASCII codes (codes preceded by an ASCII NUL, 00).
—	No ASCII code is generated.
*	No ASCII code is generated, but the special function described in the Remarks column is performed. If no comment is included, the key does not generate a code and no function is performed.

Note: All numeric values in the table are expressed in hexadecimal.

QWERTY (USA) — MODEL 1000

As of Oct. 22 1984

Scan Code	Keyboard Legend		ASCII Codes Normal	SHIFT	CTRL	ALT	Remarks
01	ESC		1B	1B	1B	x8B	
02	1	!	31	21	xE1	x78	
03	2	@	32	40	x03	x79	
04	3	#	33	23	xE3	x7A	
05	4	$	34	24	xE4	x7B	
06	5	%	35	25	xE5	x7C	
07	5	^	36	5E	1E	x7D	
08	7	&	37	26	xE7	x7E	
09	8	*	38	2A	xE8	x7F	
0A	9	(	39	28	xE9	x80	
0B	0	)	30	29	xE0	x81	
0C	-	_	2D	5F	1F	x82	
0D	=	+	3D	2B	xF5	x83	
0E	BACK SPACE		08	08	7F	x8C	
0F	TAB		09	x0F	x8D	x8E	
10	Q		71	51	11	x10	
11	W		77	57	17	x11	
12	E		65	45	05	x12	
13	R		72	52	12	x13	
14	T		74	54	14	x14	
15	Y		79	59	19	x15	
16	U		75	55	15	x16	
17	I		69	49	09	x17	
18	O		6F	4F	0F	x18	
19	P		70	50	10	x19	
1A	[	{	5B	7B	B	xEB	
1B	]	}	5D	7D	1D	xF0	
1C	ENTER		0D	0D	0A	x8F	Main Keyboard
1D	CTRL		*	*	*	*	Control Mode
1E	A		61	41	01	x1E	
1F	S		73	53	13	x1F	
20	D		64	44	04	x20	
21	F		66	46	06	x21	
22	G		67	47	07	x22	
23	H		68	48	08	x23	
24	J		6A	4A	0A	x24	
25	K		6B	4B	0B	x25	
26	L		6C	4C	0C	x26	
27	;	:	3B	3A	xF6	xF8	
28	'	"	27	22	xF7	xF1	
29	UP ARROW		x48	x85	x90	x91	
2A	SHIFT		*	*	*	*	Left SHIFT
2B	LEFT ARROW		x4B	x87	x73	x92	
2C	Z		7A	5A	1A	x2C	
2D	X		78	58	18	X2D	
2E	C		63	43	03	x2E	
2F	V		76	56	16	x2F	

Scan Code	Keyboard Legend		ASCII Code Normal	SHIFT	CTRL	ALT	As of Oct. 22 1984 Remarks
30	B		62	42	02	x30	
31	N		6E	4E	0E	x31	
32	M		6D	4D	0D	x32	
33	,	<	2C	3C	xF9	x89	
34	.	>	2E	3E	xFA	X8A	
35	/	?	2F	3F	xFB	xF2	
36	SHIFT		*	*	*	*	Right SHIFT
37	PRINT		10	*	x72	x46	SCR Print Toggle
38	ALT		*	*	*	*	Alternate Mode
39	space bar		20	20	20	20	
3A	CAPS		*	*	*	*	Caps lock
3B	F1		x3B	x54	x5E	x68	
3C	F2		x3C	x55	x5F	x69	
3D	F3		x3D	x56	x60	x6A	
3E	F4		x3E	x57	x61	x6B	
3F	F5		x3F	x58	x62	x6C	
40	F6		x40	x59	x63	x6D	
41	F7		x41	x5A	x64	x6E	
42	F8		x42	x5B	x65	x6F	
43	F9		x43	x5C	x66	x70	
44	F10		x44	x50	x67	x71	
45	NUM LOCK		*	*	*	*	number lock
46	HOLD		*	*	*	*	Freeze display
47	7	\	37	5C	x93	*	
48	8	-	38	7E	x94	*	
49	9	PG UP	39	x49	x84	*	
4A	DOWN ARROW		x50	x86	x96	x97	
4B	4	|	34	7C	x95	*	
4C	5		35	xF3	xFC	*	
4D	6		36	xF4	xFD	*	
4E	RIGHT ARROW		x4D	x88	x74	xEA	
4F	1	END	31	x4F	x75	*	
50	2	‘	32	60	x9A	*	
51	3	PG DN	33	x51	x76	*	
52	0		30	x9B	x9C	*	
53	-	DELETE	2D	x53	x9D	x9E	
54	BREAK		x00	x00	*	*	scroll lock bit toggle control brk routine (INT 1BH)
55	+	INSERT	2B	x52	x9F	xA0	
56			2E	xA1	xA4	xA5	Numeric keypad
57	ENTER		0D	0D	0A	x8F	Numeric keypad
58	HOME		x47	x4A	x77	xA6	
59	F11		x98	xA2	xAC	xB6	
5A	F12		x99	xA3	xAD	xB7	

* Indicates special functions performed

— means this key combination is suppressed in the keyboard driver

X values preceded by "X" are extended ASCII codes (codes preceded by an ASCII NUL)

† The [ALT] key provides a way to generate the ASCII codes of decimal numbers between 1 and 255. Hold down the [ALT] key while you type *on the numeric keypad* any decimal number between 1 and 255. When you release ALT, the ASCII code of the number typed is generated and displayed.

Note: When the NUM LOCK light is off, the Normal and SHIFT columns for these keys should be reversed.

MS-DOS Memory Map

HEXADECIMAL STARTING ADDRESS (SEGMENT:OFFSET)	DESCRIPTION
000:00	BIOS Interrupt Vectors
000:80	Available Interrupt Vectors
0040:00[1]	ROM BIOS Data Area
0050:00	MSDOS and BASIC Data Area
0070:00	I/O.SYS Drivers
0190.00[2]	MS-DOS
05B0:00[2]	Available to user
X800:00[3]	Video RAM in 32K video modes
XC00:00[3]	Video RAM in 16K video modes
B800:00[4]	Video RAM Window (32K)
F000:00	Reserved for system ROM
FC00:00	System BIOS ROM

Notes:

1. Detailed description in following pages.
2. Approximate address; subject to change.
3. "X" is defined as follows:

Memory Size	X Value
128K	1
256K	3
384K	5
512K	7
640K	9
768K	B

4. Video memory accessed through the B800:0 window for all video modes.

ROM BIOS Data Area

The following table gives the starting offset, and length of each BIOS device driver. This area is located at segment 40:00.

Comm card addresses	0000	8 (1 word per card)
Printer addresses	0008	8 (1 word per printer)
Devices installed	0010	2 (16 bits)
Not used	0012	1
Memory size	0013	2 (1 word)
I/O channel RAM size	0015	2 (1 word)
KBD data area	0017	39
Disk data area	003E	11
Video data area	0049	30
Not used	0067	5
Clock data area	006C	5
KBD Break & Reset flags	0071	3
Not used	0074	4
Printer Timeout counter	0078	4 (1 byte per printer)
Comm Timeout counter	007C	4 (1 byte per card)
KBD extra data area	0080	4 (2 words)

The structure and usage of the Video driver RAM data area is as follows:

HEX Offset From Segment 0040:000	Length and Intended Use
49H	1 byte - current CRT mode (0-7)
4AH	1 word - screen column width
4CH	1 word - byte length of screen
4EH	1 word - address/offset of beginning of current display page
50H	8 words - row/col coordinates of the cursor for each of up to 8 display pages
60H	1 word - current cursor type (See "set cursor type" for correct encoding)
62H	1 byte - current display page
63H	1 word - base address + 4 of the CRT controller card
65H	1 byte - copy of value written to the Mode Select Register
66H	1 byte - current color palette setting

The equipment check BIOS call (INT 11H) and memory size BIOS call (INT 12H) return information from the following data areas:

HEX Offset From Segment 0040:000	Length and Intended Use
10H	Devices installed word
13H	Memory installed word

The structure and usage of the floppy disk driver RAM data area is as follows:

HEX Offset From Segment 0040:0000	Length and Intended Use
3EH	1 byte - drive recalibration status - bit 3-0, if 0 then drive 3-0 needs recal before next seek bit 7 indicates interrupt occurrence
3FH	1 byte - motor status - bit 3-0 drive 3-0 motor is on/off, bit 7 - current operation is write, requires delay
40H	1 byte - motor turn off time out counter (see Timer ISR)
41H	1 byte - disk status - codes defined below
42H	7 bytes - 7 bytes of status returned by the controller during result phase of operation

Value	Error Condition
01H	Illegal Function
02H	Address Mark Not Found
03H	Write Protect Error
04H	Sector Not Found
08H	DMA Overrun
09H	Attempt to DMA Across a 64K Boundary
10H	Bad CRC on Disk Read
20H	Controller Failure
40H	Seek Failure
80H	Device Timeout, Device Failed to Respond

The structure and usage of the RS232 driver RAM data area is as follows:

HEX Offset From Segment 0040:00	Length and Intended Use
00H	4 words - Base address of each one of 4 possible comm cards
7CH	4 words - 1 word timeout count for each of 4 possible comm cards

The structure and usage of the Keyboard driver RAM data area is as follows:

HEX Offset From Segment 0040:0010		Length and Intended Use
17	1 byte	- Keyboard shift state flag returned by function 02
	bits 7	- INSERT state active, 6 - CAPS LOCK on/off, 5 - NUM LOCK on/off, 4 - SCROLL LOCK on/off, 3 - ALT key depressed, 2 - CTRL key depressed, 1 - Left SHIFT key depressed, 0 - Right SHIFT key depressed
18	1 byte bits	- Secondary shift state flag INSERT key depressed, 6 - CAPS LOCK depressed, 5 - NUM LOCK depressed, 4 - SCROLL LOCK NUM LOCK depressed, 4 - SCROLL depressed, 4 - SCROLL LOCK depressed, 3 - Pause on/off, depressed, 3 - Pause on/off, 2,1,0 - not used
19	1 byte	- used to store ALT keypad entry
1A	1 word	- pointer to beginning of the keyboard buffer
1C	1 word	- pointer to end of the keyboard buffer
1E	16	- keyboard buffer (enough for words)
	15	- typeahead entries

The structure and usage of the clock service routine is as follows:

HEX Offset From Segment 0040:0000	Length and Intended Use	
6CH	1 word	- Least significant 16 bits of clock count
6EH	1 word	- Most significant 16 bits of clock count
70H	1 byte	- Twenty four hour rollover flag

ADDITIONAL DATA AREA

HEX Offset From Segment 0040:000

B0H	2 words	international support
B4H	1 byte	0 = No monochrome monitor FFH = monochrome monitor
B5H	1 byte	Bit 0: 0 = drive A is 5-1/4 1 = drive A is 3-1/2 Bit 1: 0 = drive B is 5-1/4 1 = drive B is 3-1/2 Bit 2: 0 = Tandy 1000 keyboard layout 1 = IBM keyboard layout Bit 3: 0 = Slow CPU speed mode 1 = Fast CPU speed mode Bit 4: 0 = Internal color video support enabled 1 = Internal color video support disabled, external color video enabled Bit 5: 0 = No external monochrome video installed 1 = External monochrome video installed
B6H	1 byte	Bit 0: 0 = drive C is 5-1/4 1 = drive C is 3-1/2

Tandy 1000 HX
Page Insertion Guide

Important Customer Note:

A gray stripe has been printed along the right edge of the title page of each of the sections to facilitate your finding the begining of the section. Also, a tabbed divider for each section has been provided for insertion at this point.

Foldout Pages To Be Inserted after page 16 of the Main Logic Section

Light Blue To System Timing Diagram	Sheets 1 of 2 and 2 of 2
Big Blue To System Timing Diagram	Sheets 1 of 2 and 2 of 2

Foldout Pages To Be Inserted at the end of the Main Logic Section

Main Logic Schematic	8000287
Version A	Sheets 1 of 9 thru 9 of 9
Version B	Revised Sheets 1,5 and 6 of 9

Foldout Pages To Be Inserted at the end of the 28 Watt Single Input Power Supply

Schematic	8790083 3P-M1-0163

Foldout Page To Be Inserted at the end of the 28 Watt Dual Input Power Supply

Schematic	8790086 3P-M1-0159

Foldout Page To Be Inserted at the end of the 25.6 Watt Power Supply

Schematic	8790093 3P-M1-0345A

Foldout Pages To Be Inserted At The End of the Keyboard Section

Keyboard Circuit	B-8080079 Sheets 5 and 6 of 7

Foldout Page To Be Inserted At The End of the Disk Drive Section

Exploded View	8790142 Sheets 1 of 1
Schematic	8790142 Sheets 1 of 1

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