AK4510

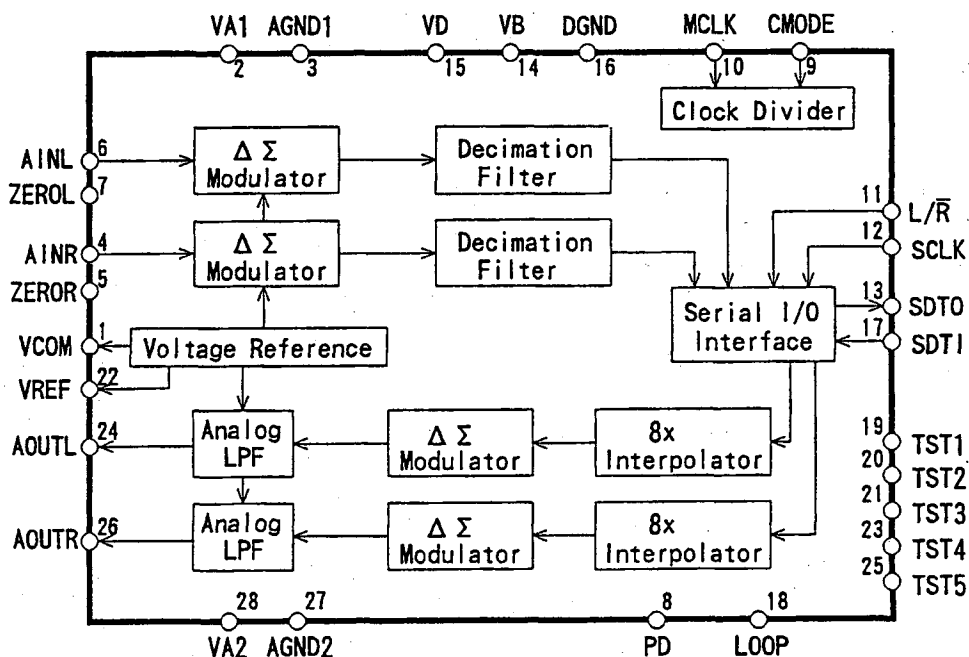## 16-Bit Stereo Δ Σ ADC & DAC for Multimedia

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General Description

The AK4510 is a stereo A/D & D/A Converter for multimedia audio system. The AK4510 achieves high accuracy and low cost by using 4th order Δ Σ techniques. The DAC outputs are filtered in the analog domain by a combination of switched-capacitor and continuous-time filters. Because they remove the very high frequency noise of the DAC Δ Σ output, the DAC keeps almost constant S/N ratio regardless of sampling frequency. The AK4510 does not require any external components.

Features

- ☐ Δ Σ Stereo ADC
  - On-Chip Digital Anti-Alias Filtering
- ☐ Δ Σ Stereo DAC
  - On-Chip 8 Times Interpolation Filter
  - On-Chip Post Filter
  - On-Chip Output Buffer with Single-Ended Output
  - Very Low Noise at Low Sampling Rate
- ☐ High Tolerance to Clock Jitter
- ☐ Sampling Rate Ranging from 4kHz to 50kHz
- ☐ Single +5V Power Supply
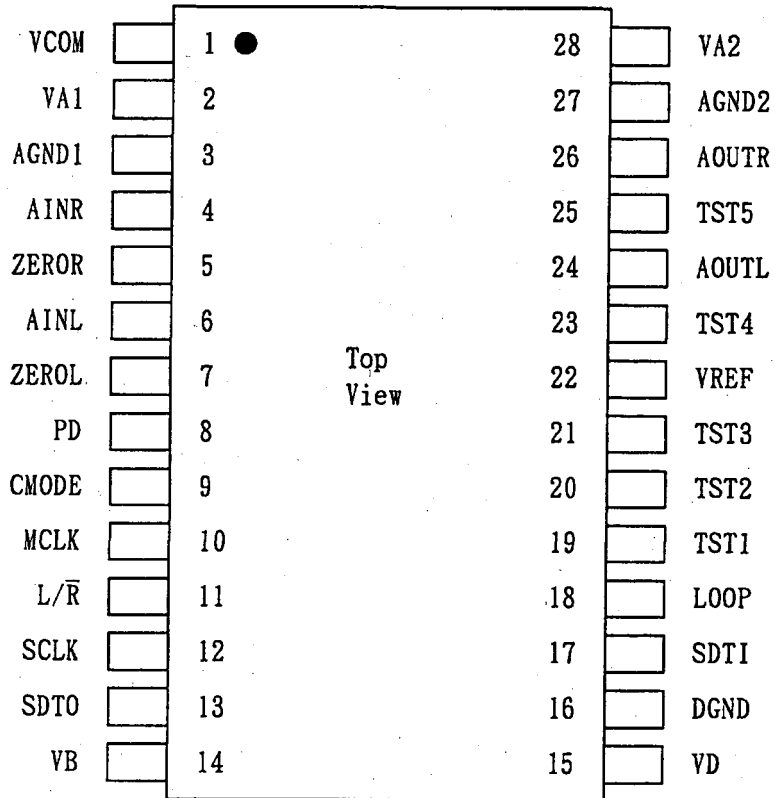- ☐ Low Power Dissipation: 150mW
- ☐ 28pin SOP Package

■ Ordering Guide

AK4510-VS   -10～+70℃   28pin SOP
AKD4510   Evaluation Board

■ Pin Layout

VCOM	1 ●		28	VA2
VA1	2		27	AGND2
AGND1	3		26	AOUTR
AINR	4		25	TST5
ZEROR	5		24	AOUTL
AINL	6		23	TST4
ZEROL	7	Top View	22	VREF
PD	8		21	TST3
CMODE	9		20	TST2
MCLK	10		19	TST1
L/R̄	11		18	LOOP
SCLK	12		17	SDTI
SDTO	13		16	DGND
VB	14		15	VD

	PIN/FUNCTION		
No.	Pin Name	I/O	Function
1	VCOM	O	Voltage Common Output Pin, 2.5V Normally connected to AGND1 with a 0.1uF ceramic capacitor in parallel with an electrolytic capacitor less than 10uF.
2	VA1	-	ADC,VREF Section Analog Supply Pin, +5V
3	AGND1	-	ADC,VREF Section Analog Ground Pin
4	AINR	I	Rch Analog Input Pin
5	ZEROR	I	Rch Zero Input Pin
6	AINL	I	Lch Analog Input Pin
7	ZEROL	I	Lch Zero Input Pin
8	PD	I	Power-Down Pin When "H", the circuit is in power-down mode. Upon returning to "L", the AK4510 starts an offset calibration cycle. A calibration cycle should always be initiated after power-up.
9	CMODE	I	Master Clock Select Pin "L": MCLK=256fs, "H": MCLK=384fs
10	MCLK	I	Master Clock Input Pin
11	L/R̄	I	Left/Right Channel Select Pin The fs clock is input to this pin. "H": Lch, "L": Rch
12	SCLK	I	Serial Data Clock Pin Output data is clocked out on the falling edge of SCLK. Input data is clocked in on the rising edge of SCLK. SCLK requires a continuously supplied clock at any frequency from 32fs to 64fs.
13	SDTO	O	Serial Data Output Pin Data bits are presented MSB first, in 2's complement format. This pin is "L" in the power-down mode.
14	VB	-	Substrate Voltage Supply Pin, +5V
15	VD	-	Digital Power Supply Pin, +5V
16	DGND	-	Digital Ground Pin
17	SDTI	I	Serial Data Input Pin 2's complement MSB-first data is input via this pin.
18	LOOP	I	Digital Loopback Pin "L":Normal operation. "H":A/D to D/A loopback.
19 20 21	TST1 TST2 TST3	O O O	Test Pins Must be left floating.
22	VREF	O	Voltage Reference Output Pin, 2.5V Normally connected to AGND2 with a 0.1uF ceramic capacitor in parallel with an electrolytic capacitor less than 10uF.
23 25	TST4 TST5	I I	Test Pins (Pull-down pin) Must be left floating or tied to AGND2.
24	AOUTL	O	Lch Analog Output Pin
26	AOUTR	O	Rch Analog Output Pin
27	AGND2	-	DAC Section Analog Ground Pin
28	VA2	-	DAC Section Analog Supply, +5V

ABSOLUTE MAXIMUM RATINGS

(AGND1, AGND2, DGND=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supplies: Analog	VA1, VA2	-0.3	6.0	V
Digital(VD pin)	VD	-0.3	VB+0.3	V
Substrate(VB pin)	VB	-0.3	6.0	V
Input Current, Any Pin Except Supplies	IIN	-	±10	mA
Analog Input Voltage AINL, AINR pins	VINA	-0.3	VA+0.3	V
Digital Input Voltage	VIND	-0.3	VB+0.3	V
Ambient Temperature (power applied)	Ta	-10	70	℃
Storage Temperature	Tstg	-65	150	℃

Note: 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND1, AGND2, DGND=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supplies: Analog	VA1, VA2	4.75	5.0	5.25	V
Digital(VD pin)	VD	4.75	5.0	VB	V
(Note 2) Substrate(VB pin)	VB	4.75	5.0	5.25	V

Notes: 1. All voltages with respect to ground.
2. VA1, VA2 and VB are connected together on the chip through a few Ω resistance.
These pins should be supplied from the same power supply.

∗ AKM assumes no responsibility for the usage beyond the conditions in this data
sheet.

ANALOG CHARACTERISTICS

(Ta=25℃; VA1,VA2,VD,VB=5.0V; fs=44.1kHz; Signal Frequency=1kHz;
Measurement frequency=10Hz~20kHz; unless otherwise specified)

Parameter		min	typ	max	Units
Resolution				16	Bits
ADC Analog Input Characteristics: Analog Source Impedance=470Ω					
S/(N+D)	(Note 3)	74	83		dB
S/N	(A-Weighted)	85	90		dB
Dynamic Range (A-Weighted)	(Note 4)	85	90		dB
Interchannel Isolation		70	80		dB
Interchannel Gain Mismatch		0.3	0.1		dB
Gain Drift			100	-	ppm/℃
Offset Error (after calibration)			±10	±30	LSB
Input Voltage	(Note 5)	2.65	2.80	2.95	Vp-p
Input Resistance		35	60		kΩ
DAC Analog Output Characteristics: RL≧10kΩ					
S/(N+D)	(Note 3)	78	85		dB
S/N	(A-Weighted)	84	89		dB
Dynamic Range (A-Weighted)	(Note 4)	84	89		dB
Interchannel Isolation		80	80		dB
Interchannel Gain Mismatch		0.3	0.1		dB
Gain Drift			100	-	ppm/℃
Output Voltage	(Note 5)	2.50	2.65	2.80	Vp-p
Load Resistance		10			kΩ
Out-of-band Noise	(Note 6)	-	-83		dB
Power Supplies					
Power Supply Current (Note 7) Normal Operation (PD="L") VA1+VA2+VB VD Power-Down-Mode (PD="H") VA1+VA2+VB VD			20 10 10 10	30 15 20 20	mA mA uA uA
Power Dissipation Normal Operation Power-Down-Mode			150 100	225 200	mW uW
Power Supply Rejection		-	50		dB

Notes:3. The ratio of the rms value of the signal to the rms sum of all the spectral
       components less than 20kHz bandwidth, including distortion components.
    4. S/(N+D) which is measured with an input signal of -60dB below full-scale.
    5. These values are the full scale(0dB) of the input voltage and the output
       voltage.
    6. Noise level less than 100kHz bandwidth at fs=44.1kHz.
       S/N at low samplig rate (fs=8kHz) also shows the same value(83dB).
    7. Almost no current is supplied from VB pin.

FILTER CHARACTERISTICS

(Ta=25℃; VA1,VA2,VD,VB=5.0V±5%; fs=44.1kHz)

Parameter	Symbol	min	typ	max	Units
ADC Digital Filter:					
Passband ±0.1dB (Note 8)	PB	0		16.8	kHz
-0.5dB		0		17.7	kHz
-3.0dB		0		19.9	kHz
Stopband (Note 8)	SB	28.3			kHz
Passband Ripple	PR			±0.1	dB
Stopband Attenuation	SA	70			dB
Group Delay Distortion	△GD			0	us
Group Delay (Note 9)	GD		8		1/fs
DAC Digital Filter:					
Passband ±0.1dB (Note 8)	PB	0		18.0	kHz
-1.0dB		0		20.0	KHz
-6.0dB		0		22.05	kHz
Stopband (Note 8)	SB	26.1			kHz
Passband Ripple	PR			±0.1	dB
Stopband Attenuation	SA	65			dB
Group Delay (Note 9)	GD		15		1/fs
DAC Analog Post Filter:					
Frequency Response 20.0kHz			-0.1		dB
22.05kHz			-0.6		dB
44.1kHz			-18		dB

Notes: 8. The passband and stopband frequencies scale with fs.
For example, PB=0.401*fs at -0.5dB in ADC, PB=0.454*fs at -1.0dB in DAC.
9. The calculating delay time which occurred by digital filtering. This time is from the input of analog signal to setting the 16bit data of both channels to the output register for ADC.
For DAC, this time is from setting the 16bit data of both channels to input register to the output of analog signal.

DIGITAL CHARACTERISTICS

(Ta=25℃; VA1,VA2,VD,VB=5.0V±5%)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%VD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%VD	V
High-Level Output Voltage Iout=-20uA	VOH	4.4	-	-	V
Low-Level Output Voltage Iout=20uA	VOL	-		0.1	V
Input Leakage Current	Iin	-	-	±10	uA

SWITCHING CHARACTERISTICS

(Ta=25℃; VA1, VA2, VD, VB=5.0V±5%; CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Control Clock Frequency					
Master Clock 256fs:	fCLK	1.024	11.2896	12.800	MHz
Pulse Width Low	tCLKL	31.25			ns
Pulse Width High	tCLKH	31.25			ns
384fs:	fCLK	1.536	16.9344	19.200	MHz
Pulse Width Low	tCLKL	20.83			ns
Pulse Width High	tCLKH	20.83			ns
SCLK Frequency	fSLK		1.4112	3.200	MHz
L/R̄ Frequency (Note 10)	fs	4	44.1	50	kHz
Serial Interface Timing (Note 11)					
SCLK Period	tSLK	312.5			ns
SCLK Pulse Width Low	tSLKL	100			ns
Pulse Width High	tSLKH	100			ns
SCLK "↓" to L/R̄ Edge (Note 12)	tSLR	-tSLKH+30		tSLKL-30	ns
L/R̄ Edge to SDTO(MSB) Valid	tDLR			70	ns
SCLK "↓" to SDTO Valid	tDSS			70	ns
SDTI Hold Time	tSDH	40			ns
SDTI Setup Time	tSDS	40			ns
Power-Down/Calibration Timing					
PD Pulse Width	tPDW	150			ns
PD "↓" to SDTO delay (Note 13)	tPDV		8224		1/fs

Notes: 10. If the duty of L/R̄ changes larger than ±1/8 from 50%, the AK4510 is reset by
            the internal phase detect circuit automatically.
       11. Refer to the operating overview section "Serial Data Interface".
       12. SCLK rising edge must not occur at the same time as L/R̄ edge.
       13. These cycles are the number of L/R̄ rising from PD falling.

■ Timing Diagram
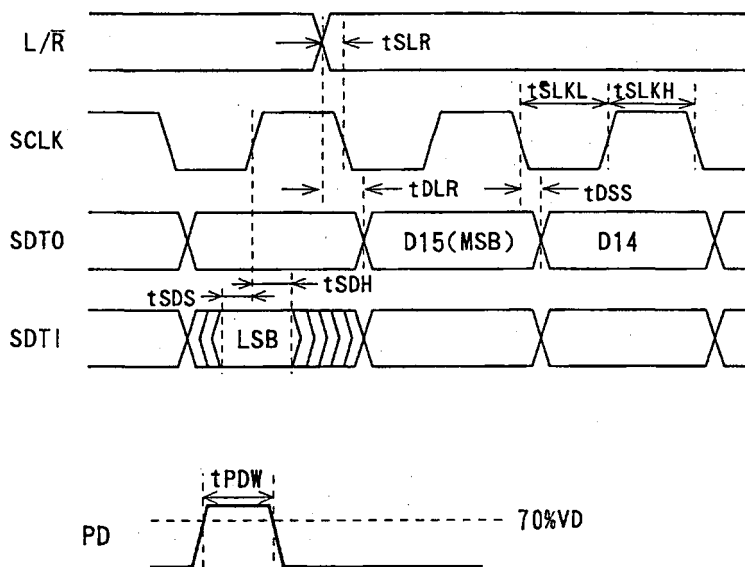
OPERATION OVERVIEW

■ System Clock Input

The external clocks which are required to operate the AK4510 are MCLK(256/384fs), L/R̄(1fs),
SCLK(32fs~). MCLK should be synchronized with L/R̄ but the phase is free of care. The
frequency of MCLK is determined by the desired Input Word Rate(1fs), and the setting of
the Clock Select, CMODE pin. Setting CMODE "L" selects an MCLK frequency of 256fs while
setting CMODE "H" selects 384fs. When the 384fs is selected, the internal master clock
becomes 256fs(=384fs*2/3). Table 1 illustrates standard audio word rates and
corresponding frequencies used in the AK4510.

As the AK4510 includes the phase detect circuit for L/R̄, the AK4510 is reset
automatically when the synchronization is out of phase by changing the clock frequencies.
Therefore, the reset is not required except only upon power-up. (Please refer to the
"System Reset" section.)

All external clocks(MCLK,SCLK,L/R̄) should always be present whenever the AK4510 is in
normal operation mode(PD="L"). If these clocks are not provided, the AK4510 may draw
excess current and do not possibly operate properly because the device utilizes dynamic
refreshed logic internally. If the external clocks are not present, the AK4510 should be
in the power-down mode(PD="H").

fs	MCLK		SCLK(32fs)
	256fs	384fs	
32.0kHz	8.1920MHz	12.2880MHz	1.0240MHz
44.1kHz	11.2896MHz	16.9344MHz	1.4112MHz
48.0kHz	12.2880MHz	18.4320MHz	1.5360MHz

Table 1. Examples of System Clock

■ Serial Data Interface

Data bits are input/output via the SDTI/SDTO pin using the SCLK and L/R̄ inputs.
The falling edge of SCLK causes the AK4510 to output each bit, except the MSB, which is
clocked out via the SDTO pin by L/R̄ edge. DAC data is clocked into the AK4510 via STDI pin
and is latched by L/R̄ edge. When SCLK is 32fs, the input data time slot is same as the
output data time slot. The format of input/output data is 2's complement MSB first.
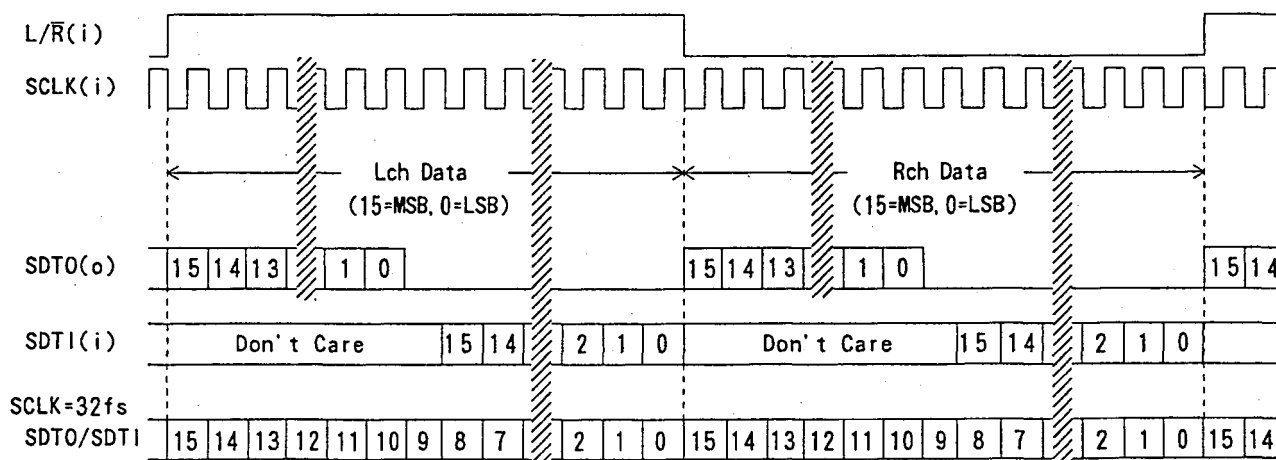
Figure 1. DATA Input/Output Timing

■ Digital Loopback mode

Digital loopback mode is supported for device and system testing. This mode is enabled by
setting LOOP pin "H" when SCLK cycle is 32fs only. The ADC outputs are passed
internally to the DAC inputs. ADC outputs are presented on SDTO pin but the DAC inputs on
SDTI pin are ignored during this mode.

■ Power-Down and Offset Calibration(★)

The AK4510 is placed in the power-down mode by bringing PD "H". The digital filter is
reset by in the power-down mode. Exiting from the power-down mode by bringing PD "L"
initiates an offset calibration procedure for ADC. Upon the initial application of power
to the supply pins, the data in the calibration registers are indeterminate. A calibration
cycle should always be initiated after power-up. In the power-down mode, the VREF and VCOM
are AGND level and the analog outputs are floating.

During calibration, the ADC digital data outputs of both channels are forced to a 2's
complement "0" and the DAC analog output is the voltage corresponding to "0" input.
The ADC outputs settle in the data corresponding to the input signals and the DAC outputs
settle in the voltage corresponding to the input data after the end of calibration
(Settling approximately takes the group delay time).

Figure 2. Power-down/up sequence example
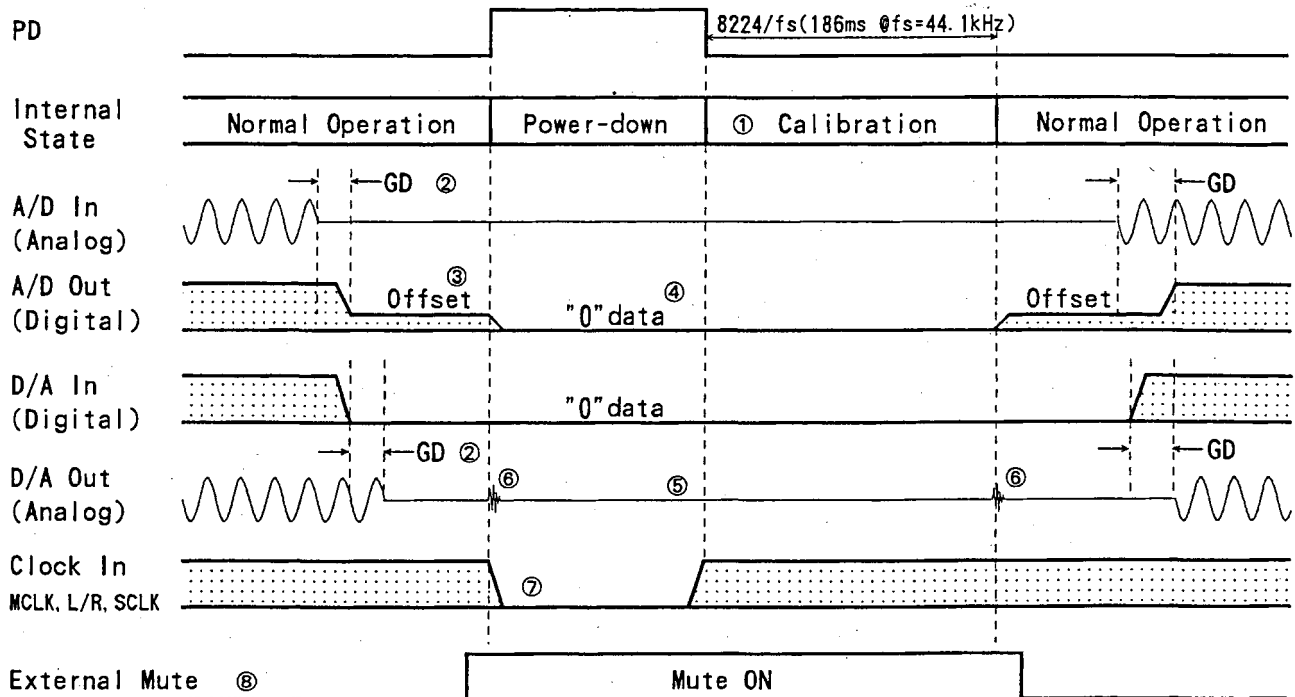
Notes:

①An offset calibration starts after exiting the power-down state.

②Digital output corresponding to analog input and analog output corresponding to digital input have the group delay(GD).

③Even if no signal is input to analog input pin, the digital output has some offset due to an offset of the input op-amp and the internal offset error of ADC.

④A/D output is "0" data at the power-down state.

⑤D/A output is Hi-Z at the power-down state.

⑥Click noise of about -50dB occurs at PD=" ⌐ " and the end of an offset calibration.

⑦When the external clocks(MCLK,SCLK,L/R̄) are stopped, AK4510 should be in the power-down state.

⑧Please mute the analog output externally if the click noise(⑥) influences system application. Timing example is shown in this figure.

■ System Reset

The AK4510 should be reset once by bringing PD "H" after power-up. The internal timing starts clocking by the rising edge of L/R̄ upon exiting from reset. If the phase difference between L/R̄ and internal control signals is larger than +1/16∼-1/16 of a word period(1/fs), the synchronization of internal control signals with L/R̄ is done automatically at the first rising edge of L/R̄. (★)Since RAM address shifts during this synchronization, correct data would not be output until 18 sampled data are input even if the AK4510 returns to the normal operation. Even if "0" data is being input to the D/A, some noise occurs under this condition.

SYSTEM DESIGN

Figure 3 shows the system connection diagram. Very few external components are required to support the AK4510. An evaluation board[AKD4510] is available which demonstrates the optimum layout and power supply arrangements.
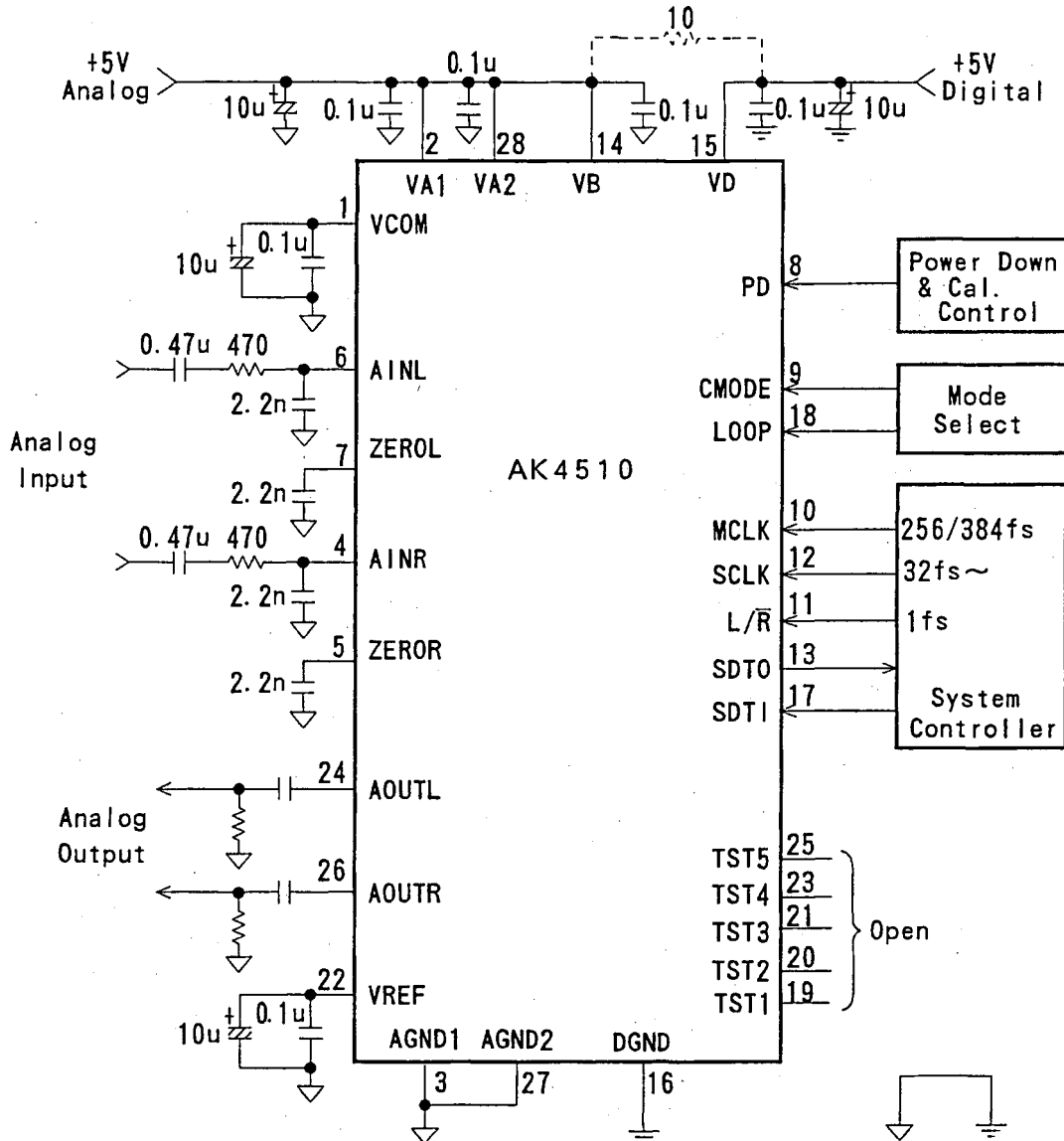
Figure 3. Typical Connection Diagram

■ System design consideration

1. Grounding and Power Supply Decoupling

The AK4510 requires careful attention to power supply and grounding arrangements. VA1, VA2 and VB are connected together on the chip through a few Ω resistance. If VA1, VA2, VB and VD are supplied separately, VA1, VA2, VB and VD should be powered up at the same time or VA1, VA2, VB should be powered up earlier than VD. When all supplies are not separated, VD should be supplied from analog power supply. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4510 as possible, with the small value ceramic capacitor being the nearest.

2. On-chip voltage reference

The on-chip voltage reference is output on the VREF and VCOM pins for decoupling. The VREF is used as the reference of A/D and D/A conversion. The VCOM is a signal ground of this chip. An electrolytic capacitor less than 10uF in parallel with a 0.1uF ceramic capacitor attached to these pins eliminates the effects of high frequency noise. No load current may be drawn from the VREF and VCOM pins. All signals, especially clocks, should be kept away from the VREF and VCOM pins in order to avoid unwanted coupling into the modulators.

3. Analog Inputs

The analog inputs are single-ended and internally biased to the VCOM voltage with 60kΩ(typ) resistance. The input signal range is typically 2.8Vp-p(1Vrms). AIN capacitance(Ca) and ZERO capacitance(Cz) in Figure 4 should be same value to cancel the offset error. However, even if AC coupling is used, ADC outputs approximately have ±10LSB after offset calibration. Figure 5 shows a example for 2Vrms line-level input circuit.

The output data format is 2's complement. The AK4510 accepts input voltages from AGND1 to VA1. The output code is 7FFFH for inputs above a positive full scale and 8000H for input below a negative full scale. The ideal code is 0000H with no input signal. As the capacitor for DC cut may cause the loss of distortion, the type of capacitor should be selected depending on the system application.
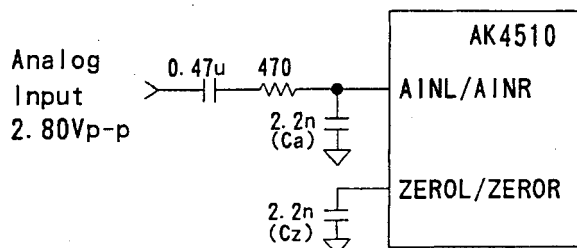
Figure 4. Input capacitance
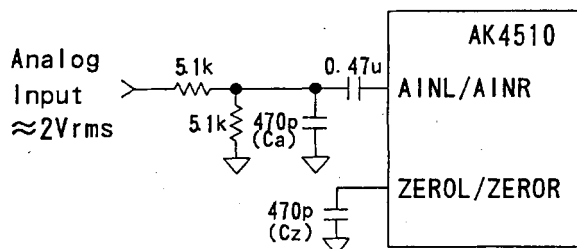
Figure 5. 2Vrms Line level Input

The AK4510 samples the analog inputs at 64fs. The digital filter rejects all noise higher than the stop band. However, the filter will not reject frequencies right around 64fs(and multiples of 64fs). Most audio signals do not have significant energy at 64fs. Nevertheless, a simple RC filter(fc≈150kHz at fs=44.1kHz) will attenuate any noise energy at 64fs, in addition to providing the optimum source impedance for the modulators. This input capacitor(Ca in Figure 4) is also needed to bypass the clock feedthrough noise of internal input switch.

4. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The output signal range is typically 2.65Vp-p(0.94Vrms). The input data format is 2's complement. The output voltage is a positive full scale for 7FFFH and a negative full scale for 8000H. The ideal output is VCOM voltage for 0000H.

The internal switched-capacitor filter and continuous-time filter almost remove the noise generated by the delta-sigma modulator of DAC beyond the audio passband, especially low sampling rate. The noise floor level is almost constant and the audible noise level is -83dB(typ) at 8kHz sampling.
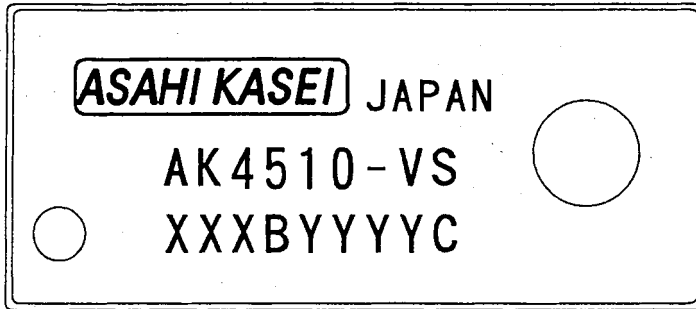
PACKAGE

● 28pin SOP (Unit: mm)
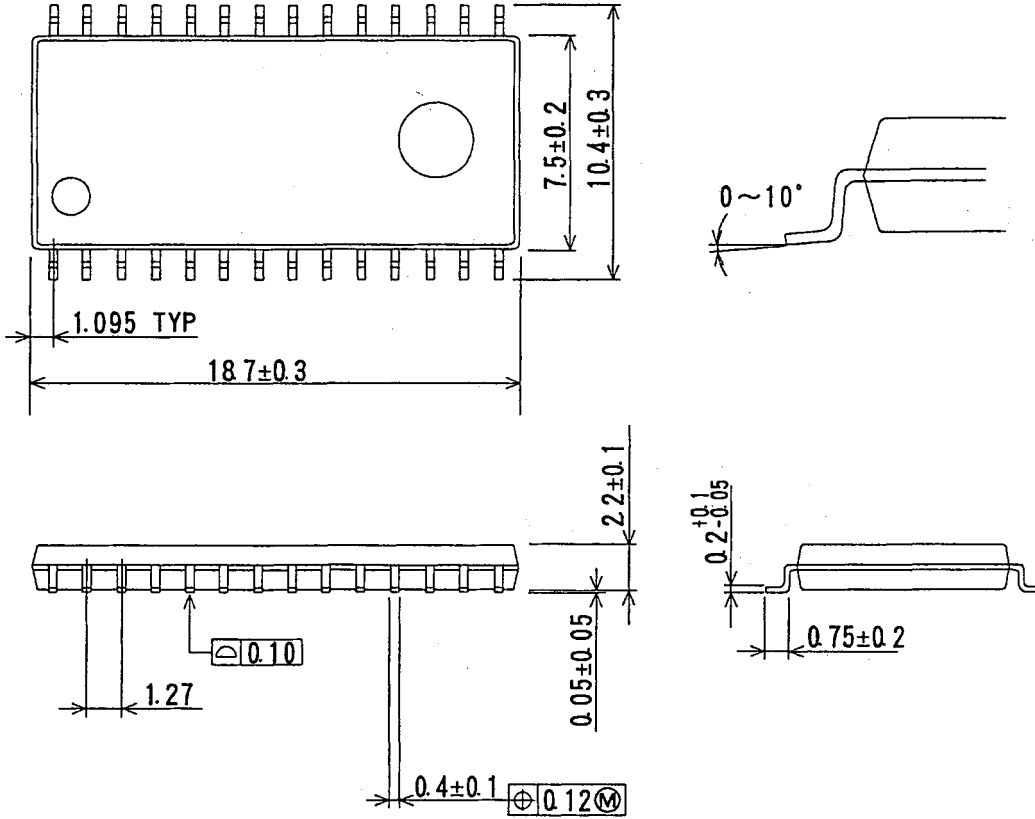
■ Package & Lead frame material

Package molding compound :   Epoxy
Lead frame material :   Cu
Lead frame surface treatment: Solder plate

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MARKING
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- 14 -

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   X X X B :   Lot# (X : numbers, B : alphabet)
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